QL3040 pASIC 3 FPGA Data Sheet

QuickLogic

• • • • • • 40,000 Usable PLD Gate pASIC 3 FPGA Combining High Performance and High Density

Device Highlights

High Performance & High Density

- 40,000 Usable PLD Gates with 252 I/Os
- 300 MHz 16-bit Counters, 400 MHz Datapaths
- 0.35 µm four-layer metal non-volatile CMOS process for smallest die sizes

Easy to Use / Fast Development Cycles

- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high quality Verilog/VHDL synthesis

Advanced I/O Capabilities

- Interfaces with both 3.3 V and 5.0 V devices
- PCI compliant with 3.3 V and 5.0 V buses for -1/-2/-3/-4 speed grades
- Full JTAG boundary scan
- I/O Cells with individually controlled Registered Input Path and Output Enables

Total of 252 I/O Pins

- 244 bidirectional input/output pins, PCI-compliant for 5.0 V and 3.3 V buses for -1/-2/-3/-4 speed grades
- Eight high-drive input/distributed network pins

Eight Low-Skew Distributed Networks

- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs — each driven by an input-only pin
- Six global clock/control networks available to the logic cell; F1, clock set, reset inputs and the input, I/O register clock, reset, and enable inputs as well as the output enable control — each driven by an input-only or I/O pin, or any logic cell output or I/O cell feedback

High Performance

- Input + logic cell + output total delays under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz

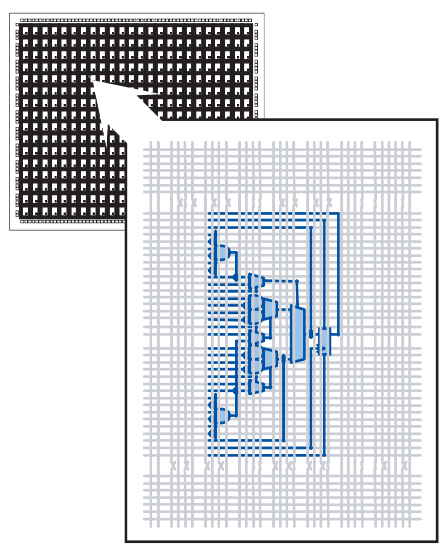


Figure 1: 1,008 pASIC 3 Logic Cells

Architecture Overview

The QL3040 is a 40,000 usable PLD gate member of the pASIC 3 family of FPGAs. pASIC 3 FPGAs are fabricated on a 0.35 µm four-layer metal process using QuickLogic®'s patented ViaLink® technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The QL3040 contains 1,008 logic cells. With a maximum of 252 I/Os, the QL3040 is available in 208-PQFP and 456-pin PBGA packages.

Software support for the complete pASIC 3 family, including the QL3040, is available through three basic packages. The turnkey Quick*Works*® package provides the most complete FPGA software solution from design entry to logic synthesis, to place and route, to simulation. The QuickTools™ for Workstations package provides a solution for designers who use Cadence®, Exemplar™, Mentor®, Synopsys®, Synplicity®, Viewlogic™, Aldec™, or other third-party tools for design entry, synthesis, or simulation.

Electrical Specifications

AC Characteristics at V_{CC} = 3.3 V, TA = 25°C (K = 1.00)

To calculate delays, multiply the appropriate K factor from **Table 7** by the numbers provided in **Table 1** through **Table 5**.

Table 1: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{PD}	Combinatorial Delay [b]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time [b]	1.7	1.7	1.7	1.7	1.7
t_{H}	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.
b. These limits are derived from a representative selection of the slowest paths through the pASIC 3 logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 2: Input-Only/Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.

Table 3: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [a]						
		1	2	3	4	8	10	11
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 40 half columns and the global distributed networks consist of 44 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to eight loads per half column. The global clock has up to 11 loads per half column.

Table 4: Input-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock To Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.

Table 5: Output-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-State [a]	2.0	-	-	-	-
t_{PLZ}	Output Delay Low to Tri-State	1.2	-	-	-	-

a. The loads presented in **Figure 2** are used for t_{PXZ}:

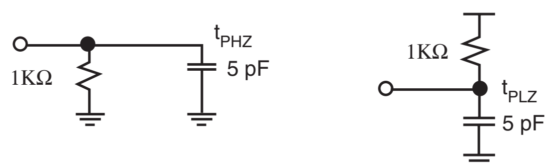


Figure 2: Loads used for t_{PXZ}

DC Characteristics

The DC specifications are provided in **Table 6** through **Table 8**.

Table 6: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to V_{CCIO} +0.5 V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Lead Temperature	300°C

Table 7: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-55	-	-40	85	0	70	°C
TC	Case Temperature		-	125	-	-	-	-	°C
K	Delay Factor	-0 Speed Grade	-	-	0.43	1.90	0.46	1.85	n/a
		-1 Speed Grade	0.42	1.64	0.43	1.54	0.46	1.50	n/a
		-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	n/a
		-3 Speed Grade			0.43	0.90	0.46	0.88	n/a
		-4 Speed Grade			0.43	0.82	0.46	0.80	n/a

Table 8: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage		0.5 V_{CC}	V_{CCIO}+0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.3 V_{CC}	V
V_{OH}	Output HIGH Voltage	I_{OH} = -12 mA	2.4		V
		I_{OH} = -500 µA	0.9 V_{CC}		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA[a]		0.45	V
		I_{OL} = 1.5 mA		0.1 V_{CC}	V
I_I	I or I/O Input Leakage Current	V_I = V_{CCIO} or GND	-10	10	µA
I_{OZ}	3-State Output Leakage Current	V_I = V_{CCIO} or GND	-10	10	µA
C_I	Input Capacitance[b]			10	pF
I_{OS}	Output Short Circuit Current[c]	V_O = GND	-15	-180	mA
		V_O = V_{CC}	40	210	mA
I_{CC}	D.C. Supply Current[d]	V_I, V_{IO} = V_{CCIO} or GND	0.50 (typ)	2	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}		0	100	µA

a. Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.
b. Capacitance is sample tested only. Clock pins are 12 pF maximum.
c. Only one output at a time. Duration should not exceed 30 seconds.
d. For -1/-2/-3/-4 commercial grade devices only. Maximum I_{CC} is 3 mA for -0 commercial grade and all industrial grade devices, and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group (see **Contact Information**).

Kv and Kt Graphs

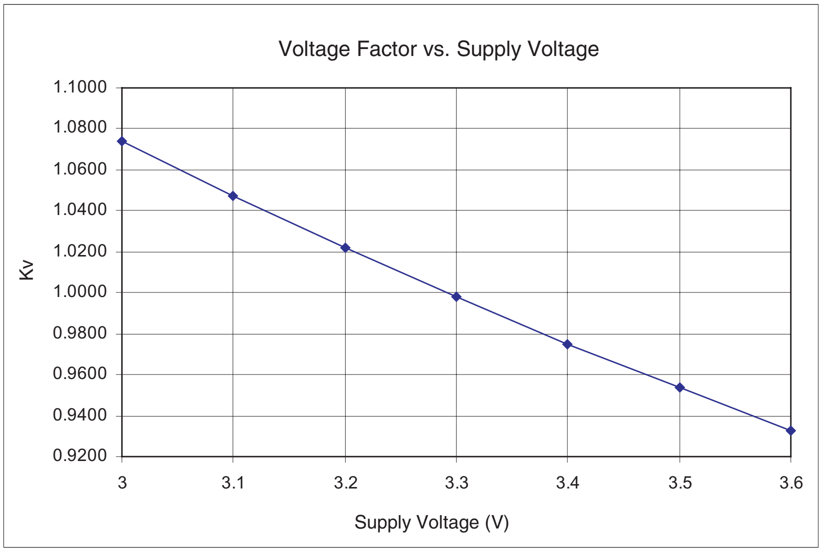


Figure 3: Voltage Factor vs. Supply Voltage

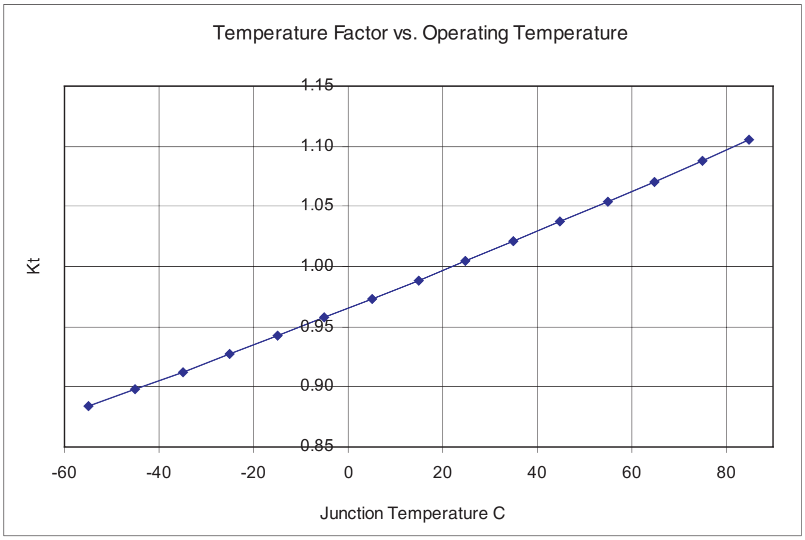


Figure 4: Temperature Factor vs. Operating Temperature

Power-up Sequencing

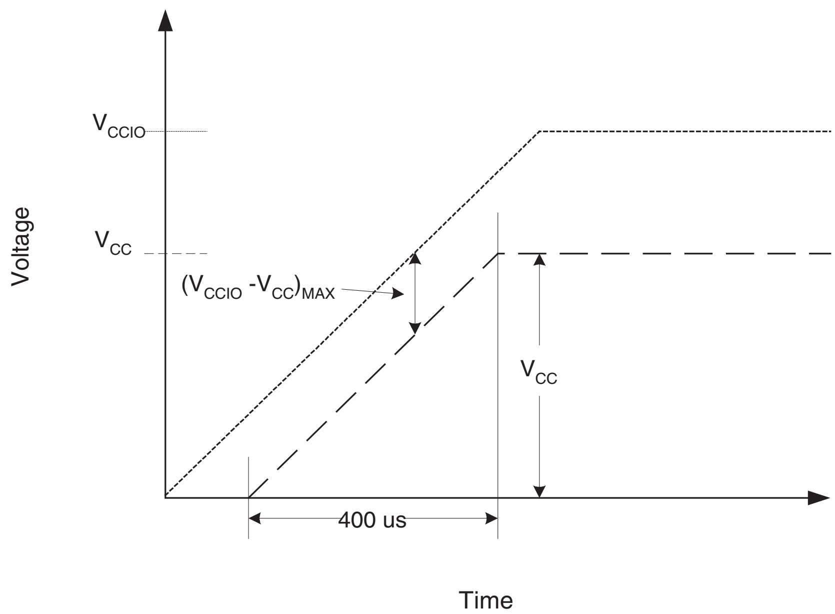


Figure 5: Power-up Requirements

The following requirements must be met when powering up the device (refer to **Figure 5**):

- When ramping up the power supplies keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV. Deviation from this recommendation can cause permanent damage to the device.
- V_{CCIO} must lead V_{CC} when ramping the device.
- The power supply must take greater than or equal to 400 µs to reach V_{CC}. Ramping to V_{CC}/V_{CCIO} earlier than 400 µs can cause the device to behave improperly.

An internal diode is present in-between V_{CC} and V_{CCIO}, as shown in **Figure 6**.

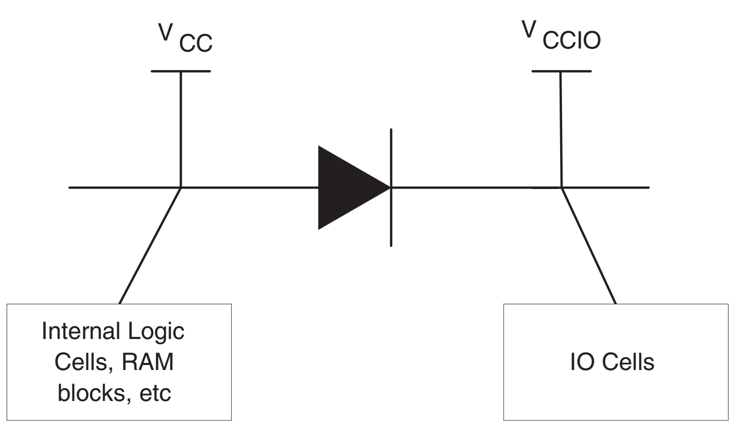


Figure 6: Internal Diode Between V_{CC} and V_{CCIO}

JTAG

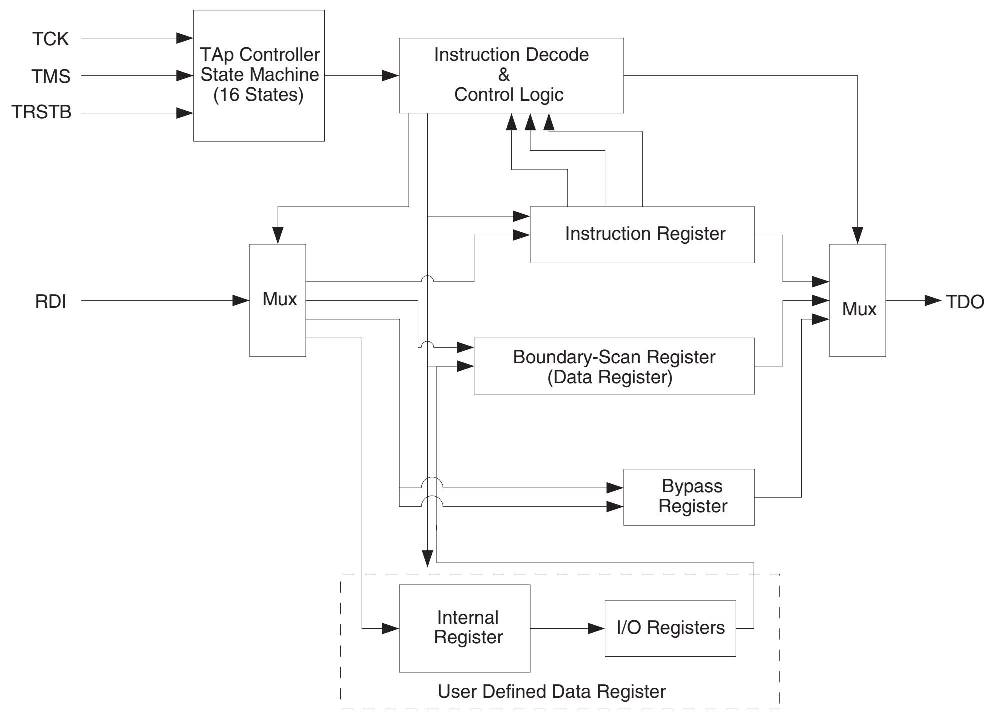


Figure 7: JTAG Block Diagram

Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, not the least of which concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR); these allow users to run three required tests, along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

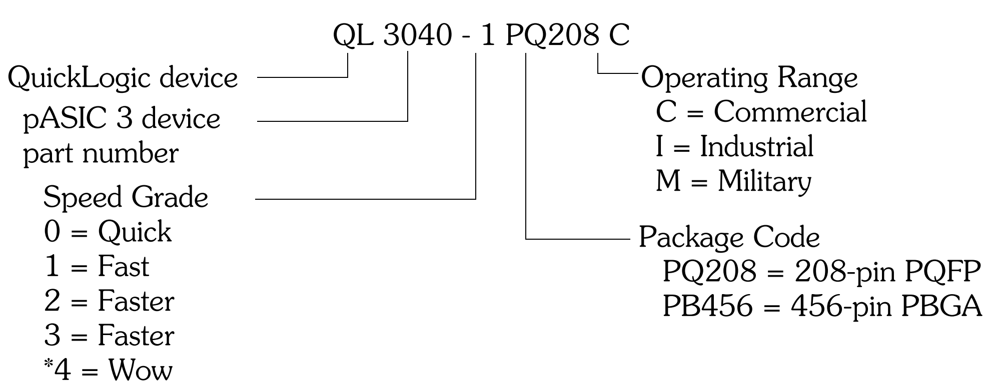
- **Extest Instruction.** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** This instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass instruction allows data to skip a device's boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

Pin Descriptions

Table 9: Pin Descriptions

Pin	Function	Description
TDI	Test Data In for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TRSTB	Active low Reset for JTAG	Hold LOW during normal operation. Connect to ground if not used for JTAG.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V_{CC} or ground if not used for JTAG.
TDO	Test data out for JTAG	Output that must be left unconnected if not used for JTAG.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/Output pin	Can be configured as an input and/or output.
V_{CC}	Power supply pin	Connect to 3.3 V supply.
V_{CCIO}	Input voltage tolerance pin	Connect to 5.0 V supply if 5 V input tolerance is required, otherwise connect to 3.3 V supply.
GND	Ground pin	Connect to ground.

Ordering Information



* Contact QuickLogic regarding availability (see **Contact Information**)

208 PQFP Pinout Diagram

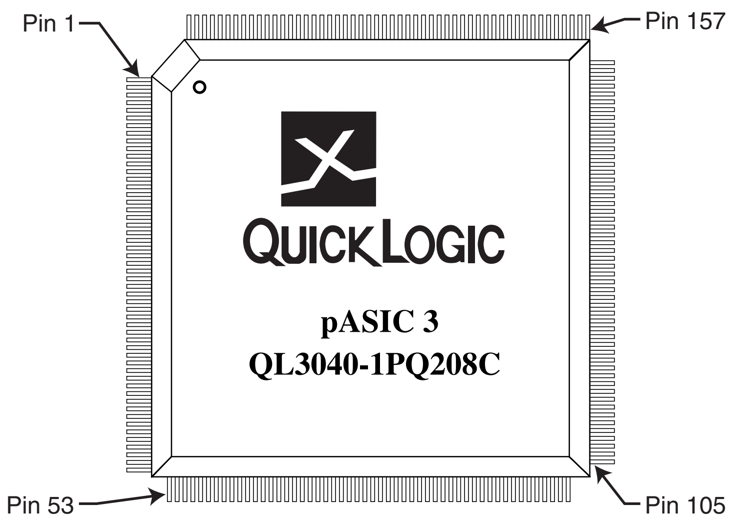


Figure 8: Top View of 208 Pin PQFP

208 PQFP Pinout Table

Table 10: 208 PQFP Pinout Table

208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function	208 PQFP	Function
208	I/O	43	GND	84	I/O	125	I/O	168	I/O
1	I/O	44	I/O	85	I/O	126	I/O	169	I/O
2	I/O	45	I/O	86	I/O	127	GND	NC	I/O
3	I/O	46	I/O	87	I/O	128	I/O	170	I/O
4	I/O	47	I/O	88	I/O	NC	I/O	171	I/O
5	I/O	48	I/O	89	I/O	129	GCLK/I	172	I/O
NC	I/O	NC	I/O	90	I/O	130	ACLK/I	173	I/O
6	I/O	49	I/O	91	I/O	131	V_{CC}	174	I/O
7	I/O	50	I/O	92	I/O	132	GCLK/I	175	I/O
8	I/O	51	I/O	NC	I/O	133	GCLK/I	NC	I/O
9	I/O	52	I/O	93	I/O	134	V_{CC}	176	I/O
10	V_{CC}	53	I/O	94	I/O	135	I/O	177	GND
11	I/O	54	TDI	95	GND	136	I/O	178	I/O
12	GND	NC	I/O	96	I/O	NC	I/O	179	I/O
13	I/O	NC	I/O	97	V_{CC}	137	I/O	NC	I/O
14	I/O	55	I/O	98	I/O	NC	GND	180	I/O
NC	I/O	56	I/O	99	I/O	138	I/O	181	I/O
15	I/O	NC	I/O	100	I/O	139	I/O	182	GND
16	I/O	57	I/O	NC	I/O	140	I/O	NC	V_{CC}
17	I/O	58	I/O	101	I/O	141	I/O	183	I/O
18	I/O	59	GND	NC	I/O	142	I/O	184	I/O
19	I/O	60	I/O	102	I/O	NC	I/O	185	I/O
20	I/O	61	V_{CC}	NC	I/O	143	I/O	186	I/O
NC	I/O	62	I/O	NC	I/O	144	I/O	187	V_{CCIO}
21	I/O	63	I/O	103	TRSTB	145	V_{CC}	188	I/O
22	I/O	64	I/O	104	TMS	NC	I/O	NC	I/O
23	GND	NC	I/O	105	I/O	146	I/O	189	I/O
24	I/O	65	I/O	NC	I/O	147	GND	190	I/O
25	GCLK/I	66	I/O	106	I/O	148	I/O	191	I/O
26	GCLK/I	67	I/O	107	I/O	149	I/O	192	I/O
27	V_{CC}	NC	I/O	108	I/O	150	I/O	193	I/O
28	I/O	68	I/O	109	I/O	151	I/O	194	I/O
29	I/O	69	I/O	NC	I/O	152	I/O	NC	I/O
30	V_{CC}	70	I/O	110	I/O	153	I/O	195	I/O
31	I/O	NC	I/O	111	I/O	154	I/O	196	I/O
32	I/O	71	I/O	112	I/O	155	I/O	197	I/O
NC	GND	NC	I/O	113	I/O	156	I/O	198	I/O
33	I/O	72	I/O	114	V_{CC}	157	TCK	NC	I/O
NC	I/O	73	GND	115	I/O	158	STM	199	GND
34	I/O	74	I/O	116	GND	NC	I/O	200	I/O
35	I/O	NC	V_{CC}	117	I/O	159	I/O	201	V_{CC}
36	I/O	75	I/O	NC	I/O	160	I/O	202	I/O
NC	I/O	76	I/O	118	I/O	161	I/O	203	I/O
37	I/O	77	I/O	119	I/O	162	I/O	204	I/O
38	I/O	78	GND	120	I/O	163	GND	205	I/O
39	I/O	79	I/O	121	I/O	164	I/O	206	I/O
NC	I/O	80	I/O	NC	I/O	165	V_{CC}	207	TDO
40	I/O	81	I/O	122	I/O	166	I/O		
41	V_{CC}	82	I/O	123	I/O	NC	I/O		
42	I/O	83	V_{CCIO}	124	I/O	167	I/O		

456 PBGA Pinout Diagram

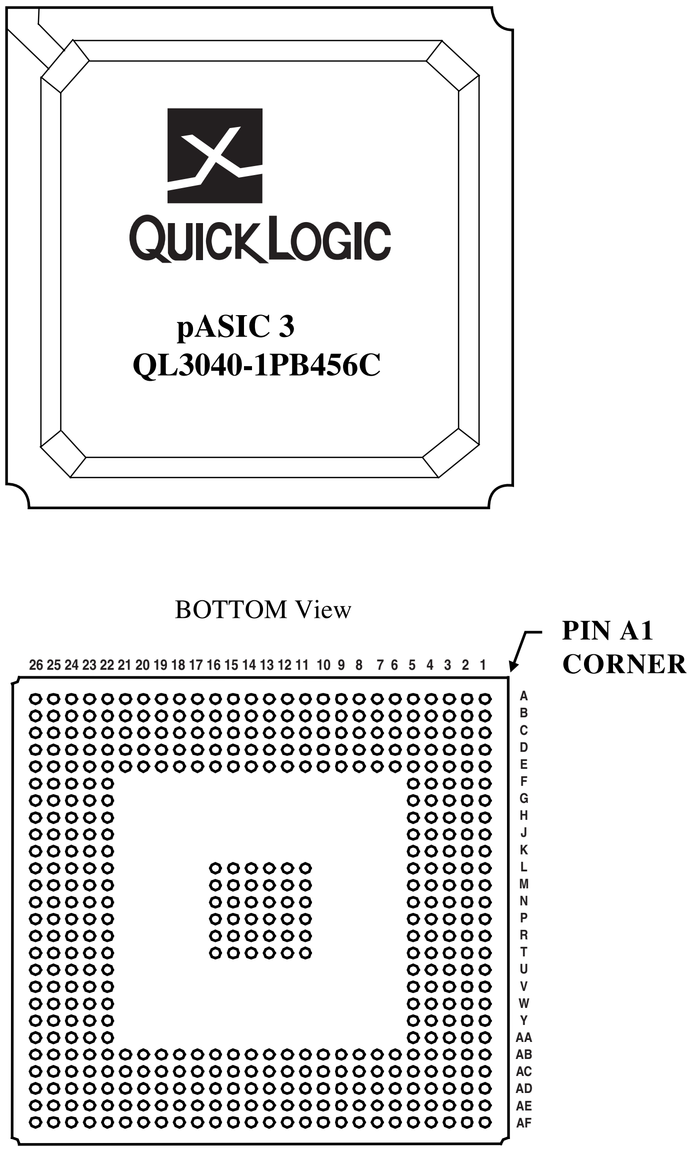


Figure 9: 456-Pin PBGA Pinout Diagram

456 PBGA Pinout Table

Table 11: 456 PBGA Pinout Table

456	Function	456	Function	456	Function	456	Function	456	Function
A1	I/O	B26	STM	D25	I/O	H4	I/O	M14	GND/THERM
A2	I/O	C1	I/O	D26	I/O	H5	NC	M15	GND/THERM
A3	I/O	C2	I/O	E1	I/O	H22	NC	M16	GND/THERM
A4	I/O	C3	I/O	E2	I/O	H23	I/O	M22	NC
A5	I/O	C4	TDO	E3	I/O	H24	I/O	M23	NC
A6	I/O	C5	I/O	E4	I/O	H25	I/O	M24	I/O
A7	I/O	C6	I/O	E5	GND	H26	I/O	M25	I/O
A8	I/O	C7	I/O	E6	V_{CC}	J1	I/O	M26	I/O
A9	I/O	C8	I/O	E7	GND	J2	I/O	N1	GCLK/I
A10	I/O	C9	I/O	E8	NC	J3	I/O	N2	I/O
A11	I/O	C10	I/O	E9	GND	J4	NC	N3	I/O
A12	V_{CCIO}	C11	I/O	E10	I/O	J5	GND	N4	GCLK/I
A13	I/O	C12	I/O	E11	GND	J22	NC	N5	V_{CC}
A14	I/O	C13	I/O	E12	GND	J23	NC	N11	GND/THERM
A15	I/O	C14	I/O	E13	V_{CC}	J24	I/O	N12	GND/THERM
A16	I/O	C15	I/O	E14	GND	J25	I/O	N13	GND/THERM
A17	I/O	C16	I/O	E15	GND	J26	I/O	N14	GND/THERM
A18	I/O	C17	I/O	E16	GND	K1	I/O	N15	GND/THERM
A19	I/O	C18	I/O	E17	NC	K2	I/O	N16	GND/THERM
A20	I/O	C19	I/O	E18	GND	K3	I/O	N22	GND
A21	I/O	C20	I/O	E19	NC	K4	I/O	N23	I/O
A22	I/O	C21	I/O	E20	GND	K5	V_{CC}	N24	I/O
A23	I/O	C22	I/O	E21	V_{CC}	K22	GND	N25	I/O
A24	I/O	C23	I/O	E22	GND	K23	I/O	N26	I/O
A25	I/O	C24	I/O	E23	I/O	K24	I/O	P1	I/O
A26	I/O	C25	TCK	E24	I/O	K25	I/O	P2	I/O
B1	I/O	C26	I/O	E25	I/O	K26	I/O	P3	I/O
B2	I/O	D1	I/O	E26	I/O	L1	I/O	P4	I/O
B3	I/O	D2	I/O	F1	I/O	L2	I/O	P5	NC
B4	I/O	D3	I/O	F2	I/O	L3	I/O	P11	GND/THERM
B5	I/O	D4	GND	F3	I/O	L4	I/O	P12	GND/THERM
B6	I/O	D5	I/O	F4	NC	L5	NC	P13	GND/THERM
B7	I/O	D6	NC	F5	V_{CC}	L11	GND/THERM	P14	GND/THERM
B8	I/O	D7	I/O	F22	V_{CC}	L12	GND/THERM	P15	GND/THERM
B9	I/O	D8	I/O	F23	NC	L13	GND/THERM	P16	GND/THERM
B10	I/O	D9	GND	F24	I/O	L14	GND/THERM	P22	NC
B11	I/O	D10	I/O	F25	I/O	L15	GND/THERM	P23	GCLK / I
B12	I/O	D11	I/O	F26	I/O	L16	GND/THERM	P24	GCLK / I
B13	I/O	D12	GND	G1	I/O	L22	NC	P25	I/O
B14	I/O	D13	I/O	G2	I/O	L23	I/O	P26	ACLK / I
B15	I/O	D14	I/O	G3	I/O	L24	I/O	R1	I/O
B16	I/O	D15	GND	G4	I/O	L25	I/O	R2	I/O
B17	I/O	D16	I/O	G5	NC	L26	I/O	R3	I/O
B18	I/O	D17	I/O	G22	GND	M1	ACLK / I	R4	NC
B19	I/O	D18	GND	G23	I/O	M2	GCLK/I	R5	NC
B20	I/O	D19	I/O	G24	I/O	M3	I/O	R11	GND/THERM
B21	I/O	D20	I/O	G25	I/O	M4	NC	R12	GND/THERM
B22	I/O	D21	NC	G26	I/O	M5	GND	R13	GND/THERM
B23	I/O	D22	I/O	H1	I/O	M11	GND/THERM	R14	GND/THERM
B24	I/O	D23	GND	H2	I/O	M12	GND/THERM	R15	GND/THERM
B25	I/O	D24	I/O	H3	I/O	M13	GND/THERM	R16	GND/THERM

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Table 11: 456 PBGA Pinout Table (Continued)

456	Function	456	Function	456	Function	456	Function	456	Function
R22	V_{CC}	W1	I/O	AB12	NC	AD1	I/O	AE16	I/O
R23	NC	W2	I/O	AB13	I/O	AD2	NC	AE17	I/O
R24	I/O	W3	I/O	AB14	GND	AD3	I/O	AE18	I/O
R25	I/O	W4	I/O	AB15	V_{CC}	AD4	I/O	AE19	I/O
R26	GCLK / I	W5	NC	AB16	I/O	AD5	I/O	AE20	I/O
T1	I/O	W22	NC	AB17	NC	AD6	I/O	AE21	I/O
T2	I/O	W23	I/O	AB18	V_{CC}	AD7	I/O	AE22	I/O
T3	I/O	W24	I/O	AB19	GND	AD8	I/O	AE23	NC
T4	I/O	W25	I/O	AB20	NC	AD9	I/O	AE24	TMS
T5	V_{CC}	W26	I/O	AB21	V_{CC}	AD10	I/O	AE25	I/O
T11	GND/THERMAL	Y1	I/O	AB22	GND	AD11	I/O	AE26	I/O
T12	GND/THERMAL	Y2	I/O	AB23	I/O	AD12	I/O	AF1	I/O
T13	GND/THERMAL	Y3	I/O	AB24	I/O	AD13	I/O	AF2	I/O
T14	GND/THERMAL	Y4	I/O	AB25	I/O	AD14	I/O	AF3	I/O
T15	GND/THERMAL	Y5	I/O	AB26	I/O	AD15	I/O	AF4	I/O
T16	GND/THERMAL	Y22	GND	AC1	I/O	AD16	I/O	AF5	I/O
T22	GND	Y23	I/O	AC2	I/O	AD17	I/O	AF6	I/O
T23	I/O	Y24	I/O	AC3	NC	AD18	I/O	AF7	I/O
T24	I/O	Y25	I/O	AC4	GND	AD19	I/O	AF8	I/O
T25	I/O	Y26	I/O	AC5	I/O	AD20	I/O	AF9	I/O
T26	I/O	AA1	I/O	AC6	NC	AD21	I/O	AF10	I/O
U1	I/O	AA2	I/O	AC7	I/O	AD22	I/O	AF11	I/O
U2	I/O	AA3	NC	AC8	I/O	AD23	TRSTB	AF12	I/O
U3	I/O	AA4	NC	AC9	NC	AD24	I/O	AF13	I/O
U4	I/O	AA5	V_{CC}	AC10	I/O	AD25	I/O	AF14	I/O
U5	GND	AA22	V_{CC}	AC11	I/O	AD26	I/O	AF15	I/O
U22	NC	AA23	NC	AC12	NC	AE1	TDI	AF16	I/O
U23	I/O	AA24	I/O	AC13	I/O	AE2	I/O	AF17	I/O
U24	I/O	AA25	I/O	AC14	V_{CCIO}	AE3	I/O	AF18	I/O
U25	I/O	AA26	I/O	AC15	NC	AE4	I/O	AF19	I/O
U26	I/O	AB1	I/O	AC16	I/O	AE5	I/O	AF20	I/O
V1	I/O	AB2	I/O	AC17	I/O	AE6	I/O	AF21	I/O
V2	I/O	AB3	I/O	AC18	NC	AE7	I/O	AF22	I/O
V3	I/O	AB4	I/O	AC19	I/O	AE8	I/O	AF23	I/O
V4	NC	AB5	GND	AC20	I/O	AE9	I/O	AF24	I/O
V5	NC	AB6	V_{CC}	AC21	I/O	AE10	I/O	AF25	I/O
V22	GND	AB7	NC	AC22	NC	AE11	I/O	AF26	I/O
V23	NC	AB8	NC	AC23	GND	AE12	I/O		
V24	I/O	AB9	NC	AC24	I/O	AE13	I/O		
V25	I/O	AB10	V_{CC}	AC25	I/O	AE14	I/O		
V26	I/O	AB11	GND	AC26	I/O	AE15	I/O		
(Sheet 2 of 2)									

456 PBGA Mechanical Drawing

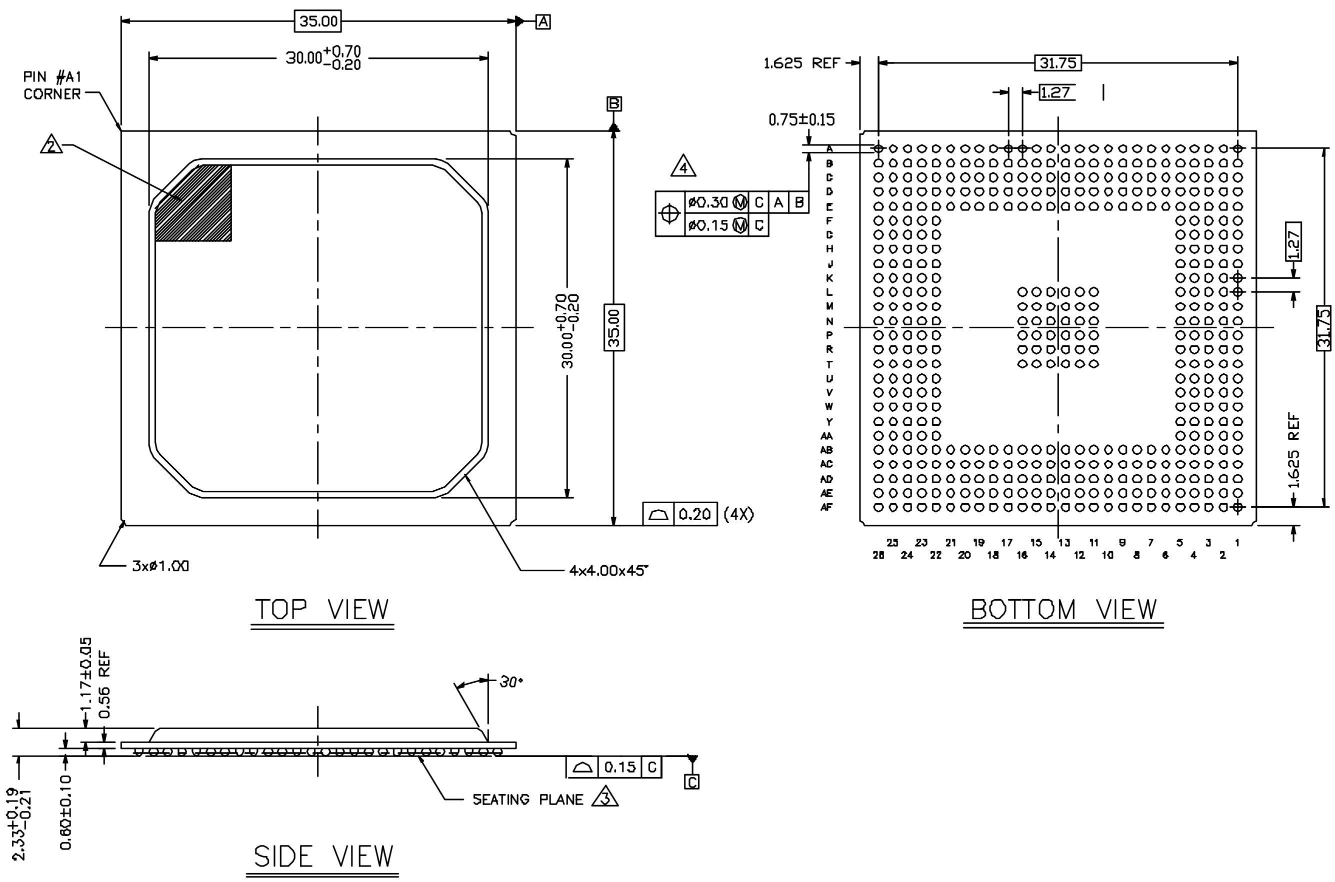

Figure 10: 456 PBGA Mechanical Drawing

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Revision History

Table 12: Revision History

Revision	Date	Comments
A	not avail.	First release.
B	not avail.	
C	not avail	
D	May 2001	Update of AC/DC Specs and reformat
E	June 2002	Added Kfactor, Power-up, JTAG, and mechanical drawing information. Reformatted.

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