ICs for Communications

DSP Embedded Line and Port Interface Controller
DELIC-LC

PEB 20570 Version 2.1

DELIC-PB

PEB 20571 Version 2.1

Preliminary Data Sheet 2003-08 DS 1.1

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Preface

This document provides reference information on the DELIC-PB and -LC version 2.1.

Organization of this Document

This Preliminary Data Sheet is divided into 11 chapters and appendices. It is organized as follows:

- Chapter 1, Introduction
  Gives a general description of the product and its family, lists the key features, and presents some typical applications.

- Chapter 2, Pin Description
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- Chapter 3, Interface Description
  Describes the DELIC external interfaces.

- Chapter 4, Functional IC Description
  Describes the features of the main functional blocks.

- Chapter 5, Memory Structure

- Chapter 6, Register Descriptions
  Containes the detailed register description.

- Chapter 7, Package Outlines

- Chapter 8, Electrical Characteristics
  Containes the DC specification.

- Chapter 9, Timing Diagrams
  Contains the AC specification (as far as available).

- Chapter 10, Application Hints

- Chapter 11, Mailbox Protocol Description
  Describes the communication protocol to an external µP.

Your Comments

We welcome your comments on this document as we are continuously aiming at improving our documentation. Please send your remarks and suggestions by e-mail to

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document type (Preliminary Data Sheet), issue date (2003-08) and document revision number (DS 1.1).

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1 Introduction

The DELIC and VIP chipset realizes multiple ISDN S/T and Up interfaces together with controller functionality typically needed in PBX or Central Office systems. This functionality comprises voice channel handling, signaling control, layer-1 control, and even signal processing tasks.

Moreover it provides a programmable master/slave clock generator with 2 PLLs, an universal µP interface and a DMA interface.

The controller part, **DELIC,** is planned in three different versions:

- **DELIC-LC** (**PEB 20570**) is a line card controller providing voice channel switching, multiple HDLC and layer-1 control for up to three VIPs (24 ISDN channels). Other transceiver ICs (32 analog or 16 digital channels) may additionally be connected via IOM-2/GCI interface.
- **DELIC-PB (PEB 20571**) additionally provides a programmable telecom DSP including program and data RAM. This DSP can be used for layer-1 control, protocol support and signal processing. The flexibility gained by the programmability allows Infineon to offer different application specific solutions with the same silicon just by software configuration.
  A configuration tool assists the user in finding a valid system configuration. Even more customer specific DSP-routines can be integrated with the assistance of Infineon.
- **DELIC-HD** (**PEB 20572)** (in definition) includes up to 64 time-slot oriented HDLC controllers, and 2 independent serial communication controllers. Additional transfer and signalling protocols such as ASYNC and SS7 (PEB 3040 replacement) will be provided in DSP software.

VIP PEB 20590 is the first (8 channel) ISDN transceiver that implements multiple U_{PN} and S/T interfaces within one device. The user can decide by programming in which mode a desired channel shall work.

A total of 8 channels are provided for layer-1 subscriber or trunk line characteristic. The VIP is programmed by the DELIC via the IOM-2000 interface.

VIP's eight channels are programmable in the following maximum partitioning between U_{PN} and S/T channels:

	Max. number of U_{PN} and S/T Channels				
U_{PN}	8	7	6	5	4
S/T	0	1	2	3	4

VIP-8 PEB 20591

Additionally to the features of the VIP, the VIP-8 allows any combination of U_{PN} S/T interface (i.e. each of the 8 channels may be programmed to S/T or U_{PN} mode)

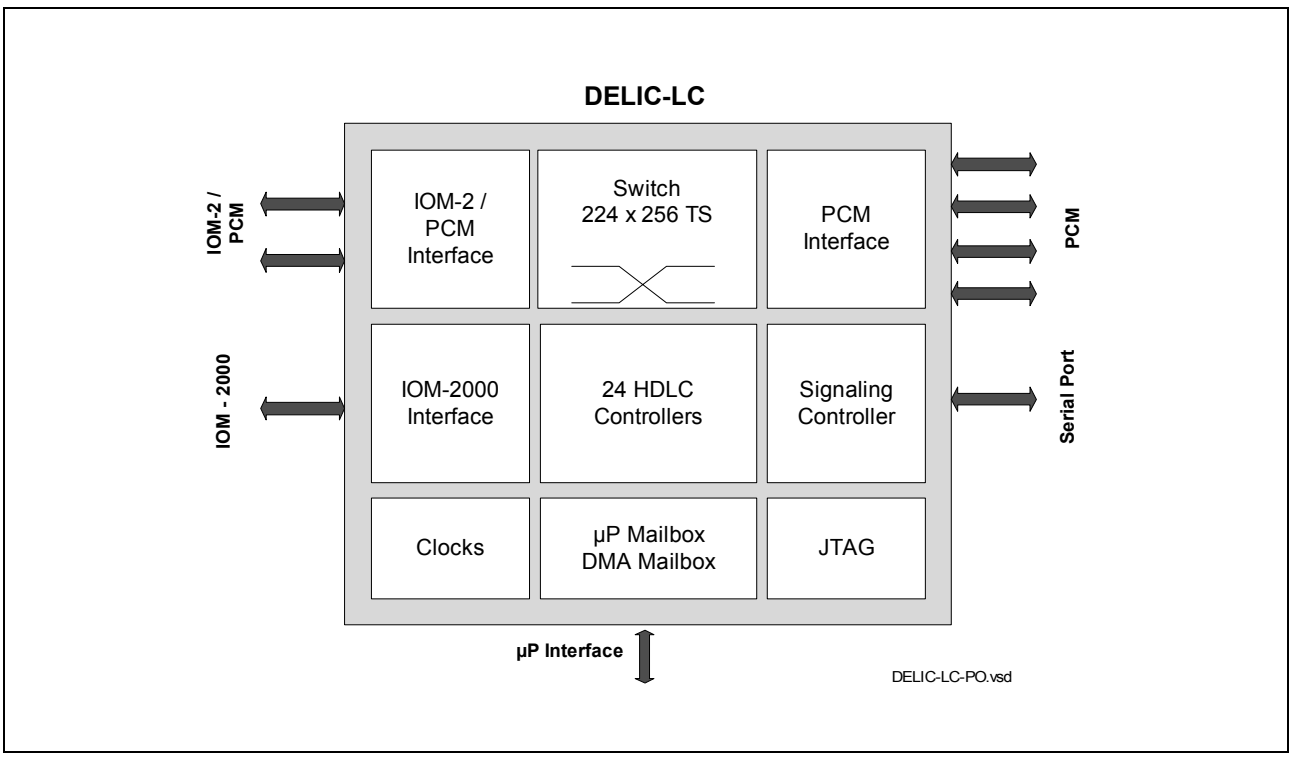


Figure 1-1 Block Diagram of the DELIC-LC

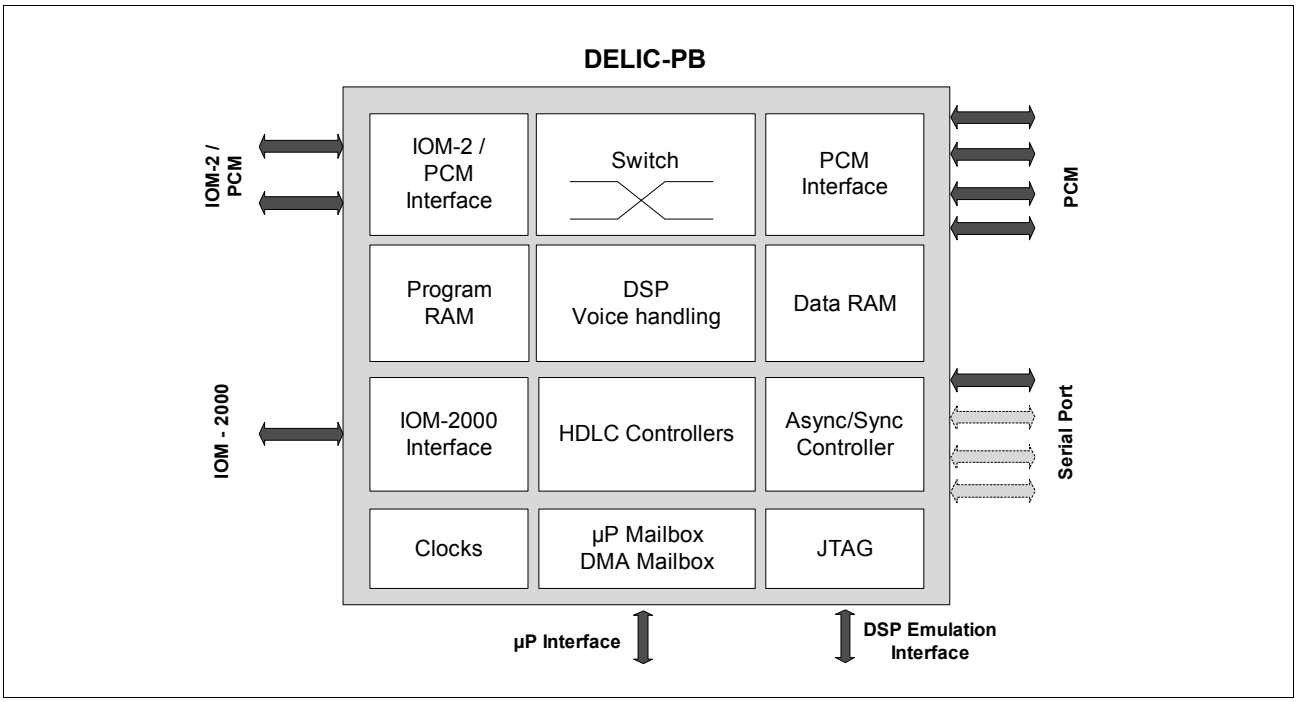


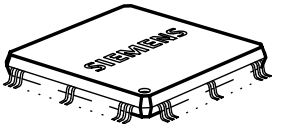
Figure 1-2 Block Diagram of the DELIC-PB

DSP Embedded Line and Port Interface Controller
DELIC-LC/ DELIC-PB

PEB 20570
PEB 20571

Version 2.1 **CMOS**

1.1 DELIC-LC Key Features



P-TQFP-100-1

DELIC-LC is optimized for line card applications:

- One IOM-2000 interface supporting three VIPs i.e. up to 24 ISDN channels
- Two IOM-2 (GCI) ports (configurable as PCM ports) supporting up to 16ISDN channels or 32 analog subscribers
- Four PCM ports with up to 4 x 2.048 Mbit/s (4 x 32 TS) or 2 x 4.096 Mbit/s or 1 x 8.192 Mbit/s
- Switching matrix 224 x 256 TS (8-bit switching)
- 24 HDLC controllers assignable to any D- or B-channel (at 16 kbit/s or 64 kbit/s)
- Serial communication controller: high-speed signaling channel for 2.048 Mbit/s
- Standard multiplexed and de-multiplexed µP interface: Siemens, Intel, Motorola
- Programmable PLL based Master/Slave clock generator, providing all system clocks from a single 16.384 MHz crystal source
- JTAG compliant test interface
- single 3.3 V power supply, 5 V tolerant inputs

1.2 DELIC-PB Key Features

Compared to the DELIC-LC, having a fixed functionality, the DELIC-PB provides a high degree of flexibility (in terms of selected number of ports or channels).

Additionally it features computing power for typical DSP-oriented PBX tasks like conferencing, DTMF..

A Microsoft Windows based configuration tool, the Configurator, enables to generate an application specific functionality. Its features are mainly determined by the firmware of the integrated telecom DSP.

Type	Package
PEB 20570/ PEB 20571	P-TQFP-100-1

List of maximum available features:

- One IOM-2000 interface supporting up to three VIPs i.e. up to 24 ISDN channels
- Up to two IOM-2 (GCI) ports (also configurable as PCM ports) supporting up to 16 ISDN channels or 32 analog subscribers
- Up to four PCM ports with up to 4 x 2.048 Mbit/s (4 x 32 TS) or 2 x 4.096 Mbit/s or 1 x 8.192 Mbit/s
- Switching matrix 224 x 256 TS (switching of 4-/8- bit time slots)
- Up to 32 HDLC controllers assignable to any D- or B-channel (at 16 kbit/s or 64 kbit/s)
- Serial communication controller: high-speed signaling channel of up to 16.384 Mbit/s
- DECT synchronization support
- Standard multiplexed and de-multiplexed µP interface: Siemens, Intel, Motorola
- Dedicated DMA support mailbox
- Integrated DSP core OAK®+ (up to 60 MIPS for layer 1 control, signalling and DSP-algorithms)
- 4 KW on-chip program memory
- 2 KW on-chip data memory
- 2 KW ROM
- DSP work load measurement for run-time statistics, DSP alive indication
- On chip debugging unit
- Serial DSP program debugging interface connected via JTAG port
- A-/µ-law conversion unit
- Programmable PLL based Master/Slave clock generator, providing all system clocks from a single 16.384 MHz crystal source
- JTAG compliant test interface
- single 3.3 V power supply, 5 V compatible inputs

Note: As each feature consumes system resources (DSP-performance, memory, port pins), the maximum available number of supported interfaces or HDLC channels is limited by the totally available resources. A System Configurator tool helps to determine a valid configuration.

1.3 Logic Symbol

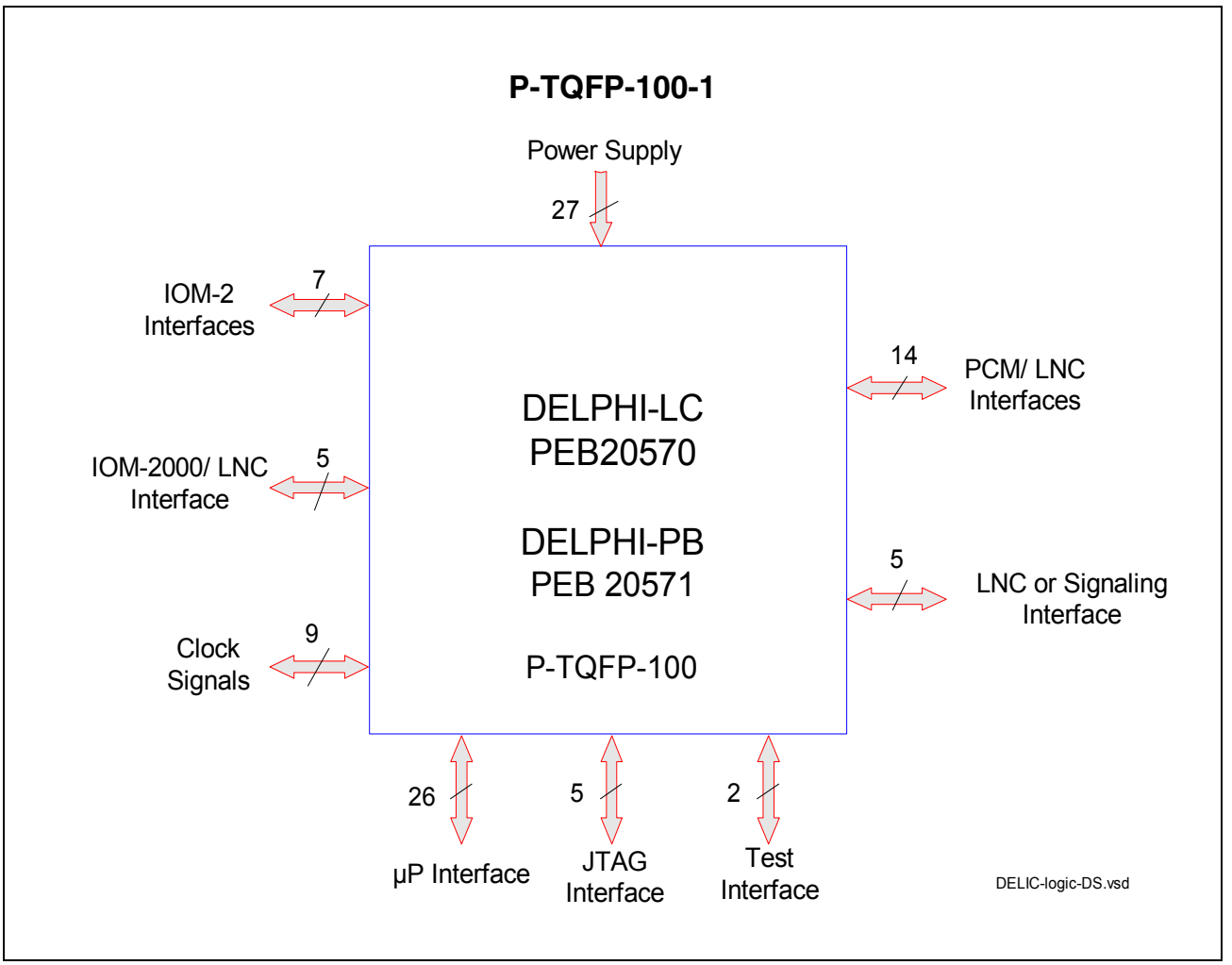


Figure 1-1 Logic Symbol

1.4 Typical Applications

The following two figures show example configurations of DELIC-PB Line card applications for different ISDN interface standards.

In **Figure 1-2**, three VIP transceiver ICs are connected to the DELIC-PB via the new IOM-2000 interface, whereas in **Figure 1-3** and **Figure 1-4** IOM-2 (GCI) interfaces are used.

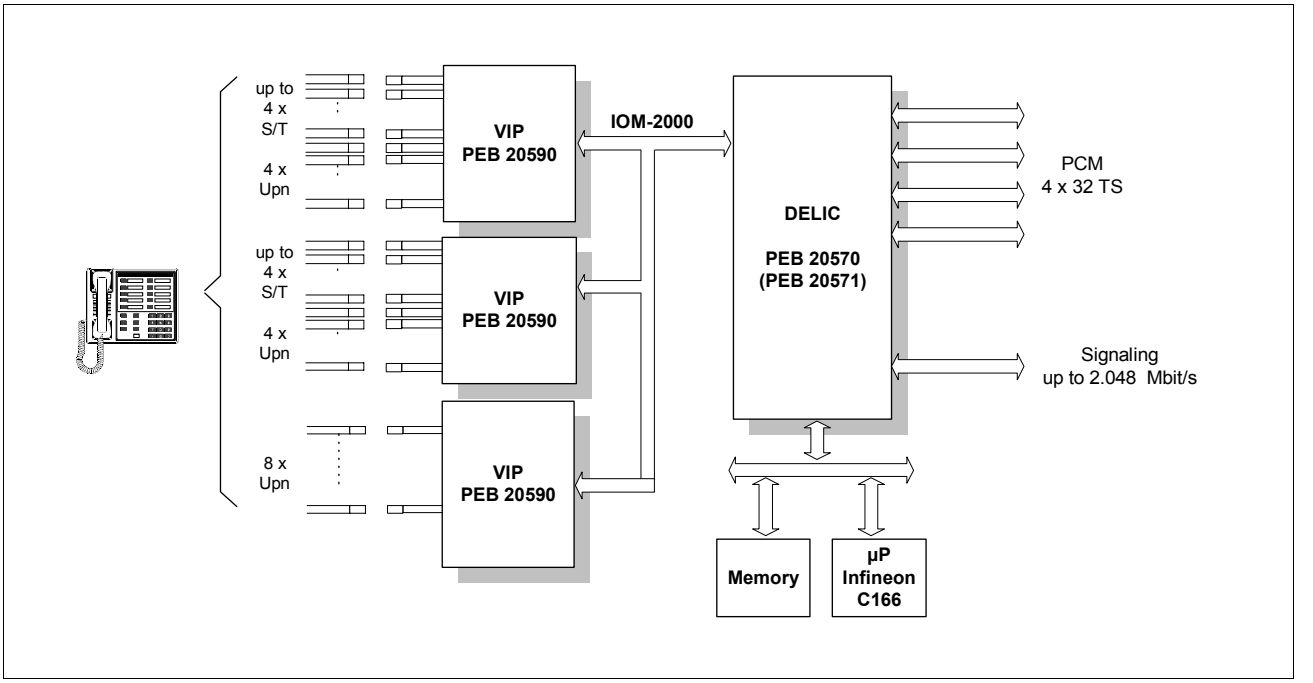


Figure 1-2 DELIC-LC in S/T and Upn Line Cards (up to 8 S/T and 16 Upn)

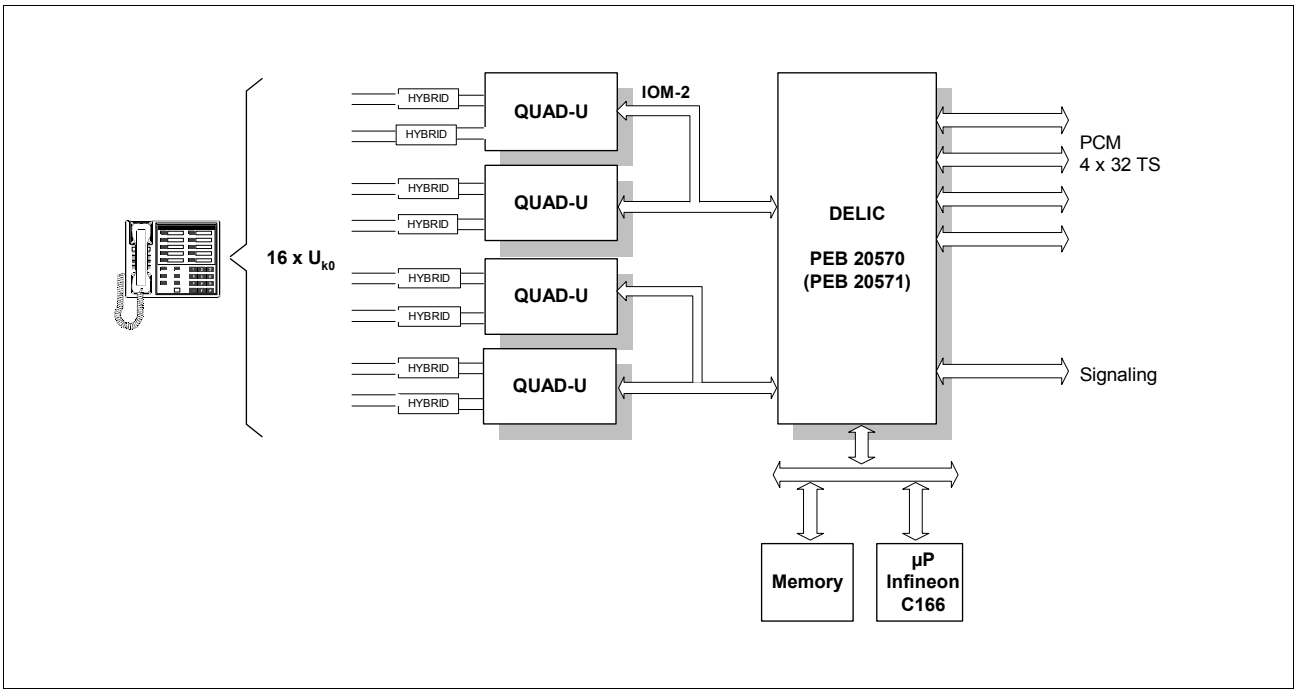


Figure 1-3 DELIC-LC in Uk0 Line Card for 16 Subscribers

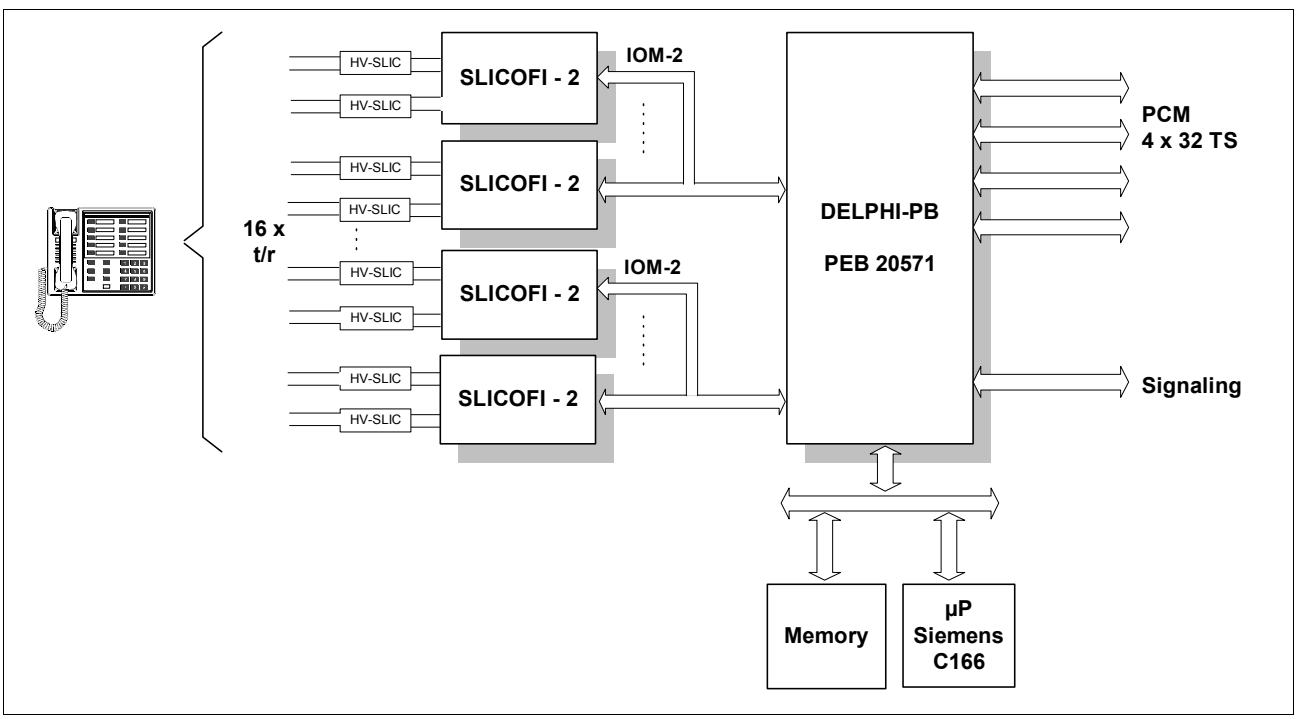


Figure 1-4 DELIC-PB in Analog Line Card for 16 Subscribers

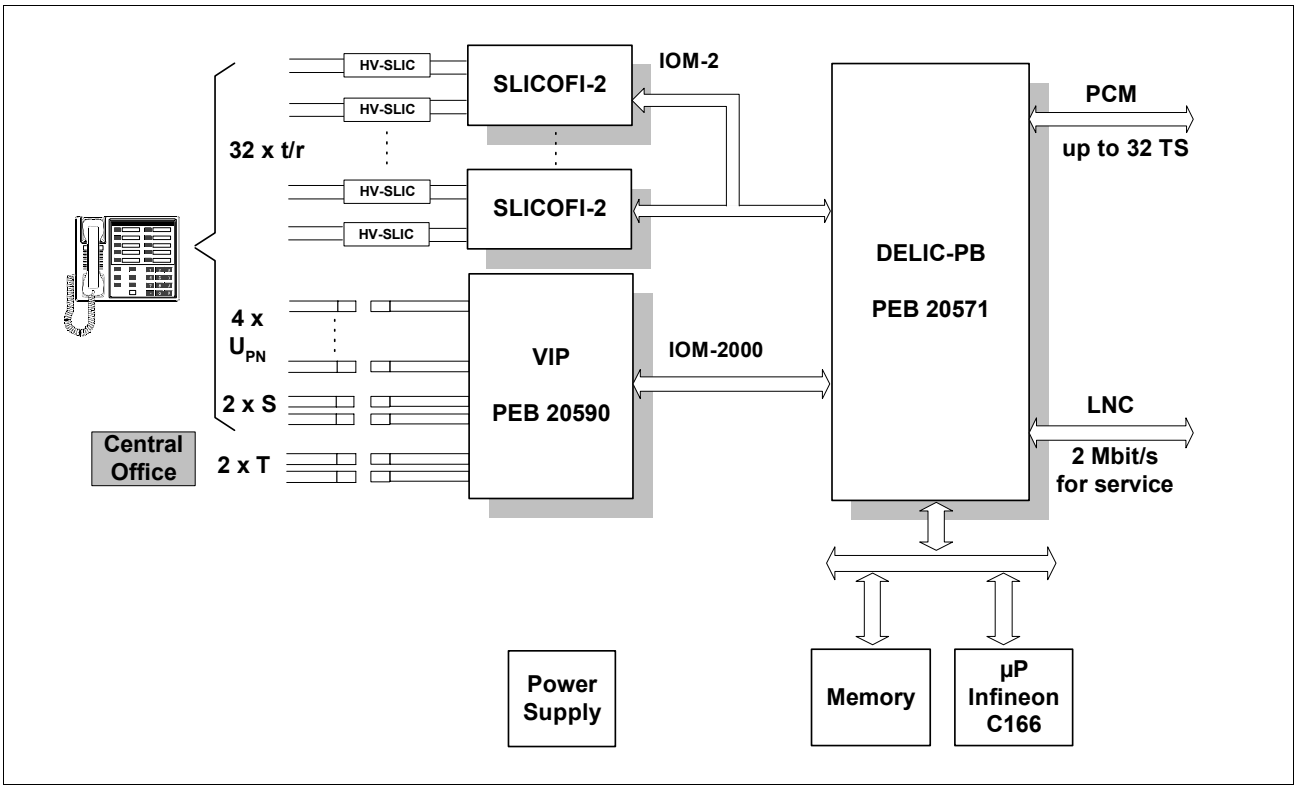


Figure 1-5 DELIC-PB in Small PBX

2 Pin Descriptions

2.1 Pin Diagram DELIC-LC

(top view)

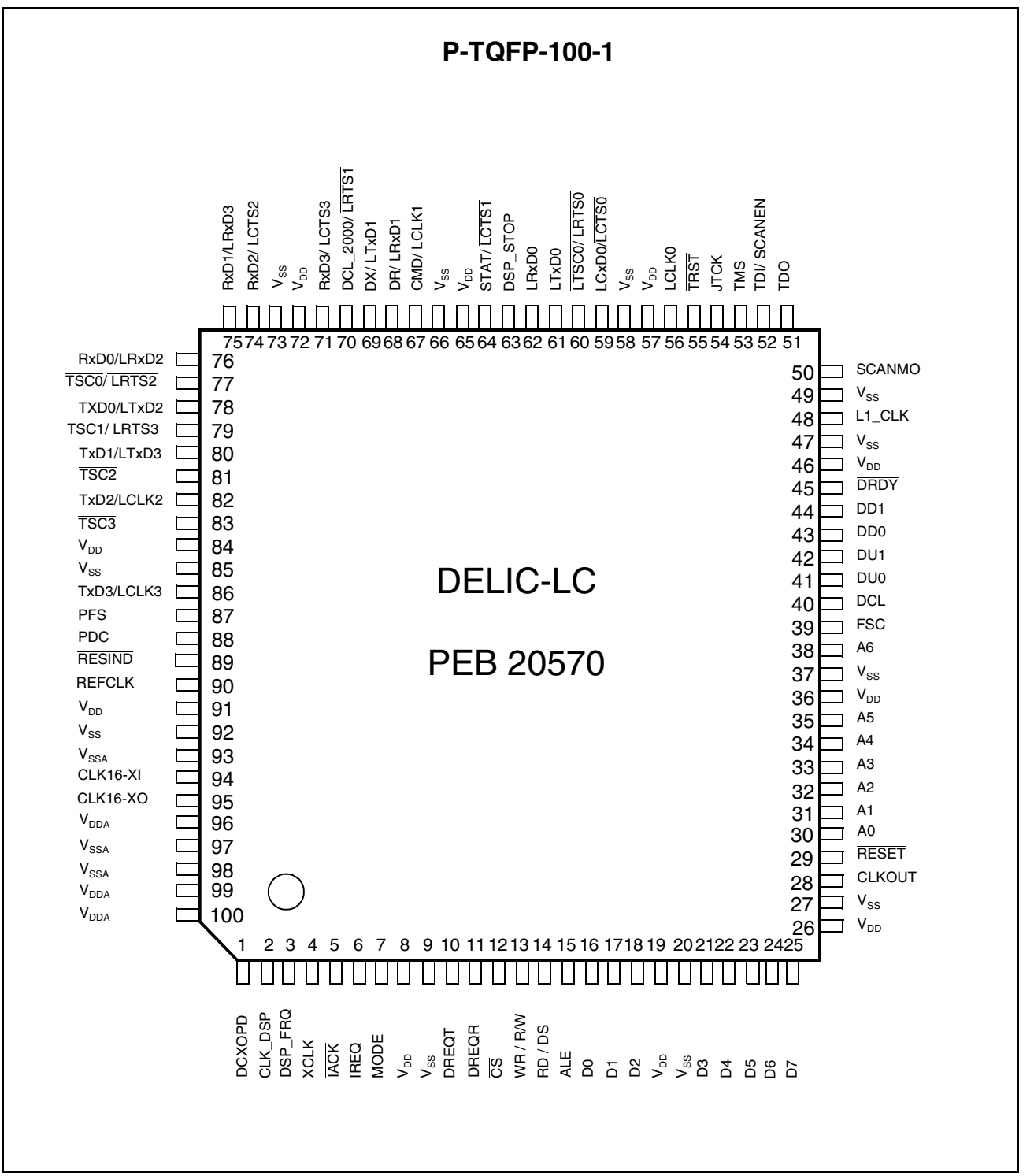


Figure 2-1 Pin Configuration DELIC-LC

2.2 Pin Diagram DELIC-PB

(top view)

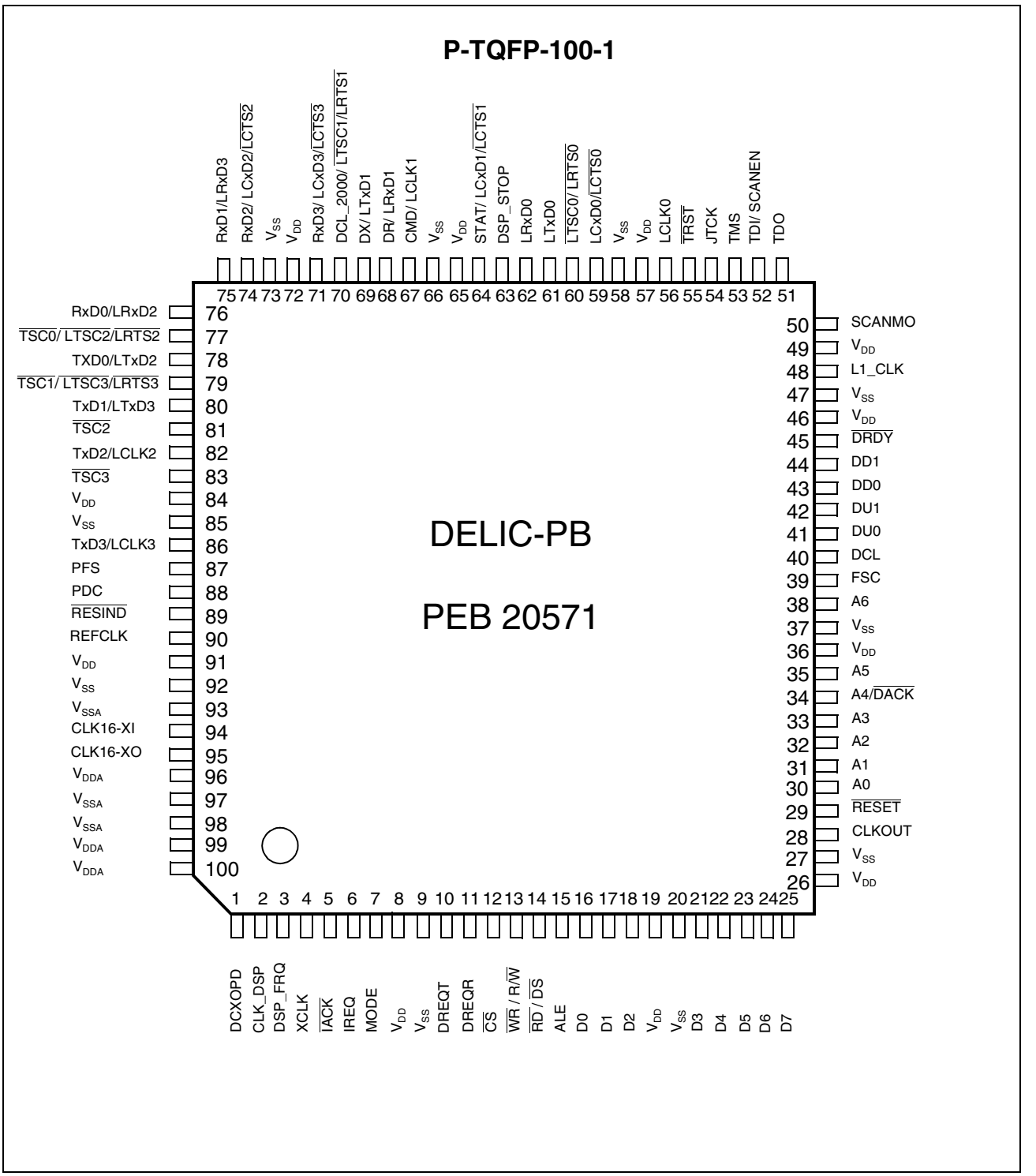


Figure 2-2 Pin Configuration DELIC-PB

2.3 Pin Definitions and Functions for DELIC-LC

*Note: The column "During Reset" refers to the time period that starts with activation of $\overline{RESET}$ input and ends with the deactivation of the $\overline{RESIND}$ output. During this period, the DELIC's strap pins (refer to **Table 2-19**) may be driven by external pull-down or pull-up resistors to define DELIC's configuration. If external pull-down or pull-up resistors are not connected to the strap pins, the value of each strap pin during reset will be determined by an internal pull-up or pull-down resistor, according to the default strap value of each pin.*
The user must ensure that connected circuits do not influence the sampling of the strap pins during reset.
The column "After Reset" describes the behavior of every pin, from the deactivation of the $\overline{RESIND}$ output until the DELIC's registers are programmed.

Table 2-1 IOM®-2 Interface Pins (DELIC-LC)

Pin No.	Symbol	In (I) Out(O)	During Reset	After Reset	Function
39	FSC	O	O	O	Frame Synchronization Clock (8 kHz) Used for both the IOM-2 and the IOM-2000 interface
40	DCL	O	TEST-Strap (3), (internal pull-up), refer to ***Table 2-19***	O	IOM-2 Data Clock 2.048 MHz or 4.096 MHz
43	DD0	O(OD)	High Z	High Z	Data Downstream IOM-2 Interface Channel0
44	DD1	O(OD)	High Z	High Z	Data Downstream IOM-2 Interface Channel1
41	DU0	I	I	I	Data Upstream IOM-2 Interface Channel 0
42	DU1	I	I	I	Data Upstream IOM-2 Interface Channel 1
45	$\overline{DRDY}$	I	I	I	D- Channel Ready Stop/Go information for D-channel control on S/T interface in LT-T. Affects only IOM-2 port 0. $\overline{DRDY}$ = 1 means GO $\overline{DRDY}$ = 0 means STOP

Table 2-2 IOM-2000 Interface / LNC Port 1 (DELIC-LC)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
70	DCL_2000 /	O	O	O	IOM-2000 Data Clock 3.072, 6.144 or 12.288 MHz
	$\overline{\text{LRTS1}}$	O			'request-to-send' functionality (Async mode)
69	DX /	O	High Z	High Z	Data Transmit Transmits IOM-2000 data to VIP
	LTxD1	O (OD)			LNC Transmit Serial Data Port 1 (Async mode).
68	DR /	I	I	I	Data Receive Receives IOM-2000 data from VIP
	LRxD1	I			LNC Receive Serial Data Port 1 (Async mode).
67	CMD /	O	High Z	High Z	IOM-2000 Command Transmits DELIC commands to VIP.
	LCLK1	I/O			LNC Clock Port 1. When configured as output may be driven at the following frequencies: 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz
64	STAT /	I	I	I	IOM-2000 Status Receives status information from VIP.
	$\overline{\text{LCTS1}}$	I			LNC1 Clear to Send 'clear-to-send' functionality (Async mode)

Table 2-3 LNC Port 0 (DELIC-LC)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
62	LRxD0	I	I	I	LNC Receive Serial Data Port 0 (HDLC and Async mode).
61	LTxD0	O (OD)	High Z	High Z	LNC Transmit Serial Data Port 0 (HDLC and Async mode).
60	$\overline{\text{LTSC0}}$ / $\overline{\text{LRTS0}}$	O	$\overline{\text{PLL-Bypass}}$" strap. Internal pull-up refer to page 2-28	H	LNC0 Tristate Control / Request to Send 2 modes per S/W selectable: 1) TxD output is valid (HDLC mode). Supplies a control signal for an external driver. ('low' when the corresponding TxD-output is valid). 2) 'request-to-send' functionality (Async mode)
59	LCxD0 / $\overline{\text{LCTS0}}$	I	I	I	LNC0 Collision Data / Clear to Send 2 modes per S/W selectable: 1) Collision Data (HDLC Mode). 2) 'clear-to-send' functionality (Async mode)
56	LCLK0	I/O	I	I	LNC Clock Port 0 When configured as output may be driven at the following frequencies: 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz

Table 2-4 Microprocessor Bus Interface Pins (DELIC-LC)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
25 24 23 22 21 18 17 16	D7 D6 D5 D4 D3 D2 D1 D0	I/O The direction of these pins depends on the value of the following pins: $\overline{CS}$, $\overline{RD}$/$\overline{DS}$, $\overline{WR}$ / R/$\overline{W}$ and MODE			Data Bus *Note: When operated in address/data multiplex mode, this bus is used as a multiplexed AD bus. The Address pins are externally connected to the AD bus.*
38 35 34 33 32 31 30	A6 A5 A4 A3 A2 A1 A0	I	I	I	Address Bus (bits 6 ... 0) *Note: When operated in address/data multiplex mode, this bus is used as a multiplexed AD bus. The Data pins are externally connected to the AD bus.*
11	DREQR	O	CLOCK MASTER Strap (internal pull-down), refer to **Table 2-19**	L	Strap pin
10	DREQT	O	EMUL-ATION BOOT Strap (internal pull-down), refer to **Table 2-19**	L	Strap pin
12	$\overline{CS}$	I	I	I	Chip Select A "low" on this line selects all registers for read/write operations.

Table 2-4 Microprocessor Bus Interface Pins (DELIC-LC) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
13	$\overline{WR}$/ R/$\overline{W}$	I	I	I	Write (Intel/Siemens Mode) Indicates a write access. Read/Write (Motorola Mode) Indicates the direction of the data transfer
14	$\overline{RD}$/ $\overline{DS}$	I	I	I	Read (Intel/Siemens Mode) Indicates a read access. Data Strobe (Motorola Mode) During a read cycle, $\overline{DS}$ indicates that the DELIC should place valid data on the bus. During a write access, $\overline{DS}$ indicates that valid data is on the bus.
15	ALE	I	I	I	Address Latch Enable Controls the on-chip address latch in multiplexed bus mode. While ALE is 'high', the latch is transparent. The falling edge latches the current address. ALE is also evaluated to determine the bus mode ('low'=multiplexed, 'high'=demultiplexed)
7	MODE	I	I	I	Bus Mode Selection Selects the µP bus mode ('low'=Intel/Infineon, 'high'=Motorola)
6	IREQ	O (OD)	High Z (OD)	High Z (OD)	Interrupt Request is programmable to push/pull (active high or low) or open-drain. This signal is activated when the DELIC requests a µP interrupt. When operated in open drain mode, multiple interrupt sources may be connected.
5	$\overline{IACK}$	I	I	I	Interrupt Acknowledge

Table 2-4 Microprocessor Bus Interface Pins (DELIC-LC) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
29	$\overline{\text{RESET}}$	I	I	I	System Reset DELIC is forced to go into reset state.
89	$\overline{\text{RESIND}}$	O	O	O	Reset Indication Indicates that the DELIC is executing a reset. The DELIC remains in reset state for at least 500 µs after the termination of the $\overline{\text{RESET}}$ pulse.

Table 2-5 PCM Interface Ports 0 ... 3 / LNC Ports 2 ... 3 (DELIC-LC)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
87	PFS	I/O	I	I	PCM Frame Synchronization Clock. 8 kHz/4 kHz when input or 8 kHz when output. *Note: When PFS is configured as 4 kHz input, PDC configuration is restricted to 2.048 MHz input.*
88	PDC	I/O	I	I	PCM Data Clock (input or output) 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz
76	RxD0 / LRxD2	I I	I	I	PCM Receive Data Port 0 LNC Receive Serial Data Port 2 (Async mode)
78	TxD0 / LTxD2	O O(OD)	High Z	High Z	PCM Transmit Data Port 0 LNC Transmit Serial Data Port 2 Async mode)

Table 2-5 PCM Interface Ports 0 ... 3 / LNC Ports 2 ... 3 (DELIC-LC) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
77	$\overline{\text{TSC0}}$ /	O	$\overline{\text{Reset}}$ $\overline{\text{Counter}}$ $\overline{\text{Bypass}}$" strap Internal pull-up refer to **page 2-28**	H	PCM Tristate Control Port 0 Supplies a control signal for an external driver ('low' when the corresponding TxD-output is valid).
	$\overline{\text{LRTS2}}$	O			LNC2 Tristate Control / Request To Send 'request-to-send' functionality (Async mode)
74	RxD2 /	I	I	I	PCM Receive Data Port 2
	$\overline{\text{LCTS2}}$	I			LNC2 'clear-to-send' functionality (Async mode)
82	TxD2 /	O	weak low	weak low	PCM Transmit Data Port 2
	LCLK2	I/O			LNC External Clock Port 2 When configured as output may be driven at the following frequencies: 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz
81	$\overline{\text{TSC2}}$	O	TEST(1) strap refer to **page 2-28**	H	PCM Tristate Control Port 2 Supplies a control signal for an external driver ('low' when the corresponding TxD-output is valid).
75	RxD1 /	I	I	I	PCM Receive Data Port 1
	LRxD3	I			LNC Receive Serial Data Port 3 (Async mode)
80	TxD1 /	O	High Z	High Z	PCM Transmit Data Port 1
	LTxD3	O(OD)			LNC Transmit Serial Data Port 3 (Async mode)

Table 2-5 PCM Interface Ports 0 ... 3 / LNC Ports 2 ... 3 (DELIC-LC) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
79	$\overline{\text{TSC1}}$ /	O	$\overline{\text{PLL}}$ $\overline{\text{Power-Down}}$ strap Internal pull-up refer to **page 2-28**	H	PCM Tristate Control Port 1 Supplies a control signal for an external driver (’low’ when the corresponding TxD-output is valid).
	$\overline{\text{LRTS3}}$				LNC3 Request to Send ’request-to-send’ functionality (Async mode)
71	RxD3 /	I	I	I	PCM Receive Data Port 3
	$\overline{\text{LCTS3}}$	I			LNC3 ’clear-to-send’ functionality (Async mode)
86	TxD3 /	O	weak low	weak low	PCM Transmit Data Port 3
	LCLK3	I/O			LNC External Clock Port 3 When configured as output may be driven at the following frequencies: 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz
83	$\overline{\text{TSC3}}$	O	TEST(1) strap refer to **page 2-28**	H	PCM Tristate Control Port 3 Supplies a control signal for an external driver (’low’ when the corresponding TxD output is valid).

Table 2-6 Clock Generator Pins (DELIC-LC) (additionally to IOM/PCM clocks)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
94	CLK16-XI	I	I	I	16.384 MHz External Crystal Input
95	CLK16-XO	O	O	O	16.384 MHz External Crystal Output
1	DCXOPD	I	I	I	DCXO Power Down and Bypass Activating this input powers down the on-chip DCXO PLL. The input CLK16-XI is used directly as the internal 16.384 MHz clock, and the oscillator and the shaper are bypassed. Required for testing; during normal operation this input should be permanently low (‘0’).
2	CLK_DSP	I	I	I	External DSP Clock Provides a DSP clock other than 61.44 MHz from an external oscillator.
3	DSP_FRQ	I	I	I	DSP Operational Frequency Selection (e.g. for test purpose) 0: The DSP is clocked internally at 61.44 MHz 1: The DSP clock is driven by the CLK_DSP input pin
48	L1_CLK	O	O	O	Layer-1 Clock 15.36 MHz or 7.68 MHz
28	CLKOUT	O	O	O	General Purpose Clock Output 2.048 MHz, 4.096 MHz, 8.192 MHz, 15.36 MHz or 16.384 MHz
4	XCLK	I	I	I	External Reference Clock Synchronization input from Layer-1 ICs (8 kHz, 512 kHz or 1.536 MHz) This pin is connected to the VIP’s REFCLK output at 1.536 MHz.
90	REFCLK	I/O	I	I	Reference Clock Input: Synchronization of DELIC clock system Output: Used to drive a fraction of XCLK to the system clock master (8 kHz or 512 kHz programmable)

Table 2-7 Power Supply Pins (DELIC-LC)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
8 19 26 36 46 57 65 72 84 91	V_{DD}	I	I	I	Power Supply 3.3 V Used for core logic and interfaces in pure 3.3 V environment
9 20 27 37 47 49 58 66 73 85 92	V_{SS}	I	I	I	Digital Ground (0 V)
96 99 100	V_{DDA}	I	I	I	Power Supply 3.3 V Analog Logic Used for DCXO and PLL
93 97 98	V_{SSA}	I	I	I	Analog Ground Used for DCXO and PLL

Table 2-8 JTAG and Emulation Interface Pins (DELIC-LC)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
Used for boundary scan according to IEEE 1149.1					
54	JTCK	I	I	I	JTAG Test Clock Provides the clock for JTAG test logic. Used also for serial emulation interface.
53	TMS	I	I	I	Test Mode Select A '0' to '1' transition on this pin is required to step through the TAP controller state machine.
52	TDI / SCANEN	I	I	I	Test Data Input In the appropriate TAP controller state test data or a instruction is shifted in via this line. Used also for serial emulation interface. *Note: This pin must not be driven to low on the board during reset and operation to ensure functioning of DELIC* SCAN Enable When both SCANMO and SCANEN are asserted, the full-scan tests of DELIC are activated. Not used during normal operation.
51	TDO	O	O	O	Test Data Output In the appropriate TAP controller state test data or an instruction is shifted out via this line. Used also for serial emulation interface.

Table 2-8 JTAG and Emulation Interface Pins (DELIC-LC) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
55	$\overline{\text{TRST}}$	I	I	I	Test Reset Provides an asynchronous reset to the TAP controller state machine.
63	DSP_STOP	O	$\overline{\text{BOOT}}$ Strap (internal pull-down) refer to **Table 2-19**	O	DSP Stop Pin Stops external logic during breakpoints. Activated when a stop to the DSP is issued.

Table 2-9 Test Interface Pins (DELIC-LC)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
50	SCANMO	I	I	I	Scan Mode If driven to '1' during device tests, TDI input is used as enable for full scan tests of the DELIC. SCANMO should be tied to GND during normal operation.

2.4 Pin Definitions and Functions for DELIC-PB

*Note: The column "During Reset" refers to the time period that starts with activation of $\overline{RESET}$ input and ends with the deactivation of the $\overline{RESIND}$ output. During this period, the DELIC's strap pins (refer to **Table 2-19**) may be driven by external pull-down or pull-up resistors to define DELIC's configuration. If external pull-down or pull-up resistors are not connected to the strap pins, the value of each strap pin during reset will be determined by an internal pull-up or pull-down resistor, according to the default strap value of each pin.*
The user must ensure that connected circuits do not influence the sampling of the strap pins during reset.
The column "After Reset" describes the behavior of every pin, from the deactivation of the $\overline{RESIND}$ output until the DELIC's registers are programmed.

Table 2-10 IOM®-2 Interface Pins (DELIC-PB)

Pin No.	Symbol	In (I) Out(O)	During Reset	After Reset	Function
39	FSC	O	O	O	Frame Synchronization Clock (8 kHz) Used for both the IOM-2 and the IOM-2000 interface
40	DCL	O	TEST-Strap (3), (internal pull-up), refer to **Table 2-19**	O	IOM-2 Data Clock 2.048 MHz or 4.096 MHz
43	DD0	O(OD)	High Z	High Z	Data Downstream IOM-2 Interface Channel0
44	DD1	O(OD)	High Z	High Z	Data Downstream IOM-2 Interface Channel1
41	DU0	I	I	I	Data Upstream IOM-2 Interface Channel 0
42	DU1	I	I	I	Data Upstream IOM-2 Interface Channel 1
45	$\overline{DRDY}$	I	I	I	D- Channel Ready Stop/Go information for D-channel control on S/T interface in LT-T. Affects only IOM-2 port 0. $\overline{DRDY}$ = 1 means GO $\overline{DRDY}$ = 0 means STOP

Table 2-11 IOM-2000 Interface / LNC Port 1 (DELIC-PB)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
70	DCL_2000 /	O	O	O	IOM-2000 Data Clock 3.072, 6.144 or 12.288 MHz
	$\overline{\text{LTSC1}}$/ $\overline{\text{LRTS1}}$	O			LNC1 Tristate Control /Request to Send 2 modes per S/W selectable: 1) TxD output is valid (HDLC mode). Supplies a control signal for an external driver. (’low’ when the corresponding TxD-output is valid). 2) ’request-to-send’ functionality (Async mode)
69	DX /	O	High Z	High Z	Data Transmit Transmits IOM-2000 data to VIP
	LTxD1	O (OD)			LNC Transmit Serial Data Port 1 (HDLC and Async mode).
68	DR /	I	I	I	Data Receive Receives IOM-2000 data from VIP
	LRxD1	I			LNC Receive Serial Data Port 1 (HDLC and Async mode).
67	CMD /	O	High Z	High Z	IOM-2000 Command Transmits DELIC commands to VIP.
	LCLK1	I/O			LNC Clock Port 1. When configured as output may be driven at the following frequencies: 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz
64	STAT /	I	I	I	IOM-2000 Status Receives status information from VIP.
	LCxD1/ $\overline{\text{LCTS1}}$	I			LNC1 Collision Data / Clear to Send 1) Collision Data (HDLC Mode). 2) ’clear-to-send’ functionality (Async mode)

Table 2-12 LNC Port 0 (DELIC-PB)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
62	LRxD0	I	I	I	LNC Receive Serial Data Port 0 (HDLC and Async mode).
61	LTxD0	O (OD)	High Z	High Z	LNC Transmit Serial Data Port 0 (HDLC and Async mode).
60	$\overline{\text{LTSC0}}$ / $\overline{\text{LRTS0}}$	O	$\overline{\text{PLL-Bypass}}$" strap. Internal pull-up refer to page 2-28	H	LNC0 Tristate Control / Request to Send 2 modes per S/W selectable: 1) TxD output is valid (HDLC mode). Supplies a control signal for an external driver. ('low' when the corresponding TxD-output is valid). 2) 'request-to-send' functionality (Async mode)
59	LCxD0 / $\overline{\text{LCTS0}}$	I	I	I	LNC0 Collision Data / Clear to Send 2 modes per S/W selectable: 1) Collision Data (HDLC Mode). 2) 'clear-to-send' functionality (Async mode)
56	LCLK0	I/O	I	I	LNC Clock Port 0 When configured as output may be driven at the following frequencies: 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz

Table 2-13 Microprocessor Bus Interface Pins (DELIC-PB)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
25 24 23 22 21 18 17 16	D7 D6 D5 D4 D3 D2 D1 D0	I/O The direction of these pins depends on the value of the following pins: $\overline{CS}$, $\overline{RD}$/$\overline{DS}$, $\overline{WR}$ / R/$\overline{W}$ and MODE			Data Bus *Note: When operated in address/data multiplex mode, this bus is used as a multiplexed AD bus. The Address pins are externally connected to the AD bus.*
38 35 33 32 31 30	A6 A5 A3 A2 A1 A0	I	I	I	Address Bus (bits 6 ... 0 except bit 4) *Note: When operated in address/data multiplex mode, this bus is used as a multiplexed AD bus. The Data pins are externally connected to the AD bus.* *Note: In non-DMA mode $\overline{DACK}$/A4 input pin should be connected to A4 of the µP address-bus. In DMA mode A4 is internally connected to '0'.*
34	A4 $\overline{DACK}$/	I	I	I	DMA Acknowledge Bit 4 of the address bus, when the DELIC is configured to non-DMA mode. *Note: In DMA mode A4 is internally connected to '0'.*
11	DREQR	O	CLOCK MASTER Strap (internal pull-down), refer to **Table 2-19**	L	DMA Request for Receive Direction *Note: May be configured to active high or active low (the default is active high)*

Table 2-13 Microprocessor Bus Interface Pins (DELIC-PB) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
10	DREQT	O	EMUL-ATION BOOT Strap (internal pull-down), refer to **Table 2-19**	L	DMA Request for Transmit Direction *Note: May be configured to active high or active low (the default is active high)*
12	$\overline{CS}$	I	I	I	Chip Select A "low" on this line selects all registers for read/write operations.
13	$\overline{WR}$/ R/$\overline{W}$	I	I	I	Write (Intel/Siemens Mode) Indicates a write access. Read/Write (Motorola Mode) Indicates the direction of the data transfer
14	$\overline{RD}$/ $\overline{DS}$	I	I	I	Read (Intel/Siemens Mode) Indicates a read access. Data Strobe (Motorola Mode) During a read cycle, $\overline{DS}$ indicates that the DELIC should place valid data on the bus. During a write access, $\overline{DS}$ indicates that valid data is on the bus.
15	ALE	I	I	I	Address Latch Enable Controls the on-chip address latch in multiplexed bus mode. While ALE is 'high', the latch is transparent. The falling edge latches the current address. ALE is also evaluated to determine the bus mode ('low'=multiplexed, 'high'=demultiplexed)
7	MODE	I	I	I	Bus Mode Selection Selects the µP bus mode ('low'=Intel/Infineon, 'high'=Motorola)

Table 2-13 Microprocessor Bus Interface Pins (DELIC-PB) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
6	IREQ	O (OD)	High Z (OD)	High Z (OD)	Interrupt Request is programmable to push/pull (active high or low) or open-drain. This signal is activated when the DELIC requests a µP interrupt. When operated in open drain mode, multiple interrupt sources may be connected.
5	$\overline{\text{IACK}}$	I	I	I	Interrupt Acknowledge
29	$\overline{\text{RESET}}$	I	I	I	System Reset DELIC is forced to go into reset state.
89	$\overline{\text{RESIND}}$	O	O	O	Reset Indication Indicates that the DELIC is executing a reset. The DELIC remains in reset state for at least 500 µs after the termination of the $\overline{\text{RESET}}$ pulse.

Table 2-14 PCM Interface Ports 0 ... 3 / LNC Ports 2 ... 3 (DELIC-PB)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
87	PFS	I/O	I	I	PCM Frame Synchronization Clock. 8 kHz/4 kHz when input or 8 kHz when output. *Note: When PFS is configured as 4 kHz input, PDC configuration is restricted to 2.048 MHz input.*
88	PDC	I/O	I	I	PCM Data Clock (input or output) 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz
76	RxD0 / LRxD2	I I	I	I	PCM Receive Data Port 0 LNC Receive Serial Data Port 2 (HDLC and Async mode)
78	TxD0 / LTxD2	O O(OD)	High Z	High Z	PCM Transmit Data Port 0 LNC Transmit Serial Data Port 2 (HDLC and Async mode)

Table 2-14 PCM Interface Ports 0 ... 3 / LNC Ports 2 ... 3 (DELIC-PB) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
77	$\overline{\text{TSC0}}$ /	O	$\overline{\text{Reset}}$ $\overline{\text{Counter}}$ $\overline{\text{Bypass}}$" strap Internal pull-up refer to **page 2-28**	H	PCM Tristate Control Port 0 Supplies a control signal for an external driver ('low' when the corresponding TxD-output is valid).
	$\overline{\text{LTSC2}}$/ $\overline{\text{LRTS2}}$	O			LNC2 Tristate Control / Request To Send 2 modes per S/W selectable: 1) TxD output is valid (HDLC mode). Supplies a control signal for an external driver. ('low' when the corresponding TxD-output is valid). 2) 'request-to-send' functionality (Async mode)
74	RxD2 /	I	I	I	PCM Receive Data Port 2
	LCxD2/ $\overline{\text{LCTS2}}$	I			LNC2 Collision Data 2 modes per S/W selectable: 1) Collision Data (In HDLC Mode). 2) 'clear-to-send' functionality (Async mode)
82	TxD2 /	O	weak low	weak low	PCM Transmit Data Port 2
	LCLK2	I/O			LNC External Clock Port 2 When configured as output may be driven at the following frequencies: 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz
81	$\overline{\text{TSC2}}$	O	TEST(1) strap refer to **page 2-28**	H	PCM Tristate Control Port 2 Supplies a control signal for an external driver ('low' when the corresponding TxD-output is valid).

Table 2-14 PCM Interface Ports 0 ... 3 / LNC Ports 2 ... 3 (DELIC-PB) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
75	RxD1 / LRxD3	I I	I	I	PCM Receive Data Port 1 LNC Receive Serial Data Port 3 (HDLC and Async mode)
80	TxD1 / LTxD3	O O(OD)	High Z	High Z	PCM Transmit Data Port 1 LNC Transmit Serial Data Port 3 (HDLC and Async mode)
79	$\overline{\text{TSC1}}$ / $\overline{\text{LTSC3}}$/ $\overline{\text{LRTS3}}$	O	$\overline{\text{PLL}}$ $\overline{\text{Power-Down}}$ strap Internal pull-up refer to **page 2-28**	H	PCM Tristate Control Port 1 Supplies a control signal for an external driver (’low’ when the corresponding TxD-output is valid). LNC3 Tristate Control / Request to Send 2 modes per S/W selectable: 1) TxD output is valid (HDLC mode). Supplies a control signal for an external driver. (’low’ when the corresponding TxD-output is valid). 2) ’request-to-send’ functionality (Async mode)
71	RxD3 / LCxD3/ $\overline{\text{LCTS3}}$	I I	I	I	PCM Receive Data Port 3 LNC3 Collision Data 2 modes per S/W selectable: 1) Collision Data (HDLC Mode). 2) ’clear-to-send’ functionality (Async mode)

Table 2-14 PCM Interface Ports 0 ... 3 / LNC Ports 2 ... 3 (DELIC-PB) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
86	TxD3 / LCLK3	O I/O	weak low	weak low	PCM Transmit Data Port 3 LNC External Clock Port 3 When configured as output may be driven at the following frequencies: 2.048 MHz, 4.096 MHz, 8.192 MHz, 16.384 MHz
83	$\overline{\text{TSC3}}$	O	TEST(1) strap refer to **page 2-28**	H	PCM Tristate Control Port 3 Supplies a control signal for an external driver (’low’ when the corresponding TxD output is valid).

Table 2-15 Clock Generator Pins (DELIC-PB) (additionally to IOM/PCM clocks)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
94	CLK16-XI	I	I	I	16.384 MHz External Crystal Input
95	CLK16-XO	O	O	O	16.384 MHz External Crystal Output
1	DCXOPD	I	I	I	DCXO Power Down and Bypass Activating this input powers down the on-chip DCXO PLL. The input CLK16-XI is used directly as the internal 16.384 MHz clock, and the oscillator and the shaper are bypassed. Required for testing; during normal operation this input should be permanently low (‘0’).
2	CLK_DSP	I	I	I	External DSP Clock Provides a DSP clock other than 61.44 MHz from an external oscillator.
3	DSP_FRQ	I	I	I	DSP Operational Frequency Selection (e.g. for test purpose) 0: The DSP is clocked internally at 61.44 MHz 1: The DSP clock is driven by the CLK_DSP input pin
48	L1_CLK	O	O	O	Layer-1 Clock 15.36 MHz or 7.68 MHz
28	CLKOUT	O	O	O	General Purpose Clock Output 2.048 MHz, 4.096 MHz, 8.192 MHz, 15.36 MHz or 16.384 MHz
4	XCLK	I	I	I	External Reference Clock Synchronization input from Layer-1 ICs (8 kHz, 512 kHz or 1.536 MHz) This pin is connected to the VIP’s REFCLK output at 1.536 MHz.
90	REFCLK	I/O	I	I	Reference Clock Input: Synchronization of DELIC clock system Output: Used to drive a fraction of XCLK to the system clock master (8 kHz or 512 kHz programmable)

Table 2-16 Power Supply Pins (DELIC-PB)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
8 19 26 36 46 49 57 65 72 84 91	V_{DD}	I	I	I	Power Supply 3.3 V Used for core logic and interfaces in pure 3.3 V environment
9 20 27 37 47 58 66 73 85 92	V_{SS}	I	I	I	Digital Ground (0 V)
96 99 100	V_{DDA}	I	I	I	Power Supply 3.3 V Analog Logic Used for DCXO and PLL
93 97 98	V_{SSA}	I	I	I	Analog Ground Used for DCXO and PLL

Table 2-17 JTAG and Emulation Interface Pins (DELIC-PB)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
Used for boundary scan according to IEEE 1149.1					
54	JTCK	I	I	I	JTAG Test Clock Provides the clock for JTAG test logic. Used also for serial emulation interface.
53	TMS	I	I	I	Test Mode Select A ’0’ to ’1’ transition on this pin is required to step through the TAP controller state machine.
52	TDI / SCANEN	I	I	I	Test Data Input In the appropriate TAP controller state test data or a instruction is shifted in via this line. Used also for serial emulation interface. *Note: This pin must not be driven to low on the board during reset and operation to ensure functioning of DELIC* SCAN Enable When both SCANMO and SCANEN are asserted, the full-scan tests of DELIC are activated. Not used during normal operation.
51	TDO	O	O	O	Test Data Output In the appropriate TAP controller state test data or an instruction is shifted out via this line. Used also for serial emulation interface.

Table 2-17 JTAG and Emulation Interface Pins (DELIC-PB) (Continued)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
55	$\overline{\text{TRST}}$	I	I	I	Test Reset Provides an asynchronous reset to the TAP controller state machine.
63	DSP_STOP	O	$\overline{\text{BOOT}}$ Strap (internal pull-down) refer to **Table 2-19**	O	DSP Stop Pin Stops external logic during breakpoints. Activated when a stop to the DSP is issued.

Table 2-18 Test Interface Pins (DELIC-PB)

Pin No.	Symbol	In (I) Out (O)	During Reset	After Reset	Function
50	SCANMO	I	I	I	Scan Mode If driven to '1' during device tests, TDI input is used as enable for full scan tests of the DELIC. SCANMO should be tied to GND during normal operation.

2.5 Strap Pin Definitions

Table 2-19 Strap Pins (Evaluated During Reset)

Pin No.	Strap Name	Strap Function	
DREQR (11)	CLOCK MASTER	0: (default)	Clock Slave PDC and PFS are used as inputs. PDC = 2.048 MHz PFS = 4 kHz
		1:	Clock Master PDC and PFS are used as outputs. PDC = 2.048 MHz PFS = 8 kHz
DSP_STOP (63)	$\overline{\text{BOOT}}$	0: (default)	The DSP starts running from address $FFFE_H$, and executes the µP boot routine.
		1:	The DSP starts running directly from address 0000_H. The boot routine is not executed.
DCL (40): $\overline{\text{TSC3}}$ (83): $\overline{\text{TSC2}}$ (81)	TEST (3:1)	111 or 110: (default)	Regular Work Mode
		101	Test mode 1
		100	Test mode 2
		011	Test mode 3
		010	Test mode 4
		001	Test mode 5
DREQT (10)	EMULATION BOOT	0: (default)	After reset the boot-routine loads the program RAM via the µP-interface (via the general mail-box).
		1:	After reset the boot-routine loads the program RAM via the CDI mail-box (via the JTAG interface).
$\overline{\text{LTSC}}$ (60)	$\overline{\text{PLL BYPASS}}$	0:	DSP_CLK input pin (the DSP fall-back clock) is used as source for the 61 MHz clock division chain. (Only for testing).
		1: (default)	The PLL output is used as the source for the 61 MHz clock division chain.

Table 2-19 Strap Pins (Evaluated During Reset) (Continued)

$\overline{\text{TSC1}}$ (79)	$\overline{\text{PLL POWER DOWN}}$	0:	The PLL is powered-down. (for IDDQ tests)
		1: (default)	The PLL is on.
$\overline{\text{TSC0}}$ (77)	$\overline{\text{RESET COUNTER BYPASS}}$	0:	The reset-counter is bypassed, thus the internal reset is the filtered reset. The internal reset lasts 1-2 16 MHz cycles after a deactivation of $\overline{\text{RESET}}$.
		1: (default)	The internal reset lasts 4-5 8 kHz cycles (> 500 µs) after a deactivation of $\overline{\text{RESET}}$

Note: When the strap pins are not driven externally during reset, they are driven by internal pull-ups/pull-downs. To reduce power consumption, the internal pull-up/pull-down resistors are connected only during activated $\overline{\text{RESET}}$ input.
To ensure the default value of the straps, the pins must not be driven during reset. In case of fixed external pull-up/pull-down, a pull-up/pull-down resistance of 10 KΩ +/-10% is recommended.

3 Interface Description

3.1 Overview of Interfaces

The DELIC provides the following system interfaces:

IOM-2000 Interface

- A new serial layer 1 interface driving up to three VIP/ VIP8 (Versatile ISDN Port, PEB 20590/ PEB 20591). Each VIP provides eight 2B+D ISDN channels, which can be programmed via IOM-2000 to S/T mode or U_{PN} mode.

IOM-2 (GCI) Interface

- Two standard IOM-2 (GCI) ports with eight 2B+D ISDN channels each, at a data rate of up to 2 x 2.048 Mbit/s. They can be combined to a 4.096 Mbit/s highway.

PCM Interface

- Four standard Master/Slave PCM interfaces with up to 32 time slots each, at a data rate of up to 4 x 2.048 Mbit/s. They can be combined to two 4.096 Mbit/s highways or one 8.192 Mbit/s highway. Additionally, 128 time slots of 256 time slots per 8 kHz frame can be transmitted at a rate of 16.384 Mbit/s.

Serial Communication Interface (GHDLC)

- An asynchronous serial port supporting HDLC formatted data frames at a data rate of up to 16.384 Mbit/s.

Microprocessor Interface

- A standard 8-bit multiplexed/de-multiplexed µP interface, compatible to Intel/Siemens (e.g. 80386EX, C166) and Motorola (e.g. 68340, 801) bus systems. It includes two separate mailboxes, one for normal data transfer, and one for fast DMA transfers.

JTAG Boundary Scan Test Interface

- DELIC provides a standard test interface according to IEEE 1149.1. The 4-bit TAP controller has an own reset input.
- The JTAG pins TDI, TDO and JTCK may also be used as interface for DSP emulation.

3.2 IOM-2000 Interface

3.2.1 Overview

The IOM-2000 interface represents a new concept for connecting ISDN layer-1 devices to the DELIC. The transceiver unit (TRANSIU) and the DSP perform the layer-1 protocol, which enables flexible and efficient operation of the transceiver IC (VIP/ VIP8).

VIP/ VIP8 supports two types of ISDN interfaces: 2-wire (ping-pong) U_{PN} interfaces and 4-wire S/T interfaces. For detailed description please refer to VIP/ VIP8 Data Sheet.

The IOM-2000 interface consists of the following signals:

- **Frame Synchronization:** IOM-2000 uses the same 8 kHz FSC as the IOM-2 ports.
- **Data Interface:** Data is transmitted via DX line from DELIC to VIP with DCL_2000 rising edge. Data is received via DR line from VIP to DELIC, sampled with DCL_2000 falling edge.
- **Command/Status Interface:** Configuration and control information of VIP's layer-1 transceivers is exchanged via CMD and STAT lines.
- **Data/Command Clock:** Data and commands for one VIP are transmitted at 3.072 MHz. When DELIC drives 2 or 3 VIPs, the transmission rate is increased.
- **Reference Clock:** In LT-T mode, the VIP provides a reference clock synchronized to the exchange. In LT-S or U_{PN} mode, DELIC is always the clock master to VIP.

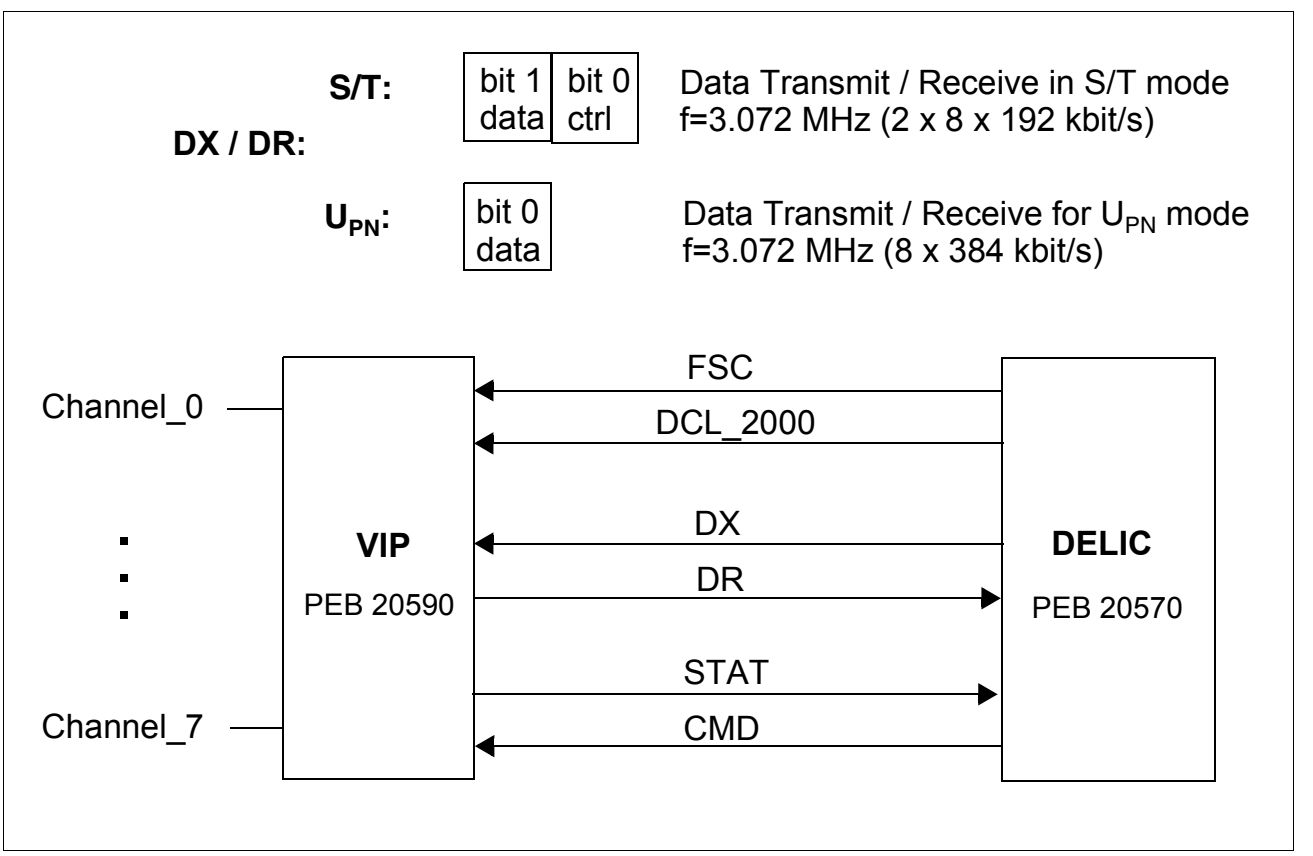


Figure 3-1 Overview of IOM-2000 Interface Structure (Example with One VIP)

3.2.2 IOM-2000 Frame Structure

3.2.2.1 Data Interface

On the ISDN line side of the VIP, data is ternary coded. Since the VIP contains logic to detect the level of the signal, only the data value is transferred via IOM-2000 to DELIC.

U_{PN} Mode

- In U_{PN} mode, only data is sent via the IOM-2000 data interface.

S/T Mode

- In S/T mode, data and control information is sent via IOM-2000 data interface. Every data bit has a control bit associated with it. Thus, for each S/T line signal, 2 bits are transferred via DX and DR. Bit0 is assigned to the user data, and bit1 carries control information.

Table 3-1 Control Bits in S/T Mode on DR Line

ctrl (bit1)	data (bit0)	Function
0	0	Logical ’0’ received on line interface
0	1	Logical ’1’ received on line interface
1	0	Received E-bit = inverted transmitted D-bit (E=$\overline{D}$) (LT-T only)
1	1	F-bit (Framing) received; indicates the start of the S frame

Table 3-2 Control Bits in S/T Mode on DX Line

ctrl (bit1)	data (bit0)	Function
0	0	Logical ’0’ transmitted on line interface
0	1	Logical ’1’ transmitted on line interface
1	0	not used
1	1	F-bit (Framing) transmitted; indicates the start of the S frame

*Note: ’data’ is always transmitted prior to ’ctrl’ via DX/DR lines (refer to **Figure 3-2**).*

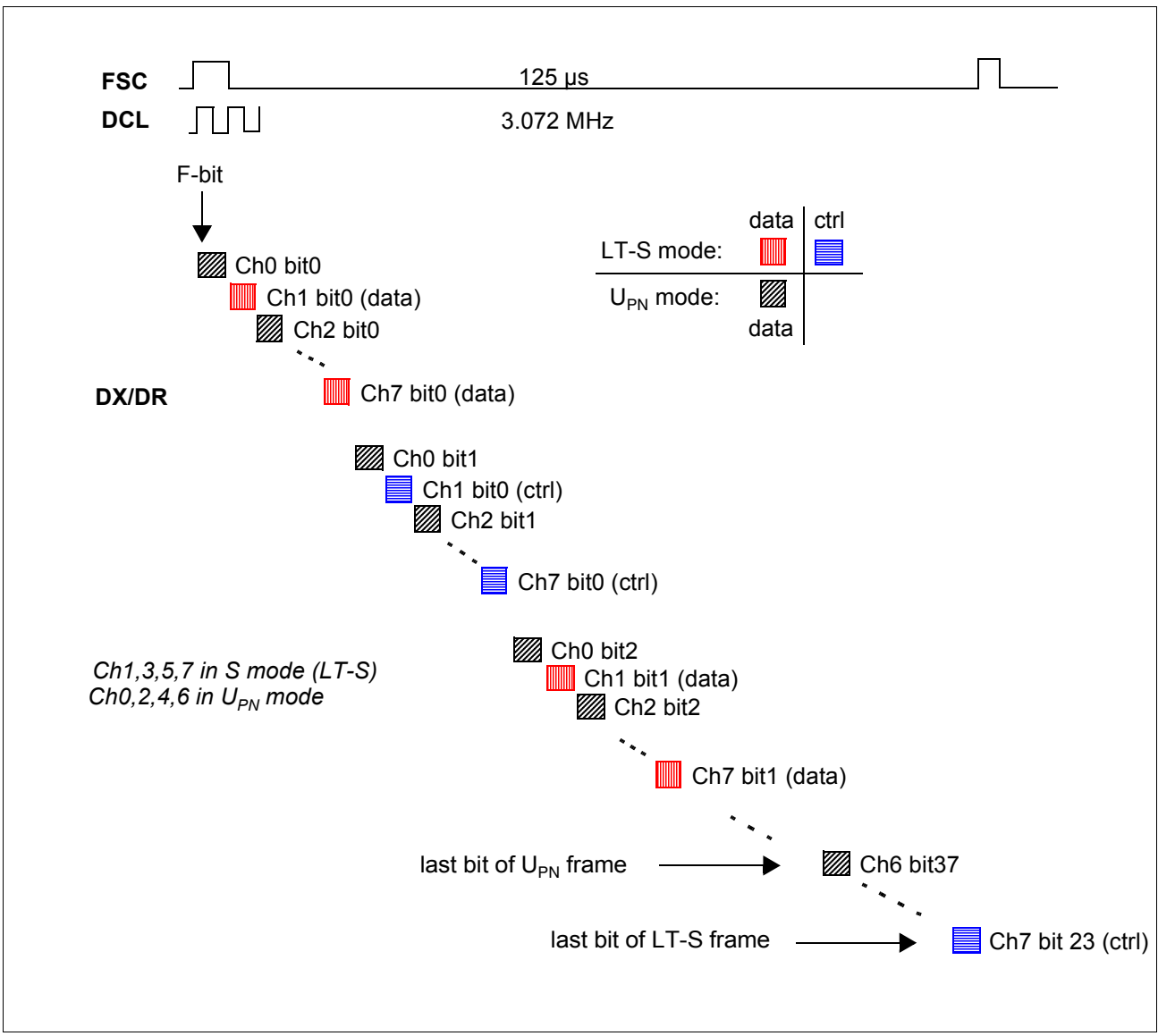


Figure 3-2 IOM-2000 Data Sequence (1 VIP with 8 Channels)

Note: 1. Data transfer on IOM-2000 interface always starts with the MSB (related to B channels), whereas CMD and STAT bits transfer always starts with LSB (bit 0) of any register

2. All registers follow the Intel structure (LSB=2^0, MSB=2^{31})

3. Unused bits are don't care ('x')

4. The order of reception or transmission of each VIP channel is always channel 0 to channel 7. A freely programmable channel assignment of multiple VIPs on IOM-2000 (e.g., ch0 of VIP_0, ch1 of VIP_0, ch0 of VIP_1, ch2 of VIP_0, ...) is not possible.

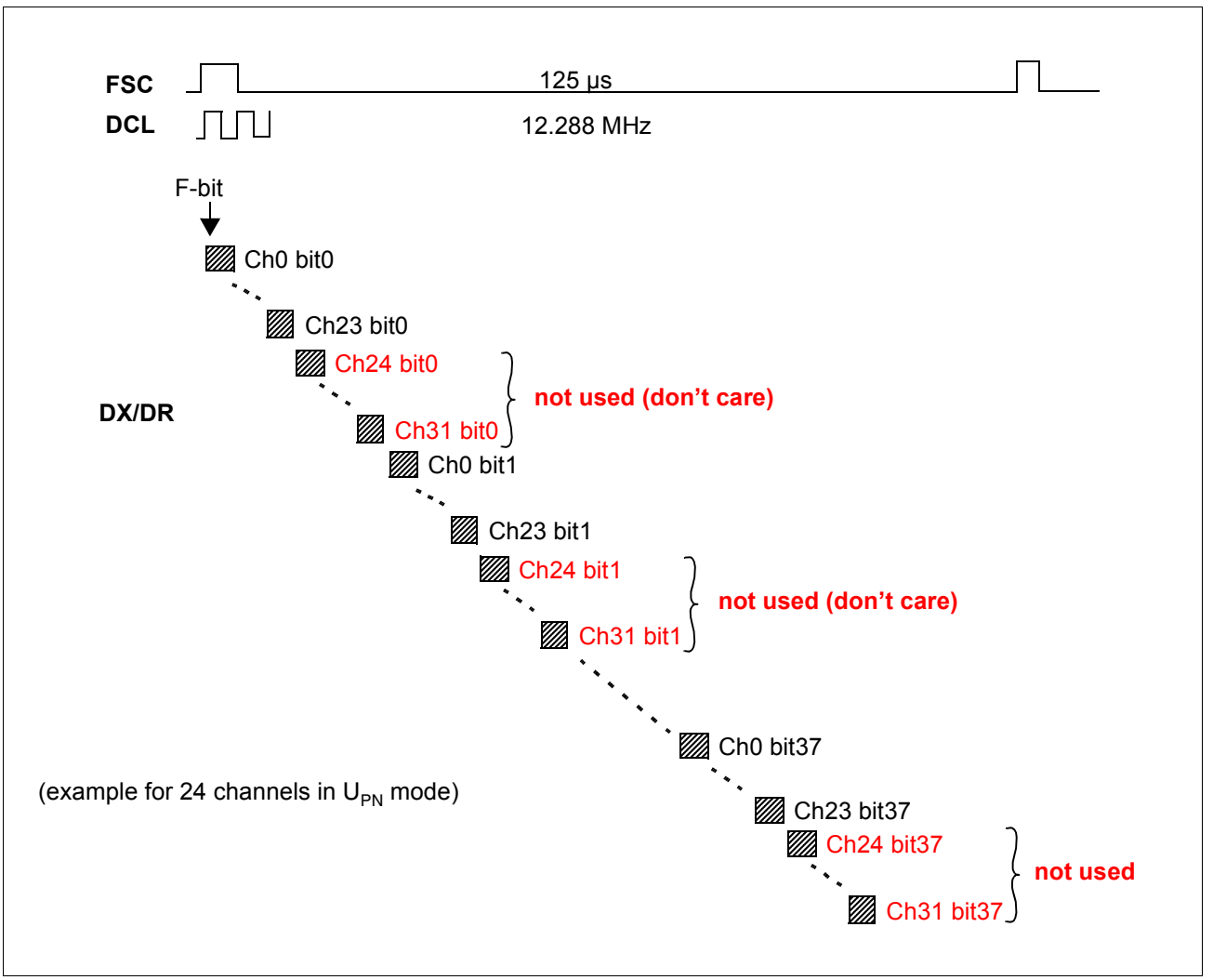


Figure 3-3 IOM-2000 Data Order (3 VIPs with 24 Channels)

Receive Data Channel Shift

In receive direction (DR), data of all IOM-2000 channels (ch0...7 if one VIP is used, ch0 ... ch23 if three VIPs are used) is shifted by 2 channels with respect to the transmitted data channels (DX), assuming a start of transmission of ch0 bit0 with the FSC signal. DELIC is transmitting ch0, while receiving ch2 via DR the same time, etc.

DX	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch0
DR	ch2	ch3	ch4	ch5	ch6	ch7	ch0	ch1	ch2

3.2.2.2 Command and Status Interface

The CMD and STAT lines are the configuration and control interface between DELIC and VIP. The bit streams are partitioned into 32-bit words carrying information *dedicated to the VIPs* (CMD_0 / STAT_0) followed by information *dedicated to the individual channels* of the same VIP (CMD_0_0 ... CMD_2_7 or STAT_0_0 ... STAT_2_7).

Note: As opposed to data, command and status bits are sent channel-wise, starting with channel_0. The transmission clock is the same as the DR/DX data clock.

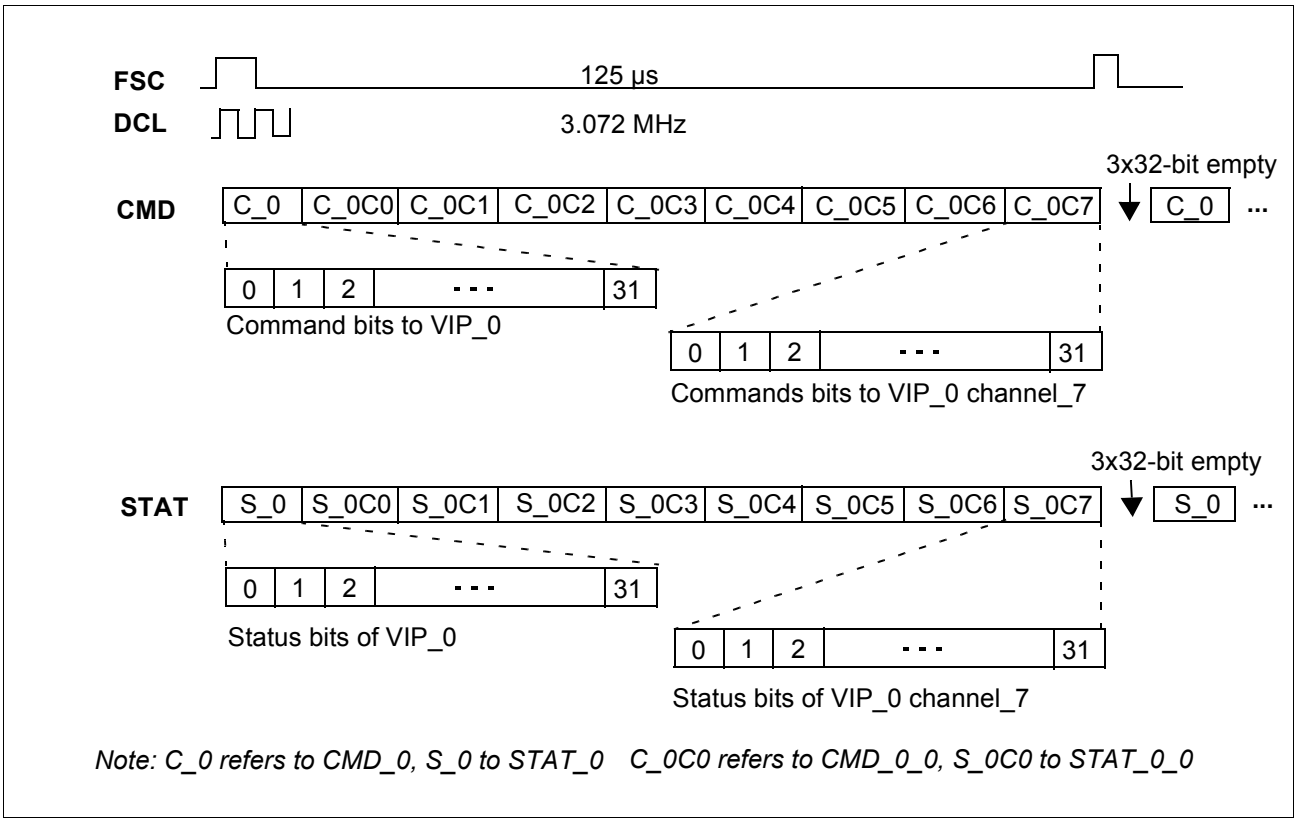


Figure 3-4 IOM-2000 CMD/STAT Handling (1 VIP with 8 Channels)

Note: The position of each VIP within the IOM-2000 frame is programmable by two VIP pins (VIP_ADR0, VIP_ADR1) to IOM-2000 channels 0..7, 8..15 or 16..23.

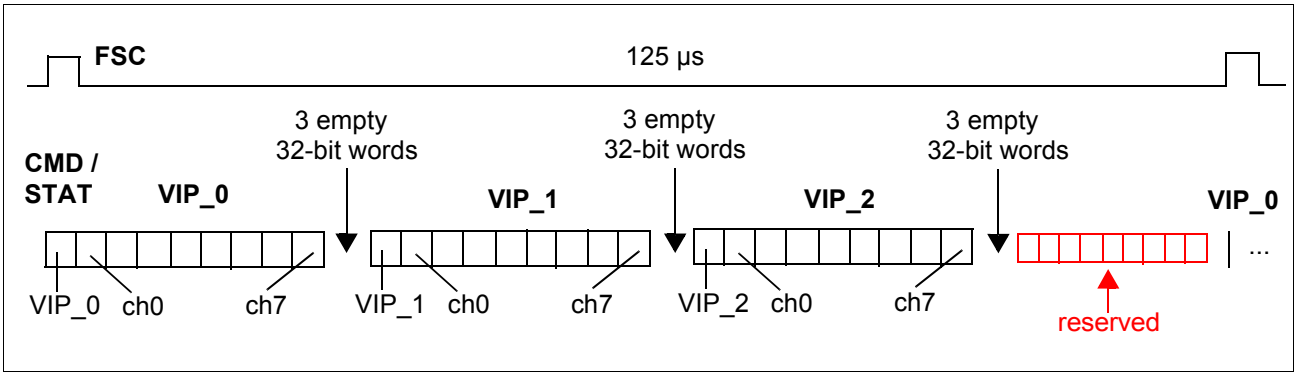


Figure 3-5 IOM-2000 Command/Status Sequence (3 VIPs with 24 Channels)

Commands to VIP_n (CMD_n, n = 0 ... 2)

Initialization and control information for each VIP is sent by DELIC in the following sequence every 125 µs via the IOM-2000 CMD line (32 CMD_n bits per VIP_n):

Note: All bits are programmed in VIP Command register (VIPCMR0..2).

	31							24
	x	x	x	x	x	x	x	x
	23							16
	x	x	x	x	x	x	x	x
	15							8
	x	x	x	x	RD_n	PLLPPS	SH_FSC	DELRE
	7							0
CMD_n	DELCH(2:0)			EXREF	REFSEL(2:0)			WR_n

Commands to VIP_n, Channel_m (CMD_n_m, m = 0 ... 7)

Initialization and control information for each VIP channel is sent by DELIC in the following sequence every 125 µs via the IOM-2000 CMD line (32 CMD_n_m bits per VIP_n Channel_m):

Note: All bits except WR_ST, SMINI(2:0) and MSYNC are programmed in TRANSIU Initialization Channel Command register (TICCR);
bits WR_ST, SMINI(2:0) and MSYNC reside in the TRANSIU Tx data RAM.

	31							24
CMD_n_m	FIL	SMINI(2:0)			MSYNC	EXLP	PLLS	PD
	23							16
	x	DHEN	x	x	PDOWN	LOOP	TX_EN	PLLINT
	15							8
	AAC(1:0)		BBC(1:0)		OWIN(2:0)			MF_EN
	7							0
	MODE(2:0)			MOSEL(1:0)		WR_ST	RD	WR

Status from VIP_n (n = 0 ... 2)

Status information is sent by each VIP in the following sequence via the STAT line (32 STAT_n bits per VIP_n):

STAT_n	31							24
	x	x	x	x	x	x	x	x
	23							16
	x	x	x	x	x	x	x	x
	15							8
	x	x	x	x	x	x	x	x
	7							0
	DELAY(7:0)							

Note: Bits DELAY are read from VIP Status register (VIPSTR) in TRANSIU. x = unused

Status from VIP_n, Channel_m (m = 0 ... 7)

Status information is sent by each VIP channel in the following sequence via the STAT line (32 STAT_n_m bits per VIP_n Channel_m):

STAT_n_m	31							24
	x	x	x	x	x	x	x	x
	23							16
	x	x	x	x	x	x	x	x
	15							8
	x	x	x	x	x	x	x	x
	7							0
	x	MSYNC*	FCV*	FSYNC*	SLIP	FECV	RxSTA(1:0)	

Note: Marked bits (*) are not evaluated by the DELIC, only for VIP testing.
Bits SLIP, FECV and are directly accessible in the TRANSIU receive data RAM.
x = unused

3.2.3 U_{PN} State Machine

3.2.3.1 INFO Structure on the U_{PN} Interface

Signals controlling and indicating the internal state of all U_{PN} transceiver state machines are called INFOs. Four different INFOs (INFO 0, 1W, 1, 2, 3, 4) may be sent over the U_{PN} interface, depending on the actual state (Synchronized, Activated, Pending Activation, ...). When the line is deactivated, INFO 0 (=no signal on the line) is exchanged by the U_{PN} transceivers at either end of the line.

When the line is activated, INFO 3 (in upstream direction) and INFO 4 (in downstream direction) are continuously sent. INFO 3 and 4 contain the transmitted data (B1, B2, D, M). INFO 1/2 are used for activation and synchronization.

Table 3-3 INFO Structure on U_{PN} Interface

Name	Direction	Description
INFO 0	Upstream Downstream	No signal on the line
INFO 1W	Upstream	Asynchronous Wake Signal 4 kHz burst rate F000100010001000100010101010001011111 1 Code violation in the framing bit
INFO 1	Upstream	4 kHz burst rate F000100010001000100010101010001011111M[1]DC Code violation in the framing bit
INFO 2	Downstream	4 kHz burst rate F000100010001000100010101010001011111M[1] Code violation in the frame bit
INFO 3	Upstream	4 kHz burst rate No code violation in the framing bit User data in B, D and M channels B channels scrambled, DC bit[2] optional
INFO 4	Downstream	4 kHz burst rate No code violation in the framing bit User data in B, D and M channels B channels scrambled, DC bit[2]) optional

Note: [1] The M channel superframe contains:
CV code violation [1 kbit/s (once in every fourth frame)]
S bits transparent [1 kbit/s channel]
T bits transparent [2 kbit/s channel]
[2] DC balancing bit; F = Framing bit

3.2.3.2 U_{PN} Mode State Diagram

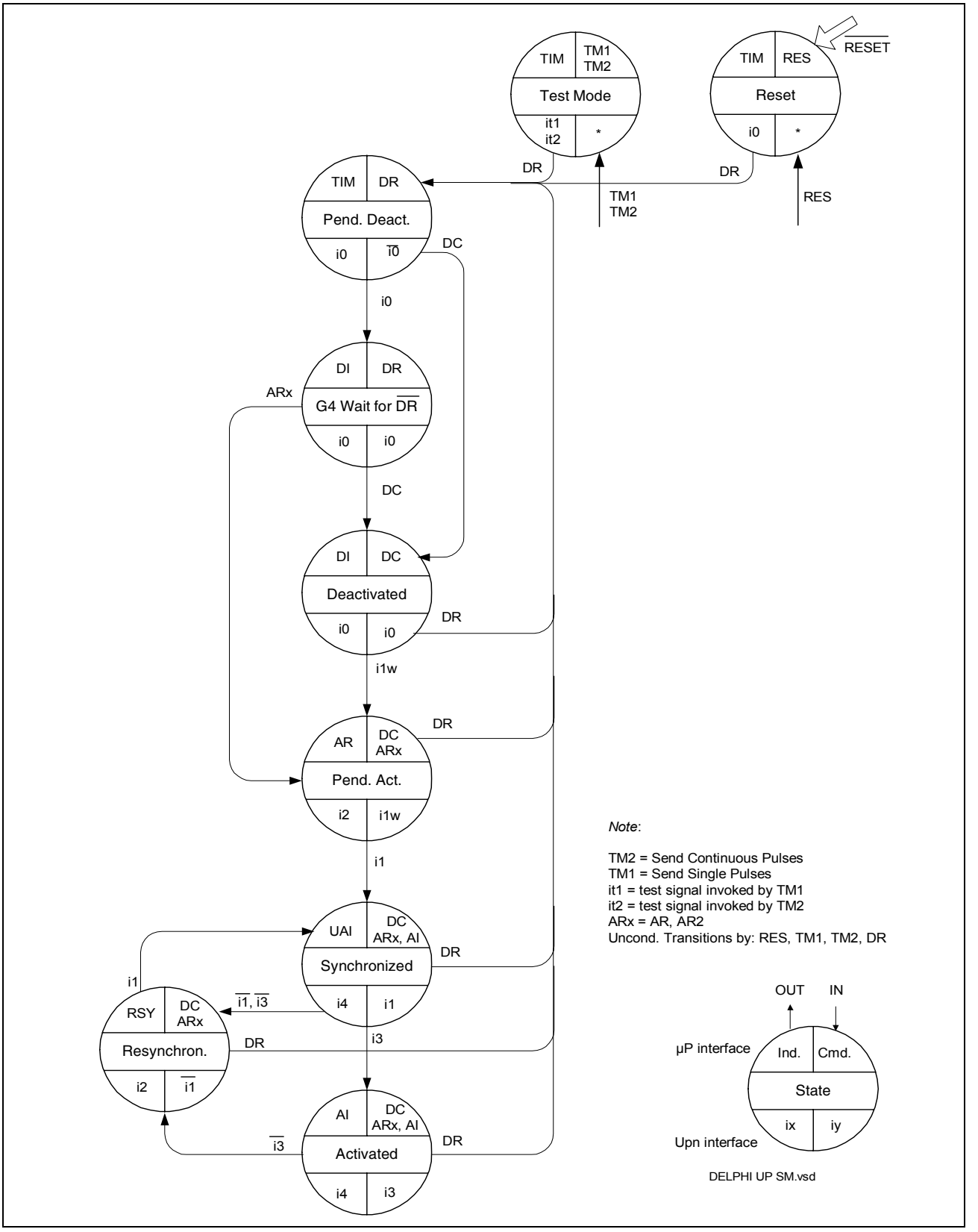


Figure 3-6 U_{PN} State Diagram

The U_{PN} state machine has unconditional and conditional states (refer to **Figure 3-6**):

Unconditional States

Reset

This state is entered unconditionally after a low appears on the $\overline{\text{RESET}}$ pin or after the receipt of command RES (software reset). The analog transceiver part is disabled (transmission of INFO 0) and the U_{PN} interface awake detector is inactive. Hence, activation from terminal (TE) is not possible.

Test Mode

The test signal (it_i) sent to the U_{PN} interface in this state is dependant on the command which originally invoked the state. TM1 causes single alternating pulses to be transmitted (it_1); TM2 causes continuous alternating pulses to be transmitted (it_2). The burst mode technique normally employed on the U_{PN} interface is suspended in this state and the test signals are transmitted continuously.

Pending Deactivation

To access any of the conditional states from any of the above unconditional states, the pending deactivation state must be entered. This occurs after the receipt of a DR command. In this state the awake detector is activated and the state is left only when the line has settled (i.e., INFO 0 has been detected for 2 ms) or by the command DC.

Note: Although DR is shown as a normal command, it may be seen as an unconditional command. No matter which state the LT is in, the reception of a DR command will always result in the pending deactivation state being entered.

Conditional States

Wait for $\overline{\text{DR}}$

This state is entered from the pending deactivation state once INFO 0 or DC has been identified. From here the line may be either activated, deactivated or a test loop may be entered.

Deactivated

This is the power down state of the physical protocol. The awake detection is active and the device will respond to an INFO 1w (wake signal) by initiating activation.

Pending Activation

This state results from a request for activation of the line, either from the terminal (INFO 1w) or from the layer-2 device (AR, AR2). INFO 2 is then transmitted and the DSP waits for the responding INFO 1 from the remote device.

Synchronized

This state is reached after synchronization upon the receipt of INFO 1, i.e. after a maximum of 10 ms. In this state, INFO 2 is supplied to the remote terminal for synchronization.

Activated

Info 1 has a code violation in the framing bit (F-bit), whereas INFO 3 has none. Upon the reception of two frames without a code violation in the F bit, the activated state is entered and INFO 4 is transmitted. The line is now activated; INFO 4 is sent to the remote and INFO 3 is received from the remote.

Re synchronization

If the recognition of INFO 3 fails, the receiver will attempt to resynchronize. Upon entering this state, INFO 2 is transmitted. This is similar to the original synchronization procedure in the pending activation state (the indication given to layer 2 is different). However, as before, recognition of INFO 1 leads to the synchronized state.

Table 3-4 U_{PN} State Machine Codes

Command	Abbr.	Code	Remark
Deactivate request	DR	0000	Initiates a complete deactivation from the exchange side by transmitting INFO 0 (x)
Reset	RES	0001	(x)
Test mode 1	TM1	0010	Transmission of pseudo-ternary pulses at 2 kHz frequency (x)
Test mode 2	TM2	0011	Transmission of pseudo-ternary pulses at 192 kHz frequency (x)
Activate request	AR	1000	Used to start an exchange initiated activation
Activate request test loop 2	AR2	1010	Transmission of INFO 2, switching of loop 2 (at TE), T bit set to one

Table 3-4 U_{PN} State Machine Codes (Continued)

Command	Abbr.	Code	Remark
Activate indication = "blocked"	AI	1100	Transmission of INFO 4, T bit set to zero
Deactivate confirmation	DC	1111	Deactivation acknowledgement, quiescent state

(x) unconditional commands

Note: The U_{PN} state machine does not support loops. So neither C/I commands nor Indications are provided by the mailbox protocol.
An loop can be programmed by setting bits TICCMR:LOOP and TICCMR:EXLP for the respective channel.

Indication	Abbr.	Code	Remark
Timing	TIM	0000	Deactivate state, activation from the line not possible
Resynchronizing	RSY	0100	Receiver is not synchronous
Activate request	AR	1000	INFO 1w received
U only activation indication	UAI	0111	INFO 1 received, synchronous receiver
Activate indication	AI	1100	Receiver synchronous, i.e., activation completed
Deactivate indication	DI	1111	INFO 0 or DC received after deactivation request

3.2.4 S/T State Machine

A finite state machine in the DELIC controls the VIP S/T line activation/deactivation procedures and transmission of special pulse patterns. Such actions can be initiated by primitives (INFOs) on the S/T interface or by C/I codes sent via the mailbox.

Depending on the application mode and the transfer direction, the S/T state machines support different codes in conditional and unconditional states:

LT-S mode

Codes: data downstream = Commands: reset, test mode, activate req, ..
data upstream = Indications: not sync, code violation, timer out, ..
States: deactivated, activated, pending, lost framing, test mode

The state diagram is shown in **Figure 3-7.**

LT-T mode

Codes data upstream = Commands: reset, test, activate request,..
data downstream = Indications: command x acknowledged,..
Conditional states: power up, pending deactivation, synchronized, slip detected,..

The state diagram is shown in **Figure 3-8.**

Unconditional states may be entered from any conditional state and should be left with the command TIM: test mode, reset state,..

The S/T layer-1 activation and deactivation procedures implemented in the DELIC are similar to the ones implemented in the PEB 2084, QUAT-S.

3.2.4.1 LT-S Mode

Table 3-5 LT-S State Machine Codes

Command	Abbr.	Code	Remark
Deactivate request	DR	0000	Initiates a complete deactivation from the exchange side by transmitting INFO 0 (x)
Reset	RES	0001	(x)
Test mode 1	TM1	0010	Transmission of pseudo-ternary pulses at 2 kHz frequency (x)
Test mode 2	TM2	0011	Transmission of pseudo-ternary pulses at 96 kHz frequency (x)

Table 3-5 LT-S State Machine Codes (Continued)

Command	Abbr.	Code	Remark
Activate request	AR	1000	Used to start an exchange initiated activation
Deactivate confirmation	DC	1111	Deactivation acknowledgement, quiescent state

(x) unconditional commands

Note: The LT-S state machine does not support loops. So neither C/I commands nor Indications are provided by the mailbox protocol.
A loop can be programmed by setting bits TICCMR:LOOP and TICCMR:EXLP for the respective channel.

Indication	Abbr.	Code	Remark
Timing	TIM	0000	
Resynchronizing	RSY	0100	Receiver is not synchronous
Activate request	AR	1000	$\overline{\text{INFO 0}}$ received
Code violation received	CVR	1011	After each multi-frame the reception of at least one illegal code violation is indicated four times
Activate indication	AI	1100	Receiver synchronous, i.e., activation completed
Deactivate indication	DI	1111	Timer (32 ms) expired or INFO 0 received after deactivation request

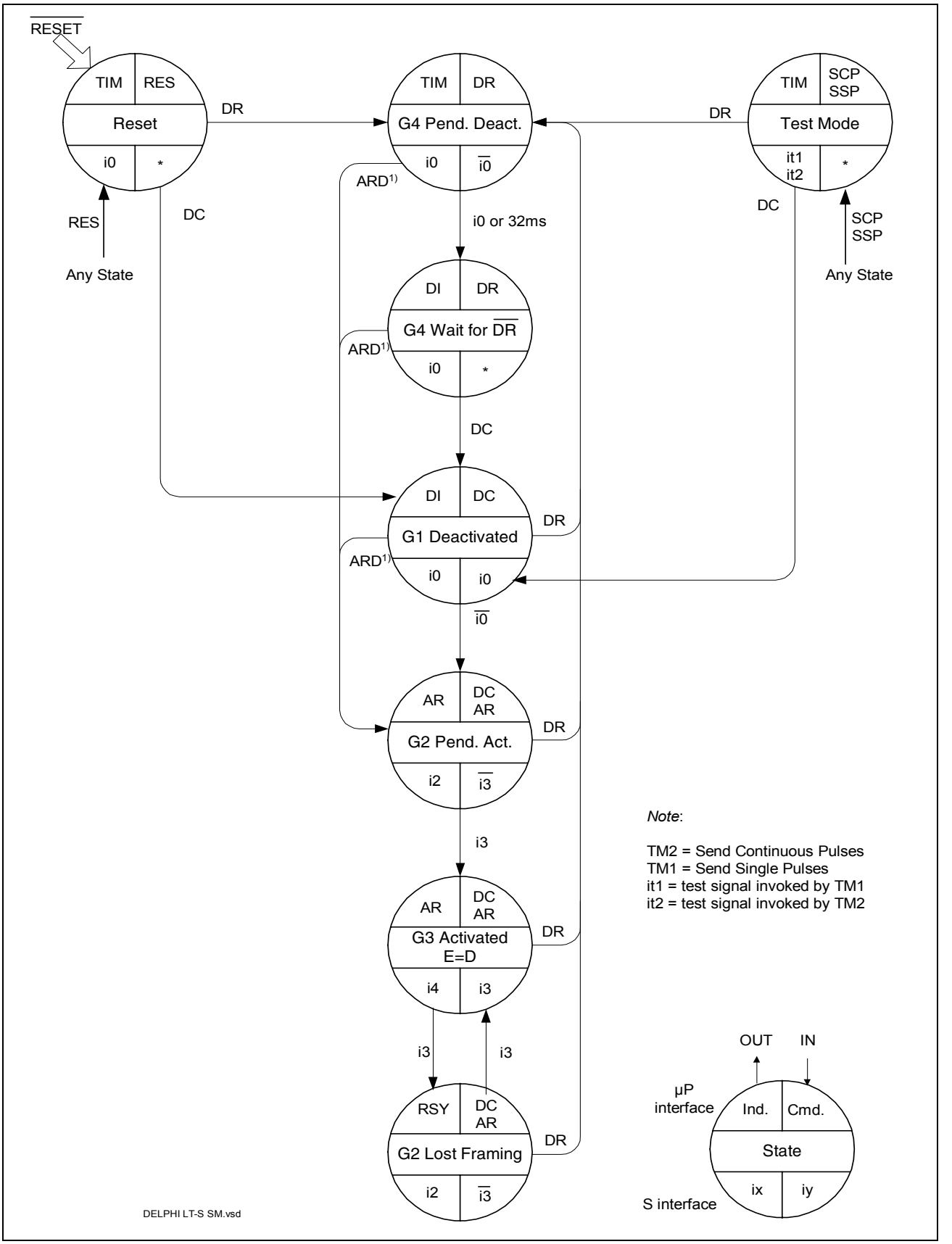


Figure 3-7 State Diagram of LT-S Mode

LT-S Mode States

- G1 deactivated
  The line interface is not transmitting. There is no signal detected on the S interface, and no activation command is received.
- G2 pending activation
  As a result of an INFO 1 detected on the S line or an AR command, the line interface begins transmitting INFO 2 and waits for reception of INFO 3. The timer to supervise reception of INFO 3 is to be implemented in software. In case of an ARL command, loop 2 is closed.
- G3 activated
  Normal state where INFO 4 is transmitted to the S interface. The line interface remains in this state as long as neither a deactivation nor a test mode is requested, and the receiver does not loose synchronism. When receiver synchronism is lost, INFO 2 is sent automatically. After reception of INFO 3, the transmitter continues sending INFO 4.
- G2 lost framing
  This state is reached when the line interface has lost synchronism in the state G3 activated.
- G4 pending deactivation
  This state is triggered by a deactivation request DR. It is an unstable state: status DI (state “G4 wait for DR”) is issued by the DELIC when either INFO 0 is received, or an internal timer of 32 ms expires.
- G4 wait for DR
  Final state after a deactivation request. The line interface remains in this state until a response to DI (in other words DC) is issued.
- Test mode 1
  Single alternating pulses are sent on the S interface (2 kHz repetition rate).
- Test mode 2
  Continuous alternating pulses are sent on the S interface (96 kHz).

3.2.4.2 LT-T Mode

Table 3-6 LT-T Mode State Machine Codes (Conditional States)

Command	Abbr.	Code	Remark
Timing Request	TIM	0000	Requests the line interface to change into power-up state
Reset	RES	0001	Reset of state machine. Transmission of Info 0. No reaction to incoming infos (x)
Test mode 1	TM1	0010	Transmission of single pulses on the S/T-interface. The pulses are transmitted with alternating polarity at a frequency of 2 kHz. (x)
Test mode 2	TM2	0011	Transmission of continuous pulses on the S/T-interface. The pulses are sent with alternating polarity at a rate of 96 kHz. TM2 is an unconditional command (x).
Activate request, priority 8	AR8	1000	Activation Request with priority 8 for D-channel transmission. This command is used to start a LT-T initiated activation. D-channel priority 8 is the highest priority. It should be used to request signaling information transfer.
Activate request, priority 10	AR10	1001	Activation request with priority 10 for D-channel transmission. This command is used to start a LT-T initiated activation. D-channel priority 10 is a lower priority. It should be used to request packet data transfer.
Deactivate indication	DI	1111	This command forces the line interface into “F3 power down” mode.

(x) unconditional commands

Note: The LT-T state machine does not support loops. So neither C/I commands nor Indications are provided by the mailbox protocol.
A loop can be programmed by setting bits TICCMR:LOOP and TICCMR:EXLP for the respective channel.

Indication	Abbr.	Code	Remark
Deactivate request	DR	0000	Deactivation request if left from F7/F8
Reset	RES	0001	Reset acknowledge
Test mode 1	TM1	0010	TM1 acknowledge
Test mode 2	TM2	0011	TM2 acknowledge
Slip detected	SLIP	0011	Frame wander larger than +/- 25 µs
Resynchronization during level detect	RSY	0100	Signal received, receiver not synchronous
Power up	PU	0111	Line interface is powered up
Activate request	AR	1000	INFO 2 received
Code violation received	CVR	1011	After each multiframe the reception of at least one illegal code violation is indicated four times.
Activate indication with priority class 8	AI8	1100	INFO 4 received, D-channel priority is 8 or 9
Activate indication with priority class 10	AI10	1101	INFO 4 received, D-channel priority is 10 or 11
Deactivate confirmation	DC	1111	Line interface is powered down

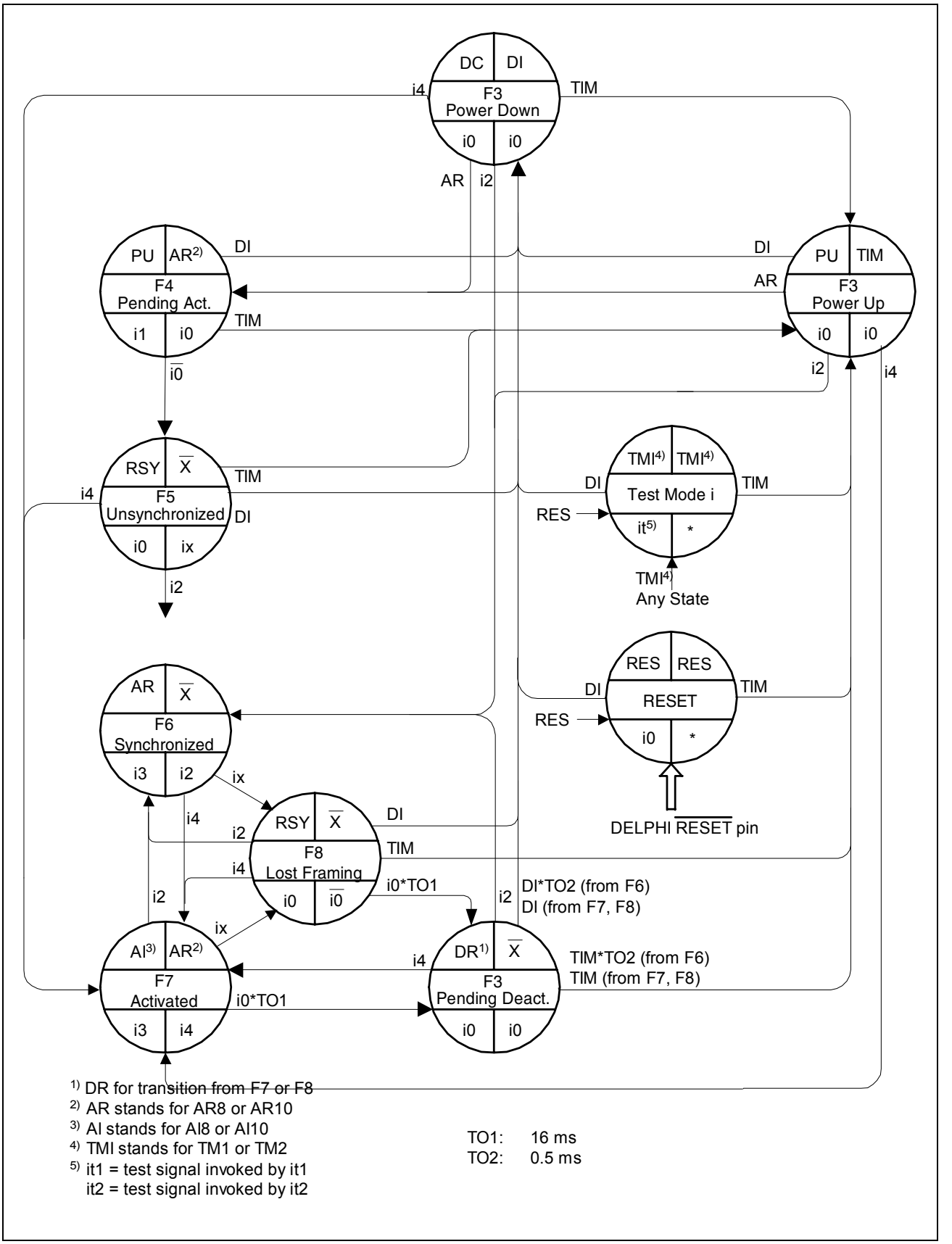


Figure 3-8 LT-T Mode State Diagram (Conditional and Unconditional States)

LT-T Mode (Conditional States)

- F3 power down
  This is the deactivated state of the physical protocol. The receive line awake unit is active.
- F3 power up
  This state is similar to “F3 power down”. The state is invoked by a Command TIM = “0000” (or DI static low).
- F3 pending deactivation
  The line interface reaches this state after receiving INFO 0 (from states F5 to F8). From this state an activation is only possible from the line (transition “F3 pending deactivation” to “F5 unsynchronized”). The power down state may be reached only after receiving DI.
- F4 pending activation
  Activation has been requested from the terminal; INFO 1 is transmitted; INFO 0 is still received; “Power Up” is transmitted in the C/I channel. This state is stable: timer T3 (ITU I.430) is to be implemented in software.
- F5/8 unsynchronized
  At the reception of any signal the VIP ceases to transmit INFO 1, adapts its receiver circuit, and awaits identification of INFO 2 or INFO 4. This state is also reached after the line interface has lost synchronism in the states F6 or F7 respectively.
- F6 synchronized
  When the VIP receives an activation signal (INFO 2), it responds with INFO 3 and waits for normal frames (INFO 4).
- F7 activated
  This is the normal active state with the layer 1 protocol activated in both directions. From state “F6 synchronized”, state F7 is reached almost 0.5 ms after reception of INFO 4.
- F7 slip detected
  When a slip is detected between the T interface clocking system and the IOM-2 interface clocks (phase wander of more than 25 µs, data may be disturbed) the line interface enters this state, synchronizing again the internal buffer. After 0.5 ms this state is relinguished.

LT-T Mode (Unconditional States)

The unconditional states should be left with the command TIM.

- Test mode 1
  Single alternating pulses are sent on the T interface (2 kHz repetition rate).
- Test mode 2
  Continuous alternating pulses are sent on the T interface (120 kHz).
- Reset state
  A hardware or software reset (RES) forces the line interface to an idle state where the analog components are disabled (transmission of INFO 0) and the T line awake detector is inactive.

3.3 IOM®-2 Interface

IOM-2 is a standardized interface for interchip communication in ISDN line cards for digital exchange systems developed by ALCATEL, Siemens, Plessey and ITALTEL.

The IOM-2 interface is a four-wire interface with a bit clock, a frame clock and one data line per direction. It has a flexible data clock. This way, data transmission requirements are optimized for different applications.

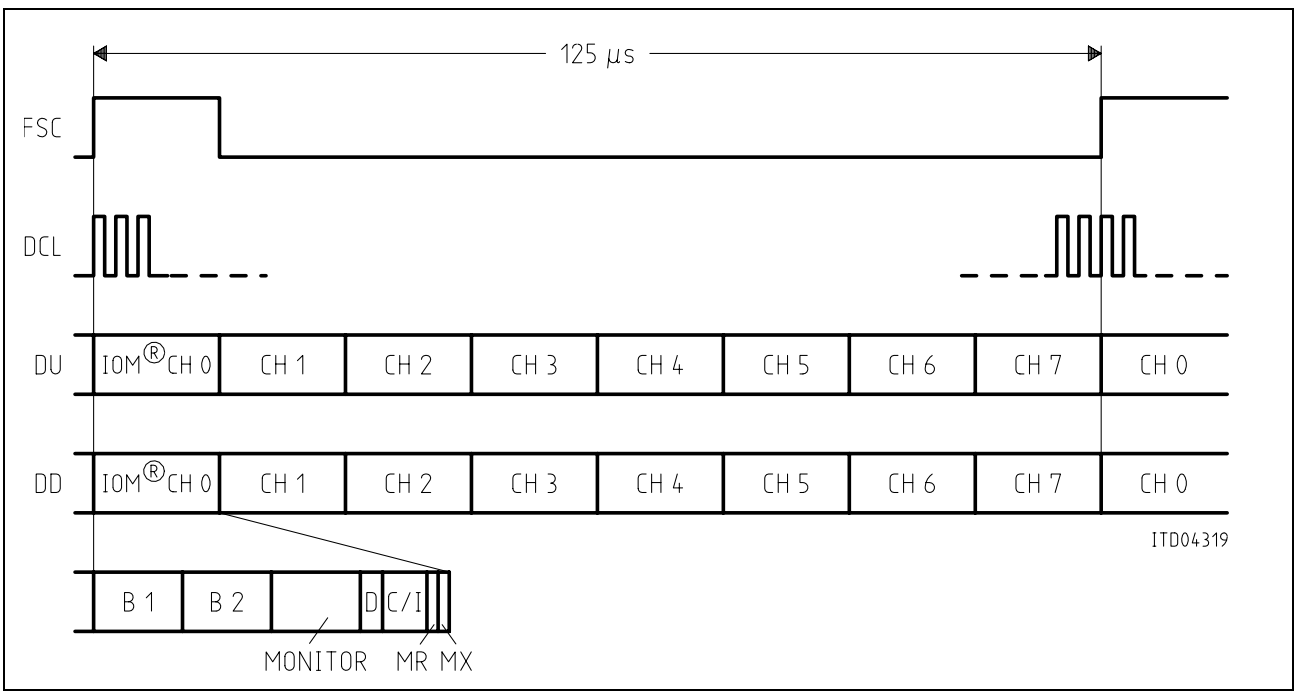


Figure 3-9 IOM®-2 Interface in Digital Linecard Mode

Note: In Linecard mode, 8 identical IOM-2 subchannels are provided. In analog Linecards, a 6-bit C/I Channel is available for signaling information. In digital Linecards, a dedicated 2-bit D-channel carries the signaling information.

3.3.1 Signals / Channels

FSC	Frame Synchronization Clock, 8 kHz
DCL	Data Clock, up to 4.096 MHz *)
DD	Data Downstream, up to 4.096 Mbit/s *)
DU	Data Upstream, up to 4.096 Mbit/s *)
B1, B2	User data channels, 64 kbit/s each
MONITOR	Monitor Channel
D	Signaling Channel, 16 kbit/s
C/I	Command/Indication Channel
MR	Monitor Receive handshake signal
MX	Monitor Transmit handshake signal

*) For detailed clock and data rates, refer to IOMU feature description in **Chapter 4.3.2**

3.4 µP Interface

The µP interface may be operated in different modes. This chapter describes how to configure the DELIC to each mode.

3.4.1 Intel/Siemens or Motorola Mode

The processor mode is selected by the MODE input pin of the DELIC. "Low" level selects Siemens/ INTEL mode, "HIGH" level selects Motorola mode.

3.4.2 De-multiplexed or Multiplexed Mode

In both modes, the A-bus and the D-bus are used in parallel. The A-bus should be connected to the 8 LSBs of AD-bus, coming from the µP, also in multiplexed mode. The mode is determined according to the ALE input pin. When ALE is permanently driven to ‘1’, the DELIC works in de-multiplexed mode. Otherwise the DELIC works in multiplexed mode.

The next figure describes the connection of the DELIC to the address and data buses in the different modes.

Note: Motorola mode is used only with de-multiplexed AD bus. Intel/Infineon mode may be used with both, multiplexed or de-multiplexed AD bus.

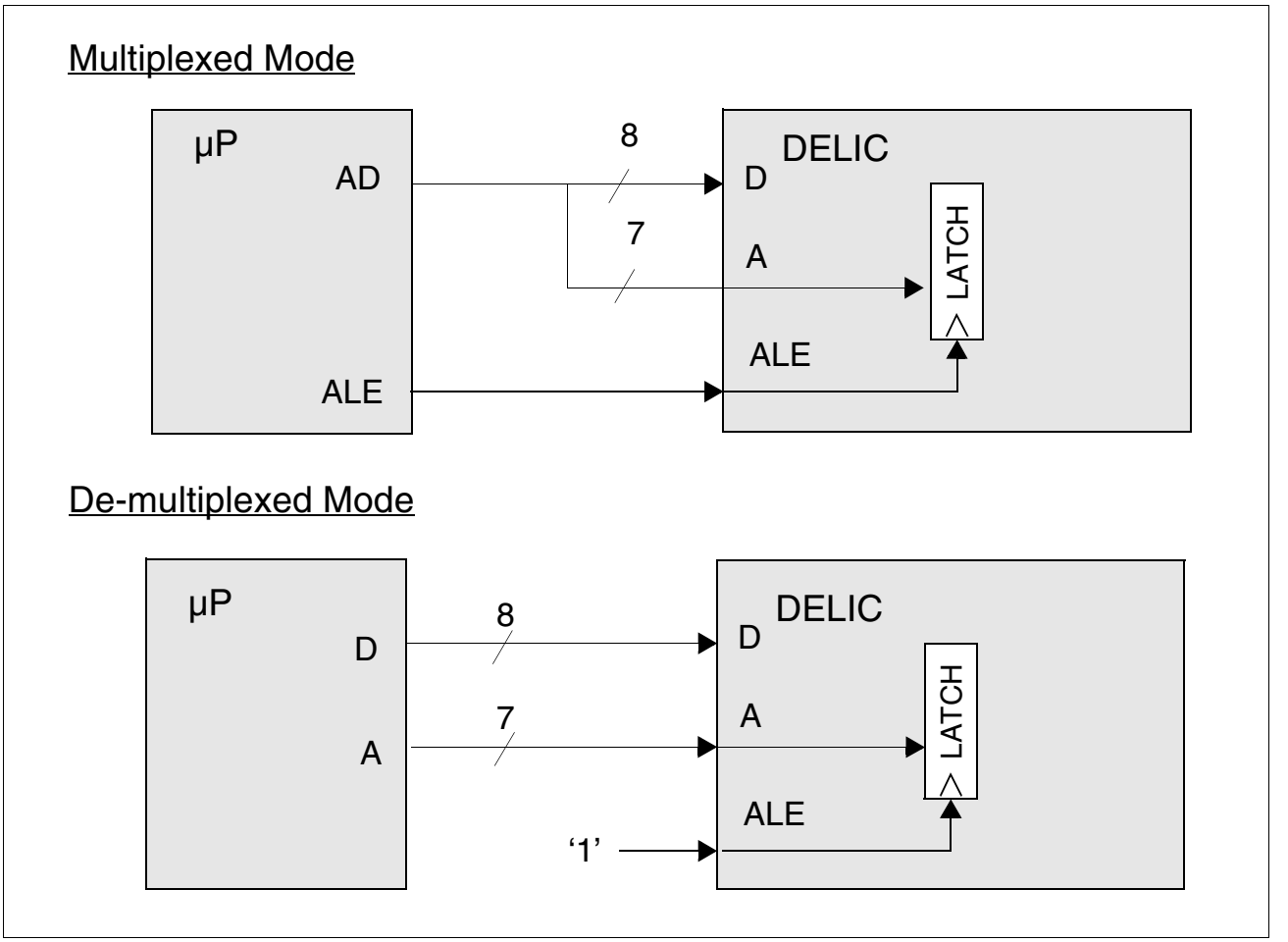


Figure 3-10 DELIC in Multiplexed and in De-multiplexed Bus Mode

Note: In both modes only the 7 LSBs of A-bus or AD/bus are connected to the Address inputs of the DELIC. In DMA mode $\overline{DACK}$/A4 input pin is used as $\overline{DACK}$, and A4 is internally driven to ‘0’. In this case A4 of the µP A/AD-bus is also not connected to the DELIC.

3.4.3 DMA or Non-DMA Mode

The internal interface between the on-chip DSP and µP is established by two Mailboxes: a ’general’ Mailbox and a dedicated DMA Mailbox. The non-DMA mode provides the option to combine them together building a double-sized ’general’ Mailbox. The DELIC is configured to DMA or non-DMA mode by a dedicated bit in the µP interface configuration register (MCFG:DMA).

DMA Mode

The DMA Mailbox can be accessed only by a DMA controller. The $\overline{DACK}$ input pin (together with the $\overline{RD}$ and $\overline{WR}$ signals) is used to access the DMA Mailbox. Only the general Mailbox can be accessed directly by the µP. In DMA mode, the pin $\overline{DACK}$/A4 is

used as $\overline{\text{DACK}}$, and A4 of the A-bus or AD-bus coming from the µP must not be used as an address line for the DELIC. In this case A4 is driven internally to ‘0’.

Note: In de-multiplexed mode AD4 should be connected to DELIC’s D4input pin.

Non-DMA mode

This is the default mode (after reset).The general Mailbox and the DMA Mailbox data registers are concatenated into one double-sized general Mailbox, accessible by the µP. This broad Mailbox consists of a dedicated µP Mailbox and a DSP Mailbox. Each of them contains 32 data bytes and 1 command byte. In non-DMA mode, $\overline{\text{DACK}}$/A4 is used as A4, in order to include the DMA Mailbox data registers in the µP interface address space.

3.4.4 DELIC External Interrupts

The DELIC contains only one source for an external interrupt - the general Mailbox. This interrupt source is the OCMD register of the DSP Mailbox. Releasing the interrupt is done by the µP resetting bit OBUSY:BUSY. Masking it may be done by resetting the MASK bit of the µP interface Configuration Register (MCFG:IMASK).

The interrupt vector issued is the contents of the DSP Mailbox command register MCMD. In Motorola mode, the interrupt vector is issued upon the first $\overline{\text{IACK}}$ pulse, while in Siemens/Intel mode it is issued upon the second $\overline{\text{IACK}}$ pulse. In the latter case, the interrupt vector due to the first $\overline{\text{IACK}}$ pulse (if needed), should be issued by an external interrupt controller.

3.5 JTAG Test Interface

The DELIC provides fully IEEE Standard 1149.1 compatible boundary scan support to allow cost effective board testing. It consists of:

- Complete boundary scan test
- Test access port controller (TAP)
- Five dedicated pins: JTCK, TMS, TDI, TDO (according to JTAG) and an additional $\overline{\text{TRST}}$ pin to enable asynchronous resets to the TAP controller
- One 32-bit IDCODE register

3.5.1 Boundary Scan Test

- Depending on the pin functionality one or two boundary scan cells are provided.

Pin Type	Number of Boundary Scan Cells	Usage
Input	1	Input
Output	2	Output, enable

When the TAP controller is in the appropriate mode data is shifted into/out of the boundary scan via the pins TDI/TDO using a clock of up to 6.25 MHz on pin JTCK.

The sequence of the DELIC pins can be taken from the BSDL files.

3.5.2 TAP Controller

The Test Access Port (TAP) controller implements the state machine defined in the JTAG standard IEEE 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

The TAP controller supports a set of 5 standard instructions:

Table 3-7 TAP Controller Instruction Codes

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code register
1111	BYPASS	Bypass operation

EXTEST is used to verify the board interconnections.

When the TAP controller is in the state “update DR”, all output pins are updated with the falling edge of JTCK. When it has entered state “capture DR” the levels of all input pins

are latched with the rising edge of JTCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST supports internal chip testing.

When the TAP controller is in the state “update DR”, all inputs are updated internally with the falling edge of JTCK. When it has entered state “capture DR” the levels of all outputs are latched with the rising edge of JTCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

Note: 0011 (IDCODE) is the default value of the instruction register.

SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to either preload (TDI) or shift out (TDO) the boundary scan test vector. Both activities are transparent to the system functionality.

IDCODE

The 32-bit identification register is serially read out via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to ’1’. The code for the DELIC version 1.1 is ’0001’.

Version	Device Code	Manufacturer Code		Output
0001	0000 0000 0101 0111	0000 1000 001	1	--> TDO

Note: In the state “test logic reset” the code “0011” is loaded into the instruction code register.

BYPASS, a bit entering TDI is shifted to TDO after one JTCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

4 Functional Description

As the functionality of the DELIC-PB comprises the functionality of the DELIC-LC, the following chapter discribes the functionality of the DELIC-PB. The Differences between the two chip versions can be seen below:

Table 4-1 Differences between DELIC-LC - DELIC-PB

Functionality	DELIC-LC	DELIC-PB
GHDLC channels (maximum configuration)	Cha. 0	Cha. 0..3
HDLC channels (maximum configuration)	Cha. 0..23	Cha. 0..31
DMA interface	not available	available
DMA- mailbox	not available; it is used to increment the general mailbox	can be used for DMA operation or as general mailbox
Pinout		
Free programmability of DSP-system	no	yes

Note: As the functionality is also dependent on the firmware package, please also refer to the respective documentation.

4.1 Functional Overview and Block Diagram

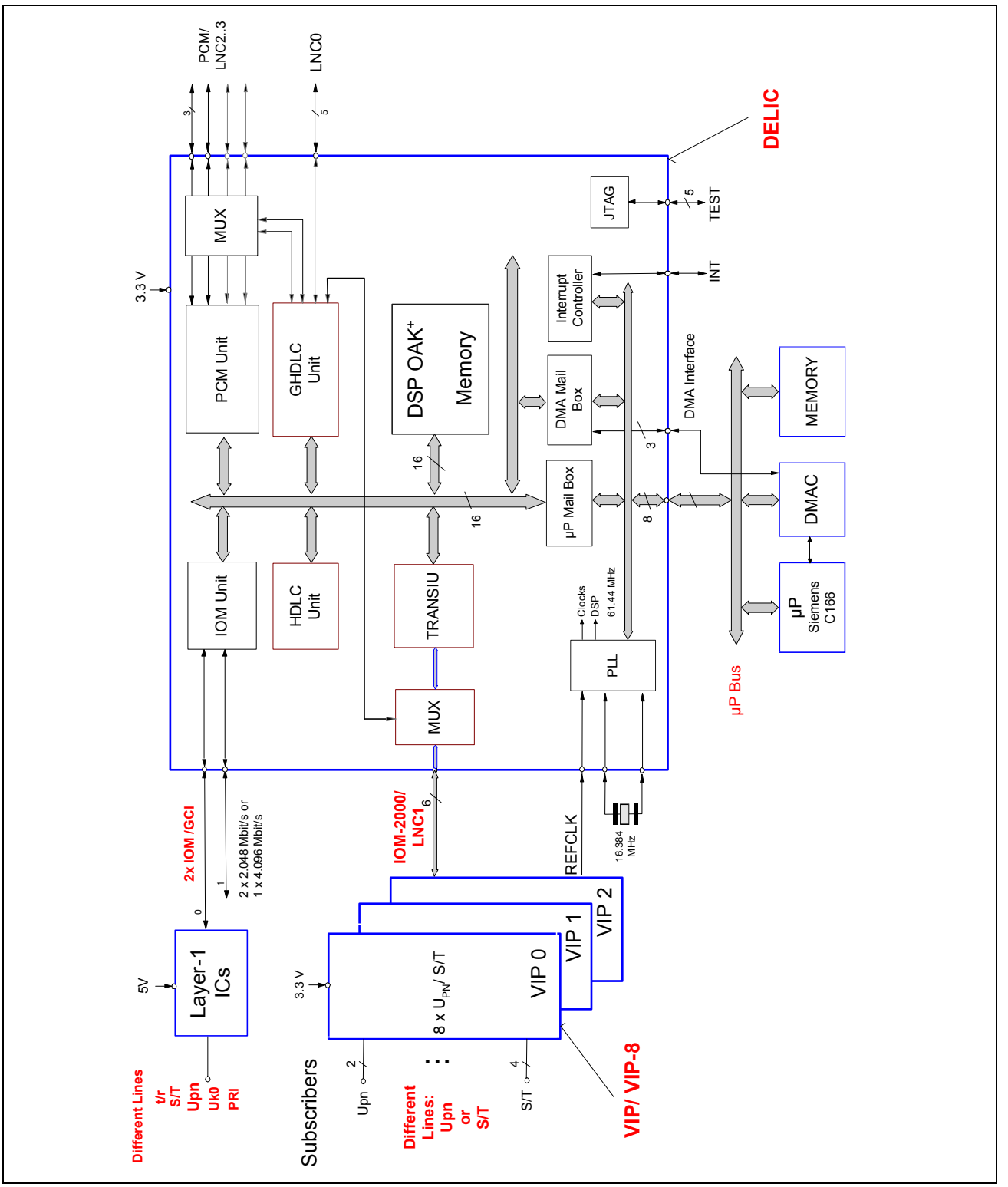


Figure 4-1 Block Diagram

4.2 IOM-2000 Transceiver Unit

4.2.1 TRANSIU Overview of Features

- The TRANSIU controls up to 24 layer-1 channels via up to three VIP/ VIP8 connected on IOM-2000 interface
- IOM-2000 interface: all channels may be programmed in the TRANSIU to:

– U_{PN} interface
– S/T interface in LT-S (subscriber master) or LT-T (trunk slave) mode

Note: The number of S/T interfaces in VIP PEB 20590 is limited to 4. Therefore it is required to program the TRANSIU correctly to the required mode (refer to TRANSIU register description)

- Data rates: 3.072 Mbit/s (1 VIP), 6.144 Mbit/s (2 VIPs) or 9.216 Mbit/s (3 VIPs)
- Data and maintenance bit handling for S/T and U_{PN} interface, including multiframe control and D-channel collision control.

4.2.2 TRANSIU Initialization

Reset Status

- All IOM-2000 channels are configured to S/T interface, LT-S mode
- The data rate in the TRANSIU is set to 3.072 Mbit/s
- All buffers related to the IOM-2000 are undefined
- The Command and Status buffers have the value ‘0’

Channel Programming

Every IOM-2000 channel may be configured in the TRANSIU as:

- U_{PN} mode
- S/T channel in LT-S mode
- S/T channel in LT-T mode

Data Rate Programming

The TRANSIU supports three configurations regarding the number of VIPs connected via IOM-2000:

- One VIP connected at data rate of 3.072 Mbit/s: 8 IOM-2000 channels at a clock rate of 3.072 MHz
- Two VIPs connected at data rate of 6.144 Mbit/s: 16 IOM-2000 channels at a clock rate of 6.144 MHz
- Three VIPs connected at data rate of 9.216 Mbit/s: 24 IOM-2000 channels at a clock rate of 12.288 MHz. (Note the difference between clock rate and actual data rate)

4.2.3 Initialization of VIP

During startup the VIP requires 3 frames with the right FSC and DCL_2000 to synchronize to the DELIC. During this time the VIP is not able to detect commands or data from the DELIC.

4.2.4 S/T Mode Control and Framing Bits on IOM-2000

4.2.4.1 Framing Bit (F-Bit)

The framing (F) bit is recognized on the IOM-2000 interface, when both data and control bits are equal to ‘1’. In the transmit direction the data and control bits are inserted by the TRANSIU at the beginning of every transmitted frame; in the receive direction the framing bit is used for frame start recognition.

4.2.4.2 Multiframing Bits

In S/T interface, the multiframe includes 20 S/T frames. The start of a multiframe is indicated by the M- and F_a-bits (the M-bit is set to ‘1’ in every 20-th frame, the F_a-bit is set to ‘1’ in every 5-th frame).

The S/Q channel provides the additional capability for data exchange between LT-S and TE or between the Central Office (CO) and the LT-T at the multiframe level. In the LT-S-to-TE direction the S-channel (S-bit in S/T frame) is used. In the opposite direction (TE to LT-S) the data is transferred on the Q-channel. The Q-bits are defined to be the bits in the F_a bit position of every 5-th frame. The Q-bit position is identified by F_a = ‘1’ in the TE to LT-S direction. A multiframe is provided for structuring the Q-bits in groups of four (Q1-Q4).

The Q- and S-channel coding with respect to the frame number is shown in **Table 4-2**.

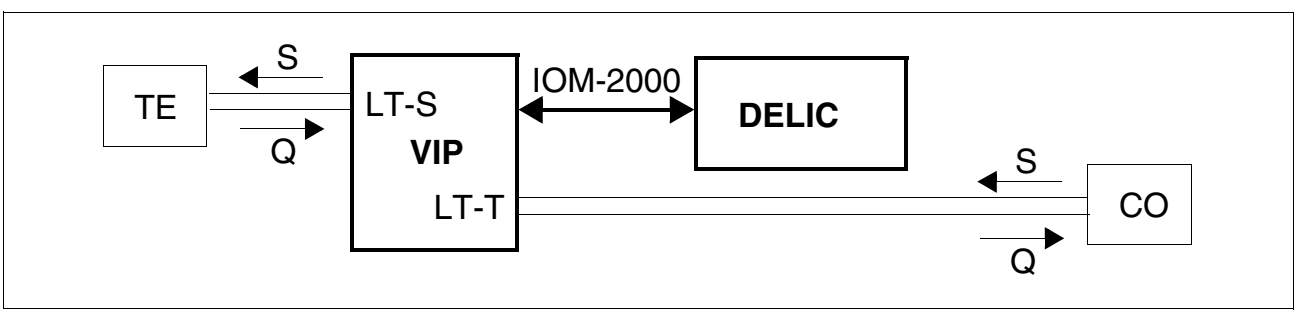


Figure 4-2 S/Q Channel Assignment

Table 4-2 S/T Mode Multiframe Bit Positions

Frame number	LT-S to TE or CO to LT-T, F_a bit position	LT-S to TE or CO to LT-T, M-bit	LT-S to TE or CO to LT-T, S-bit	TE to LT-S or LT-T to CO F_a bit position
1	1	1	S11	Q1
2	0	0	S21	0
6	1	0	S12	Q2
7	0	0	S22	0
11	1	0	S13	Q3
12	0	0	S23	0
16	1	0	S14	Q4
17	0	0	S24	0
...	...	...	...	...

Note: 1.Only frame positions (within the 20-frame multiframe) that carry S- or Q-channel information are shown here
2.The Q- and S-bits, which are not used, are set to '1'.

On the IOM-2000 interface, the S/T multiframe information is included in the DX/DR data stream (transparently to the VIP). The values of the multiframe are controlled by the DSP software in the DELIC.

When multiframe synchronization is not achieved or lost, the VIP mirrors the received F_a bits. Once the multiframe synchronization is established, the DSP sends the multiframe synchronization command to the VIP (MSYNC bit). Upon reception of the MSYNC, the VIP stops mirroring the F_a -bit.

4.2.4.3 F_a/N Bit

In the transmit direction the F_a/N bit pair is coded in such a way that N is the binary opposite of the F_a. The F_a bit is equal to binary '0', except every 5-th frame when it is set to '1', which indicates the Q-bit position to the TE.

The receive direction, the F_a bit positions represent the Q-channel.

4.2.4.4 DC-Balancing Bit (L-Bit)

In transmit (downstream) direction the L-bit is generated in compliance with ITU-T I.430:

- A balance bit is '0' if the number of 0's following the previous balance bit is odd.
- A balance bit is '1' if the number of 0's following the previous balance bit is even.

It is inserted by the VIP according to the Balancing Bit Control (BBC) bit sent to the VIP by the DELIC via the CMD line.

In receive (upstream) direction, the DC balancing bit is received on the line, but not evaluated

4.2.5 U_{PN} Mode Control and Framing Bits on IOM-2000

4.2.5.1 Framing Bit (LF-Bit)

On the U_{PN} interface the framing (LF) bit is always logical ‘1’.

In the transmit direction the LF-bit is inserted by the TRANSIU at the beginning of every transmitted U_{PN} frame. The VIP assumes the start of the U_{PN} frame when detecting the first '1' (LF-bit) in the data stream on IOM-2000 DX line together with the 8 kHz IOM-2000 FSC pulse. This is required due to the 8 kHz clock rate of the FSC signal in comparison to the 4 kHz frame length in the U_{PN} interface.

The code violation in the LF position is generated by the VIP when INFO1 is transmitted, according to the DSP command bits SMINI(2:0).

In the receive direction the first ‘1’ recognized on the line after “no signal”, which is represented by logic ‘0’, is treated as the LF-bit. The code violation in the LF-bit position is recognized by the VIP when INFO 2 is received. This information is forwarded to the DELIC as part of the VIP receiver status bits RxSTA(1:0).

4.2.5.2 Multiframing Bit (M-Bit)

On the U_{PN} interface, multiframes are composed of four U_{PN} frames. The multiframe is included at the M-bit position. Every fourth M-bit, a code violation indicates the start of a new multiframe.

In transmit direction, the VIP extracts the multiframe bits out of the IOM-2000 data coming from DELIC and inserts them in the U_{PN} frame at the line side.

In receive direction, the VIP extracts the multiframe bits out of the data coming from the U_{PN} line and inserts them in the IOM-2000 frame to the DELIC.

A multiframe counter in the VIP guarantees the timing of the multiframe. It is synchronized (reset) every 20th U_{PN} frame (=every 40th IOM-2000 frame) by the command bit ’SH_FSC’ issued by the DELIC.

Note: The SH_FSC bit performs the functionality of the short FSC pulse in OCTAT-P and QUAT-S.

T-bit

The T-bit received on the U_{PN} line is inserted by the VIP in the IOM-2000 data receive (DR) line at the multiframe (M-bit) position in every frame; i.e. not only at the usual T-bit position every third frame, but also at the S-bit position and the code violation (CV)

position. The DELIC DSP software may evaluate the received T-bit to provide the user with an additional data channel (under consideration). Note that this is an additional feature to the OCTAT-P.

In transmit direction, the T-bit value is sent in the data stream from the DELIC to the VIP, and passed on transparently to the U_{PN} terminal. The T-bit value may be programmed in DELIC's data RAM. It is required e.g. for DECT synchronization.

S-bit

The S-bit received on the U_{PN} line interface is extracted by the VIP out of the data stream, and is logical OR' ed with the detected far-end code violation. The result is sent to the DELIC as status bit 'FECV'.

In transmit direction, the S-bit value is sent in the data stream from the DELIC to the VIP, and passed on transparently to the U_{PN} terminal. The S-bit value may be programmed in DELIC's data RAM. It is required e.g. for switching a digital loop in the terminal.

CV-bit

The code violation bit received on the line is not transmitted to the DELIC.

4.2.5.3 DC-Balancing Bit

A DC-balancing bit is inserted by the VIP according to the Balancing Bit Control (BBC) bit transmitted to the VIP on the command line.

In receive direction, the DC balancing bit is received, but not evaluated.

4.2.6 IOM-2000 Command and Status Interface

All Command/Status bits used for VIP channel programming are divided into one group used only during initialization, and one group used during normal operation.

Initialization Mode Command Bits

The bits of this group are used for VIP initialization or in operation modes where an immediate reaction is not required. The initialization group includes command bits and the channel address, stored in register TICCMR. Note that the usage of this group of bits is limited in a way that only one channel may be accessed in each frame.

In test mode, the command word to VIP_n (CMD_n) and to Channel_m of VIP_n (CMD_n_m) may be read by the DELIC in the next frame after issuing bits 'RD_n' or 'RD'. The VIP mirrors the command word exactly as it was received, despite the bits 'WR', 'WR_ST', 'RD'. The VIP status is saved in the TRANSIU initialization status (TICSTR) register, which includes status bits and the channel address.

Note: The commands must not be read during normal operation, since in this case the reporting of the VIP status to the DELIC would not be possible.

Operational Mode Command/Status Bits

The bits of this group are used during normal operation, hence they are evaluated in every frame. They include all VIP receiver status bits and some of the command bits. The operational mode command/status bits are buffered in the Data RAM.

The VIP receiver status bits do not reflect a status change, but the status itself, i.e. the current value of the line interface INFOs, until the values change.

The FECV is only reported to the DELIC upon changes.

Command/Status Transmission

The command/status bits are transmitted/received by the TRANSIU at the same rate as data transmission rate, starting with the 8 kHz FSC.

Transmit Direction

- The command information per VIP is prepared by the DSP in the VIPCMR0-2 registers
- The command bits from initialization command group are prepared by the DSP in the ICCMR register for one of the channels
- TRANSIU operation mode command format in the Data RAM:

7	6	5	4	3	2	1	0
data byte 1							
data byte 2							
data byte 3							
x	x	x	SMINI(2:0)			MSYNC	WR_ST

WR_ST **Write Command to TST1 Bits (S/T, U_{PN})**

0 = Data sent in these bits is invalid

1 = SMINI(2:0) and MSYNC contain valid data

MSYNC **Multiframe Synchronization (LT-T)**

0 = VIP mirrors the F_A-bit

1 = VIP stops the F_A-bit mirroring (for multiframe synchronization)

SMINI(2:0) **State Machine Initialization (S/T, U_{PN})**

Command to VIP from the DELIC layer-1 state machine. Depending on the state, the VIP may transmit data on the U_{PN} or S/T interface. The VIP responds by sending the receiver status bits STAT_n_m.RxSTA(1:0) to the DELIC.

000 = INFO 0 in S/T or U_{PN}

001 = INFO 1w in U_{PN}

010 = INFO 1 in LT-T, INFO 2 in LT-S or U_{PN}

011 = INFO 3 in LT-T, INFO 4 in LT-S or U_{PN}

100 = Test mode 'Send Continuous Pulses SCP':
'1s' transmitted at 96 kHz (U_{PN}) and at 192 kHz S/T)

101 = Test mode 'Send Single Pulses SSP' (at 2 kHz burst rate)

Note: all other states are reserved

Receive Direction

- The received status per VIP is stored in the VIPSTR0-2 registers
- If the "read_status" command was transmitted in the previous frame for one of the channels, the received status from this channel is saved in the TICSTR register together with the 5-bit channel address
- TRANSIU operation mode status format in the Data RAM:

7	6	5	4	3	2	1	0
data byte 1							
data byte 2							
data byte 3							
x	MSYNC	FCV	FSYNC	SLIP	FECV	RxSTA(1:0)	

RxSTA(1:0) **Receiver Status Change (S/T, U_{PN})**

00 = Receiver is not synchronized to the line; no signal on line (INFO 0)

01 = Level detected on line (any signal) (INF 1 in LT-S mode)

10 = Receiver is synchronized to the line, but not activated (INFO 2 in LT-T mode)

11 = Receiver is synchronized and activated (INFO 4 for LT-T mode INFO 3 for LT-S and U_{PN})

FECV **Far-end Code Violation (S/T, U_{PN})**

0 = Normal operation

1 = Illegal code: FECV according to ANSI T1.605 detected (S/T)

SLIP **Frame Slip Detected (LT-T)**

0 = No frame slip detected

1 = A frame slip of more than 25 µs (tbd) was detected on the LT-T channel

FSYNC * **F-Bit Synchronous (S/T + U_{PN} test mode only!!)**

FCV * **Code Violation in F-Bit detected (U_{PN} test mode only!!)**

MSYNC / LD * **Multiframe Synchronous (U_{PN}), Level Detected (S/T), test mode!!**

*Note: with * marked bits are not evaluated by the DELIC, only for VIP testing.*
Bits SLIP, FECV and are directly available to the DSP software in the TRANSIU receive data RAM.

4.2.7 IOM-2000 Data Interface

Data processing and frame handling in the TRANSIU is fully DSP controlled. Serial data received and transmitted on the IOM-2000 Interface is arranged in the Shift Receive RAM and Shift Transmit RAM.

The DSP processed bytes are stored in the TRANSIU Current Buffer. Every 8 kHz frame the TRANSIU and DSP Current Buffers are switched.

4.2.7.1 U_{PN} Mode

The data is received and transmitted at a nominal bit rate of 384 kbit/s. In the first half of the 4 kHz U_{PN} frame data is transmitted and ‘zeros’ are received, in the second half of the frame ‘zeros’ are transmitted and data is received.

Scrambling and de-scrambling of the B-channel data is done automatically. The received and transmitted data is stored in the Data RAM in the following format:

U_{PN} Mode Receive / Transmit Data Format

7	6	5	4	3	2	1	0
B1-channel data							
B2-channel data							
D-channel		M-bit	x	x	x	x	x
Operation Mode Command/Status bits							

In transmit direction, depending on the multiframe position, the M-bit contains either the T-bit or the S-bit with the following functionality:

- T-bit: a) D-channel available info to the terminal
  b) DECT synchronization signal
- S-bit: switches remote loop in terminal device

4.2.7.2 U_{PN} Scrambler/Descrambler

B-channel data on all U_{PN} channels of the IOM-2000 interface is scrambled to give a flat continuous power density spectrum on the line.

Scrambling is done according to ITU-T V.27 with the generator polynomial $1 + x^6 + x^7$

Initialization via History RAM (HRAM)

The scrambler is activated/de-activated for each U_{PN} channel separately by a DSP write to the history RAM address.

During initialization the DSP writes a value with '0' in its LSB (other bits are of no importance) to every History RAM address associated to an U_{PN} channel that is not to be scrambled, and a value with '1' in its LSB for every U_{PN} channel that must be scrambled. The same values must be written to the descrambler history RAM.

The HRAM addresses are:

- 0x9000 - 0x9017 (scrambler U_{PN} channel 0..23)
- 0x9020 - 0x9037 (descrambler U_{PN} channel 0..23)

For example, in order to activate scrambling and descrambling for channel number 3, the DSP must execute two write operations as follows:

- Write "xxxxxxxxxxxxxxx1" to address 0x9002
- Write "xxxxxxxxxxxxxxx1" to address 0x9022

These writes are executed only when the scrambler is in idle mode, i.e. value 0x0003 was written by the OAK to address 0xD010.

4.2.7.3 S/T Mode

Data is received/transmitted at a nominal rate of 192 kbit/s. Each S/T data bit is translated into two bits on IOM_2000: data (bit0) and control (bit1).

LT-S Mode Transmit Data Format

7	6	5	4	3	2	1	0
B1-channel data							
B2-channel data							
D-channel		x	F_a	M	S	x	x
Operation Mode Command/Status bits							

LT-S Mode Receive Data Format

7	6	5	4	3	2	1	0
B1 - channel data							
B2 - channel data							
D-channel		F_a	x	x	x	x	x
Operation Mode Command/Status bits							

LT-T Mode Receive Data Format

7	6	5	4	3	2	1	0
B1-channel data							
B2-channel data							
D-channel		x	F_a	M	S	CBN	CDI
Operation Mode Command/Status bits							

CBN **Collision Detection Bit Number**

0 = Collision was detected in the first D-bit of the frame

1 = Collision was detected in the second D-bit of the frame

CDI **Collision Detection Indication**

0 = No collision in D-channel

1 = Collision in D-channel detected

LT-T Mode Transmit Data Format

7	6	5	4	3	2	1	0
B1-channel data							
B2-channel data							
D-channel		F_a	x	x	x	x	x
Operation Mode Command/Status bits							

4.3 IOM-2 Unit

4.3.1 IOMU Overview of Features

The IOMU provides the DSP access to incoming time slots from the IOM-2 interface. The DSP may switch the timeslots to the other DELIC system interfaces.

Features

- DSP access for switching of B1 and B2 data to the PCMU and the TRANSIU (providing a constant switching delay of two 8 kHz frames)
- DSP access for extracting of D-channel information
- DSP access for control of IOM-2 Command/Indication (C/I) and Monitor channel information

Interface Configuration

- Two IOM-2 ports providing up to 16 IOM-2 channels (up to 16 ISDN or 32 analog subscribers)
- Available data rate modes:

– Two ports of 384 kbit/s each (2 x 6 time slots per frame)
– Two ports of 768 kbit/s each (2 x 12 time slots per frame)
– Two ports of 2.048 Mbit/s each (2 x 32 time slots per frame)
– One port of 4.096 Mbit/s (1 x 64 time slots per frame)

- Single or double data rate clock selectable in each data rate mode
- Programmable tri-state control for each port and channel (=4 time slots)
- Push-pull or open-drain configuration
- DRDY signal for D-channel control when connected to QUAT-S PEB 2084

4.3.2 IOMU Functional and Operational Description

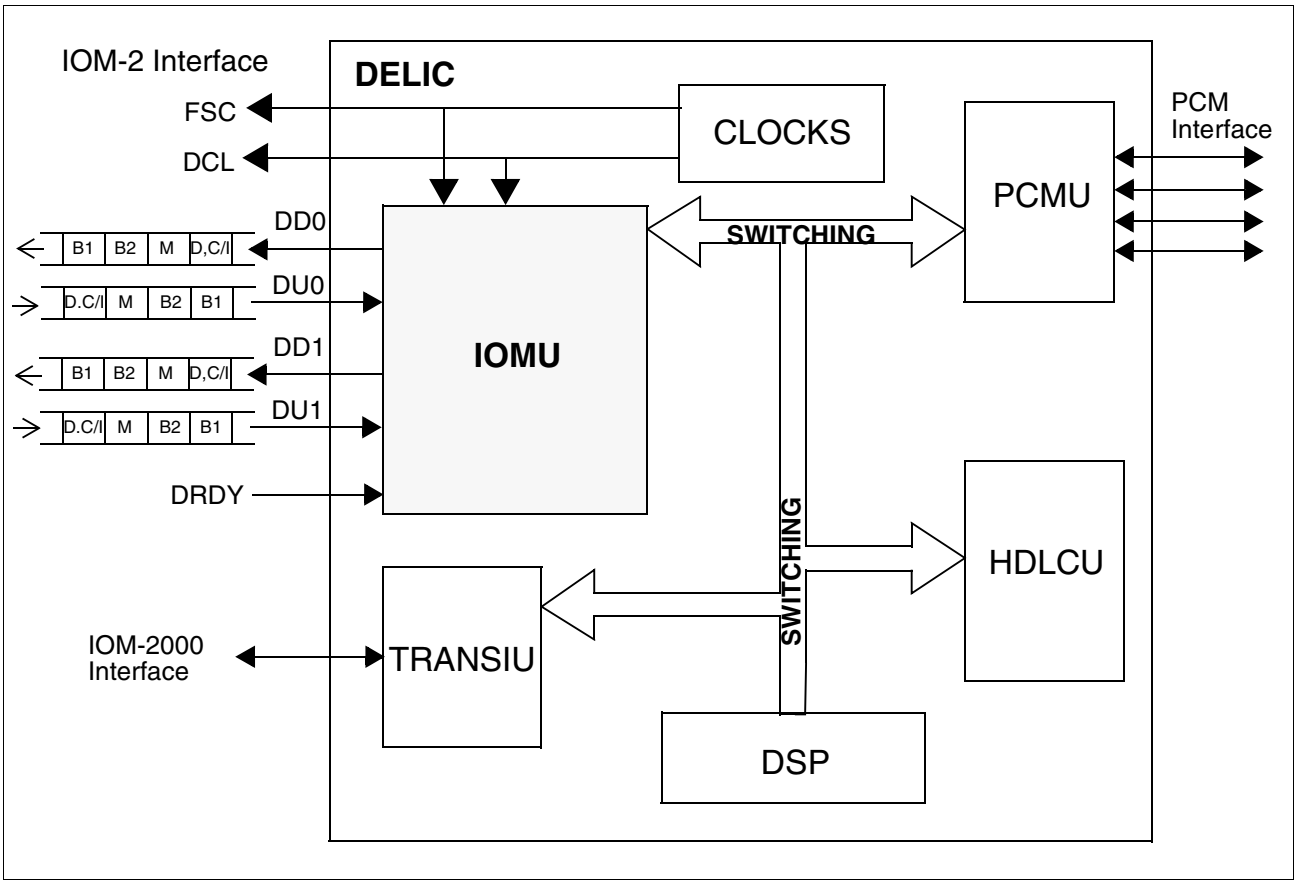


Figure 4-3 IOMU Integration in DELIC

4.3.2.1 Frame-Wise Buffer Swapping

The main task of the IOMU is the serial-to-parallel conversion of incoming IOM-2 data to a parallel data format which is directly read by the DSP. This access is required for the DSP to perform switching of B-channels, extraction of D-channels, and layer-1 control via the IOM-2 C/I and Monitor channels.

The data conversion in the IOMU is done by frame-wise swapping based on a circular buffer structure. During each 8 kHz frame, one buffer is assigned to the IOMU (I-buffer), and the other one to the DSP (D-buffer). At the end of every frame, the buffers are swapped.

4.3.2.2 I-buffer Logical Structure

The logical partitioning of each frame buffer into input and output blocks is determined according to the requested data rate as shown in the table below.

The address of each data byte in the I-buffer output blocks by the DSP must be selected according to the IOM port and time slot index, in which it should be transmitted.

Table 4-3 I-Buffer Logical Memory Mapping

Data Rate	Input Blocks		Output Blocks	
	in0	in1	out0	out1
2 x 2.048 Mbit/s 2 x 384 kbit/s 2 x 768 kbit/s	00_H - $1F_H$	20_H - $3F_H$	40_H - $5F_H$	60_H - $7F_H$
1 x 4.096 Mbit/s	00_H - $3F_H$	--	40_H - $7F_H$	--

Note: In 2 x 384 / 768 kbit/s mode, only the first 6 / 12 bytes of each block are used.

4.3.2.3 DSP Access to the D-Buffer

The D-buffer is mapped to a fixed DSP address space. Every DSP access to the D-buffer space is directed automatically to the appropriate sub-buffer.

Table 4-4 D-Buffer Address Space

Data-Rate Mode	D-Buffer			
	in0	**in1**	**out0**	**out1**
2 x 6/12/32 time slots/frame	8000_H - $801F_H$	8020_H - $803F_H$	8040_H - $805F_H$	8060_H - $807F_H$
1 x 64 time slots/frame	8000_H - $803F_H$	-	8040_H - $807F_H$	-

4.3.2.4 IOM-2 Interface Data Rate Modes

The IOMU may support different serial data rates of the IOM-2 interface:

- 384 kbit/s (6 time slots per frame)
- 768 kbit/s (12 time slots per frame)
- 2.048 Mbit/s (32 time slots per frame = 8 IOM-2 channels per frame)
- 4.096 Mbit/s (64 time slots per frame = 16 IOM-2 channels per frame)

The IOMU circular buffer may handle up to 64 time slots per frame. Thus, when in 4.096 Mbit/s mode, only IOM-2 port 0 is used. In this case IOM-2 port 1 remains in IDLE mode, i.e. the DD1 output pin is tri-stated.

Note that when using any of the two lower data rates, both IOM-2 ports are used.

In all data rate modes, single rate Data Clock (DCL) or double rate Data Clock may be selected.

Table 4-5 DCL Frequency in Different IOM-2 Modes

Single/Double Rate DCL Mode	IOM-2 Mode			
	2x384 kbit/s	2x768 kbit/s	2x2.048 Mbit/s	1x4.096 Mbit/s
Single	384 kHz	768 kHz	2.048 MHz	4.096 MHz
Double	768 kHz	1536 kHz	4.096 MHz	8.192 MHz

The IOMU meets the IOM-2 interface timing specifications as described below.

Single Data Rate DCL Mode

- Serial transmission via DD0/DD1 with every DCL rising edge
- Sampling of the incoming serial data (DU0/DU1) with every DCL falling edge
- Sampling FSC with every DCL falling edge. Sampling of FSC = 1 after sampling of FSC = 0 is considered to be the start of a frame.

Double Data Rate DCL Mode

- Two DCL cycles per bit (the bits are aligned to the frame start)
- Serial transmission via DU0/1 with every second DCL rising edge.
- Sampling of incoming serial data (DD0/1) with the second DCL falling edge of each bit.
- Sampling of FSC every DCL falling edge. Sampling of FSC = 1 after sampling of FSC = 0, is considered to be the start of a new frame.

Figure 4-4 shows the IOM-2 interface timing with single and double rate DCL. For more details refer to the general IOM-2 interface description.

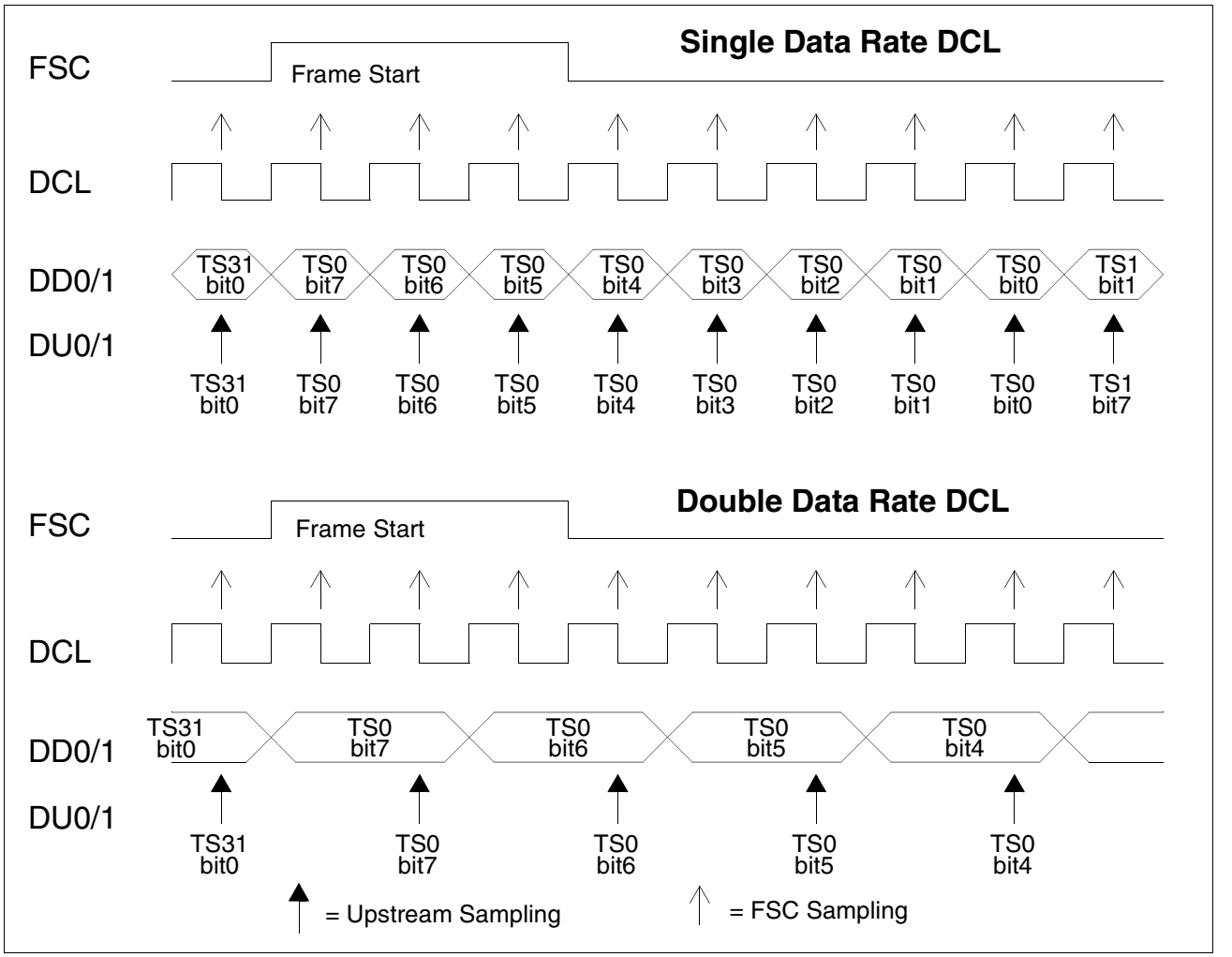


Figure 4-4 IOM-2 Interface Timing in Single/Double Clock Mode

4.3.2.5 IOMU Serial Data Processing

The IOMU serial data processing is according to the IOM-2 specifications. Incoming serial data is converted into parallel bytes, and stored in the I-buffer input blocks. The sequence for every time slot received is from MSB (bit 7) to LSB (bit 0). Transmission is performed in the opposite direction, from MSB (bit 7) to LSB (bit 0).

4.3.2.6 IOMU Parallel Data Processing

The data read from the IOMU frame buffers by the DSP always reside in the low byte of the 16-bit word. The high byte of the read word is driven by the 8-bit IOMU Data Prefix Register (IDPR). The data prefix is used to accelerate the A-/µ-law to linear conversions (refer to **Chapter 4.5**).

Note: Any octet written by the DSP to any location in the IOMU frame buffers should reside in the low byte (8 LSB). The high byte of the written word is “don’t care”.

4.3.2.7 IOM-2 Push-Pull and Open-Drain Modes

The IOM-2 ports can be configured to Push-Pull or Open-Drain modes by a dedicated bit in the IOMU Control Register. When programmed to Open-Drain, DD0/DD1 is tri-stated when a ‘1’ is supposed to be transmitted, or during a time slot quadruplet with the associated Tri-State Register bit set.

In both cases the external pull-up resistor, which is used when working in open-drain mode, will “pull” the value to ‘1’.

Note: When the IOMU is programmed to 1x 64 time slots per frame mode, DD1 is tri-stated, independently of the IOM-2 interface push-pull or open-drain mode.

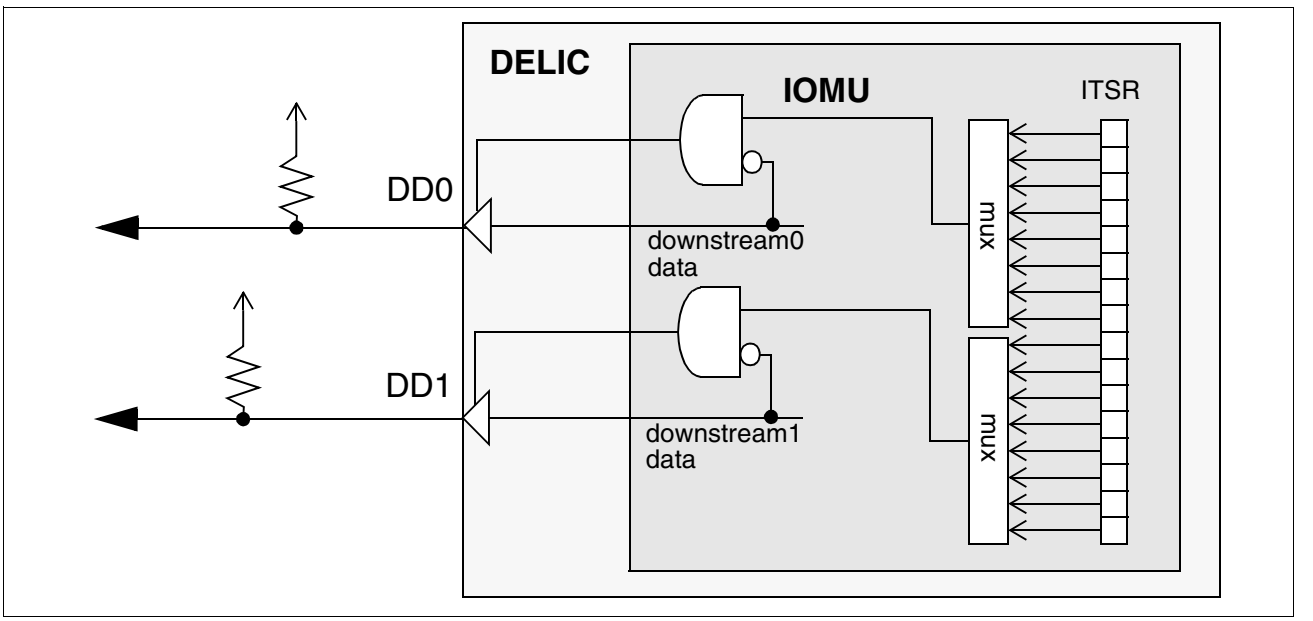


Figure 4-5 IOM-2 Interface Open-Drain Mode

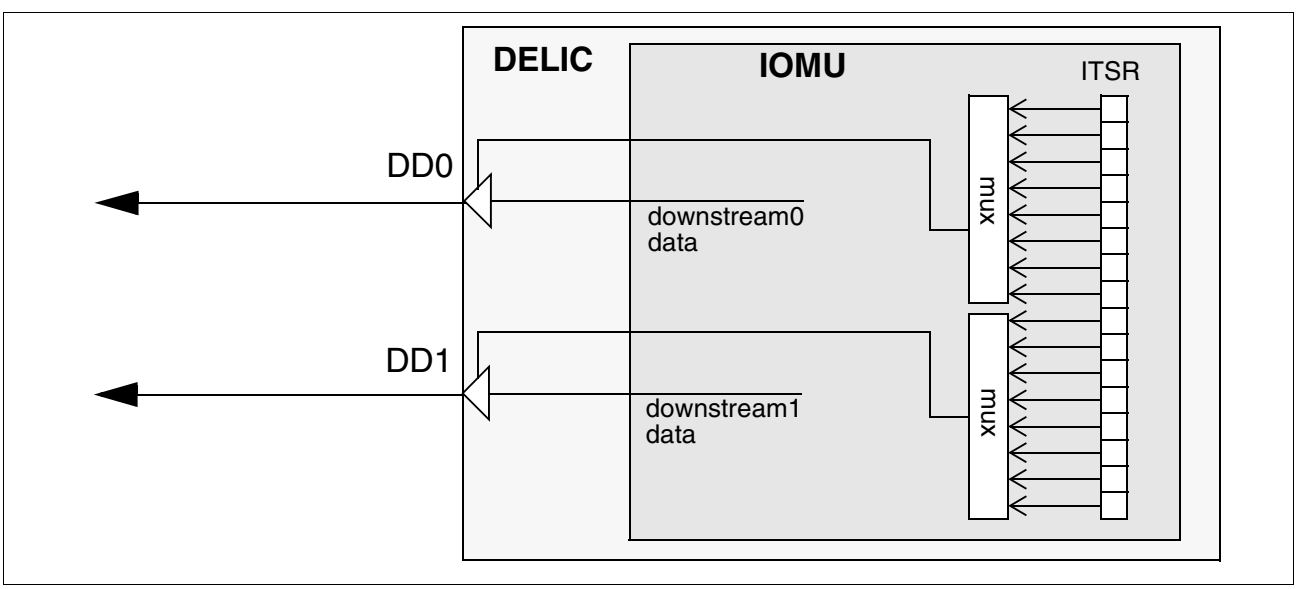


Figure 4-6 IOM-2 Interface Push-Pull Mode

4.3.2.8 Support of DRDY Signal from QUAT-S

The DRDY input is used when connecting a Siemens QUAT-S transceiver to the DELIC via the IOM-2 interface. It is driven by the QUAT-S to inform the DELIC when a D-channel is occupied by another S-interface device.

The IOMU supports the synchronous DRDY mode, i.e. the QUAT-S is operated in LT-T mode. In this mode, the DRDY signal is valid only during the D-channels.

DRDY = ‘0’ means STOP (ABORT HDLC message), and DRDY = ‘1’ means GO.

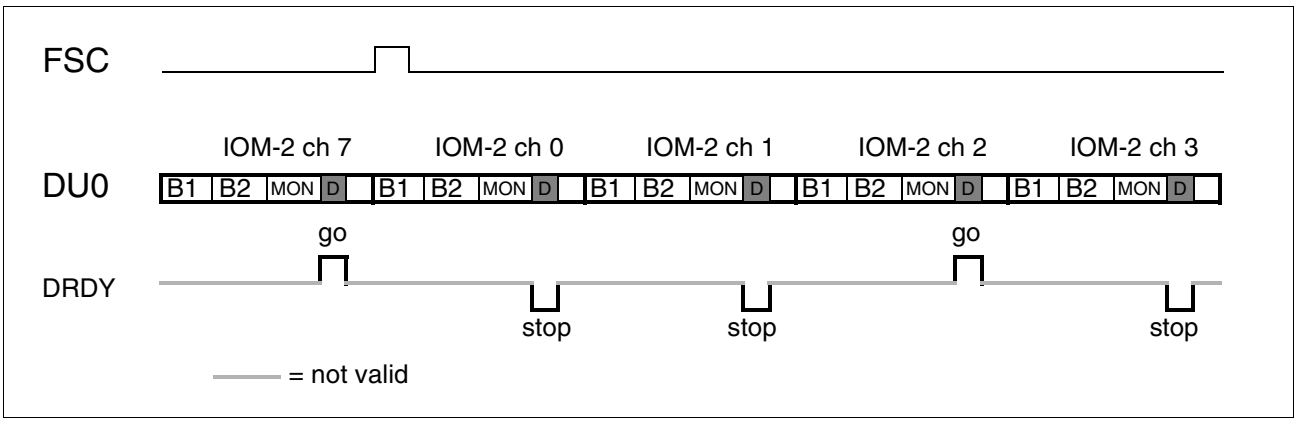


Figure 4-7 DRDY Signal Behavior

IOMU DRDY support features:

- Sampling DRDY only once every D-channel, at the first bit.
- Sampling with the first DCL falling edge (in single data-rate DCL mode), or with the second falling DCL edge (in double data-rate DCL mode), refer to **Figure 4-8**.
- DRDY support via IOM-2 port 0 only (with a constant delay of one 8 kHz frame)
- The status of the DRDY line can be read from register IDRDYR

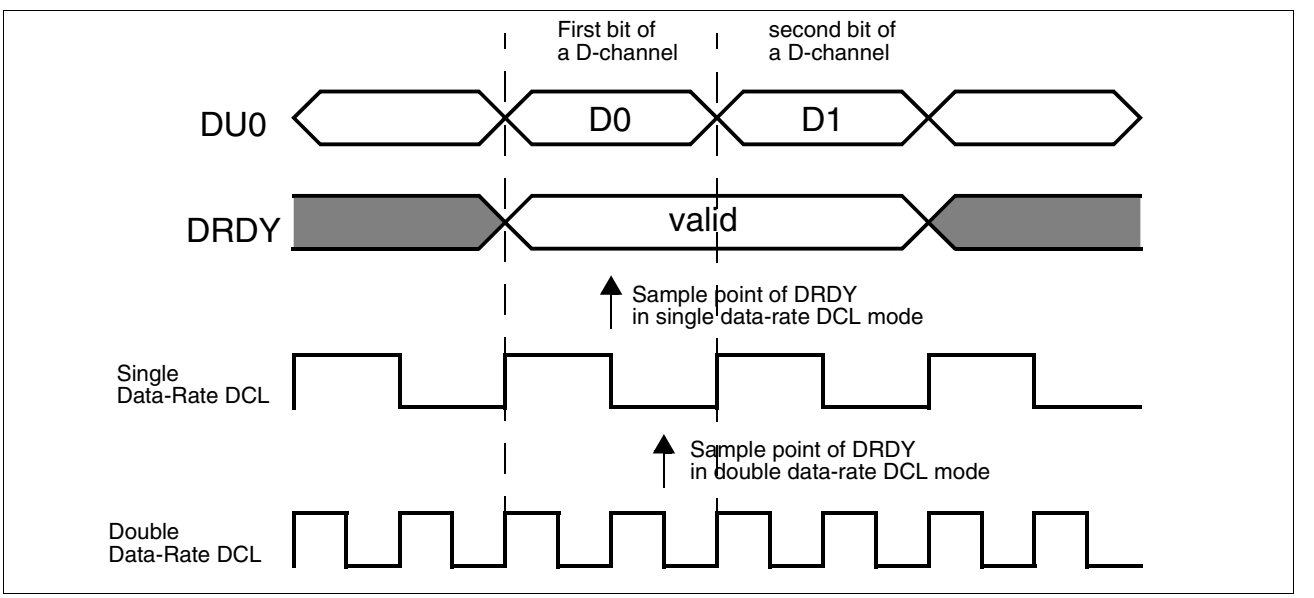


Figure 4-8 DRDY Sampling Timing

4.4 PCM Unit

PCM Interface Features

The PCMU enables the DSP to control the 4 PCM ports. The DSP accesses the incoming PCM time slots, and prepares the outgoing PCM time slots. In general, the PCMU enables the DSP to switch time slots from and to the PCM ports.

The basic structure and programming model of the PCMU is similar to the IOMU. Note that the PCMU provides the double capacity of the IOMU. Thus it may handle up to 4 PCM ports and an overall of 128 time slots per frame in the receive direction and 128 time slots per frame in the transmit direction.

The following PCMU data rate modes are available:

- Four streams of 2.048 Mbit/s each (single and double clock)
- Two streams of 4.096 Mbit/s each (single and double clock)
- One stream of 8.192 Mbit/s (single and double clock)
- One stream of 16.384 Mbit/s (single clock). It is programmable, whether the first or the second 128 time slots of the 8 kHz frame are handled in the PCMU.

Tristate control is performed via pins $\overline{\text{TSC}}$n, programmable per time slot and port.

4.4.1 PCMU Functional and Operational Description

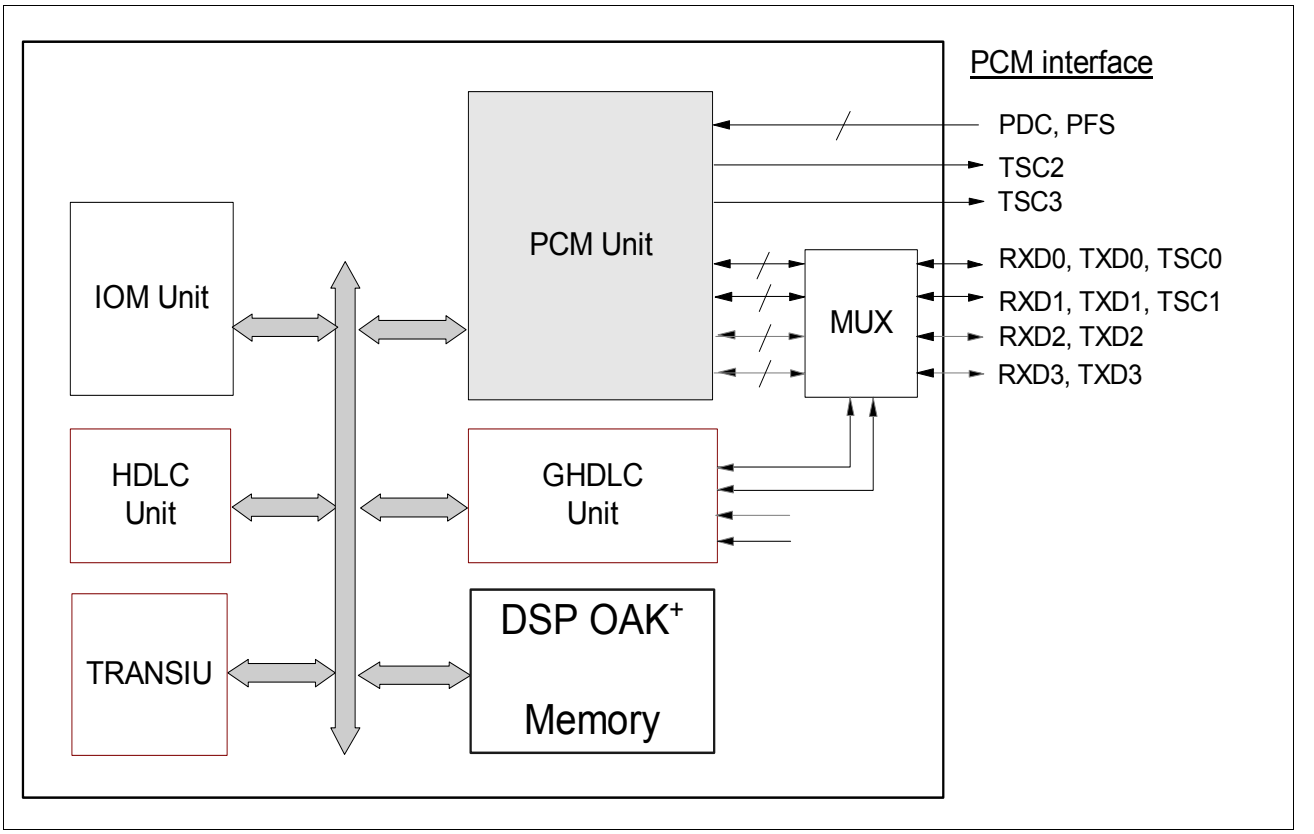


Figure 4-9 PCMU Integration in DELIC

The PCM-unit signals share port pins with the GHDLC-unit. A multiplexer controlled by register MUXCTRL allows to define the required functionality.

4.4.1.1 Frame-Wise Buffer Swapping

The main task of the PCMU is the serial-to-parallel conversion of incoming data to a parallel data format (and vice versa) which is directly read by the DSP. This access is required for the DSP to perform switching of B-channels.

The data conversion in the PCMU is done by frame-wise swapping based on a circular buffer structure. During each 8 kHz frame, one buffer is assigned to the PCMU (I-buffer), and the other one to the DSP (D-buffer). At the end of every frame, the buffers are swapped.

4.4.1.2 DSP Inaccessible Buffer (I-buffer)

The logical partitioning of each frame buffer into input and output blocks is determined according to the requested data rate as shown in the table below.

The address of each data byte in the I-buffer output blocks by the DSP must be selected according to the PCM port and time slot index, in which it should be transmitted.

Table 4-6 I-Buffer Logical Memory Mapping of Input Buffers

Data Rate	Input Blocks			
	in0	in1	in2	in3
related port	RXD0	RXD1	RXD2	RXD3
4 x 2.048 Mbit/s	00_H - $1F_H$	20_H - $3F_H$	40_H - $5F_H$	60_H - $7F_H$
2 x 4.096 Mbit/s	00_H - $3F_H$	40_H - $7F_H$		
1 x 8.192 Mbit/s	00_H - $7F_H$			
1 x 16.384 Mbit/s	00_H - $7F_H$			

Table 4-7 I-Buffer Logical Memory Mapping of Output Buffers

Data Rate	Output Buffer Blocks			
	out0	out1	out2	out3
related port	TXD0	TXD1	TXD2	TXD3
4 x 2.048 Mbit/s	80_H - $9F_H$	$A0_H$ - BF_H	$C0_H$ - DF_H	$E0_H$ - FF_H
2 x 4.096 Mbit/s	80_H - BF_H	$C0_H$ - FF_H		
1 x 8.192 Mbit/s	80_H - FF_H			
1 x 16.384 Mbit/s	80_H -FF_H			

Note: In 1 x 16.384 Mbit/s only the first half of the frame is saved in the buffer

4.4.1.3 DSP Accessible Buffer (D-Buffer)

The D-buffer is mapped to a fixed DSP address space. Every DSP access to the D-buffer space is directed automatically to the appropriate sub-buffer.

Table 4-8 DSP Access to D-Buffer Input Blocks

Data Rate	Input Buffer Blocks			
	in0	in1	in2	in3
related port	RXD0	RXD1	RXD2	RXD3
4 x 2.048 Mbit/s	$A000_H$ - $A01F_H$	$A020_H$ - $A03F_H$	$A040_H$ - $A05F_H$	$A060_H$ - $A07F_H$
2 x 4.096 Mbit/s	$A000_H$ - $A03F_H$	$A040_H$ - $A07F_H$		
1 x 8.192 Mbit/s	$A000_H$ - $A07F_H$			
1 x 16.384 Mbit/s	$A000_H$ - $A07F_H$			

Table 4-9 DSP Access to D-Buffer Output Blocks

Data Rate	Output Buffer Blocks			
	out0	out1	out2	out3
related port	TXD0	TXD1	TXD2	TXD3
4 x 2.048 Mbit/s	$A080_H$ - $A09F_H$	$A0A0_H$ - $A0BF_H$	$A0C0_H$ - $A0DF_H$	$A0E0_H$ - $A0FF_H$
2 x 4.096 Mbit/s	$A080_H$ - $A0BF_H$	$A0C0_H$ - $A0FF_H$		
1 x 8.192 Mbit/s	$A080_H$ - $A0FF_H$			
1 x 16.384 Mbit/s	$A080_H$ - $A0FF_H$			

Note: In 1 x 16.384 Mbit/s only the first half of the frame is saved in the buffer

4.4.1.4 PCMU Interface Data Rate Modes

The PCMU may support different serial data rates:

- up to 4 ports with 2048 Mbit/s (32 time slots per frame)
- up to 2 ports with 4.096 Mbit/s (64 time slots per frame)
- 1 port with 8.196 Mbit/s (128 time slots per frame)
- 1 port with 16.384 Mbit/s (only 128 time slots of the frame are supported)

The PCMU circular buffer may handle up to 128 time slots per frame. Thus, when e.g. configured in 4.096 Mbit/s mode, only PCM port 0 and 2 are used. In this case PCM port 1 and 3 remain in IDLE mode, i.e. the TXD1, TXD3 output pins are tri-stated.

For the data rate modes up to 8.192 MBit/s, single rate Data Clock (PDC) or double rate Data Clock may be selected. For 16.384 MHz mode only single clock is supported.

Single Data Rate PDC Mode

- Serial transmission via TXDn with every DCL rising edge
- Sampling of the incoming serial data (RXDn) with every PDC falling edge
- Sampling PFS with every PDC falling edge. Sampling of PFS = 1 after sampling of PFS = 0 is considered to be the start of a frame.

Double Data Rate PDC Mode

- Two PDC cycles per bit (the bits are aligned to the frame start)
- Serial transmission via TXDn with every second PDC rising edge.
- Sampling of incoming serial data (RXDn) with the second PDC falling edge of each bit.
- Sampling of PFS every PDC falling edge. Sampling of PFS = 1 after sampling of PFS = 0, is considered to be the start of a new frame.

Figure 4-4 shows the PCM interface timing with single and double rate PDC.

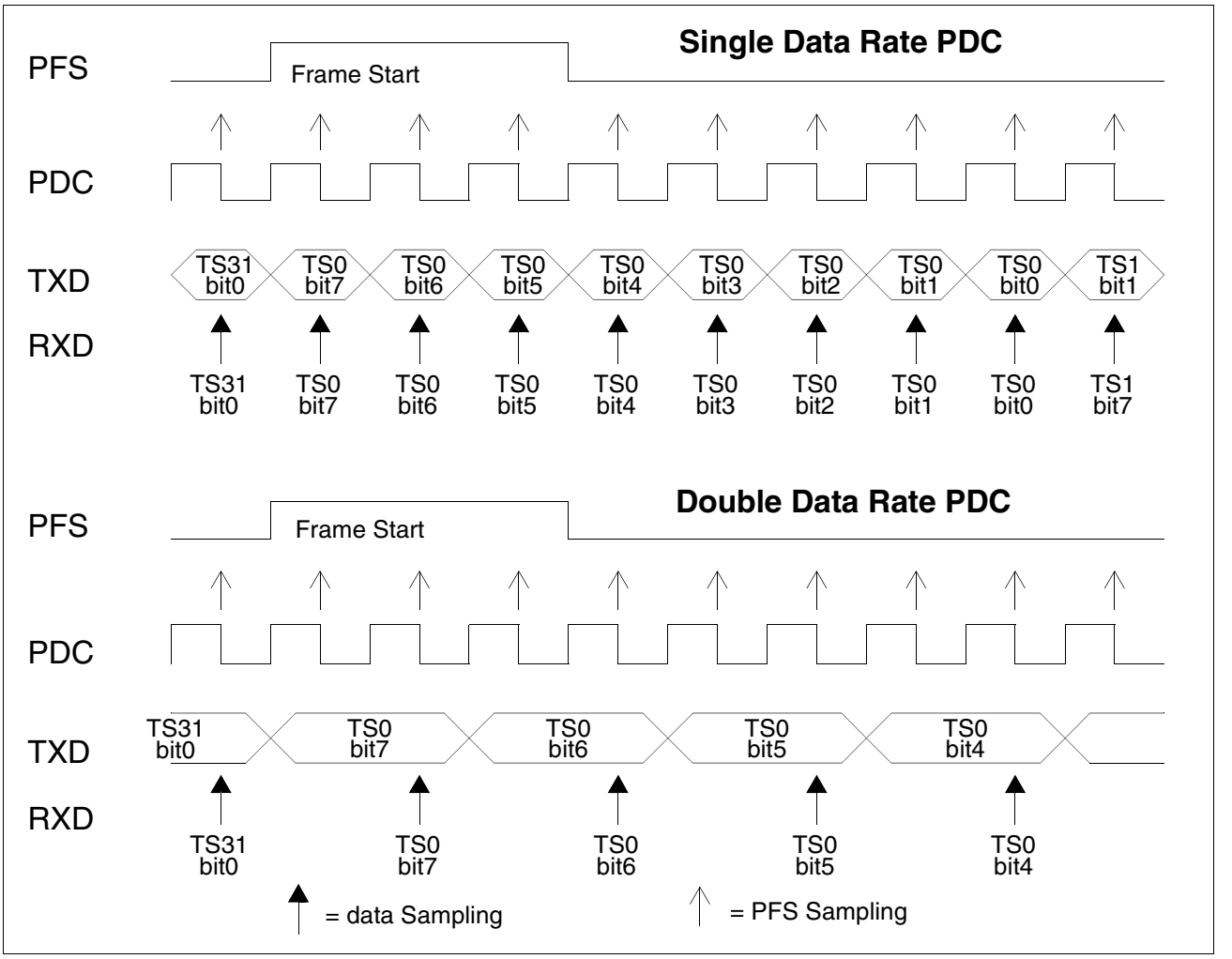


Figure 4-10 IOM-2 Interface Timing in Single/Double Clock Mode

4.4.1.5 PCMU Serial Data Processing

The incoming serial data is converted into parallel bytes, and stored in the I-buffer input blocks. The sequence for every time slot received is from MSB (bit 7) to LSB (bit 0). Transmission is performed from MSB (bit 7) to LSB (bit 0).

4.4.1.6 PCMU Parallel Data Processing

The data read from the PCMU frame buffers by the DSP always reside in the low byte of the 16-bit word. The high byte of the read word is driven by the 8-bit PCMU Data Prefix Register (PDPR). The data prefix is used to accelerate the A-/µ-law to linear conversions (refer to **Chapter 4.5**).

Any octet written by the DSP to any location in the PCMU frame buffers should reside in the low byte (8 LSB). The high byte of the written word is “don’t care”.

4.4.1.7 PCMU Tri-state Control Logic

There are eight 16-bit tri-state control registers in the PCMU. Each bit determines whether its associated time slot is valid or invalid.

- '0' = the controlled time slot is invalid
- '1' = the controlled time slot is valid

The tri-state bits control the data transmit pins TXD0 - TXD3.

A special set/reset write method is used for updating the tri-state control registers. Every tri-state control register is mapped to 2 addresses: the first is used for set operation, the second for reset operation. Both addresses may be used for read operation.

- Set operation: This operation is executed during DSP write access to the set address of one of the TSC registers. The bits in the TSC register are set to '1' according to the bits in the written word. The other bits maintain their value.
- Reset operation: This operation is executed during DSP write access to the reset address of one of the TSC registers. The bits in the TSC register are reset to '0' according to the bits in the written word. The other bits maintain their value.

The Tristate Control Registers (PTSR0-7) can be accessed by the DSP. Every bit of them controls the TSC signal of one of the 4 PCM ports, for one time slot. The time slot and the port controlled by every bit depend on the data rate mode. In 1x256 TS/frame, it depends also on the selected half of the frame. Each TSC signals controls directly its respective TxD port, and is also driven outward via the corresponding TSCn output pin.

For the 4 x 32 time slot per frame mode, the next table depicts which port is controlled by each TSC register, and during which time slot. Bit 0 of each TSC register controls the first time slot of the listed time slot range, bit 1 controls the second one etc.

Table 4-10 PCM TSC in 4 x 32 TS Mode

Time Slots	TSC0	TSC1	TSC2	TSC3
0..15	PTSC0	PTSC2	PTSC4	PTSC6
16..31	PTSC1	PTSC3	PTSC5	PTSC7

In 2 x 64 time slot per frame mode, only PCM ports 0 and 2 are used. TSC1 and TSC3 are permanently '0' (all time slots are invalid).

Table 4-11 PCM TSC in 2 x 64 TS Mode

Time Slots	TSC0	TSC1	TSC2	TSC3
0..15	PTSC0	inactive	PTSC4	inactive
16..31	PTSC1	inactive	PTSC5	inactive
32..47	PTSC2	inactive	PTSC6	inactive
48..63	PTSC3	inactive	PTSC7	inactive

In 1 x 128 time slot per frame mode, only PCM port 0 is used. TSC1, TSC2 and TSC3 are permanently '0' (all time slots are invalid). In 1 x 256 time slot per frame mode, only one half of the frame is used. All TSC pins are permanently '0' during the other half of the frame.

Table 4-12 PCM TSC in 1 x 128 TS and 1 x 256 TS (1st Half) Mode

Time Slots	TSC0	TSC1	TSC2	TSC3
0..15	PTSC0	inactive	inactive	inactive
16..31	PTSC1	inactive	inactive	inactive
32..47	PTSC2	inactive	inactive	inactive
48..63	PTSC3	inactive	inactive	inactive
64..79	PTSC4	inactive	inactive	inactive
80..95	PTSC5	inactive	inactive	inactive
96..111	PTSC6	inactive	inactive	inactive
112..127	PTSC7	inactive	inactive	inactive

Note: The same structure applies to the 256 TS per frame (first frame half) mode, except that all time slots (0..127) are transmitted in the first half of the 8 kHz frame.

Table 4-13 PCM TSC in 1 x 256 TS (2nd Half) Mode

Time Slots	TSC0	TSC1	TSC2	TSC3
0..127	inactive	inactive	inactive	inactive
128..143	PTSC0	inactive	inactive	inactive
144..159	PTSC1	inactive	inactive	inactive
160..175	PTSC2	inactive	inactive	inactive
176..191	PTSC3	inactive	inactive	inactive
192..207	PTSC4	inactive	inactive	inactive

Table 4-13 PCM TSC in 1 x 256 TS (2nd Half) Mode

Time Slots	TSC0	TSC1	TSC2	TSC3
208..223	PTSC5	inactive	inactive	inactive
224..239	PTSC6	inactive	inactive	inactive
240..255	PTSC7	inactive	inactive	inactive

4.5 A-law/µ-law Conversion Unit

The A-/µ-law Unit performs a bi-directional conversion between a linear representation of voice data and its companded representation (according to **A-law** or **µ-law**). The conversion is possible for all B-channels transceived via IOM-2, IOM-2000 or PCM.

A-/µ-law to Linear Conversion

The conversion is done via a 512 x 16 ROM table. The low 256 bytes translate the A-law value into linear, while the high 256 words translate the µ-law to linear.

The DSP issues a read cycle, in which the 8 MSBs of the 16-bit address represent the ROM table address, and the 8 LSBs are the actual value which is to be converted. The converted linear value is the contents read from the ROM. Note that no wait states are required for this direction of conversion.

A-law values in the ROM are stored in the 13 MSBs. The 3 LSBs are always '0'. The µ-law values in the ROM are stored in the 14 MSBs. The 2 LSBs are always '0'.

Linear to A-/µ-law Conversion

The conversion is done by dedicated hardware. The DSP programs the control register to perform either A-law or µ-law conversion. The linear value is written into the Input register (AMIR), and the A-law or µ-law value is read from the Output register (AMOR). Note that this is only possible one cycle later.

4.6 HDLC Unit

4.6.1 HDLCU Unit Overview

The HDLCU decodes and encodes HDLC messages to and from the DSP. It may process up to 32 full-duplex HDLC channels in parallel. It is controlled by the DSP through software and is thus very flexible.

The HDLCU includes a Receive Input Buffer, a Receive Output Buffer, a Transmit Input Buffer and a Transmit Output Buffer, some HDLC protocol processing logic and a command RAM.

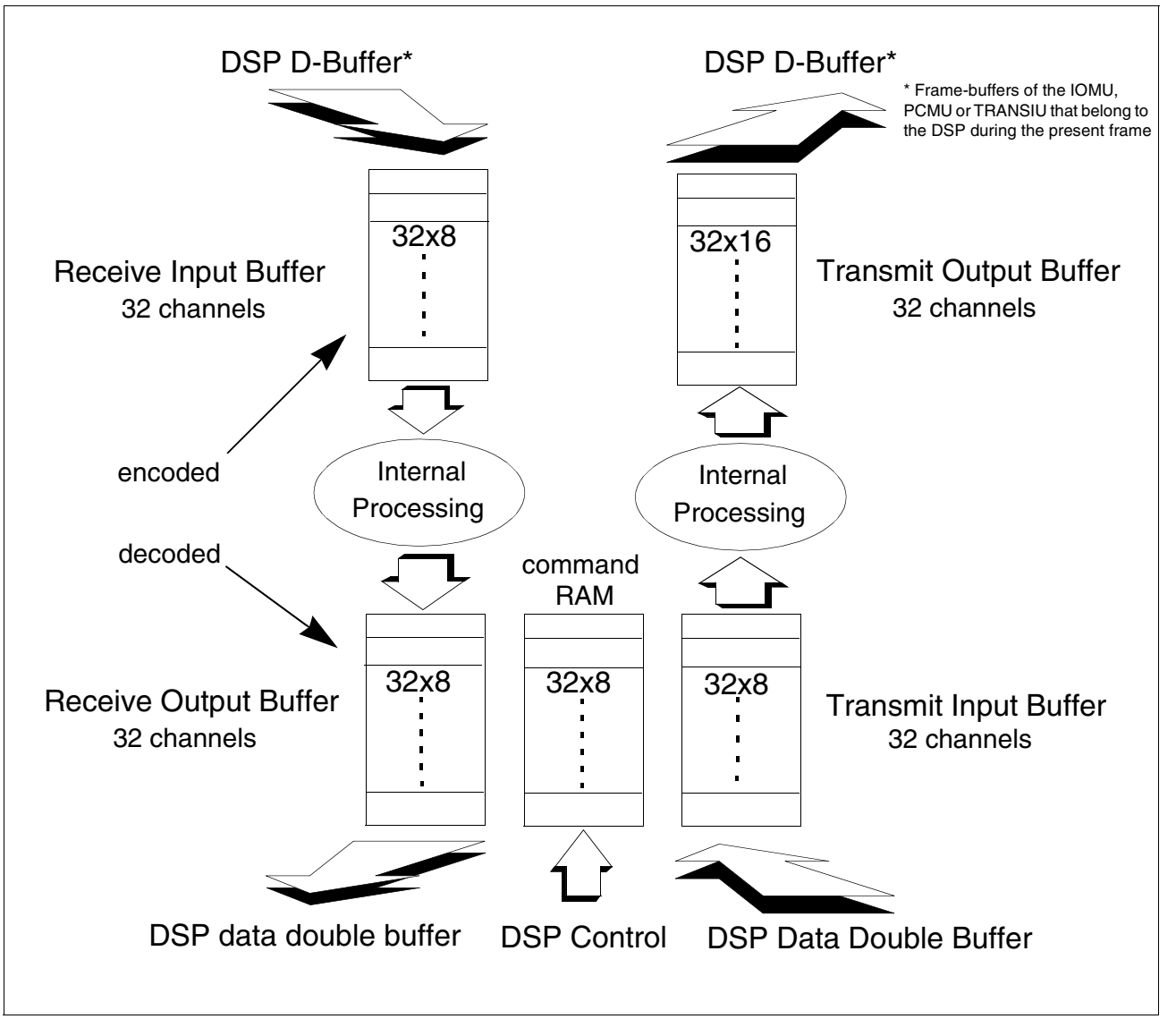


Figure 4-11 HDLCU General Block Diagram

Figure 4-11 shows the HDLCU structure. Each buffer, except the Transmit Output Buffer, is a 32 x 8 RAM, hence one byte is assigned to each HDLC time slot channel.

The Transmit Output Buffer is a 32 x 15 RAM because, in addition to each HDLC channel, there is also a 7 bit status vector assigned to each channel stored in this buffer.

The DSP assigns each time slot used for transceiving an HDLC message to a different address in the Receive/Transmit Input Buffers. The HDLCU decodes/encodes the time slots into the corresponding addresses in the Receive/Transmit Output Buffers.

During every frame, two HDLCU activities are performed:

1. DSP access to the HDLCU
2. HDLCU encoding/decoding

At the beginning of a frame the DSP checks if the HDLCU is busy (HHOLD = ’0’). Note that the DSP may only access the buffers and command RAM when DSPCTRL = ‘1’.

In the **receive direction** the DSP places HDLC message time slots to be processed from the D-buffers into the Receive Input Buffer. Processed message time slot octets may be read by the DSP from the Receive Output Buffer.

In the **transmit direction** the DSP places HDLC message time slots to be processed in the Transmit Input Buffer. Processed time slots may be read from the Transmit Output Buffer and placed into the D-Buffer of the IOMU, PCMU or TRANSIU from which they will be transmitted during the next frame.

4.6.2 DSP Operation of the HDLCU

4.6.2.1 Initialization of the HDLCU

The first frame is used to reset the receive and transmit mechanisms of each channels.

1. The DSP asks for the HDLCU setup from the External Controller.
2. The DSP sets the bit DSPCTRL to ‘1’.
3. The DSP resets the receive mechanism and transmit mechanism of a channel by setting the RECRES flag of its command vector to ‘1’ and inserting an abort command. The DSP also writes the setup of the HDLCU.
4. The DSP sets DSPCTRL to ‘0’.
5. When the HDLCU finishes processing (HHOLD = ’1’), the HDLCU is initialized and is ready for use.

4.6.2.2 Transmitting a Message

In order to transmit a message the DSP must place a Start transmission command in the appropriate address in the command RAM.

If CRC encoding is required, then the DSP must set bit 1 to ‘1’ in the command vector. In the unshared flag mode, during the first frame a flag is transmitted over the channel. After the flag has been transmitted, the HDLCU starts to transmit the message. In the

shared flag mode the HDLCU starts transmitting the message in the frame adjacent to the reception of the Start transmission command.

Note: Messages with zero byte data content are not supported.

4.6.2.3 Ending a Transmission

When placing the last octet of the message into the Transmit Input Buffer, the DSP should place an End transmission command in place of the Start transmission command without changing the CRC bit.

If CRC encoding is required, the CRC vector will be transmitted bit by bit after the octet of the message, and then a flag will be transmitted. If CRC encoding is not required, a flag will be transmitted directly after the last octet of the message. Note that in unshared flag mode, if no adjacent frame exists, 'ones' will be transmitted after the flag.

4.6.2.4 Aborting a Transmission

In order to abort transmission of a message over a dedicated channel, the DSP places an abort command in the appropriate address in the command RAM. The message being transmitted over the channel is aborted and 'ones' are transmitted over the channel instead (even in the shared flag mode).

4.6.2.5 DSP Access to the HDLCU Buffers

Reading a channel from the Receive Output Buffer and writing to a channel in the Transmit Input Buffer is done according to the channel status vector and according to the Empty and Full procedures as shown below:

Empty procedure

- If the **EMPTY** flag of a channel is set by the HDLCU to '1', then move a new time slot to be transmitted from the pipe to the Transmit Input Buffer.
- If the pipe is empty change the pipe page and ask for the next 16 bytes of data from the external controller by means of DMA or interrupt.

Note: The B-channel buffer may be emptied within a single frame, while it takes at least 4 frames to empty a D-channel buffer.

Full procedure

- If the **FULL** flag of a channel is set by the HDLCU to '1' then the DSP moves the time slot from the Receive Output Buffer into the double buffer.
- If the pipe is full change the pipe page and transfer the next 16 bytes of data to the External Controller by means of DMA or interrupt.

Note: The B-channel buffer may be filled within a single frame, while a D-channel buffer will take at least 4 frames to fill.

Reading Data from the Receive Output Buffers

When the DSP reads a time slot from an even address in the Receive Output Buffer, the HDLCU will place it on the LSB byte of the data bus and ‘0’ on the MSB byte. When the DSP reads a time slot from an odd address, the HDLCU will place it on the MSB byte of the data bus and ‘0’ on the LSB byte.

Writing Data to the Transmit Input Buffers

When the DSP writes to an even address in the Transmit Input Buffer, the HDLCU will write the LSB of the data bus. When the DSP writes to an odd address, the HDLCU will write the MSB byte of the data bus.

4.7 GHDLC Unit

4.7.1 GHDLC Overview

The GHDLC (General HDLC) controls the dedicated serial communication interface of the DELIC. The purpose of the GHDLC is to decode incoming HDLC messages and to encode outgoing messages according to the HDLC protocol. The GHDLC transceives HDLC data streams with up to 16.384 Mbit/s. A received message is collected bit by bit from the line and stored as octets in the Receive buffer and read by the DSP. A transmitted message which is placed by the DSP as octets in the Transmit buffer, is transmitted bit by bit over the line.

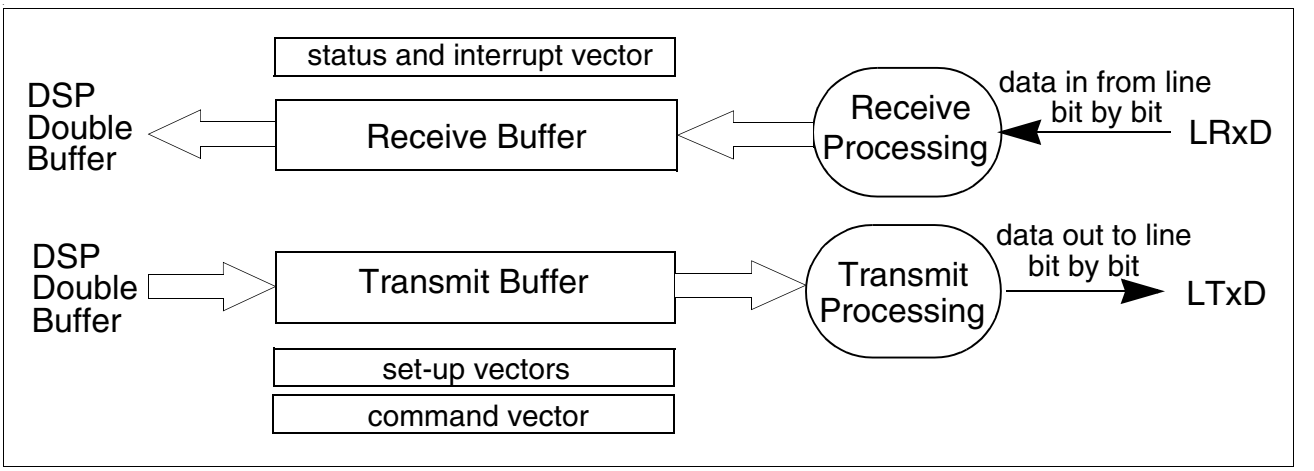


Figure 4-12 Data Processing in the GHDLC

4.7.2 GHDLC Channel External Configurations

The GHDLC line interface may be connected to other ICs in three different ways:

- Point-to-point
- Point-to-multi-point
- Multi-slave

4.7.3 GHDLC General Modes

The GHDLC provides three main modes of operation:

- **HDLC Mode:** In this mode flag recognition/insertion, zero deletion/insertion and CRC decoding/encoding are performed.
- **Asynchronous Mode:** This mode is used with request-to-send / clear-to-send handshaking. In this mode data is transmitted at a very slow rate of up to 300 baud and controlled directly by the DSP.

4.7.4 GHDLC Protocol Features

The following GHDLC features related to the HDLC protocol may be selected in HDLC mode:

- **Collision Detection:** May be active or inactive (relates only to the transmit direction)
- **Flags / Ones Interframe:** Flags or Ones are transmitted between each frame (relates to both the transmit and receive direction)
  Note that transmitted messages always use unshared flags.
- **Shared / Unshared Flag:** In shared flag mode only one flag separates adjacent messages (relates only to the receive direction)
- **CRC Mode:** Three possible settings: 16-bit CRC / 32-bit CRC / No CRC (relates to both the transmit and receive directions, and only when operating in the HDLC mode).
- **Push-Pull / Open drain:** In push pull mode a pin may be driven to ‘1’ or ‘0’. When in open drain mode a pin may be driven to ‘0’ or high z.

4.7.5 External Configuration and Handshaking in Bus Mode

The GHDLC is connected to the following DELIC interface lines:

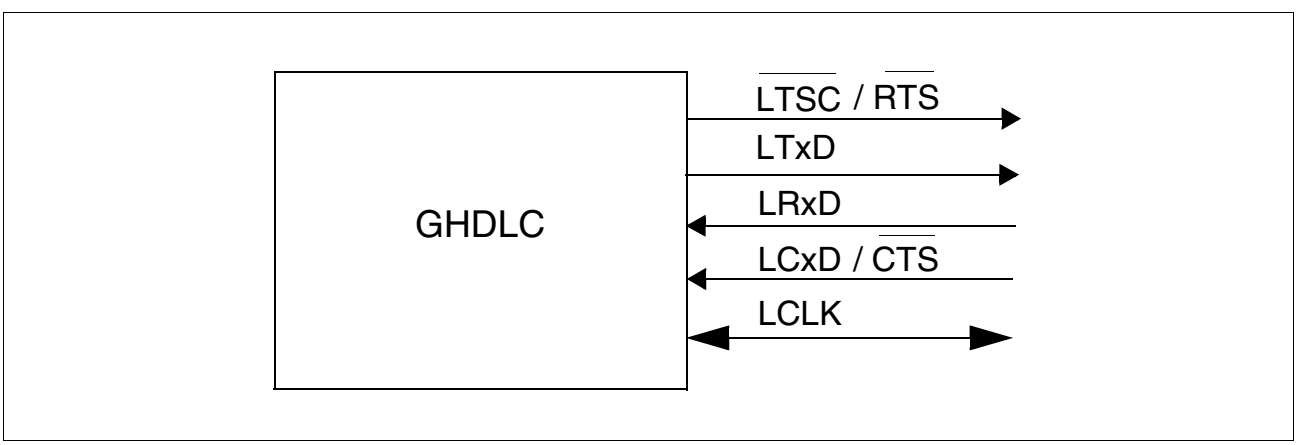


Figure 4-13 GHDLC Interface Lines

Serial data is transceived over the LRxD/LTxD lines. The line clock can be driven by an external GHDLC device or can be generated internally by the PCM clocking path. The selected internal clock is also driven outward via LCLK.

4.7.5.1 External Tri-State in Point-to-Multi-Point Mode

$\overline{\text{LTSC}}$ is the external tri-state control line. When $\overline{\text{LTSC}}$ is high LTxD is disabled and in high impedance state. When $\overline{\text{LTSC}}$ is low, LTxD may take on values 0 or 1 when in push pull mode, 0 or high impedance when in open drain mode.

4.7.5.2 Arbitration of GHDLCs on a Collision Bus

Several GHDLC channels (in a point to multi-point configuration) may be connected to an external signaling backplane. Arbitration between them may be done in two ways: Polling or Collision Detection.

In **Polling** mode the GHDLC master (in a point to multi-point configuration) is responsible to prevent collisions on the line.

In this case a DELIC-slave has to be polled by the GHDLC-master with a special requesting frame. The DELIC GHDLC-unit simply receives this frame and passes it to the µP (like any other frame).

Now it's the task of the µP to handle the message and provide a corresponding answer message.

When using **Collision Detection** many GHDLCs may start transmitting at the same time. If the GHDLC detects a difference between the transmitted bit (LTxD) and the collision bit (LCxD), the transmission is aborted. The GHDLC will try to send the message again after the bus was detected idle for a specified time, according to its priority class (refer to ITU-T I.430, section 6.1.4).

4.7.6 GHDLC Memory Allocation

The memory in the GHDLC is build by a 128x8 bit RAM equally divided between the GHDLC and the DSP. The GHDLC has a receive buffer and a transmit buffer, divided into two blocks. One block is allocated to the GHDLC channel in the receive direction, the other block is read by the DSP. Similarly in the transmit buffer, one block is allocated to the GHDLC channel in the transmit direction, the other block is written to by the DSP as shown in **Figure 4-14**. Note that the GHDLC has higher priority for the buffer access, whereas the DSP is able to read and write the RAM at a much higher frequency.

In the receive direction blocks are swapped in two cases:

- The receive buffer is full. The swap is issued immediately after the buffer has become full.
- An end of a frame indication was detected at the beginning of a FSC-frame. To avoid a loss of data in case of a buffer full indication followed by an end of frame indication, this condition becomes only true if additionally there was no **FULL** interrupt during the previous frame.

In the transmit direction blocks are swapped each time a start transmission command is issued in the command register.

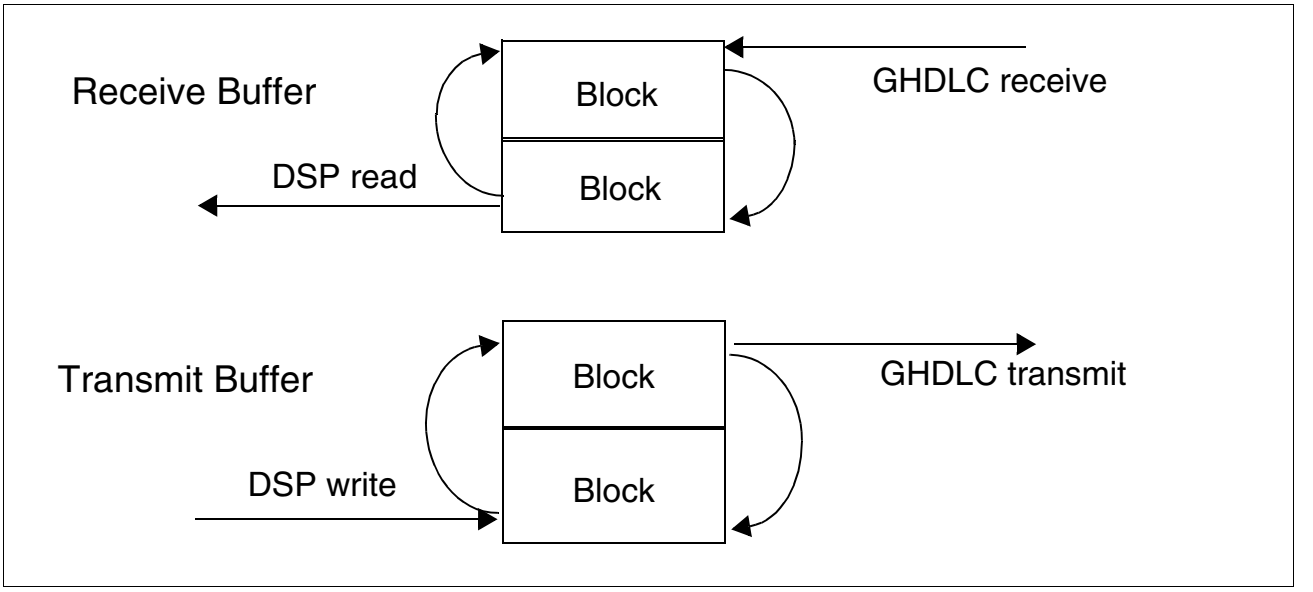


Figure 4-14 GHDLC Receive and Transmit Buffer Structure

The GHDLC unit and DSP always read and write to different areas in the RAM. Memory is equally allocated to each of the receive and transmit buffer blocks (32 bytes each).

The DSP always writes to the block addresses. The switching between blocks is done internally and does not concern the DSP.

4.7.7 GHDLC Interrupts

Full Interrupt: A full interrupt is generated if:

- The receive buffer is full. The interrupt is issued immediately after the buffer has become full.
- An end of a frame indication was detected at the beginning of a FSC frame. To avoid a loss of data in case of a buffer full indication followed by an end of frame indication, this condition becomes only true if additionally there was no **FULL** interrupt during the previous frame.

Empty Interrupt: An empty interrupt is generated every time a transmit buffer was emptied by the GHDLC.

Note: Messages with zero byte data content are not supported.

4.8 DSP Control Unit

4.8.1 General

The DCU controls the DSP access to DELIC's blocks. It performs the following tasks:

- DSP program and data address decoding
- Interrupt handling
- Data Bus and Program Bus arbitration
- DSP run time statistics
- Boot support
- Emulation support

4.8.2 DSP Address Decoding

The DCU decodes the DSP data address bus (DXAP) and the DSP program address bus (PPAP) for performing the following tasks:

- Generating the DSP memory mapped register controls, based on decoding of the 8 MSB lines of the data address bus
- Generating the GHDLC, TRANSIU, HDLCU, IOMU and PCMU RAM controls
- Generating program and data RAM controls upon detection of their address
- Generating the read signal for the program ROM

4.8.3 Interrupt Handling

The following events are reported by the various telecom peripheral blocks to the DSP:

- GHDLC
- DMA mailbox
- µP mailbox
- IOM interface Frame synchronization (FSC) interrupt
- PCM interface Frame synchronization (PFS) interrupt

The GHDLC, DMA Mailbox and Microprocessor Mailbox interrupt sources are assigned to the DSP interrupts (INT0, INT1 and INT2) as shown in **Table 4-14**. The FSC and PFS are reported as status bits (require DSP polling) in the Status Event Register (STEVE).

Table 4-14 Interrupt Map

Interrupt	Source
INT0	µP DMA Mailbox
INT1	µP General Mailbox
INT2	FSC & PFS
NMI	GHDLC

Note: The NMI interrupt maybe enabled/disabled in the INTMASK register.

4.8.4 DSP Run Time Statistics

The DSP run time statistics is used for the DSP work load estimation. By using this HW, the maximum time spent by the DSP from the FSC until the tasks ends may be found.

The DSP statistics include an eight bit counter STATC which is counting up every 1µs.

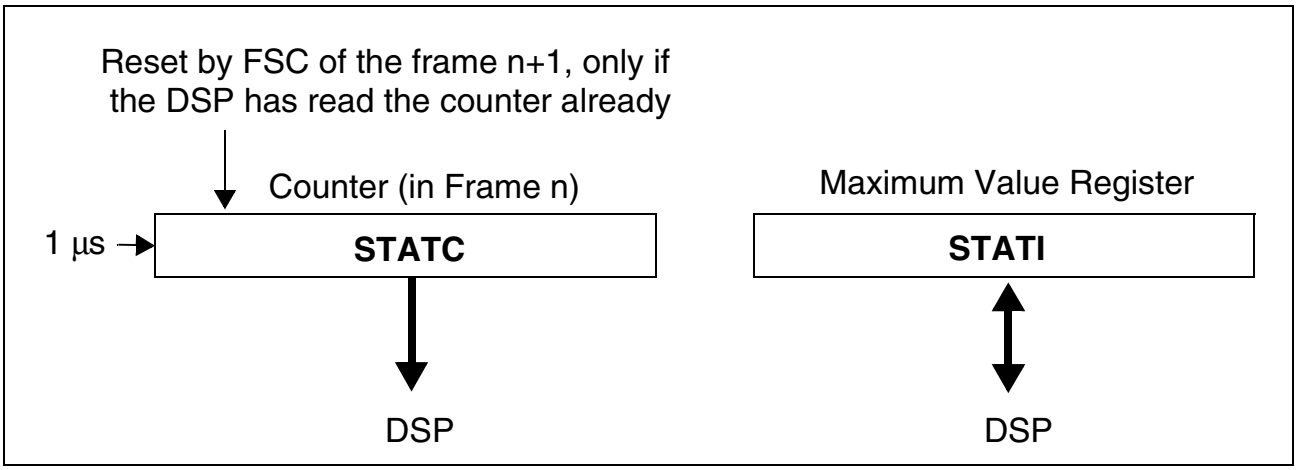


Figure 4-15 Statistics Registers

STATC is reset upon FSC rising edge. When the DSP finishes a task, it reads STATC.

The time between two consecutive FSC is always 125 µs, therefore, if the DSP is working properly, the counter value should always be less then 125 µs.

If the DSP failed to read the counter value and a new FSC rising edge has arrived, the counter is not reset. Therefore, the DSP reads a value greater then 125. It means that the DSP failed to finish it's tasks within the time frame of 125 µs.

The STATI register is added for helping the user to perform the statistics. STATI is a general purpose 8-bit read/write register.

The user program should perform statistics in the following way:

– The STATC is reset upon detection of FSC rising edge.
– The DSP finishes its activities and reads the value of STATC and STATI. The DSP compares STATC to the previous maximum value saved in STATI.
– If the new value is larger, it is written to STATI.

The system programmer can get the counter value via µP Mailbox and thus can change the DSP program.

4.8.5 Data Bus and Program Bus Arbitration

The internal data bus (GEXDBP) and program data bus (GIP) are tristate buses. Since these buses must never float, the DCU keeps track of the bus activities. If during a dedicated cycle no driver is on the bus, the DCU puts a default value on the bus.

4.8.6 Boot Support

The µP boot is the process which loads the external µP program RAM via the µP Mailbox into the on-chip DSP program RAM. The boot is controlled by a boot routine residing in the internal DSP program ROM. This routine is started upon DELIC reset according to the $\overline{\text{BOOT}}$ strap pin status.

The second boot option is the emulation boot, which loads the monitor (BI routine) to the program RAM. This routine enables the PC emulator to control the DSP.

At system start-up the program code for the DSP is transferred into the internal RAM from the external uP. The contents for the program and data boot is delivered in a so called HEX file.

The code format of the HEX file is the following:

```
Code,:,16 bit address, 16 bit opcode
C:0000 4180
C:0001 0018
C:0004 4180
C:0005 00BA
C:0006 4180
C:0007 00BD
C:000E 4180
C:000F 00BE ...
```

The program boot starts with the "Start Loading Program RAM" command which is coming from the DELIC boot routine.

```
OCMD = 0x1F
```

This command must be polled from the uP because the interrupt is still not activated.

The uP confirms this with the "Start Boot" command.

```
MCMD = 0x55
```

The program code is now transferred in pieces of maximum 15 words by use of the "Write Program Memory Command".

```
MDT0 = 0xDESTINATION_ADDRESS
MDTn = 0xOPCODE_WORDn
MCMD = 0xAn   [n=1..15 number of code words to write to address++]
```

Before writing this command, the uP must check that the mailbox is free. This is done by reading the MBUSY bit (bit 7 of address 0x41). The uP must wait until this bit is reset before sending the next command.

Missing addresses in the HEX file must not be loaded. The "Write Program Memory Command" must be repeated until the program code is fully loaded. The end of the code segment inside the HEX file is the change from C: (code) to D: (data). This is the start of the data segment, which is needed for the Data Boot, described in the next step.

After all the code has been loaded, the "Finish Boot" command must be sent:

MCMD = 0x1F

4.8.7 Reset Execution and Boot Strap Pin Setting

The reset is executed via low signals on the DELIC RESET pin (29) and the VIP RESET pin (44). It is recommended to connect the VIP RESET inputs to the DELIC RESIND output pin (89). The RESIND signal is a delayed reset signal and stays at least 500 us after termination of the DELIC RESET input. This mechanism ensures that all output clocks of the DELIC have become stable even after a short reset was applied. Connecting the VIP reset to this RESIND signal ensures stable VIP clocking after reset (Layer1 clock, DCL2000, FSC).

Together with applying the reset signal to the DELIC, the strap pin signals must be defined. There are 9 pins at the DELIC device which have a special functionality. These so called strap pins are used as inputs while reset is active and determine different modes like master/ slave mode of the PCM interface, test modes, boot mode,... Please refer to **page 2-28** for detailed information about the strap pin options.

The settings of the strap signals are sampled with the rising edge of the DELIC RESET input signal. For a uP- boot, the default settings of strap 4 (emulation boot) and strap 6 (boot strap) are needed.

After a correct reset execution and strap pin setting, the DELIC sends the command "Start Loading Program RAM" to the uP: OCMD = 0x1F

4.9 General Mailbox

4.9.1 Overview

The µP and the DSP communicate via a bidirectional Mailbox according to the mailbox protocol described in **Chapter 11**. The DELIC provides two dedicated Mailboxes that may be used in two operational modes:

- **DMA mode** in which the two Mailboxes operate independently, one serves as a general purpose Mailbox and the other serves as a DMA Mailbox.
- **Expanded Mailbox mode** in which the two Mailboxes are regarded as a enlarged general purpose Mailbox, providing a double number of registers.

The general purpose Mailbox includes two separate parts:

- **µP Mailbox** - enables transfers from the µP to the OAK.
- **OAK DSP Mailbox** - enables transfers from the OAK to the µP.

Both parts include a command register, 9 x (16-bit) registers (17 registers in expanded mode) and a busy bit. One of the data registers in every part has a special addressing mode, i.e. the OAK may access either a certain byte of a word or the whole word which is temporarily stored in the Mailbox. This requires to use 3 different addresses in OAK's direction.

Note: The Mailbox protocol commands structure is described in **Chapter 11***.*

4.9.2 µP Mailbox

The µP Mailbox includes:

- Eight 16-bit data registers (MDTn)
- A16-bit general register (MGEN)
- An 8-bit command register (MCMD)
- A 1-bit busy register (MBUSY)

Registers MDTn, MGEN and MCMD may be written by the µP and read by the OAK. The MBUSY register may be written by the DSP and read by the µP.

A write of the µP to the MCMD-register of the µP-mailbox generates an interrupt to the OAK. Thus, the user has to provide all mailbox data prior to writing to register MCMD.

The MBUSY **bit** which may be read by the µP (register MBUSY) is set automatically after a write to the µP command register (MCMD) and reset automatically by a direct OAK write operation to it.

Note: The command Opcodes are defined in **Chapter 11***.*

Data Transfer from the µP to the OAK

- The µP reads the busy bit and checks whether the Mailbox is available (MBUSY='0')

- The µP writes to the Data registers MDTn(optional)
- The µP writes to the µP Command register (MCMD), this write must be performed and sets automatically the µP Mailbox busy bit (MBUSY).
- An OAK interrupt (INT2) is activated due to the write to the Command register (MCMD).
- The OAK INT2 routine reads MCMD and performs the command (the read of the command register resets the INT2 activation signal).
- When finished, the INT2 routine resets MBUSY for enabling the µP to send the next command.

Note: The µP may perform consecutive writes to the µP Mailbox, and the user must guarantee that the data has been transferred to the OAK correctly (the busy bit has been reset) before writing new data to the µP Mailbox.

4.9.3 OAK Mailbox

The OAK Mailbox includes:

- Eight 16-bit data registers (ODTx)
- A 16-bit general register (OGEN)
- An 8-bit command register (OCMD)
- A 1-bit busy register (OBUSY)

Registers ODTx, OGEN and OCMD may be written by the OAK and read by the µP. The OBUSY bit may be written by the µP and read by the OAK. In addition, the µP can read this bit (because the µP could poll this bit).

A write of the OAK to register OCMD of the OAK mailbox generates an interrupt to the µP. Thus the OAK firmware provides all mailbox data prior to writing to register OCMD.

The OBUSY- bit which can be read by the OAK, is set automatically after a write of the OAK to register OCMD and is reset by a direct µP write to it (when the µP has finished reading the OAK Mailbox contents).

Note: The Opcodes indications are defined in **Chapter 11***.*

Data Transfer from the OAK to the µP

- The OAK reads the busy bit and checks whether the MB is available (OBUSY=’0’)
- The OAK writes to the data registers ODTn (optional)
- The OAK writes to the command register (OCMD). This write must be performed and automatically sets the OAK Mailbox busy bit (OBUSY)
- A µP interrupt is activated due to the write operation to the register OCMD.
- The µP reads the command register and performs the command.
- When finished, the µP resets OBUSY for enabling the OAK to send the next command.

Note: The OAK may perform consecutive writes to the OAK Mailbox and the OAK firmware guarantees that the data has been transferred to the µP correctly (OBUSY has been reset) before writing new data to the OAK Mailbox.

4.10 DMA Mailbox

4.10.1 Overview

This Mailbox is used for DMA transfers of data in “memory-to-memory” or “flyby” modes. In a special mode, it may be used as an extension to the General Purpose Mailbox.

The transfer is done similarly to the general Mailbox, with some differences:

1. There are 2 configurations: DMA, and secondary Mailbox.
2. The master of the transfer in DMA mode is always the OAK.

The DMA Mailbox includes two separate parts:

- **Transmit (µP) Mailbox** for fast transfers from the DMA (µP) to the GHDLC (OAK).
- **Receive (OAK) Mailbox** for fast transfers from the GHDLC (OAK) to the DMA (µP).

In transactions between µP and OAK the later indicates when it is ready for transmit / receive operation by driving DREQT/DREQR high, and µP replies by driving $\overline{\text{DACK}}$ low. $\overline{\text{DACK}}$ acts like a Chip Select signal and remains low during the whole transaction. By driving $\overline{\text{DACK}}$ high the DMA may stop the transaction on any stage, even if the data transfer has not finished yet.

There are two possible modes in DMA transfers: Memory-to-memory and Flyby. Selecting these modes is done by writing “1” or “0” to the Configuration Register.

The mode of DMA’s operation depends on the µP that initiates a DMA transfer (Intel/ Siemens or Motorola). This mode information is provided via the MODE input pin of the DELIC.

The number of bytes (words) to be transferred is written to TX_CREG and copied to TX_COUNT.

After finishing a transaction, INT1 is issued to the DSP in order to indicate that the Mailbox is empty and available for the next operation.

4.10.2 Intel/Siemens Mode and Motorola Mode (Memory-to-Memory)

In Intel/Siemens mode the control lines are $\overline{\text{DACK}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$. Driving $\overline{\text{RD}}$ low when $\overline{\text{DACK}}$ is low causes a ‘Read’ from the Mailbox. Driving $\overline{\text{WR}}$ low when $\overline{\text{DACK}}$ is low causes a ‘Write’ to the Mailbox.

In Motorola mode the control lines are $\overline{\text{DACK}}$, R/$\overline{\text{W}}$, $\overline{\text{DS}}$. Driving R/$\overline{\text{W}}$ high when $\overline{\text{DACK}}$ and $\overline{\text{DS}}$ are low causes a ‘Read’ from the Mailbox. Driving R/$\overline{\text{W}}$ low when $\overline{\text{DACK}}$ and $\overline{\text{DS}}$ are low causes a ‘Write’ to the Mailbox.

4.10.3 Fly-By Mode

In Fly-By mode DMA transfer is done in one bus transaction. The DMA should provide a ‘Read’ command to the Mailbox and, at the same time, a ‘Write’ command to the system memory (or a ‘Write’ to the Mailbox and a ‘Read’ to the memory). The system memory

must always get a ‘Write’ command for a write operation or a ‘Read’ for a read operation. The Mailbox, however, reacts in the opposite way: it writes (puts data into a register) upon receiving a ‘Read’ command and reads (drives data on the bus) upon receiving a ‘Write’ command.

4.10.4 PEC Mode

The additional mode which is possible in work with some Siemens µPs is PEC mode. In this case DMA controller is edge sensitive, so edges are provided on DREQ lines in order to initiate every DMA transfer.

4.10.5 Transmit Mailbox

The Transmit Mailbox includes:

- 18-byte FIFO which is accessed by the OAK (for Read) as 9 “regular” addressed 16-bit-wide registers and by the DMA (for Write) like a FIFO. One of the nine registers is a “special” register like in the General Mailbox and has 3 addresses associated with it.
- 5-bit counter for the general number of transactions in current transfer (TX_CREG)
- 5-bit counter for the number of transactions that remains in the transfer (TX_CNT).
- 1-bit status register (TX_STAT).

The OAK is always the master of this transfer, i.e. the transfer is initiated b the OAK, but the functions of control and arbitration during the transfer are done by the DMA.

For **DMA request**, the OAK requests transfer of data to the high-speed GHDLC channel. It writes the number of bytes needed to the TX_CREG register which sets TX_BSY bit, and causes the assertion of DREQT (“DMA Request Transmit”) pin.

For **DMA acknowledge**, the DMA grants the bus to OAK by driving $\overline{\text{DACK}}$ low, and begins toggling the control lines. In Intel/Siemens (Mem-to-Mem) mode it drives the $\overline{\text{WR}}$ line low when it writes to the Mailbox, and high when it reads from the memory on the second side. $\overline{\text{RD}}$ line stays high during the complete transfer, because there are no ‘Read’ operations from here. $\overline{\text{DACK}}$ is low all the time. In Motorola (Mem-to-Mem) mode it drives R/$\overline{\text{W}}$ line low for ‘Write’ operations when $\overline{\text{DACK}}$ and $\overline{\text{DS}}$ are low; when DMA refers to the external memory, it drives $\overline{\text{DS}}$ high.

Note that in Fly-by mode the meaning of ‘Read’ and ‘Write’ commands is opposite for the Mailbox. After every ‘Write’ operation the counter (TX_CNT) is decremented by one. If the DMA stops the transaction before finishing, it has to drive $\overline{\text{DACK}}$ high. The OAK continues driving DREQT high, stops decrementing TX_CNT and waits until $\overline{\text{DACK}}$ becomes low.

After a write of TX_CREG bytes by the DMA to the Transmit Mailbox, the TX_CNT becomes ‘0’. Then TX_BSY bit is reset to ’0’, and DREQT is deasserted. A reset of TX_BSY bit may be programmed to generate an interrupt (INT1) to the OAK.

The OAK will then read TX_CREG bytes from the Mailbox to the GHDLC, the first byte being the LSB of the least significant word of the FIFO. Note that in case of an odd

number of bytes to be transferred the last byte is available on the least significant byte of the last word in FIFO.

Note: TX_BSY is not an indication for the transaction partners. It may be used for internal software needs of the OAK.

Data Transfer via the Transmit Mailbox

- The OAK writes to TX_CREG.
- DREQT is asserted ('high'), and TX_BSY bit is set ('1').
- The DMA asserts $\overline{\text{DACK}}$ = 0 and issues TX_CREG write transactions to the Mailbox.
- DREQT is deasserted ('low'), and TX_BSY bit is reset ('0').
- If TX_MASK bit is reset ('0'): an OAK interrupt (INT1) is activated.
- The OAK reads the TX_REG bytes in the Mailbox and transfers them to the GHDLC.

*Note: 1. The OAK must not write to the TX_CREG reg **before** TX_BSY is reset.*
2. Writing'0' to TX_CREG is not allowed.

4.10.6 Receive Mailbox

The Receive Mailbox includes:

- 18-byte FIFO which is accessed by the OAK (for write) as 9 "regular" addressed 16-bit wide registers, and by the DMA (for read) like a FIFO. One of the nine registers is a "special" register like in the General Mailbox and has 3 addresses associated with it.
- 5-bit counter for the general number of transactions in current transfer (RX_CREG).
- 5-bit counter for number of transactions that remains in the transfer (RX_CNT).
- 1-bit status register (RX_STAT).

Like in the Transmit Mailbox, the OAK is always the master of this transfer, i.e. the transfer is initiated by the OAK, but controlled by DMA.

When the OAK requests a transfer of data from the high-speed GHDLC channel, it writes this data to the Receive Mailbox, the first byte to the least significant byte of the least significant word. Note that in case of odd number of bytes, the most significant byte of the last word is don't care.

Then, the OAK writes the number of bytes needed to the RX_CREG register which sets RX_BSY bit, and causes the assertion of DREQR ("DMA Request Receive") pin.

If DMA grants the bus to OAK, it drives $\overline{\text{DACK}}$ low and begins toggling the control lines. In Intel/Siemens (Mem-to-Mem) mode it drives $\overline{\text{RD}}$ line low when it reads from the Mailbox and high when it writes to the memory. $\overline{\text{WR}}$ line stays high during the complete transfer, because there are no 'Write' operations from here. $\overline{\text{DACK}}$ is low all the time. In Motorola (Mem-to-Mem) mode it drives R/$\overline{\text{W}}$ line high for 'Read' operations when $\overline{\text{DACK}}$ and $\overline{\text{DS}}$ are low; when DMA refers to the external memory, it drives $\overline{\text{DS}}$ high.

Note that in Fly-by mode the meaning of 'Read' and 'Write' commands is opposite for the Mailbox. After each 'Read' operation the counter (RX_CNT) is decremented by one. If

the DMA stops the transaction before finishing, it has to drive $\overline{\text{DACK}}$ high. The OAK continues driving DREQR high, stops decrementing RX_CNT and waits until $\overline{\text{DACK}}$ becomes low.
After a read of RX_CREG bytes by the DMA from the Receive Mailbox, the RX_CNT becomes ‘0’. Then RX_BSY bit is reset to ’0’, and DREQR is deasserted . Reset of RX_BSY bit may be programmed to cause an interrupt (INT1) to the OAK.

Note: RX_BSY is not an indication for the transaction partners. It may be used for internal software needs of the OAK .

Data Transfer via the Receive Mailbox

- The OAK writes RX_CREG bytes to Receive Mailbox.
- The OAK writes to RX_CREG.
- DREQR is asserted (’high’), and RX_BSY bit is set (’1’).
- The DMA asserts $\overline{\text{DACK}}$ and issues RX_CREG read transactions to the Mailbox.
- DREQR is deasserted (’low’), and RX_BSY bit is reset (’0’).
- If RX_MASK bit is reset (’0’): an OAK interrupt (INT2) is activated.

*Note: 1. The OAK must not write to the RX_CREG reg **before** RX_BSY is reset.*
2. Writing ’0’ to RX_CREG is not allowed.

4.10.7 Access to the DMA FIFOs

The size of the FIFOs is 18 bytes (9 words) for each Tx and Rx. On the OAK side, each FIFO contains 9 registers (TDT0-8 and RDT0-8) which may be accessed separately. On the DMA side, only the current top of the FIFO is available.
The transfer is divided to bulks, the size of the current bulk is determined in the RX_CREG/TX_CREG.

Transmit FIFO

This FIFO is written by the DMA. The first write in a bulk will be to TDT0 least significant byte, the second to TDT0 most significant byte, etc., until the size of the current bulk was reached. Then the OAK will read the data from the relevant TDTn registers.

Receive FIFO

This FIFO is written by the OAK. The OAK fills RDT0 to RDTn. The DMA will then read consecutive bytes from the FIFO, where the first byte will be RDT0 least significant byte, the 2nd RDT0 most significant byte, etc. until the size of the current bulk was reached.

*Note: This Rx FIFO and Tx FIFO functionality is only provided when the Mailbox is in DMA mode (CFG:DMA = ‘1’). In case of non DMA mode (CFG:DMA = ‘0’), the FIFOs are used as secondary (extension) to the General Purpose Mailbox, which means that the General Purpose Mailbox will have 18 words for **each** direction (OAK and µP), instead of 9.*

4.11 DSP Core OAK+

The DELIC integrates an OAK+ DSP core, an enhanced version of the OAK. It is clocked using an on-chip PLL at a frequency of 61.44 MHz. It may also be driven by lower clock rates provided by an external oscillator.

The OAK+ is a high performance fixed-point DSP with a 16-bit data and program bus. Due to an optimized cost-performance rate, it is widely used not only in Line Cards and PBX applications, but also in cellular phones, fast modems, advanced fax machines, and answering machines.

The core's main block is a high performance central processing unit, including a full-featured bit manipulation unit, RAM and ROM addressing units, and Program control logic. All other application specific peripheral blocks, are defined as part of the user on-chip logic.

The OAK+ provides an advanced set of DSP and generic microprocessor functions for straightforward generation of efficient and compact code.

For more details on OAK architecture please refer to "DOC DSP Programmer's Reference Manual, 11.97".

4.12 Clock Generator

4.12.1 Overview

The DELIC clock generator provides all necessary clock signals for the DELIC and connected clock slave devices. The internal clocks are generated by two on-chip PLLs:

1. A digital controlled oscillator (DCXO) generates a 16.384 MHz clock from an external crystal.
2. A PLL multiplies the 16.384 MHz clock to a 61.44 MHz clock.

An overview of the clock signals and a block diagram is shown below.

Table 4-15 Overview of Clock Signals

Pin	Function	I/O	During Reset
CLK16-XI	16.384 MHz External Crystal Input	I	I
CLK16-XO	16.384 MHz External Crystal Output	O	O
XCLK	External Reference Clock from layer-1 IC (2.048 MHz, 1.536 MHz or 8 kHz)	I	I (1.536 MHz)
REFCLK	PCM Reference Clock (8 kHz or 512 kHz)	I/O	tristate
PFS	PCM Frame Synchronization 8 kHz (I/O) or 4 kHz (I)	I/O	I (Slave) O (Master)
PDC	PCM Data Clock (2.048, 4.096, 8.192 or 16.384 MHz)	I/O	I (Slave) O (Master) (2.048 MHz)
CLKOUT	Auxiliary Clock (2.048, 4.096, 8.192, 16.384, or 15.36 MHz)	O	O (2.048 MHz)
DCL_2000	IOM-2000 Data Clock (3.072, 6.144 or 12.288 MHz)	O	O (3.072 MHz)
DCL	IOM-2 Data Clock (384 kHz, 768 kHz, 2.048 MHz or 4.096 MHz)	O	O (384 kHz)
FSC	IOM-2 and IOM-2000 Frame Synchronization 8 kHz.	O	O
L1_CLK	Layer-1 Clock 15.36 or 7.68 MHz (e.g. OCTAT-P / QUAT-S)	O	O (7.68 MHz)
DSP_CLK	DSP Test Clock. (to run the DSP at clock rates other than 61.44 MHz)	I	I

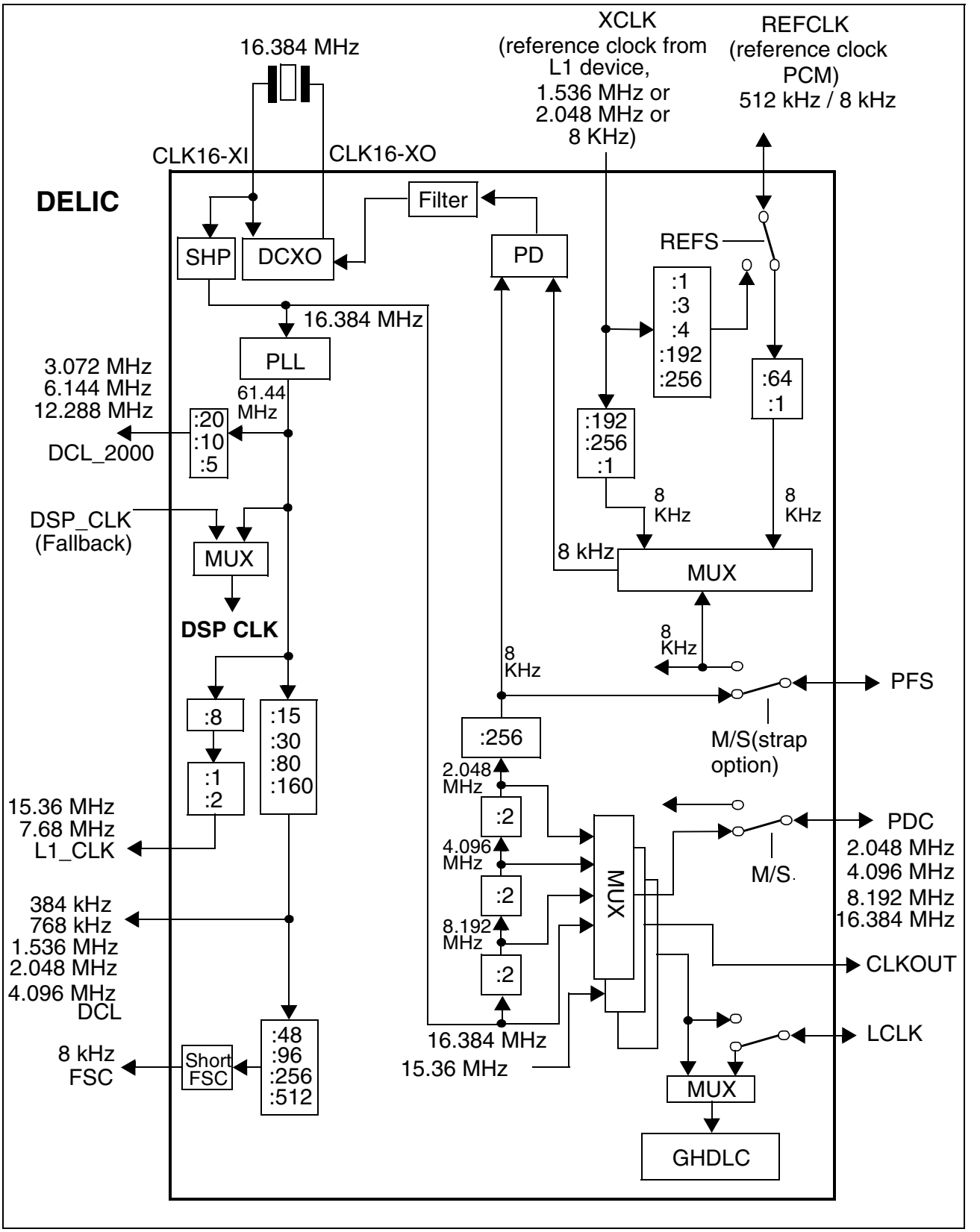


Figure 4-16 DELIC Clock Generator

4.12.2 DSP Clock Selection

The default DSP clock is the internal 61.44 MHz generated by the PLL. For test purpose, a different frequency may be provided via DSP_CLK input pin. The selection between the internal 61.44 MHz or external clock source is done by the DSP_FRQ input pin.

4.12.3 PCM Master/Slave Mode Clocks Selection

In PCM Master mode, the PFS and PDC are derived from the internal 16.384 MHz signal, and driven to the PCM interface via the PFS pin (output) and PDC pin (output). In PCM Slave mode, the PFS and PDC are generated from an external signal, and input to the DELIC via the PFS pin and the PDC pin.

Note: During reset, a strap pin determines whether the DELIC operates in clock Master or Slave mode.

4.12.4 DELIC Clock System Synchronization

The PCM clock division chain is synchronized to an external reference clock, used as one of the inputs to a phase comparator, after being divided into 8 KHz. The other phase comparator input is the 8 KHz clock, derived from the 16.384 MHz clock. The phase comparator output is used as control input of the DCXO, after being filtered by a low-pass filter. The reference clock can be driven by one of the following input pins:

- XCLK - 2.048 MHz, 1.536 MHz or 8 KHz:
  Can be driven by a layer-1 transceiver (e.g. VIP, QUAT-S) connected to the Central Office. Only a clock master DELIC can be synchronized directly according to this input. In other cases (clock slave DELIC), this input signal may be divided to 8 KHz or 512 KHz, and driven out via REFCLK, in purpose to be used for the synchronization of the clock-master DELIC.
- REFCLK - 512 KHz or 8 KHz:
  Used for synchronization of the clock master DELIC, when not synchronized by XCLK. Usually this signal is driven by a clock slave DELIC, or another PBX in the system. In a clock slave DELIC this pin is used as output.
- PFS - 8 KHz:
  Driven by the system clock master. May be used for synchronization of the clock slave DELICs. In a clock master DELIC this pin is used as output.

4.12.5 IOM-2 Clock Selection

The IOM-2 interface clocks FSC and DCL are always output.
The FSC output signal is usually generated with 50% duty cycle. A short FSC pulse is required for multiframe start indication (one DCL cycle long). One cycle after the short FSC pulse, the normal FSC is generated again with 50% duty cycle.

4.12.6 IOM-2000 Clock Selection

The IOM-2000 interface uses the same FSC like IOM-2, whereas the data clock DCL2000 is a dedicated pin (always output).

4.12.7 REFCLK Configuration

REFCLK is an I/O pin for synchronizing the PCM interface (to 8 kHz or 512 kHz).

The clock master DELIC may synchronize the internal clocks to REFCLK by selecting REFCLK as the reference clock source.

A clock slave DELIC may use REFCLK as output, when REFCLK is driven by the XCLK input pin. The slave DELIC may transfer the XCLK signal to the clock master DELIC, and enable the clock master to synchronize to a layer-1 device, which is connected to another DELIC in the system.

4.12.8 GHDLC Clock Selection

Any of the next signals may be provided to the GHDLC channel as input clock:

1. LCLK Input Pin
   This option is possible only when a LNC interface is assigned to the GHDLC unit.
2. 2.048 MHz, 4.096 MHz, or 8.192 MHz
   These clock signals are generated internally by the PCM clocking path. The selected internal clock is also driven outward via LCLK.

Note that one of these signals must be selected as the clock of the GHDLC channel when the DELIC is the clock master of this channel.

5 DELIC Memory Structure

The following tables provide the DELIC memory map for the DSP and the µP.

5.1 DSP Address Space

5.1.1 DSP Register Address Space

Table 5-1 DSP Registers Address Space

Address	Description
D000 - D01F	DCU registers
D020 - D03F	A/µ-law registers
D040 - D05F	IOMU registers
D060 - D07F	PCMU registers
D080 - D09F	Clocks registers
D0A0 - D0BF	TRANSIU registers
D0C0 - D0DF	GHDLC registers
D100 - D17F	µP Mailbox and DMA Mailbox registers
D180 - D1FF	HDLCU registers
D1A0 - DFFF	not used

5.1.2 DSP Program Address Space

Table 5-2 DSP Program address space

Address	Size	Description
0000 - 0FFF	4Kw	Program RAM
1000 - F7FF	58Kw	Not used
F800 - FFFF	2Kw	Program ROM

5.1.3 DSP Data Address Space

A1

Table 5-3 Occupied DSP Data Address space

Address	Size	Description
0000 - 03FF	1Kw	Internal XRAM
2000 - 203F	64w	GHDLC data buffer
2040 - 207F	64w	reserved for testt *(**)*
4000 - 401F	32w	HDLCU receive output buffer
4020 - 403F	32w	HDLCU transmit input buffer
4040 - 405F	32w	HDLCU command RAM
4060 - 407F	32w	HDLCU receive input buffer
4080 - 409F	32w	HDLCU transmit output buffer
40A0 - 40BF	32w	HDLCU status buffer
6000 - 605F	96w	TRANSIU receive data buffer
6080 - 60DF	96w	TRANSIU transmit data buffer
6100 - 61BF	192w	reserved for test *(**)*
6200 - 6248	72w	reserved for test *(**)*
6280 - 62C8	72w	reserved for test *(**)*
8000 - 803F	64w	IOMU receive data buffer
8040 - 807F	64w	IOMU transmit data buffer
8080 - 80FF	128w	reserved for test *(**)*
9000 - 9017	24w	HRAM for U_{PN} scrambler
9020 - 9037	24w	HRAM for U_{PN} descrambler
A000 - A07F	128w	PCMU receive data buffer
A080 - A0FF	128w	PCMU transmit data buffer
A100 - A1FF	256w	reserved for testt *(**)*
D000 - DFFF	4Kw	OAK memory mapped registers(*)
E000 - E1FF	0.5Kw	A/µ-Law ROM
F400 - F7EE	1Kw-16w	Emulation mail box (on SCDI)
F7F0 - F7FF	16w	OCEM® Registers
FC00 - FFFF	1Kw	Internal YRAM

Note: (*) The OAK memory mapped registers address space is described in the following table:
(**) Accessing these addresses may cause unpredictable results

Table 5-4 OAK memory mapped registers address space

Address	Description
D000 - D01F	DCU registers
D020 - D03F	A/m-law registers
D040 - D05F	IOMU registers
D060 - D07F	PCMU registers
D080 - D09F	Clocks registers
D0A0 - D0BF	TRANSIU registers
D0C0 - D0DF	HDLCU registers
D100 - D17F	CPU+DMA mailbox registers
D180 - D1FF	GHDLC registers
D1A0 - DFFF	not used

5.2 µP Address Space

The µP address space consists of the general mail-box registers, the DMA mail-box registers (only in non-DMA mode), the µP-interface control register, and the µP-interface status register (MISR)

.

Table 5-5 µP Address Space Table

Address	Description
00_H - 43_H 60_H - 62_H	µP- mail box registers
48_H, 68_H, $6A_H$	µP-configuration registers
$6B_H$ - $7F_H$	Reserved. Accessing these addresses may cause unpredictable results

6 Register Description

6.1 Register Map

Table 6-1 TRANSIU Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
TICR	RD/WR	$D0A0_H$	0000_H	IOM-2000 global configuration	6-10
TCCR0	RD/WR	$D0A1_H$	$FFFF_H$	Channel 7..0 configuration	6-11
TCCR1	RD/WR	$D0A2_H$	$FFFF_H$	Channel 15..8 configuration	6-11
TCCR2	RD/WR	$D0A3_H$	$FFFF_H$	Channel 23..16 configuration	6-11
VIPCMR0	WR	$D0A8_H$	0000_H	VIP_0 command registers	6-12
VIPCMR1	WR	$D0A9_H$	0000_H	VIP_1 command registers	6-12
VIPCMR2	WR	$D0AA_H$	0000_H	VIP_2 command registers	6-12
VIPSTR0	RD	D0AC	0000_H	VIP_0 status register	6-14
VIPSTR1	RD	$D0AD_H$	0000_H	VIP_1 status register	6-14
VIPSTR2	RD	$D0AE_H$	0000_H	VIP_2 status register	6-14
TICCMR	WR	$D0B0_H$ (LS-word) $D0B1_H$ (MS-word)	0000_H 0000_H	Channel initialization command	6-15
TICSTR	RD	$D0B2_H$ (LS-word) $D0B3_H$ (MS-word)	0000_H 0000_H	Channel initialization status	6-20

Table 6-2 Scrambler Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
SCMOD	RD/WR	$D010_H$	0003_H	Scrambler mode	6-21
SCSTA	RD/WR	$D011_H$	undef.	Scrambler status	6-21

Table 6-3 IOMU Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
ICR	R/W	$D040_H$	0002_H	IOMU Control	6-22
ISR	R	$D041_H$	undef.	IOMU Status	6-23
ITSCR	Set (W)	$D042_H$	0000_H	IOMU Tri-State Control	6-24
	Reset (W)	$D043_H$			
	R	$D044_H$			
IDRDYR	R	$D045_H$	undef.	IOMU DRDY	6-25
IDPR	R/W	$D046_H$	$00E0_H$	IOMU Data Prefix	6-26

Table 6-4 PCMU Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
PCR	RD/WR	$D060_H$	00_H	PCMU Control	6-27
PSR	RD	$D061_H$	undef.	PCMU Status	6-28
PTSC0	RD/WR	$D062_H$ (read/set) $D063_H$ (read/reset)	00_H	PCMU Tristate control 0	6-29
PTSC1	RD/WR	$D064_H$ (read/set) $D065_H$ (read/reset)	00_H	PCMU Tristate control 1	6-29
PTSC2	RD/WR	$D066_H$ (read/set) $D067_H$ (read/reset)	00_H	PCMU Tristate control 2	6-29
PTSC3	RD/WR	$D068_H$ (read/set) $D069_H$ (read/reset)	00_H	PCMU Tristate control 3	6-29

Table 6-4 PCMU Register Map (Continued)

Reg Name	Access	Address	Reset Value	Comment	Page No.
PTSC4	RD/WR	$D06A_H$ (read/set) $D06B_H$ (read/reset)	00_H	PCMU Tristate control 4	6-29
PTSC5	RD/WR	$D06C_H$ (read/set) $D06D_H$ (read/reset)	00_H	PCMU Tristate control 5	6-29
PTSC6	RD/WR	$D06E_H$ (read/set) $D06F_H$ (read/reset)	00_H	PCMU Tristate control 6	6-29
PTSC7	RD/WR	$D070_H$ (read/set) $D071_H$ (read/reset)	00_H	PCMU Tristate control 7	6-29
PDPR	RD/WR	$D072_H$	$E0_H$	PCMU Data Prefix	6-30

Table 6-5 A-/µ-law Unit Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
AMCR	R/W	$D020_H$	00_H	A/µ-law Unit Control	6-31
AMIR	W	$D021_H$	undefined	A/µ-law Unit Input	6-31
AMOR	R	$D022_H$	undefined	A/µ-law Output	6-32

Table 6-6 HDLCU Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
HCR	W	$D180_H$	0001_H	HDLC Control	6-33
HSTA	R	$D180_H$	0001_H	HDLC Status	6-34

Table 6-6 HDLCU Register Map (Continued)

Reg Name	Access	Address	Reset Value	Comment	Page No.
HCCV	R/W	4040_H-$405F_H$	undefined	Channel Command Vector	6-35
HCSV	R	$40A0_H$-$40BF_H$	undefined	Channel Status Vector	6-36

Table 6-7 GHDLC Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
GTEST	W	$D0C0_H$	0001_H	GHDLC Test/ Normal Mode	6-38
GCHM	W	$D0C1_H$	0000_H	GHDLC Channel Mode	6-38
GINT	R	$D0D4_H$	0000_H	GHDLC Interrupt	6-39
GFINT	R/W	$D0D3_H$	0000_H	GHDLC Frame Interrupt	6-39
GRSTA0	R	$D0C2_H$	$001F_H$	GHDLC Receive Status cha. 0	6-40
GRSTA1	R	$D0C3_H$	$001F_H$	GHDLC Receive Status cha. 1	6-40
GRSTA2	R	$D0C4_H$	$001F_H$	GHDLC Receive Status cha. 2	6-40
GRSTA3	R	$D0C5_H$	$001F_H$	GHDLC Receive Status cha. 3	6-40
RXDAT	RD	2000_H-$203F_H$	0000_H	Receive data and status	6-41
GMOD0	W	$D0C6_H$	0140_H	GHDLC Mode cha. 0	6-42
GMOD1	W	$D0C7_H$	0140_H	GHDLC Mode cha. 1	6-42
GMOD2	W	$D0C8_H$	0140_H	GHDLC Mode cha. 2	6-42
GMOD3	W	$D0C9_H$	0140_H	GHDLC Mode cha. 3	6-42
GTCMD0	W	$D0CA_H$	0000_H	GHDLC TX Command cha. 0	6-43
GTCMD1	W	$D0CC_H$	0000_H	GHDLC TX Command cha. 1	6-43
GTCMD2	W	$D0CE_H$	0000_H	GHDLC TX Command cha. 2	6-43
GTCMD3	W	$D0D0_H$	0000_H	GHDLC TX Command cha. 3	6-43
GASYNC	R/W	$D0D2_H$	0000_H	ASYNC Control/ Status	6-44
GLCLK0	R/W	$D08A_H$	0000_H	LCLK0 Control Register	6-45
GLCLK1	R/W	$D08B_H$	0000_H	LCLK1 Control Register	6-46
GLCLK2	R/W	$D08C_H$	0000_H	LCLK2 Control Register	6-47

Table 6-7 GHDLC Register Map (Continued)

Reg Name	Access	Address	Reset Value	Comment	Page No.
GLCLK3	R/W	$D08D_H$	0000_H	LCLK3 Control Register	6-48
MUXCTRL	R/W	$D14A_H$	0000_H	Multiplexer Control	6-49

Table 6-8 DCU Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
IMASK	R/W	$D002_H$	0000_H	Interrupt Mask	6-50
STEVE	R	$D003_H$	0000_H	Status Event	6-50
STATC	R	$D004_H$	unchan.	Statistics Counter	6-51
STATI	R	$D005_H$	0000_H	Statistics	6-52

Table 6-9 µP Configuration Register Map

Regist. (16 bit)	Des-cription	Reset Value	Bit	DSP Word Access	µP Byte Access	µP-Addr. MSB of Word	µP-Addr. LSB of Word	DSP Addr.	Page No.
MCFG	configur ation	0_H	6	R	R/W	none	48_H	$D148_H$	6-52
VDEV	device version	hardwired	8	none	R	none	$6A_H$	none	6-54
IVEC	int vector reg	un-changed	8	R/W	R	none	68_H	$D168_H$	6-54

Table 6-10 General Mailbox Register Map

Register (16 bit)	Description	Reset Value	Bit	DSP Word Access	µP Byte Acc.	µP-Addr. MSB of Word	µP-Addr. LSB of Word	DSP Addr.	Page No.
MCMD	µP command	00_H	8	R	W	none	40_H	$D140_H$	6-55
MBUSY	µP MB busy	0_H	1	W	R	41_H	none	$D141_H$	6-55
MGEN	µP generic data reg.	unchanged	16	R	W	43_H	42_H	$D142_H$ (LSB) $D143_H$ (MSB) $D144_H$ (All)	6-56
MDT0	µP data reg0	unchanged	16	R	W	01_H	00_H	$D100_H$	6-57
MDT1	µP data reg1	unchanged	16	R	W	03_H	02_H	$D102_H$	6-57
MDT2	µP data reg2	unchanged	16	R	W	05_H	04_H	$D104_H$	6-57
MDT3	µP data reg3	unchanged	16	R	W	07_H	06_H	$D106_H$	6-57
MDT4	µP data reg4	unchanged	16	R	W	09_H	08_H	$D108_H$	6-57
MDT5	µP data reg5	unchanged	16	R	W	$0B_H$	$0A_H$	$D10A_H$	6-57
MDT6	µP data reg6	unchanged	16	R	W	$0D_H$	$0C_H$	$D10C_H$	6-57
MDT7	µP data reg7	unchanged	16	R	W	$0F_H$	$0E_H$	$D10E_H$	6-57
OCMD	DSP command	00_H	8	W	R	none	60_H	$D160_H$	6-57
OBUSY	DSP MB busy	0_H	1	R	R/W	61_H	none	$D161_H$	6-58
OGEN	DSP generic data reg	unchanged	16	W	R	63_H	62_H	$D162_H$ (LSB) $D163_H$ (MSB) $D164_H$ (All)	6-59
ODT0	DSP data reg0	unchanged	16	W	R	21_H	20_H	$D120_H$	6-59

Table 6-10 General Mailbox Register Map (Continued)

Register (16 bit)	Description	Reset Value	Bit	DSP Word Access	µP Byte Acc.	µP-Addr. MSB of Word	µP-Addr. LSB of Word	DSP Addr.	Page No.
ODT1	DSP data reg1	unchanged	16	W	R	23_H	22_H	$D122_H$	6-59
ODT2	DSP data reg2	unchanged	16	W	R	25_H	24_H	$D124_H$	6-59
ODT3	DSP data reg3	unchanged	16	W	R	27_H	26_H	$D126_H$	6-59
ODT4	DSP data reg4	unchanged	16	W	R	29_H	28_H	$D128_H$	6-59
ODT5	DSP data reg5	unchanged	16	W	R	$2B_H$	$2A_H$	$D12A_H$	6-59
ODT6	DSP data reg6	unchanged	16	W	R	$2D_H$	$2C_H$	$D12C_H$	6-59
ODT7	DSP data reg7	unchanged	16	W	R	$2F_H$	$2E_H$	$D12E_H$	6-59

Note: MDT8..15 and ODT8..15 are accessible only in non-DMA mode, when the DMA Mailbox data registers are used for doubling the size of General Mailbox.

Table 6-11 DMA Mailbox Register Map

Register	Description	Reset Value	Bit	DSP Access	DMA / µP Acc.	µP MSB Addr.	µP LSB Addr.	DSP Addr.	Page No.
DTXCNT	Tx counter	0_H	4	R/W	none	none	none	$D150_H$	6-60
DINSTA	DMA Int status	0_H	4	R	none	none	none	$D152_H$	6-61
TDT0/ MDT8	Tx data reg0/ µP data reg8	un-changed	16	R	W	11_H	10_H	$D110_H$	6-57
TDT1/ MDT9	Tx data reg1/ µP data reg9	un-changed	16	R	W	13_H	12_H	$D112_H$	6-57
TDT2/ MDT10	Tx data reg2/ µP data reg10	un-changed	16	R	W	15_H	14_H	$D114_H$	6-57

Table 6-11 DMA Mailbox Register Map (Continued)

Register	Description	Reset Value	Bit	DSP Access	DMA / µP Acc.	µP MSB Addr.	µP LSB Addr.	DSP Addr.	Page No.
TDT3/ MDT11	Tx data reg3/ µP data reg11	un-changed	16	R	W	17_H	16_H	D116 H	6-57
TDT4/ MDT12	Tx data reg4/ µP data reg12	un-changed	16	R	W	19_H	18_H	D118 H	6-57
TDT5/ MDT13	Tx data reg5/ µP data reg13	un-changed	16	R	W	$1B_H$	$1A_H$	D11A H	6-57
TDT6/ MDT14	Tx data reg6/ µP data reg14	un-changed	16	R	W	$1D_H$	$1C_H$	D11C H	6-57
TDT7/ MDT15	Tx data reg7/ µP data reg15	un-changed	16	R	W	$1F_H$	$1E_H$	D11E H	6-57
DRXCNT	Rx counter	0_H	4	R/W	none	none	none	D170 H	6-60
RDT0/ ODT8	Rx data reg0/ DSP data reg8	un-changed	16	W	R	31_H	30_H	D130 H	6-59
RDT1/ ODT9	Rx data reg1/ DSP data reg9	un-changed	16	W	R	33_H	32_H	D132 H	6-59
RDT2/ ODT10	Rx data reg2/ DSP data reg10	un-changed	16	W	R	35_H	34_H	D134 H	6-59
RDT3/ ODT11	Rx data reg3/ DSP data reg11	un-changed	16	W	R	37_H	36_H	D136 H	6-59
RDT4/ ODT12	Rx data reg4/ DSP data reg12	un-changed	16	W	R	39_H	38_H	D138 H	6-59
RDT5/ ODT13	Rx data reg5/ DSP data reg13	un-changed	16	W	R	$3B_H$	$3A_H$	D13A H	6-59
RDT6/ ODT14	Rx data reg6/ DSP data reg14	un-changed	16	W	R	$3D_H$	$3C_H$	D13C H	6-59
RDT7/ ODT15	Rx data reg7/ DSP data reg15	un-changed	16	W	R	$3F_H$	$3E_H$	D13E H	6-59

Note: MDT8..15 and ODT8..15 are accessible only in non-DMA mode, when the DMA Mailbox data registers are used for doubling the size of General Mailbox.

Table 6-12 Clock Generator Register Map

Reg Name	Access	Address	Reset Value	Comment	Page No.
CPDC	R/W	$D080_H$	0000_H	PDC Control	6-62
CPFS	R/W	$D081_H$	0001_H	PFS Control	6-62
CLKOUT	R/W	$D082_H$	0008_H	CLKOUT Control	6-63
CREFSEL	R/W	$D083_H$	0000_H	DCXO Reference Clock Selection	6-64
CREFCLK	R/W	$D084_H$	0003_H	REFCLK Control	6-65
CDCL2	R/W	$D085_H$	0004_H	DCL_2000 Control	6-65
CDCL	R/W	$D086_H$	$000B_H$	DCL Control	6-66
CFSC	R/W	$D087_H$	0002_H	FSC Control	6-67
CL1CLK	R/W	$D088_H$	0000_H	L1_CLK Control	6-68
CPFSSY	R/W	$D089_H$	0000_H	PFS Synchronization Mode	6-69
CRTCNT	R	$D08E_H$	0000_H	Real-time Counter	6-69
CSTRAP	R/W	$D08F_H$	xxxx xxxx xxxx $xx10_B$	Strap Status Register	6-70

6.2 Detailed Register Description

6.2.1 TRANSIU Register Description

6.2.1.1 TRANSIU IOM-2000 Configuration Register

TICR Register read/write Address: $D0A0_H$

Reset value: 0000_H

Note: The reset value of bit 4KFSC is undefined, since this read-only bit is toggled every 250 µs.

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	4KFSC	CMDEN	DXEN	DR1	DR0

DR1..0 IOM-2000 Data Rate and Channel Number

00 = 3.072 Mbit/s data rate; 8 IOM-2000 channels are supported

01 = 6.144 Mbit/s data rate; 16 IOM-2000 channels are supported

10 = 12.288 Mbit/s data rate; 24 IOM-2000 channels are supported

11 = Reserved

DXEN DX Line Enable

0 = IOM-2000 DX line to the VIP is in tri-state

1 = IOM-2000 DX line to the VIP is enabled (starting with the next 4 kHz frame)

CMDEN CMD Line Enable

0 = IOM-2000 CMD line to the VIP is in tri-state

1 = IOM-2000 CMD line to the VIP is enabled

4KFSC 4 kHz FSC (read only)

0 = In the TRANSIU, the current 8 kHz IOM-2000 frame starts in the second half of the current 4 kHz Upn of S/T frame

1 = In the TRANSIU, the current 8 kHz IOM-2000 frame starts in the first half of the current 4 kHz Upn of S/T frame

Note: 'x' = unused (read as '0')

6.2.1.2 TRANSIU Channel Configuration Registers

The Channel registers are used for IOM-2000 channel disabling and mode programming. Each IOM-2000 channel may be programmed to Upn, LT-S, or LT-T mode, or completely disabled.

Important

Only four channels out of eight channels are programmable to **Upn and S/T** modes in VIP PEB 20590, the remaining four channels may be operated as Upn transceiver only. It is the user's responsiblity to ensure that the IOM-2000 channels in the TRANSIU are correctly configurated in order to match with the line configuration of the VIP (see below:

Table 6-13 Available ISDN Modes for each VIP Channel

VIP_0,1,2 channel	0	1	2	3	4	5	6	7
TRANSIU channel	0 8 16	1 9 17	2 10 18	3 11 19	4 12 20	5 13 21	6 14 22	7 15 23
Available VIP Mode	Upn	Upn S/T	Upn	Upn S/T	Upn	Upn S/T	Upn	Upn S/T
Available VIP8 Mode	Upn S/T	Upn S/T	Upn S/T	Upn S/T	Upn S/T	Upn S/T	Upn S/T	Upn S/T

Registers TCCR0 - 3 read/write Address:
TCCR0: $D0A1_H$
TCCR1: $D0A2_H$
TCCR2: $D0A3_H$

Reset values: $FFFF_H$

15	14	13	12	11	10	9	8
C7M(1:0)		C6M(1:0)		C5M(1:0)		C4M(1:0)	

7	6	5	4	3	2	1	0
C3M(1:0)		C2M(1:0)		C1M(1:0)		C0M(1:0)	

C7..0M(1:0) Operational Mode of IOM-2000 Channel7..0

00 = Channel is configured to S mode (LT-S)

01 = Channel is configured to S mode (LT-T)

10 = Channel is configured to Upn mode

11 = Channel is disabled, ’0’s are sent on the DX line

Note: TCCR0 (channel 7..0), TCCR1 (channel 15..8) and TCCR2 (channel 23..16) have the same structure, only TCRR1 is shown here.

6.2.1.3 VIP Command Registers (VIPCMR0, VIPCMR1, VIPCMR2)

The VIPCMR0-2 registers contain command information dedicated to the VIP 0, 1, 2 (only the VIPCMR0 is shown here, VIPCMR1 and VIPCMR2 have the same structure).

VIPCMR Register write Address:
VIPCMR0: $D0A8_H$
VIPCMR1: $D0A9_H$
$VIPCMR2_H$: $D0AA_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	RD_n	PLLPPS	SH_FSC	DELRE

7	6	5	4	3	2	1	0
DELCH(2:0)			EXREF	REFSEL (2:0)			WR_n

WR_n **Write Command to VIP_n (S/T, U_{PN})**

0 = Data sent to VIP_n is invalid

1 = Data sent to VIP_n is valid

REFSEL(2:0) **Reference Clock Channel Select (LT-T)**

The reference clock signal for the DELIC oscillator is generated from the internal VIP_n Channel_m coded in these 3 bits and passed on via pin REFCLK to the next cascaded VIP or directly to the DELIC

000 = Reference clock provided by Channel_0

001 = Reference clock provided by Channel_1

...

007 = Reference clock provided by Channel_7

EXREF **External Reference Clock Selection (LT-T)**

0 = No external reference clock source. Reference clock is generated from internal VIP_n channel specified in REFCLK(2:0) and passed on via REFCLK pin to VIP_n-1 or directly to DELIC.

1 = Reference clock is generated from external source via pin INCLK and passed on via REFCLK pin to VIP_n-1 or directly to DELIC. The internal reference clock generation logic is disabled.
Note that VIP_0 has the highest priority in terms of clock selection

DELCH(2:0) **Delay Measurement Channel Selection (U_{PN})**

Selects one of the eight Upn line interface channels of each VIP where the delay is to be measured.

000 = Delay is measured in Upn Channel_0

001 = Delay is measured in Upn Channel_1

...

111 = Delay is measured in Upn Channel_7

DELRE **Delay Counter Resolution (U_{PN})**

Resolution of the delay counter.

0 = Resolution of 65 ns (15.36 MHz period)

1 = Resolution of 130 ns (7.68 MHz period)

Note: Using a resolution of 65 ns, the maximum delay of 20.8 µs is not covered (refer to DELAY(7:0) bits)

SH_FSC **Short FSC Pulse**

0 = The next FSC frame is no superframe

1 = The next FSC is assumed as superframe

PLLPPS **PLL Positive Pulse Sensing**

0 = Normal operation

1 = The clock recovering PLLs of all VIP channels operate on positive line pulses only

RD_n **Read Request to VIP Status Register S_n (S/T, U_{PN})**

0 = No register read

1 = The DSP reads the VIP register (during initialization, debugging or error conditions). The register value is available for the read operation in the consecutive frame (after the next FSC).

Note: To avoid blocking, the DSP must not issue this bit during normal operation.

Note: Unused bits (x) read as '0'. The registers are reset upon every 8 kHz frame sync to avoid multiple data transmit/receive to/from the VIP.

6.2.1.4 VIP Status Registers

The VIPSTR0-2 registers contain the status bits received from the dedicated VIP for VIPs 0, 1, 2 respectively (all three registers have the same structure).

VIPSTR Register read Address: VIPSTR0: $D0AC_H$, VIPSTR1: $D0AD_H$, VIPSTR2: $D0AE_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
DELAY(7:0)							

DELAY(7:0) **Line Delay Value (U_{PN})**

Returns the value of the measured line delay (in µs) between the Upn transmit and receive frame with a resolution of 65 ns or 130 ns (programmable in VIPCMR.DELRE bits).
The value indicates the delay between the transmitted M-bit and the received LF-bit (minus the U_{PN} guard time of 2 bits). The delay for one direction equals to the measured delay divided by two.
The channel address for the delay measurement is coded in VIPCMR.DELCH(2:0) bits.

The VIP provides 2 values in one U_{PN} frame (one every 125 µs) from which the bigger one is the valid.

Note: The transceiver delays of the VIP are included in the delay measurement.

Note: Unused bits (x) read as '0'.

6.2.1.5 TRANSIU Initialization Channel Command Register

The Initialization Channel Command Register contains the Command bits for VIP_n, Channel_m together with 5 bits of the VIP channel address.

The VIP only acts upon the command bits if they were declared valid by the DELIC issuing a write command. Bit WR is dedicated to the command bits of groups CONF1, CONF2 and TST2, whereas WR_ST informs the VIP about changes in the layer 1 state machine of the DELIC (SMINI(2:0) and MSYNC bits).

The DELIC may also explicitly read the VIP's status information by issueing bit RD.

The reset value of each bit is '0' except bits MODE(2:0) which are set to '011'

Note: A read command to the VIP must not be issued during normal operation to avoid a loss of information when the VIP is reporting status information at the same time.

TICCMR Register

write
LS-word: $D0B0_H$,

Address:
MS-word: $D0B1_H$

Reset value: 0000_H

31	30	29	28	27	26	25	24
x	VIPADR(1:0)		CHADR(2:0)			FIL	EXLP

23	22	21	20	19	18	17	16
PLLS	PD	DHEN	x	x	PDOWN	LOOP	TX_EN

15	14	13	12	11	10	9	8
PLLINT	AAC(1:0)		BBC(1:0)		OWIN(2:0)		

7	6	5	4	3	2	1	0
MF_EN	MODE(2:0)			MOSEL(1:0)		RD	WR

WR **Write Command (S/T, U_{PN})**

0 = Data sent in these bits is invalid

1 = All configuration bits contain valid data

Note: Does not apply to SMINI(2:0) and MSYNC bits

RD **Read Request to VIP Command Bits (S/T, U_{PN})**

0 = Normal operation

1 = DELIC read request of the TICCMR register which was sent to the VIP. It includes initialization and configuration commands and the channel addresses. The VIP returns these values (instead of sending the actual VIP status information) within the IOM-2000 STAT_n_m bit stream. The values are available in the next frame (after next FSC) in DELIC TICSTR register.
Note: To avoid blocking, the DELIC must not issue this bit during normal operation.

MOSEL(1:0) **Interface Mode Selection (S/T, U_{PN})**

00 = Channel programmed to S/T mode

01 = Channel programmed to U_{PN} mode

10 = reserved

11 = reserved

MODE(2:0) **Mode Configuration (S/T, U_{PN})**

001 = Channel programmed to LT-T mode

011 = Channel programmed to LT-S mode (point-to-point or extended passive bus configuration) or U_{PN} mode

111 = Channel programmed to LT-S mode (short passive bus mode)

Note: All other states are reserved. The reset value is 011, e.g. the default mode of VIP is LT-S

MF_EN **Multiframe Enable (S/T)**

0 = Multiframes are disabled

1 = Multiframes are enabled

OWIN(2:0) **Oversampling Window Size (S/T, U_{PN})**

Specifies the width of the oversampling window in bit samples. The window is centered about the middle of the bit. For example, a size of 16 means that, upon detection of (16/2) = 8 times logical ’1’, the received bit is detected as ’1’. The window size is programmed in steps of two as shown below:

000 = 2

001 = 4

010 = 6

...

111 = 16

BBC(1:0) **Balancing Bit Control (U_{PN})**

0x = Adaptive generation of balancing bit (depending on line delay). upon reception of INFO3 or INFO4

10 = Balancing bit control is disabled, and no balancing bit is added

11 = Balancing bit control is disabled, and balancing bit is added after each code violation in the M-bit (INFO3 or INFO4)

AAC(1:0) **Adaptive Amplifier Control (S/T, U_{PN})**

0x = Adaptive amplifier control in VIP is enabled. The amplifier and the equalizer are switched on/off depending on the level of the received line signal with respect to the comparator threshold.

10 = Adaptive amplifier control is disabled. The amplifier and the equalizer are switched off permanently.

11 = Adaptive amplifier control is disabled. The amplifier and the equalizer are switched on permanently

PLLINT **Receive PLL Integrator (U_{PN})**

0 = Programmable deviation disabled

1 = Programmable deviation enabled, i.e., the RxPLL reacts only after a certain number of consequent deviations from the PLL controlling range.

TX_EN **Transmitter Enable (S/T, U_{PN})**

0 = Transmitter (analog line driver) is disabled (e.g. for non-transparent analog loops in LT-T)

1 = Transmitter is enabled (e.g. for switching of transparent analog loops in LT-S)

LOOP **Loop-back Mode in VIP Enable (S/T, U_{PN})**

0 = Loops disabled

1 = Loop-back enabled. Channel_m transmit data is looped back to the receive data path (either transparent or non-transparent according to state of bit TX_EN). Depending on bit EXLP the loop is closed internally or externally.

PDOWN **Power Down Mode (S/T, U_{PN})**

0 = Operational mode

1 = Channel_m in power-down mode (only the level detector in the VIP receiver is in operational mode)

DHEN **D-channel Handling Enable (LT-T)**

0 = D-channel transmitted transparently, without any condition

1 = D-channel transmitted transparently if no collision is detected (E=D), if collision is detected (E ≠ D) ’1s’ are transmitted in D-channel

PD **Phase Deviation Selection (LT-T)**

0 = Phase deviation = (2 bits - 2 oscillator periods + analog delay)

1 = Phase deviation = (2 bits - 4 oscillator periods + analog delay)

PLLS **Receive PLL Adjustment (S/T, U_{PN})**

0 = tracking step equals 0.5 oscillator period

1 = tracking step equals 1.0 oscillator period

EXLP **External Loop (S/T, U_{PN})**

0 = No external analog loop. If bit LOOP=1 the loop is closed internally

1 = External analog loop. If bit LOOP=1 the loop is closed externally

FIL **Filter Enable (U_{PN} only)**

0 = Filter of equalizer inside the VIP receiver disabled

1 = Filter of equalizer inside the VIP receiver enabled

CHADR(2:0) **Channel_m Address for Commands**

000 = Command word is dedicated to VIP_n Channel_0

001 = Command word is dedicated to VIP_n Channel_1

010 = Command word is dedicated to VIP_n Channel_2

011 = Command word is dedicated to VIP_n Channel_3

100 = Command word is dedicated to VIP_n Channel_4

101 = Command word is dedicated to VIP_n Channel_5

110 = Command word is dedicated to VIP_n Channel_6

111 = Command word is dedicated to VIP_n Channel_7

VIPADR(2:0) **VIP_n Address for Commands**

00 = Command word is dedicated to VIP_0

01 = Command word is dedicated to VIP_1

10 = Command word is dedicated to VIP_2

11 = Reserved

Note: Unused bits (x) read as ‘0’.

6.2.1.6 TRANSIU Initialization Channel Status Register (TICSTR)

The Initialization Channel Status Register contains the Command bits to VIP_n, Channel_m mirrored by the VIP in response to a read command issued by the DELIC in the previous frame.

Note: The actual Status information from the VIP channels is stored in the data RAM to make it accessible for the DELIC layer-1 state machine software in the DSP.

TICSTR Register read Address:
LS-word: $D0B2_H$, MS-word: $D0B3_H$

Reset value: 0000_H

31	30	29	28	27	26	25	24
x	VIPADR(1:0)		CHADR(2:0)			FIL	EXLP

23	22	21	20	19	18	17	16
PLLS	PD	DHEN	x	x	PDOWN	LOOP	TX_EN

15	14	13	12	11	10	9	8
PLLINT	AAC(1:0)		BBC(1:0)		OWIN(2:0)		

7	6	5	4	3	2	1	0
MF_EN	MODE(2:0)			MOSEL(1:0)		RD	WR

6.2.1.7 Scrambler Mode Register

SCMOD Register read/write Address: $D010_H$

Reset value: 0003_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	SCMOD1..0	

SCMOD1..0 Scrambling Mode of the Upn Line Interface

00 = Scrambling according to ITU-T V.27

01 = Scrambling compatible to OCTAT-P PEB 2096

10 = Reserved

11 = No scrambling

6.2.1.8 Scrambler Status Register

SCSTA Register read/write Address: $D011_H$

Reset value: undefined

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	SCSTA

SCSTA Scrambler Status

0 = Write access: start of scrambling algorithm for all channels enabled in the HRAM
read access: scrambler is processing data

1 = Write access: start of scrambling algorithm for all channels enabled in the HRAM
read access: scrambling has finished

Note: Both values '0' or '1' written to SCSTA will start the scrambling

6.2.2 IOMU Register Description

6.2.2.1 IOMU Control Register

ICR Register read/write Address: $D040_H$

Reset value: 02_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	ICDB	A	OD	DC	DR(1:0)	

ICDB Idle Current D-Buffer (for test purpose; only if IOMU is in idle mode: ICR:A = '0')

0 = Make frame buffer 0 accessible to the DSP

1 = Make frame buffer 1 accessible to the DSP

A IOMU Activation

0 = The IOMU is Idle. The state machine of the IOMU is idle, and no accesses to the I-buffer are executed by the IOMU.

1 = The IOMU is active, and works according to the programming of the other Control Register bits.

OD DD0 and DD1 Output Mode

0 = Push-Pull mode.

1 = Open-Drain mode

DC Double Data Rate Clock

0 = Single clock (DCL frequency is identical to the IOM-2 data rate)

1 = Double clock (DCL frequency is double the IOM-2 data rate)

DR(1:0) IOM-2 Data Rate

00 = IOM-2 data rate of 1 x 384 kbit/s (1 x 6 time slots/frame)

01 = IOM-2 data rate of 1 x 768 kbit/s (1 x 12 time slots/frame)

10 = IOM-2 data rate of 2 x 2.048 Mbit/s (2 x 32 time slots/frame) **(default)**

11 = IOM-2 data rate of 1 x 4.096 Mbit/s (1 x 64 time slots/frame)

6.2.2.2 IOMU Status Register

ISR Register read/write Address: $D041_H$

Reset value: undefined

15	14	13	12	11	10	9	8
IBUFF	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

IBUFF I-Buffer Index

Note: Used for testing. May also be used in double data rate mode of the IOMU to determine if the IOMU buffers have been swapped already

0 = Buffer 0 is currently used as I-buffer, buffer 1 is used as D-buffer

1 = Buffer 1 is currently used as I-buffer, buffer 0 is used as D-buffer

Note: (x) unused bits read as '0'

6.2.2.3 IOMU Tri-State Control Register

ITSCR Register read/write Address:
Set Address: $D042_H$
Reset Address: $D043_H$
Read Address: $D044_H$

Reset Value: 00_H

15	14	13	12	11	10	9	8
TS(15:8)							

7	6	5	4	3	2	1	0
TS(7:0)							

TS(15:0)

Every bit determines whether DD0/1 output is in tri-state during the time slot sequence. The time slot sequence length, indices and port controlled by each TS-bit is defined according the IOMU data rate mode (ICR.DR(1:0))

0 = DD0/1 is in tri-state during the related time slot sequence

1 = DD0/1 is driven by the IOMU during the related time slot sequence

Table 6-14 Tristate Control Assignment for IOM-2 Time Slots

ITSCR Bit	1 x 6 TS/frame		1 x 12 TS/frame		2 x 32 TS/frame		1 x 64 TS/frame	
	DD0	TS	DD0	TS	DD0/1	TS	DD0/1	TS
TS0	DD0	0	DD0	0	DD0	0-3	DD0	0-3
TS1	DD0	1	DD0	1	DD0	4-7	DD0	4-7
TS2	DD0	2	DD0	2	DD0	8-11	DD0	8-11
TS3	DD0	3	DD0	3	DD0	12-15	DD0	12-15
TS4	DD0	4	DD0	4	DD0	16-19	DD0	16-19
TS5	DD0	5	DD0	5	DD0	20-23	DD0	20-23
TS6	not used		DD0	6	DD0	24-27	DD0	24-27
TS7	not used		DD0	7	DD0	28-31	DD0	28-31
TS8	not used		DD0	8	DD1	0-3	DD0	32-35

Table 6-14 Tristate Control Assignment for IOM-2 Time Slots (Continued)

ITSCR Bit	1 x 6 TS/frame		1 x 12 TS/frame		2 x 32 TS/frame		1 x 64 TS/frame	
	DD0	TS	DD0	TS	DD0/1	TS	DD0/1	TS
TS9	not used		DD0	9	DD1	4-7	DD0	36-39
TS10	not used		DD0	10	DD1	8-11	DD0	40-43
TS11	not used		DD0	11	DD1	12-15	DD0	44-47
TS12	not used		not used		DD1	16-19	DD0	48-51
TS13	not used		not used		DD1	20-23	DD0	52-55
TS14	not used		not used		DD1	24-27	DD0	56-59
TS15	not used		not used		DD1	28-31	DD0	60-63

6.2.2.4 IOMU DRDY Register

IDRDYR Register read Address: $D045_H$

Reset value: undefined

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	0
DS(7:0)							

bit DRDY Sample

DSx indicates the availability of the D-channels of the previous frame.
0 = STOP (D-channel blocked due to collision), 1 = GO
e.g. DS1 was sampled during the D-channel of IOM-2 channel 1, etc.

DS0 corresponds to D-channel of IOM-2 port 0 cha 0

DS1 corresponds to D-channel of IOM-2 port 0 cha 1

DS2 corresponds to D-channel of IOM-2 port 0 cha 2

DS3 corresponds to D-channel of IOM-2 port 0 cha 3

DS4 corresponds to D-channel of IOM-2 port 0 cha 4

DS5 corresponds to D-channel of IOM-2 port 0 cha 5

DS6 corresponds to D-channel of IOM-2 port 0 cha 6

DS7 corresponds to D-channel of IOM-2 port 0 cha 7

Note: In 1 x 4.096 Mbit/s mode (i.e.16 IOM-2 channels/frame), DRDY is sampled only during the D-channels of the first eight IOM-2 channels of every frame.

6.2.2.5 IOMU Data Prefix Register

IDPR Register read/write Address: $D046_H$
Reset value: $E0_H$

15	14	13	12	11	10	9	8
IDP(7:0)							

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

IDP(7:0) IOMU Data Prefix

Determines the high byte of every word being read from the IOM circular-buffer (I-buffer or D-buffer). The low byte is the data being read from the circular buffer.

After reset this register contains the MSB of the base address of the A-law-to-linear ROM table: $E0_H$.

Note: (x) unused bits read as '0'

6.2.3 PCMU Register Description

6.2.3.1 PCMU Command Register

PCR Register read/write Address: $D060_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	SFH	ICDB	PA	PDCL	PDR(1:0)	

PDR(1:0) PCM Data Rate

00 = 4 x 2.048 Mbit/s (4 x 32 time slots per frame)

01 = 2 x 4.096 Mbit/s (2 x 64 time slots per frame)

10 = 1 x 8.092 Mbit/s (1 x 128 time slots per frame)

11 = 1 x 16.384 Mbit/s (1 x 256 time slots per frame, if only first or second half of 8 kHz frame is handled)

PDCL PCM Double Data Rate Clock

0 = Single Data Rate Clock

1 = Double Data Rate Clock

PA PCMU Activation

0 = The PCMU is in idle mode

1 = The PCMU is in active mode

ICDB Idle Current D-Buffer
Used only for testing of PCMU in IDLE mode (PCR:PA = '0') to determine which buffer is being accessed by the DSP

0 = Frame buffer 0 is accessed by the DSP

1 = Frame buffer 1 is accessed by the DSP

SFH Second Frame Half
Used only in 1 x 256 time slots per frame data rate mode

0 = The first 128 time slots of each frame are handled by the PCMU

1 = The second 128 time slots of each frame are handled by the PCMU

Note: 'x' = unused (read as '0')

6.2.3.2 PCMU Status Register

PSR Register read/write Address: $D061_H$

Reset value: undefined

15	14	13	12	11	10	9	8
PBUFF	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

PBUFF P-Buffer Index

Note: Used for testing. May also be used in double data rate mode of the PCMU to determine if the PCMU buffers have been swapped already

0 = Buffer 0 is currently used as P-buffer, buffer 1 is used as D-buffer

1 = Buffer 1 is currently used as P-buffer, buffer 0 is used as D-buffer

Note: (x) unused bits read as '0'

6.2.3.3 PCMU Tri-state Control Registers

PTSC0 Register	read/write (set/reset)	read Address: D062-63$_H$ set Address: D062$_H$ reset Address: D063$_H$
PTSC1 Register	read/write (set/reset)	read Address: D064-65$_H$ set Address: D064$_H$ reset Address: D065$_H$
PTSC2 Register	read/write (set/reset)	read Address: D066-67$_H$ set Address: D066$_H$ reset Address: D067$_H$
PTSC3 Register	read/write (set/reset)	read Address: D068-69$_H$ set Address: D068$_H$ reset Address: D069$_H$
PTSC4 Register	read/write (set/reset)	read Address: D06A-6B$_H$ set Address: D06A$_H$ reset Address: D06B$_H$
PTSC5 Register	read/write (set/reset)	read Address: D06C-6D$_H$ set Address: D06C$_H$ reset Address: D06D$_H$
PTSC6 Register	read/write (set/reset)	read Address: D06E-6F$_H$ set Address: D06E$_H$ reset Address: D06F$_H$
PTSC7 Register	read/write (set/reset)	read Address: D070-71$_H$ set Address: D070$_H$ reset Address: D071$_H$

Reset values (PTSC0..7): 0000$_H$

15	14	13	12	11	10	9	8
PTSCn(15:8)							

7	6	5	4	3	2	1	0
PTSCn(7:0)							

PTSCn (15..0) Tristate Control for each PCM Time Slot

0 = The controlled time slot is invalid

1 = The controlled time slot is valid

6.2.3.4 PCMU Data Prefix Register

PDPR Register read/write Address: $D072_H$

Reset value: $E0_H$

15	14	13	12	11	10	9	8
PDP(7:0)							

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

PDP(7:0) PCMU Data Prefix

The data written to this register is read as the most significant byte of every time slot read by the DSP from the PCMU frame buffers. Can be used for quick access to the a/µ-law ROM, for conversion of compressed data (received via the PCM interface) into linear value.

After reset this register contains the MSB of the base address of the a-law-to-linear ROM table: $E0_H$. To enable quick conversion from µ-law to linear, the PCMU Data Prefix Register should be programmed to $E1_H$.

Note: (x) unused bits read as '0'

6.2.4 A-/µ-law Unit Register Description

6.2.4.1 A/µ-law Unit Control Register

A/µ-law Unit Control Register (AMCR) read/write Address: $D020_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	MODE

Note: 'x' = unused bits

This register controls the conversion mode of the A/µ-law unit

MODE A/µ-law Mode Programming

0 = Conversion from linear value to A-law value (default)

1 = Conversion from linear value to µ-law value

6.2.4.2 A/µ-law Input Register

A/µ-law Unit Input Register (AMIR) write Address: $D021_H$

Reset value: undefined

15	14	13	12	11	10	9	8
IND(15:8)							

7	6	5	4	3	2	1	0
IND(7:0)							

Note: - In µ-law mode, only the 14 MSBs are processed.
- In A-law mode, only the 13 MSBs are processed.

IND(15:0) Linear Input Data

Provides the linear input data that is to be converted into logarithmic data format according to A-law or µ-law algorithm.

6.2.4.3 A/µ-law Output Register

A/µ-law Unit Output Register (AMOR) read Address: $D022_H$

Reset value: undefined

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
OUTD(7:0)							

Note: 'x' = unused bits, driven to '0'

OUTD(7:0) Logarithmic Output Data

Provides the logarithmic output data generated by the A/-µ-law unit out of the linear input data. The data format (A-law or µ-law) depends on the the selected conversion algorithm.

6.2.5 HDLCU Registers Description

6.2.5.1 HDLCU Control Register

In order to enable DSP access all the buffers and RAMS, DSPCTRL bit must be set to ‘1’.

HCR Register write Address: $D180_H$

Reset value: 0001_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	HPRS(5:0)						DSPCTRL

HPRS(5:0) HDLCU Channel Preset

The number of HDLC channels to be processed by the HDLCU

DSPCTRL DSP Access Control to the HDLCU

0 = The DSP must not access the HDLCU buffers and RAMs

1 = The DSP may access the HDLCU buffers

Note: Each time DSPCTRL is set, HPRS is also set.

6.2.5.2 HDLCU Status Register

HSTA Register read Address: $D180_H$

Reset value: 0001_H

15	14	13	12	11	10	9	8
HHOLD	BITOR	x	CHCNT(5:1)				

7	6	5	4	3	2	1	0
CHCNT(0)	HPRS(5:0)						DSPCTRL

DSPCTRL DSP Access Control to the HDLCU

0 = The HDLCU is currently processing the channel

1 = The DSP is currently accessing the HDLCU

HPRS(5:0) HDLC Channel Preset

Number of HDLC channels handled by the HDLCU (max. 32)

CHCNT(5:0) **Channel Count**

Number of channels that have already been processed in the current frame

BITOR **Bitorder**

Determines the order of bits inside an HDLC data byte going to (coming from) the IOMU, PCMU or TRANSIU.

0 = HDLC data is transmitted with MSB first

1 = HDLC data is transmitted with LSB first

HHOLD **HDLCU Busy Indicator**

0 = HDLCU is processing the current frame

1 = HDLCU has finished processing the current frame

6.2.5.3 Channel Command Vector

HCCV Registers read/ write Addresses: 4040_H - $405F_H$

Each of the 32 HDLC channels has a 7-bit command vector that resides in the corresponding address of the command RAM. The structure of a command vector is as follows:

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	DBSEL	RECRES	TXCMD(2:0)			CRC	IDLE

Note: Accesses to these registers are possible only if register bit HCR:DSPCTRL = 1
'x' = unused

DBSEL D- or B-Channel Select

0 = Indication for a B-channel. HDLC protocol is performed on all 8 data bits

1 = Indication for a D-channel. HDLC protocol is performed only on the 2 MSB data bit in the Receive Input Buffer and Transmit Output Buffer

RECRES Receiver Reset

0 = Normal operation

1 = Reset the HDLC receiver

TXCMD(2:0) Transmit Command

000= End transmition

001= Start transmission at the first bit of the D-channel

010= Start transmission at the second bit of the D-channel

011= Start transmitting a flag (beginning with the fifth bit of the flag, since '0111' is automatically inserted)

100= Abort transmission

Note: other combinations are reserved

CRC CRC Enable

0 = CRC checking algorithm off

1 = CRC checking algorithm on

IDLE IDLE Mode

0 = Transmit 'ones' over an idle channel - the unshared flag mode

1 = Transmit 'flags' over an idle channel - the shared flag mode

Note: In the receive direction, the only function of the command vector is to indicate whether the channel is a D-channel or a B-channel, and whether to use CRC decoding or not.
The main function of the command vector is to control the flow of time slots in the transmit direction.

6.2.5.4 Channel Status Vector

HCSV Registers read Addresses: $40A0_H$ - $40BF_H$

Reading a channel from the Receive Output Buffer and Writing to a channel in the Transmit Input Buffer is done according to the channel's status vector in the Transmit Output Buffer. This vector contains 7 flags:

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	FLAG	EMPTY	FULL	ABORT	STOP	CRC	NO

Note: Accesses to these registers are possible only if register bit HCR:DSPCTRL = 1
'x' = not used

NO Not Octet

0 = Normal operation

1 = The last bits of a message have not filled an octet (8 bits)

CRC CRC Error

0 = No CRC error in received message

1 = CRC error was detected in the received message

STOP Stop Indication

0 = Normal operation

1 = HDLCU has detected an end of message flag in the receive direction. The DSP must read the octet in the Receive Output Buffer before the next message start flag is detected

ABORT Abort Indication

0 = Normal operation

1 = The DSP has detected an incoming abort message (7 consecutive ’1s’). The STOP flag is also set to 1. This means that the DSP should ignore the current message being transmitted over the channel in question and report to the external microcontoller

FULL Receive Buffer Full Indication

0 = Normal operation

1 = Indicates that the Receive Output Buffer has a newly processed octet in it. The DSP must read this octet before starting the next processing session, otherwise it might be lost.

EMPTY Transmit Buffer Empty

0 = The transmit buffer is full.

1 = The transmit buffer is empty. The current time slot in the Transmit Input Buffer has been fully processed by the HDLCU. The Transmit Input buffer is ready to receive the next octet of the message by the DSP.

Note: The DSP must put a new octet into the buffer before starting the next processing session, otherwise the same octet will be read again.

FLAG Status Vector Flag

0 = Ignore the status vector and do not read or write on this channel

1 = Read the channel’s status vector and process accordingly

Note: FLAG will go to ‘1’ as soon as EMPTY or FULL go to ‘1’.

6.2.6 GHDLC Register Description

6.2.6.1 GHDLC Test/ Normal Mode Register

GTEST Register write Address: $D0C0_H$

Reset value: 0001_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	TEST

CHMOD1..0 Channel Mode

0 = Normal operation mode

1 = Test mode

Note: As GTEST has a reset value of 01H this register has to set to 0 to enable the GHDLCU

6.2.6.2 GHDLC Channel Mode Register

GCHM Register write Address: $D0C1_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	CHMOD(1..0)	

CHMOD1..0 Channel Mode

00 = Channel 0 used up to 16.384 MHz

01 = 2 channels (ch 0+3) used up to 8.192 MHz

10 = 4 channels (ch 0..3) used up to 4.096 MHz

11 = Reserved

6.2.6.3 GHDLC Interrupt Register

GINT Register read Address: $D0D4_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	INT3	INT2	INT1	INT0

INTn bits Interrupt Indication for GHDLC Channel n (= 0..3)

0 = Normal operation

1 = GHDLC interrupt has occurred

6.2.6.4 GHDLC FSC Interrupt Control Register

GFINT Register read Address: $D0D3_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	FINT3	FINT2	FINT1	FINT0

FINTn FSC Interrupt Control GHDLC Channel n (= 0..3)

0 = FSC rising edge causes a receiver interrupt only if a full interrupt has not occurred during the previous frame

1 = FSC rising edge causes a receiver interrupt regardless whether or not a full interrupt occurred during the previous frame

6.2.6.5 GHDLC Receive Channel Status Registers 0..3

GRSTA Register 0	read	Address: $D0C2_H$
GRSTA Register 1	read	Address: $D0C3_H$
GRSTA Register 2	read	Address: $D0C4_H$
GRSTA Register 3	read	Address: $D0C5_H$

Reset value: $001F_H$

15	14	13	12	11	10	9	8
x	x	x	x	x	x	COLLD	UNDER

7	6	5	4	3	2	1	0
EMPTY	OVER	FULL	RBFILL(4:0)				

RBFILL(4:0) Receive Buffer Fill

Indicates to the DSP the currently available number of bytes - 1 in the receive buffer

FULL Receive Buffer Full

0 = No receive buffer full indication

1 = Receive buffer block of the GHDLC is full. The blocks have been switched.

OVER Buffer Overrun

0 = No buffer overrun indication

1 = Two consecutive full interrupts were received without a GHDLC access to the status register in between, i.e. a buffer was missed.

EMPTY Transmit Buffer Empty

0 = No transmit buffer empty indication

1 = The transmit buffer block currently being transmitted over the GHDLC channel has been emptied

UNDER Buffer Underrun

0 = No buffer underrun indication

1 = A buffer containing an uncomplete message has been emptied without a continuation of the message in the other buffer

COLLD Collision Detected

0 = No collision detection indication

1 = Collision detected during transmission. The message needs to be re-sent.

Note: Only relevant in HDLC-Mode, if one device does not operate conform to the HDLC protocol definition

Note: Reading the register GRSTA resets its bits to the default value.

6.2.6.6 GHDLC Receive Data and Status

To each data byte in the receive buffer 4 flag bits are appended

RXDAT Registers read Address: 2000_H -$203F_H$

.

15	14	13	12	11	10	9	8
ABORT	END	CRC	NO	x	x	x	x

7	6	5	4	3	2	1	0
RDAT7..0							

NO Not Octet

0 = Received message is a multiple of eight bits

1 = Received message is not a multiple of eight bits

CRC CRC Error Flag

0 = Received byte contains no CRC error flag.

1 = Received byte contains a CRC error flag.

A CRC error was detected in the received frame.

END END Flag

0 = Received byte contains no END flag

1 = Received byte contains an END flag

ABORT ABORT Flag

0 = Received byte contains no ABORT flag

1 = Received byte contains an ABORT flag

RD7..0 Received data byte

6.2.6.7 GHDLC Mode Registers

GMOD Register 0	write	Address: $D0C6_H$
GMOD Register 1	write	Address: $D0C7_H$
GMOD Register 2	write	Address: $D0C8_H$
GMOD Register 3	write	Address: $D0C9_H$

Reset value: 0140_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	EDGE	TE

7	6	5	4	3	2	1	0
CLASS	COLLD	PPOD	IFTF	OPMOD(1:0)		CRCMOD(1:0)	

CRCMOD(1:0) CRC Mode

00 = CRC algorithm disabled

01 = 16-bit CRC algorithm $(X^{16}+X^{12}+X^5+1)$

10 = 32-bit CRC algorithm
$(X^{31}+X^{26}+X^{23}+X^{22}+X^{16}+X^{12}+X^{11}+X^{10}+X^8+X^7+X^5+X^4+X^2+X^1+1)$

11 = reserved

OPMOD(1:0) Operational Mode
Programs the mode of the GHDLC channel

00 = HDLC mode

01 = reserved

10 = Asynchronous mode (enables accesses to register GASYNC)

11 = reserved

IFTF **Interframe Time Fill**

0 = Sequence of ’1s’ is used as interframe time fill characters

1 = Flags ($7E_H$) are used as interframe time fill characters

PPOD Push-Pull / Open-Drain Configuration

0 = Open-drain

1 = Push-pull

COLLD **Collision Detection**

0 = Collision detection disabled

1 = Arbitration between several GHDLC on a bus is done using collision detection

CLASS Priority Class Assignment

0 = Channel has priority class 8

1 = Channel has priority class 10

TE **Transmit Enable**

0 = Transmit line is only enabled during the transmission of a message including opening and closing flags

1 = Transmit line is always enabled

EDGE **Edge Programming for Receive Data Sampling**

0 = Receiver samples data on rising edge of the line clock

1 = Receiver samples data on falling edge of the line clock

6.2.6.8 GHDLC Channel Transmit Command Registers

GTCMD Register 0	write	Address: $D0CA_H$
GTCMD Register 1	write	Address: $D0CC_H$
GTCMD Register 2	write	Address: $D0CE_H$
GTCMD Register 3	write	Address: $D0D0_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	STOP	TXCMD	TBFILL(4:0)				

TBFILL(4:0) Transmit Buffer Fill
Indicates to the GHDLC unit the currently available number of bytes - 1 in the transmit buffer.

TXCMD Transmission Command

0 = Transmission is not started

1 = Start transmission

STOP **Stop Command**

0 = Message continues in the next buffer

1 = End of the message is in this buffer

6.2.6.9 ASYNC Control Register

GASYNC Register read/ write Address: $D0D2_H$

Reset value: 0000

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
IOPORT(7..0)							

Accesses to register GASYNC:

IOPORT bits	Writing a "1" to the bit position sets the port pin below	Reading from the bit position indicates the current state of the port pin below
bit 0	LTXD0	LRXD0
bit 1	LTXD1	LRXD1
bit 2	LTXD2	LRXD2
bit 3	LTXD3	LRXD3
bit 4	$\overline{\text{LRTS0}}$	$\overline{\text{LCTS0}}$
bit 5	$\overline{\text{LRTS1}}$	$\overline{\text{LCTS1}}$
bit 6	$\overline{\text{LRTS2}}$	$\overline{\text{LCTS2}}$
bit 7	$\overline{\text{LRTS3}}$	$\overline{\text{LCTS3}}$

Accesses to the different bits of this register are only possible in ASYNC mode of the corresponding GHDLC channel (See “GHDLC Mode Registers” on page 42.).

Note: GHDLC channels 3..1 are only accessible, if respective bits in register MUXCTRL are set.

6.2.6.10 LCLK0 Control Register

LCLK0 Control Register (GLCLK0) read/write Address: $D08A_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	LCLK0EN	LCLK0(1:0)	

Note: 'x' = unused bits, read as 0.

LCLK0EN LCLK0 Output Enable

0 = LCLK0 is input (default)

1 = LCLK0 is driven outward via LCLK0 pin

LCLK0(1:0) LCLK0 Output Clock Rate

Note: This option is valid only when LCLK0 is output. When LCLK0 is input the frequency is determined externally.

00 = 2.048 MHz (default)

01 = 4.096 MHz

10 = 8.192 MHz

11 = 16.384 MHz

6.2.6.11 LCLK1 Control Register

LCLK1 Control Register (GLCLK1) read/write Address: $D08B_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	LCLK1EN	LCLK1(1:0)	

Note: 'x' = unused bits, read as 0.

LCLK1EN LCLK1 Output Enable

0 = LCLK1 is input (default)

1 = LCLK1 is driven outward via LCLK1 pin

LCLK1(1:0) LCLK1 Output Clock Rate

Note: This option is valid only when LCLK1 is output. When LCLK1 is input the frequency is determined externally.

00 = 2.048 MHz (default)

01 = 4.096 MHz

10 = 8.192 MHz

11 = 16.384 MHz

6.2.6.12 LCLK2 Control Register

LCLK2 Control Register (GLCLK2) read/write Address: $D08C_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	LCLK2EN	LCLK2(1:0)	

Note: 'x' = unused bits, read as 0.

LCLK2EN LCLK2 Output Enable

0 = LCLK2 is input (default)

1 = LCLK2 is driven outward via LCLK2 pin

LCLK2(1:0) LCLK2 Output Clock Rate

Note: This option is valid only when LCLK2 is output. When LCLK2 is input the frequency is determined externally.

00 = 2.048 MHz (default)

01 = 4.096 MHz

10 = 8.192 MHz

11 = 16.384 MHz

6.2.6.13 LCLK3 Control Register

LCLK3 Control Register (GLCLK3) read/write Address: $D08D_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	LCLK3EN	LCLK3(1:0)	

Note: 'x' = unused bits, read as 0.

LCLK3EN LCLK3 Output Enable

0 = LCLK3 is input (default)

1 = LCLK3 is driven outward via LCLK3 pin

LCLK3(1:0) LCLK3 Output Clock Rate

Note: This option is valid only when LCLK3 is output. When LCLK3 is input the frequency is determined externally.

00 = 2.048 MHz (default)

01 = 4.096 MHz

10 = 8.192 MHz

11 = 16.384 MHz

6.2.6.14 Muxes Control Register

MUXCTRL Register **OAK:** read/write Address: $D14A_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	PMUX1	PMUX0	IMUX

IMUX

0 = IOM-2000 pins are used for the IOM-2000 interface

1 = IOM-2000 pins are used for the GHDLC cha. 1

PMUX0

0 = PCM ports 0 & 2 pins are used for PCM

1 = PCM ports 0 & 2 pins are used for GHDLC cha. 2

PMUX1

0 = PCM ports 1 & 3 pins are used for PCM

1 = PCM ports 1 & 3 pins are used for GHDLC cha. 3

6.2.7 DCU Register Description

6.2.7.1 Interrupt Mask Register

IMASK Register read/write Address: $D002_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	IMASK

IMASK GHDLC Interrupt Mask

0 = GHDLC interrupt disabled

1 = GHDLC interrupt enabled

Note: The unused bits (x) are read as '0'.

6.2.7.2 Status Event Register

STEVE Register read Address: $D003_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	PFS	FSC	FP

PFS PFS Status Bit

0 = normal operation

1 = PFS rising edge has occurred (reset by DSP read access)

FSC FSC Status Bit

0 = normal operation

1 = FSC rising edge has occurred (reset by DSP read access)

FP FSC & PFS Status Bit

0 = normal operation

1 = Both FSC and PFS rising edges have occurred, i.e. bits PFS and FSC are set (reset by DSP read access)

Note: Unused bits ('x') are read as '0'.

6.2.7.3 Statistics Counter Register

STATC Register read/write Address: $D004_H$

Reset value: unchanged

Reset value: unchanged upon chip reset, but reset upon FSC detection if STATC was read by the DSP since last occurence of FSC.

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
STATC(7:0)							

STATC (7:0) Statistics Counter Value

Note: The unused bits (x) are read as '0'.

6.2.7.4 Statistics Register

STATI Register read/write Address: $D005_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
MSC(7:0)							

MSC(7:0) Max. Statistics Count

Note: The unused bits (x) are read as '0'.

6.2.8 µP Configuration Registers

6.2.8.1 µP Interface Configuration Register

MCFG Register

DSP: read
µP: read/write

DSP Address: $D148_H$
µP high address: none
µP low address: 48_H

Reset value: 00_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	MODE

7	6	5	4	3	2	1	0
DRQLV	IRQLV	IRQMO	IMASK	IACK	PEC	FB	DMA

DMA DMA Mode Enabled

0 = No DMA

1 = DMA enabled

FB Fly-by Mode

0 = Memory-to-memory mode used for DMA transfers

1 = Fly-by mode used for DMA transfers

PEC PEC Transfers Enable

0 = No PEC Transfers

1 = PEC transfers are supported (for connection of C16x µP)

IACK Interrupt Acknowledge Mode

0 = Interrupt vector is provided to CPU after 1st IACK pulse.

1 = Interrupt vector is provided to CPU after 2nd IACK pulse.

IMASK Interrupt Mask

0 = IREQ pin is disabled

1 = IREQ pin is enabled

IRQMO IREQ Pin Mode

0 = Open-drain mode

1 = Push-pull mode

IRQLV IREQ Pin Level

0 = Low active

1 = High active

DRQLV DREQR/DREQT Pins Level

0 = High active

1 = Low active

MODE µP Interface Mode

Contains the value of MODE input pin sampled by rising edge of $\overline{\text{RESET}}$

Note: This signal is hardwired.

0 = Intel/Siemens mode

1 = Motorola mode

6.2.8.2 Device Version Register

VDEV Register µP: read µP address: $6A_H$

Reset value: none (hardwired)

7	6	5	4	3	2	1	0
VDEV(7:0)							

VDEV Device Version
Contains the information about the device status.

1_H DELIC Version 1.1

2_H DELIC Version 2.1

6.2.8.3 Interrupt Vector Register

IVEC Register DSP: read/ write
µP: read
DSP Address: $D168_H$
µP high address: none
µP low address: 68_H

Reset value: unchanged

7	6	5	4	3	2	1	0
IVEC(7:0)							

IVEC7..0 Interrupt vector
Contains the interrupt vector address that is output during an INTA cycle of the µP

6.2.9 µP Mailbox Registers Description

6.2.9.1 µP Command Register

MCMD Register

DSP: read
µP: write

DSP address: $D140_H$
µP address: 40_H

Reset value: 00_H

7	6	5	4	3	2	1	0
MCMD							

MCMD µP Command

Contains the µP command (8-bit opcode) to the DELIC.

6.2.9.2 µP Mailbox Busy Register

MBUSY Register

DSP: write
µP: read

DSP Address: $D141_H$
µP high address: 41_H
µP low address: none

Reset value: 00_H

15	14	13	12	11	10	9	8
MBUSY	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

MBUSY µP Mailbox Busy Bit

0 = Mailbox is available for the external µP. The µP may write a command to MCMD.

1 = Mailbox is blocked for the external µP. The µP may not write a command to MCMD.

Note: MBUSY is automatically set each time a command is written to MCMD by the µP.
MBUSY is reset automatically by a direct OAK write operation to the MBUSY register.

6.2.9.3 µP Mailbox Generic Data Register

MGEN Register

DSP: read	DSP Address: $D144_H$
	DSP high: $D143_H$
	DSP low: $D142_H$
µP: write	µP high: 43_H
	µP low: 42_H

Reset value: unchanged

15	14	13	12	11	10	9	8
MGEN(15..8)							

7	6	5	4	3	2	1	0
MGEN(7..0)							

MGEN (15..0) µP Mailbox Generic Data (16 bits)

6.2.9.4 µP Mailbox (General and DMA Mailbox) Data Registers

MDTn Register (n=0..7) DSP: read Addr. see table on page 6-6
TDTn/ MDTn+8 Register (n=0..7) µP: write

Reset value: unchanged

15	14	13	12	11	10	9	8
MDTn(15..8)							

7	6	5	4	3	2	1	0
MDTn(7..0)							

MDTn (15..0) µP Mailbox Data (each byte is addressed seperately by the external µP)

Note: The 16 data registers (MDT1..7, TDT0/MDT8..TDT7/MDT15) have the same structure. The addresses are displayed in the register map (page 6-6, page 6-7).

6.2.9.5 DSP Command Register

OCMD Register DSP: write DSP address: $D160_H$
µP: read µP address: 60_H

Reset value: 00_H

7	6	5	4	3	2	1	0
OCMD							

OCMD DSP Command

Contains the DSP command/ indication (8-bit opcode) to the DELIC.

6.2.9.6 DSP Mailbox Busy Register

OBUSY Register

DSP: read
µP: read/ write

DSP Address: $D161_H$
µP high address: 61_H
µP low address: none

Reset value: 00_H

15	14	13	12	11	10	9	8
OBUSY	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x

OBUSY DSP Mailbox Busy Bit

0 = Mailbox is available for the DSP. The DSP may write a command/ indicationto OCMD.

1 = Mailbox is blocked for the DSP. The DSP may not write a command/ indication to OCMD.

Note: OBUSY is automatically set each time a command/ indication is written to OCMD by the DSP.
OBUSY is reset automatically by a direct µP write operation to the OBUSY register

6.2.9.7 DSP Mailbox Generic Data Register

OGEN Register	DSP: write	DSP address: $D164_H$ DSP high: $D163_H$ DSP low: $D162_H$
	µP: read	µP high: 63_H µP low: 62_H

Reset value: unchanged

15	14	13	12	11	10	9	8
OGEN(15..8)							

7	6	5	4	3	2	1	0
OGEN(7..0)							

OGEN 15..0 DSP Mailbox Generic Data (16 bits)

6.2.9.8 DSP Mailbox (General and DMA Mailbox) Data Registers

ODTn Register (n= 0..15) **RDTn/ ODTn+8 Register (n=0..7)**	DSP: write µP: read	Addr. see table on page 6-7

Reset value: unchanged

15	14	13	12	11	10	9	8
ODTn(15..8)							

7	6	5	4	3	2	1	0
ODTn(7..0)							

ODTn (15..0) DSP Mailbox Data (each byte is addressed seperately by the external µP)

Note: The 16 data registers (ODT1..7, RDT0/ODT8..RDT7/ODT15) have the same structure. The addresses are displayed in the register map (page 6-6, page 6-7).

6.2.10 DMA Mailbox Registers Description

6.2.10.1 DMA Mailbox Transmit Counter Register

DTXCNT Register **DSP:** read/write Address: $D150_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	TXCNT(3:0)			

Note: Writing to TXCNT initiates a DMA transfer of TXCNT bytes to the DMA Tx Mailbox. This register value does not change during the current transfer.

6.2.10.2 DMA Mailbox Receive Counter Register

DRXCNT Register **DSP:** read/write Address: $D170_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	RXCNT(3:0)			

Note: Writing to RXCNT initiates a DMA transfer of RXCNT bytes to the DMA Rx Mailbox. This register value does not change during the current transfer.

6.2.10.3 DMA Mailbox Interrupt Status Register

DINSTA Register **DSP:** read Address: $D152_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	INSTA(3:0)			

Contains the status of the DMA Mailbox.

6.2.11 Clock Generator Register Description

6.2.11.1 PDC Control Register

PDC Control Register (CPDC) read/write Address: $D080_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	PDC(1:0)	

Note: 'x' = unused bits, read as 0.

PDC(1:0) PDC Frequency Selection (Only in Master Mode when PDC is output)

00 = PDC = 2.048 MHz (default)

01 = PDC = 4.096 MHz

10 = PDC = 8.192 MHz

11 = PDC = 16.384 MHz

6.2.11.2 PFS Control Register

PFS Control Register (CPFS) read/write Address: $D081_H$

Reset value: 0001_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	PFS

Note: 'x' = unused bits, read as 0.

PFS PFS Frequency Selection
(Selectable in Slave mode when PFS is input; in Master mode PFS = 8 kHz)

0 = PFS = 4 kHz

1 = PFS = 8 kHz (default)

Note: When the PFS is output, its frequency is always 8 kHz, therefore this bit should be left in its reset-value ('1') and not to be changed.
The direction of PFS and PDC: input (slave) or output (master) is determined by the Master/Slave strap (DREQR pin) during reset.

6.2.11.3 CLKOUT Control Register

CLKOUT Control Register (CLKOUT) read/write Address: $D082_H$

Reset value: 0008_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	CLKOUTEN	CLKOUT		

Note: 'x' = unused bits, read as 0.

CLKOUTEN CLKOUT Pin Enable

0 = CLKOUT pin is in tri-state.

1 = CLKOUT pin is active. (default)

CLKOUT CLKOUT Pin Frequency

000 = 2.048 MHz (default)

001 = 4.096 MHz

010 = 8.192 MHz

011 = 15.36 MHz

100 = 16.384 MHz

6.2.11.4 DCXO Reference Clock Select Register

REFSEL Register (CREFSEL) read/write Address: $D083_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	REFSEL EN	REFSEL(2:0)		

Note: 'x' = unused bits, read as 0

This register controls the selection of the source of the DCXO 8kHz reference clock

REFSELEN DCXO Reference Clock Enable

0 = The reference clock is disabled (default)

1 = The reference clock is enabled

REFSEL(2:0) DCXO Reference Clock Select

000 = DXCLK/192 (default)

001 = XCLK/256

010 = XCLK

011 = REFCLK (when input)

100 = REFCLK (when input)/64

101 = PFS (when input)

6.2.11.5 REFCLK Control Register

REFCLK Control Register (CREFCLK) read/write Address: $D084_H$

Reset value: 0003_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	REFCLKEN	REFDIV(2:0)		

Note: 'x' = unused bits, read as 0.

REFCLK may be configured as an input or as an output. When configured as an input, it may be used as a source for the on-chip DCXO 8kHz reference clock. This option is handled by the DCXO Reference Clock Select Register (CREFSEL).

When configured as an output it is derived from XCLK input pin. In order to drive REFCLK, XCLK may be divided by 256, 192, 4, 3 or 1.

REFCLKEN REFCLK Pin Output Enable

0 = REFCLK is input, the pad is not output enabled

1 = REFCLK is output

REFDIV(2:0) REFCLK Pin Output Divider Selection

This determines the value by which the XCLK maximum clock of 2.048 MHz is divided internally.

000 = Division by 256

001 = Division by 192

010 = Division by 4

011 = Division by 3 (default)

100 = Division by 1

6.2.11.6 DCL_2000 Control Register

DCL_2000 Control Register (CDCL2) read/write Address: $D085_H$

Reset value: 0004_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	DCL2EN	DCL2(1:0)	

Note: 'x' = unused bits, read as 0.

DLC2EN DCL_2000 Clock Enable

0 = DCL_2000 clock is disabled

1 = DCL_2000 clock is enabled (default)

DCL2(1:0) DCL_2000 Clock Rate

00 = 3.072 MHz (default)

01 = 6.144 MHz

10 = 12.288 MHz

6.2.11.7 DCL Control Register

DCL Control Register (CDCL) read/write Address: $D086_H$

Reset value: $000B_H$

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	DCLEN	DCL(2:0)		

Note: 'x' = unused bits, read as 0.

DCLEN DCL Clock Enable

0 = DCL is disabled

1 = DCL is enabled (default)

DCL(2:0) DCL Clock Rate

000 = 384 kHz

001 = 768 kHz

010 = 1536 kHz

011 = 2048 kHz (default)

100 = 4096 kHz

6.2.11.8 FSC Control Register

FSC Control Register (CFSC) read/write Address: $D087_H$

Reset value: 0002_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	IFSCD	EFSC	FSCEN	FSCSH

Note: 'x' = unused bits, read as 0.

FSCEN FSC Clock Enable

0 = FSC is disabled (stuck at '0')

1 = FSC is enabled (default)

FSCSH Short FSC Pulse

0 = The next FSC pulse will be longer than 2 DCL cycles (default)

1 = The next FSC pulse will be shorter than 2 DCL cycles (short FSC)

EFSCD External FSC Delay

0 = no delay between FSC and DCL rising edge

1 = FSC rising edge is delayed by one CLK61 clock (16 ns) relative to DCL/ DCL2000

IFSCD Internal FSC Delay (only valid of CSTRAP: bit0 = 1)

0 = no delay between FSC and DCL rising edge

1 = FSC rising edge is delayed by one CLK61 clock (16 ns) relative to DCL/ DCL2000

Note: If only one short FSC pulse is needed, this bit should be reset to '0' by the DELIC software, after the next FSC rising edge detection (after the begining of the next frame). It is not executed automatically by the hardware.

6.2.11.9 L1_CLK Control Register

L1_CLK Control Register (CL1CLK) read/write Address: $D088_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x	x	x	L1CLKDIS	L1CLK

Note: 'x' = unused bits, read as 0.

L1CLKEN L1_CLK Disable

0 = L1_CLK is enabled (default)

1 = L1_CLK is disabled

L1CLK L1_CLK Clock Rate

0 = 7.68 MHz (default)

1 = 15.36 MHz

6.2.11.10 PFS Sync Register

PFS Sync Register (CPFSSY) read/write Address: $D089_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
x	x	x	x	x	x	x	x

7	6	5	4	3	2	1	0
x	x	x	x			PFSSYNC(1:0)	

Note: 'x' = unused bits, read as 0.

During read cycle the 2 LSBs are driven by the the PFS-sync state-machine's state bits. This is needed only for testing.

The PFS-sync Signal actually resets the 61.44 MHz-Clock-division-Chain. The PFS-sync signal activated with the PFS-rising edge detection, but only when the internal-reset is activated or after a "PFS-sync" instruction was carried out by the OAK. The goal of reseting the 61.44MHz-Clock-division-Chain by PFS-sync, is to lead to a situation in which FSC rises with PFS. After the initial reset by the PFS-sync a small- and flexible phase difference is maintained by the DCXO-PLL. A write access to PFS-Sync Register, resets the 61MHz clock-division chain, including FSC, by the next PFS rising-edge detection. This is true only if the write access was carried-out before the falling edge of PFS. If the write-access comes after the falling edge of PFS, the acctuall sync operation will not be carried out by the next PFS rising-edge, but with one that will come after it. The written value does not make any difference.

6.2.11.11 Realtime Counter Register

RT Counter Register (CRTCNT) read Address: $D08E_H$

Reset value: 0000_H

15	14	13	12	11	10	9	8
RTCOUNT(15:8)							

7	6	5	4	3	2	1	0
RTCOUNT(7:0)							

This 18-bit counter counts 8 kHz cycles. It is used by the software to time the handling of required tasks. One period of the counter (counting from 0000H to FFFFH and back

to 0000H) is 32.768 sec. Only the 16 MSBs of the counter may be read by the OAK, therefore the actuall resolution is 0.5 ms. .

RTCOUNT(15:0) The 16 MSBs of the realtime counter

6.2.11.12 Strap Status Register

Strap Status Register (CSTRAP) read/ write Address: $D08F_H$

Reset value: xxxx xxxx xxxx $xx10_B$

15	14	13	12	11	10	9	8
x	x	x	x	x	STRAP(10:8)		

7	6	5	4	3	2	1	0
STRAP(7:0)							

Note: 'x' = unused bits, read as 0.

STRAP (10:0) This register enables the OAK to read the straps values, as sampled during reset

bit 10 PCM Clock Master Strap

bit 9:7 Test Mode Strap

bit 6 Emulation Boot Strap

bit 5 $\overline{\text{PLL Bypass}}$ Strap

bit 4 $\overline{\text{DSP PLL Power-Down}}$ Strap

bit 3 $\overline{\text{Boot}}$ Strap

bit 2 $\overline{\text{Reset counter Bypass}}$ Strap

bit 1 DCXO Fast-Synchronization Enable

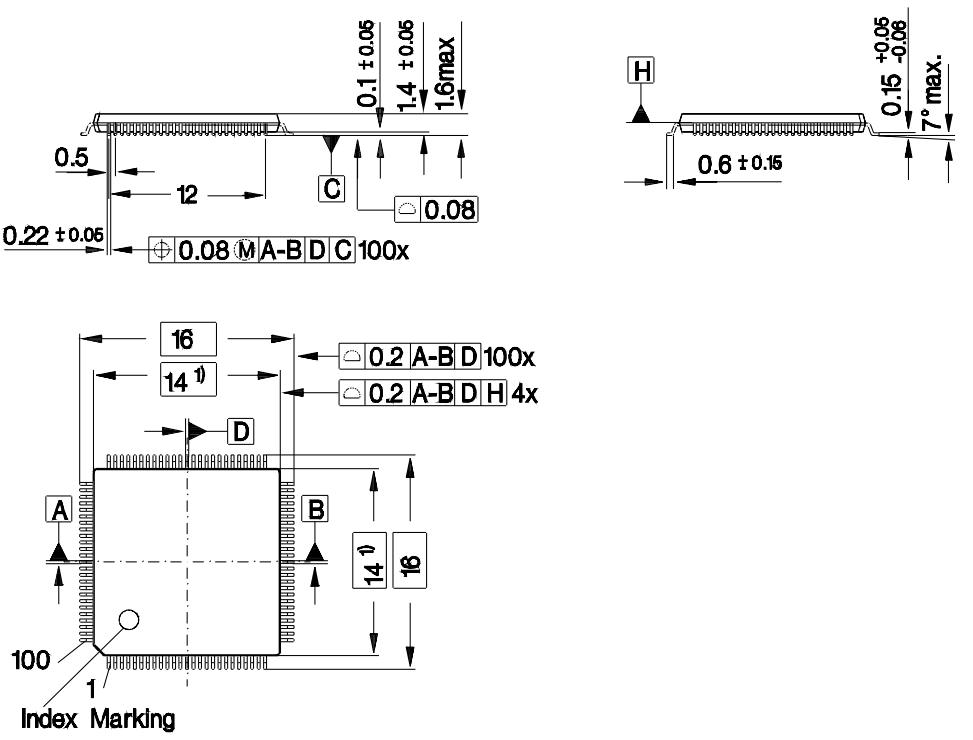
0 = Linear (slow) synchronization (for DECT applications)
1 = Fast synchronization (default)

bit 0 Internal Source Clock Strap

0 = PFS, PDC, DCL, FSC, DCL2000 are delayed by some ns (default)
1 = PFS, PDC, DCL, FSC, DCL2000 are not delayed

7 Package Outlines

P-TQFP-100-1
(Plastic Thin Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05247

Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

8 Electrical Characteristics

8.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Storage temperature	T_{stg}	– 65 to 150	°C
IC supply voltage	V_{DD}	– 0.3 to 4.6	V
DC input voltage (except I/Os)	V_I	– 0.3 to 6.0	V
DC output voltage (including I/Os); output in high or low state	V_O	– 0.3 to V_{DD} + 0.3	V
DC output voltage (including I/Os); output in tri-state	V_I, V_O	– 0.3 to 6.0	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	1000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993. The Pins (TBD) are not protected against voltage stress > (TDB) V (versus V_S or GND). The (TBD) performance prohibits the use of adequate protective structures.

Note: ***Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.***

8.2 Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Power Supply Voltage	V_{DD}	3.13	3.47	V
Ground	V_{SS}	0	0	V
Voltage applied to input pins	V_{IN}	0	5.5	V
Voltage applied to output or I/O pins outputs enabled outputs high-Z	 V_{OUT} V_{OUT}	 0 0	 V_{DD} 5.5	 V V
Operating temperature PEB PEF	T_A T_A	0 -40	70 85	°C °C
Input transition rise or fall time	Δt/Δv	0	10	ns/V

Note: In the operating range, the functions given in the circuit description are performed.

8.3 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
High-Level Input Voltage	V_{IH}	2.0	V_{DD} + 0.3	V	V_{OUT} >= V_{OH} (min)
Low-Level Input Voltage	V_{IL}	– 0.3	0.8	V	V_{OUT} <= V_{OL} (max)
High-Level Output voltage (all pins except DD0, DD1, DX, LTxD0, TxD0, TxD1)	V_{OH}	2.4		V	V_{DD} = min, I_{OH} = – 2 mA
Low-Level Output voltage (all pins except DD0, DD1, DX, LTxD0, TxD0, TxD1)	V_{OL}		0.4	V	V_{DD} = min, I_{OL} = 2 mA
High-Level Output voltage (pins DD0, DD1, DX, LTxD0, TxD0, TxD1)	V_{OH}	2.4		V	V_{DD} = min, I_{OH} = – 7 mA
Low-Level Output voltage (pins DD0, DD1, DX, LTxD0, TxD0, TxD1)	V_{OL}		0.4	V	V_{DD} = min, I_{OL} = 7 mA
Input leakage current	I_{IL}		1	µA	V_{DD} = 3.3 V, GND = 0 V; all other pins are floating; V_{IN} = 0 V
Output leakage current	I_{OZ}		1	µA	V_{DD} = 3.3 V, GND = 0 V; V_{OUT} = 0 V
Avg. power supply current	I_{CC} (AV)		TBD	mA	V_{DD} = 3.3 V, T_A = 25 °C: PDC = 8 MHz DSP @ 61.44 MHz

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

8.4 Capacitances

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Input Capacitance I/O Capacitance	C_{IN} $C_{I/O}$		7 7	pF pF	f_C = 1 MHz, The pins, which are not under test, are connected to GND
Output Capacitance	C_{OUT}		10	pF	
Crystal input capacitance (pin CLK16-XI)	C_{XIN}		3.3 (TBD)	pF	
Crystal output capacitance (pin CLK16-XO)	C_{XOUT}		3.3 (TBD)	pF	

8.5 Recommended 16.384 MHz Crystal Parameters

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Motional Capacitance	C_1	25		fF	
Shunt Capacitance	C_0	7		pF	
External Load Capacitance	C_L	≤15		pF	
Resonance Resistance	R_r	≤30		Ω	
Frequency Calibration Tolerance		≤150		ppm	

9 Timing Diagrams

9.1 General

For TTL and CMOS voltage levels refer to the relevant JEDEC specifications, e.g. to JEDEC8-A for 3V/3.3V devices which are 5V compatible.

Note: The complete AC characteristics will be provided after the electrical characterization of the device.
All timing shown are preliminary.

9.2 µP Access Timing

µP accesses of the DELIC are performed by an activation of the address and $\overline{CS}$.

- By driving the MODE pin ‘high’ the user selects Motorola mode, by driving it ‘low’ - Intel/Infineon mode. The pin is sampled during the rising edge of $\overline{RESET}$.
- In Intel/Infineon mode, a distinction is needed between working in multiplexed address/data bus mode and de-multiplexed address and data bus mode. In Motorola Mode, only de-multiplexed buses are used. The selection between multiplexed and de-multiplexed bus configurations is done by using the ALE pin.

9.2.1 µP Access Timing in Motorola mode

In this mode R/$\overline{W}$ distinguishes between Read and Write interactions, and $\overline{DS}$ is used for timing.

Table 9-1 Timing For Write Cycle In Motorola Mode

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
R/$\overline{W}$ setup time before $\overline{DS}$ x $\overline{CS}$ rising edge	t_{SRWS}	15		ns	Output load capacity of 50 pF
R/$\overline{W}$ hold time after $\overline{DS}$ x $\overline{CS}$ rising edge	t_{HRWS}	5		ns	
A-bus setup time before $\overline{DS}$ x $\overline{CS}$ rising edge	t_{SAS}	15		ns	
A-bus hold time after $\overline{DS}$ x $\overline{CS}$ rising edge	t_{HAS}	5		ns	
D-bus setup time before $\overline{DS}$ x $\overline{CS}$ rising edge	t_{SDS}	12		ns	
D-bus hold time after $\overline{DS}$ x $\overline{CS}$ rising edge	t_{HDS}	10		ns	
$\overline{DS}$ X $\overline{CS}$ pulse width	t_{WS}	15		ns	

Note: $\overline{DS}$ X $\overline{CS}$ is active (low) when both, $\overline{DS}$ and $\overline{CS}$, are active (low)

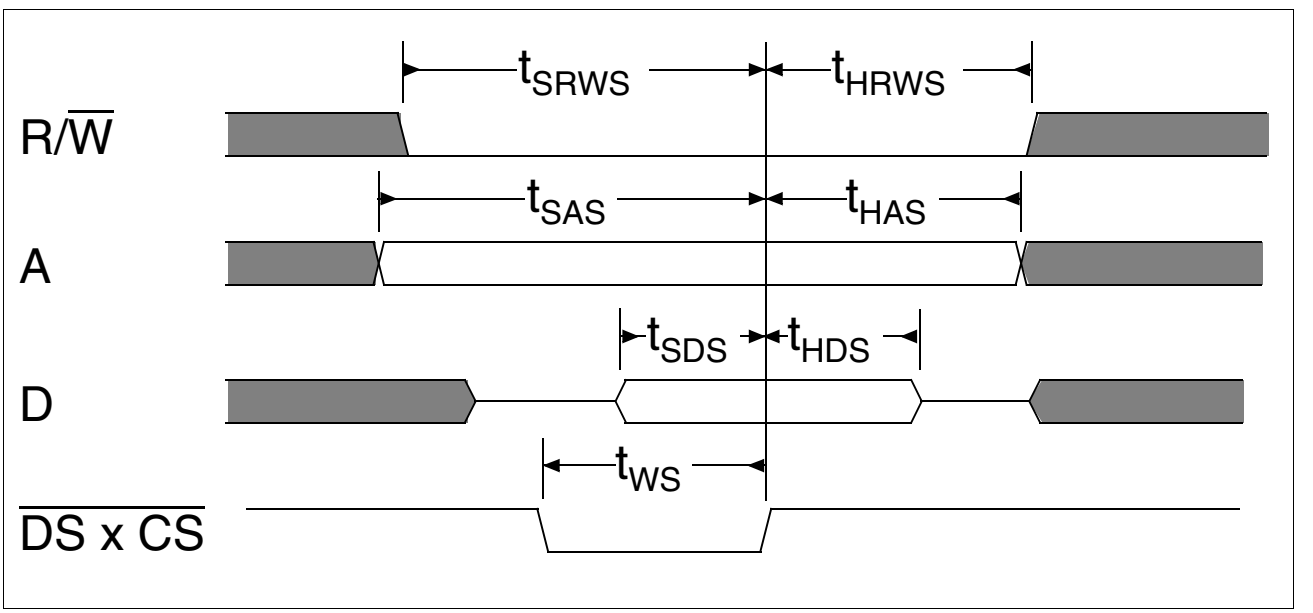


Figure 9-1 Write Cycle in Motorola Mode

Table 9-2 Timing For Read Cycle In Motorola Mode

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
R/$\overline{W}$ setup time before $\overline{DS\ X\ CS}$ falling edge	t_{SRWS}	0		ns	Output load capacity of 50 pF
R/$\overline{W}$ hold time after $\overline{DS\ X\ CS}$ rising edge	t_{HRWS}	5		ns	
A-bus valid to D-bus valid	t_{DAD}	0	20	ns	
$\overline{DS\ X\ CS}$ falling edge to D-bus	t_{DSD}	0	20	ns	
D-bus float after $\overline{DS\ X\ CS}$ rising edge	t_{DSDH}	0	15	ns	

Note: $\overline{DS\ X\ CS}$ is active (low) when both, $\overline{DS}$ and $\overline{CS}$ are active (low)

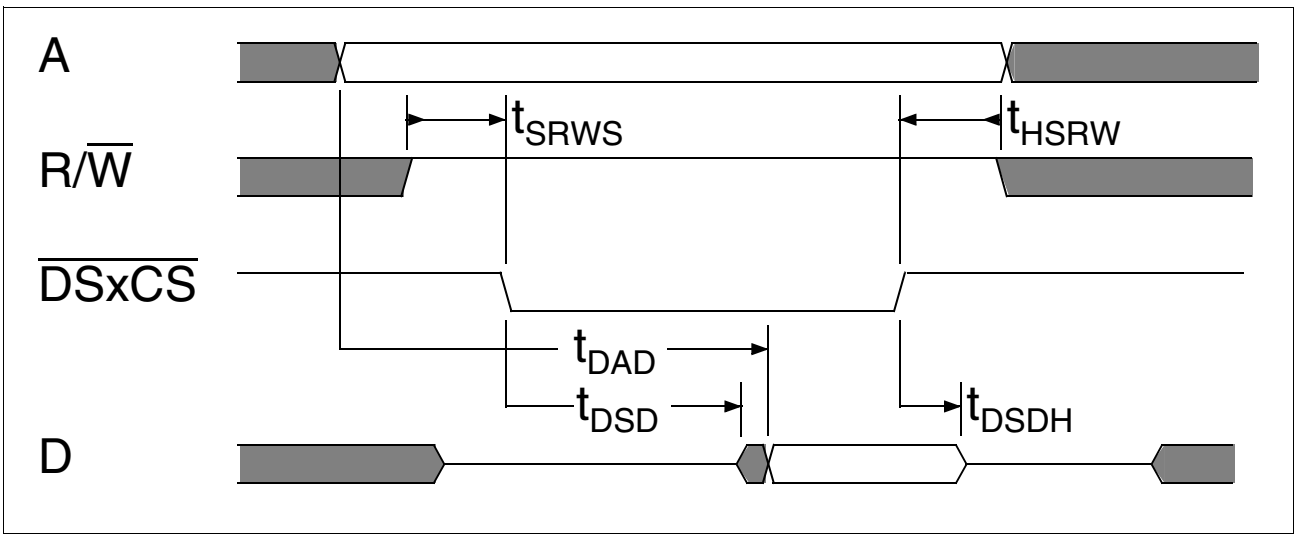


Figure 9-2 Read Cycle in Motorola Mode

9.2.2 µP Access Timing in Intel/Infineon Mode

In this mode driving $\overline{RD}$ ‘low’ causes a read access, driving $\overline{WR}$ ‘low’ causes a write access.

Timing for Demultiplexed Bus

In de-multiplexed bus configuration, ALE must be driven ‘high’.

Table 9-3 Timing For Write Cycle In Intel/Infineon Demultiplexed Mode

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
A-bus setup time before $\overline{WR}$ rising edge	t_{SAW}	12		ns	Output load capacity of 50 pF
A-bus hold time after $\overline{WR}$ rising edge	t_{HAW}	5		ns	
$\overline{CS}$ setup time before $\overline{WR}$ rising edge	t_{SCW}	12		ns	
$\overline{CS}$ hold time after $\overline{WR}$ rising edge	t_{HCW}	5		ns	
D-bus setup time before $\overline{WR}$ rising edge	t_{SDW}	12		ns	
D-bus hold time after $\overline{WR}$ rising edge	t_{HDW}	10		ns	
$\overline{WR}$ pulse width	t_{WW}	15		ns	

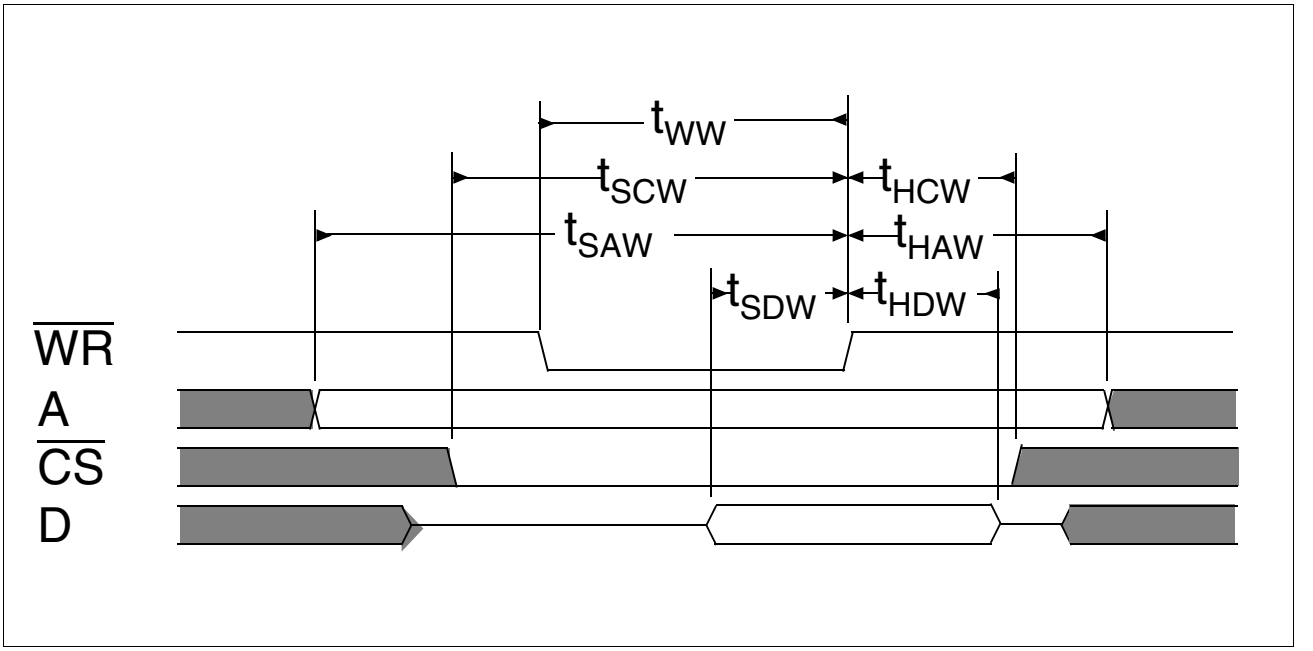


Figure 9-3 Write Cycle in Intel/Infineon De-multiplexed Mode

Table 9-4 Timing For Read Cycle In Intel/Infineon De-multiplexed Mode

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
A-bus valid to D-bus valid	t_{DAD}	0	20	ns	Output load capacity of 50 pF
$\overline{RD\ X\ CS}$ falling edge to D-bus	t_{DRD}	0	20	ns	
D-bus float after $\overline{RD\ X\ CS}$ rising edge	t_{DRDH}	0	15	ns	

Note: $\overline{RD\ X\ CS}$ is active (low) when both $\overline{RD}$ and $\overline{CS}$ are active (low)

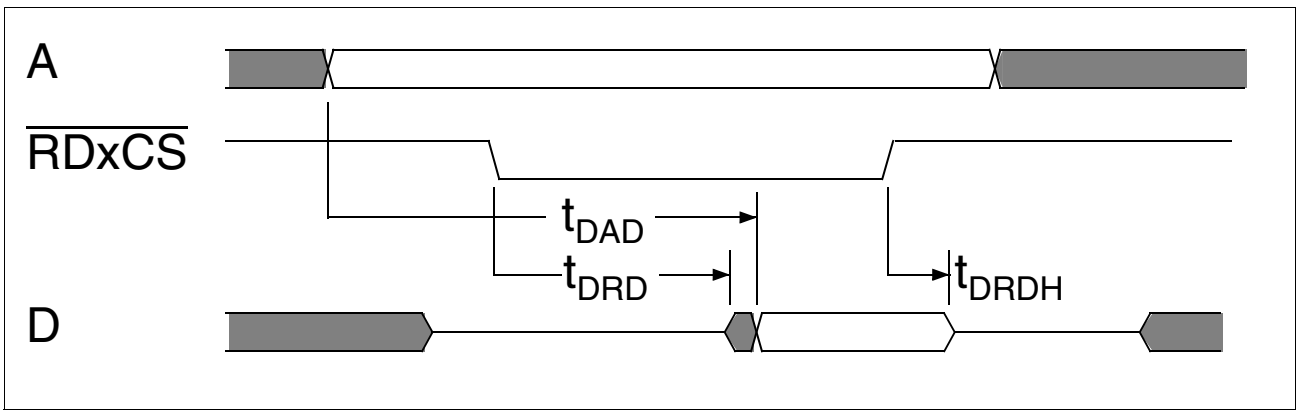


Figure 9-4 Read Cycle in Intel/Infineon De-multiplexed Mode

Timing for Multiplexed Bus

In this mode the ALE pin is used to lock the address send via the multiplexed A/D bus.

Table 9-5 Timing For Write Cycle In Intel/Infineon Multiplexed Mode

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
A-bus setup time before ALE falling edge	t_{SAL}	12		ns	Output load capacity of 50 pF
A-bus hold time after ALE falling edge	t_{HAL}	5		ns	
ALE pulse width	t_{WL}	10		ns	
$\overline{CS}$ setup time before $\overline{WR}$ rising edge	t_{SCW}	12		ns	
$\overline{CS}$ hold time after $\overline{WR}$ rising edge	t_{HCW}	5		ns	
D-bus setup time before $\overline{WR}$ rising edge	t_{SDW}	12		ns	
D-bus hold time after $\overline{WR}$ rising edge	t_{HDW}	10		ns	
ALE hold time after $\overline{WR}$ rising edge	t_{HLW}	5		ns	
$\overline{WR}$ pulse width	t_{WW}	15		ns	

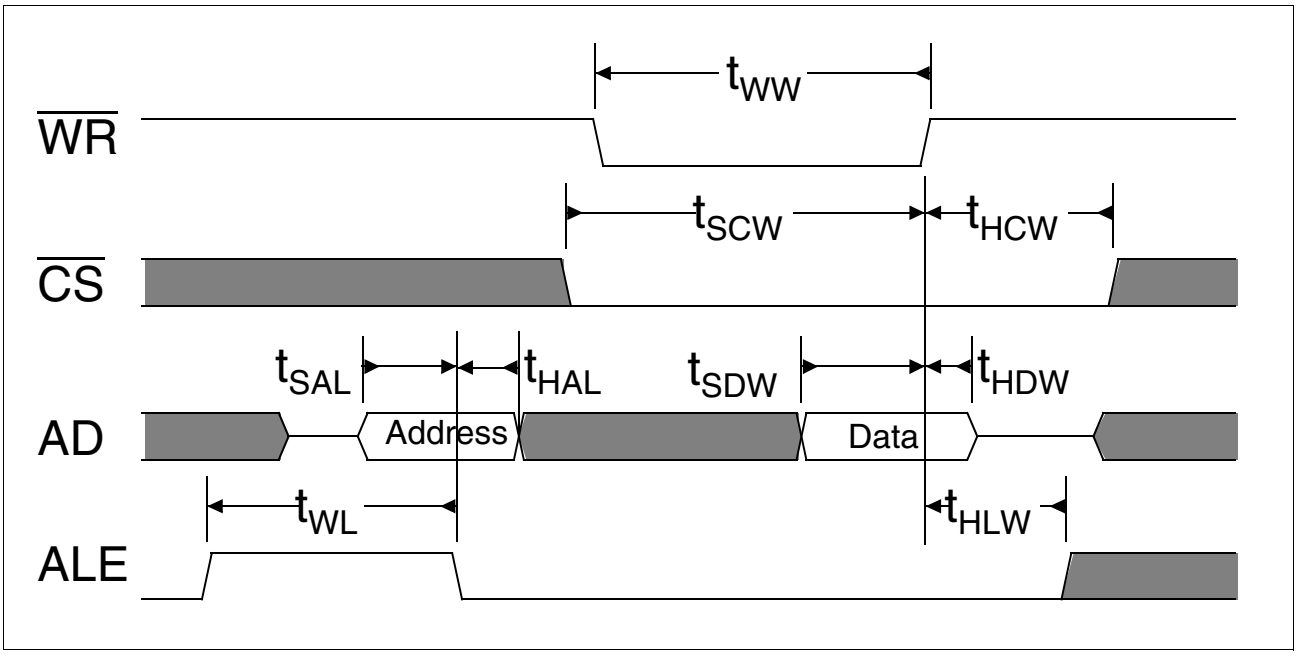


Figure 9-5 Write Cycle in Intel/Infineon Multiplexed Mode

Table 9-6 Timing For Read Cycle In Intel/Infineon Multiplexed Mode

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
ALE low before $\overline{\text{RD X CS}}$ falling edge	t_{HRL}	5		ns	Output load capacity of 50 pF
ALE hold time after $\overline{\text{RD X CS}}$ rising edge	t_{HLR}	5		ns	
ALE pulse width	t_{WL}	10		ns	
A-bus setup time before ALE falling edge	t_{SAL}	12		ns	
A-bus hold time after ALE falling edge	t_{HAL}	5		ns	
$\overline{\text{RD X CS}}$ falling edge to D-bus valid	t_{DRD}	0	20	ns	
D-bus float after $\overline{\text{RD X CS}}$ rising edge	t_{DRDH}	0	15	ns	

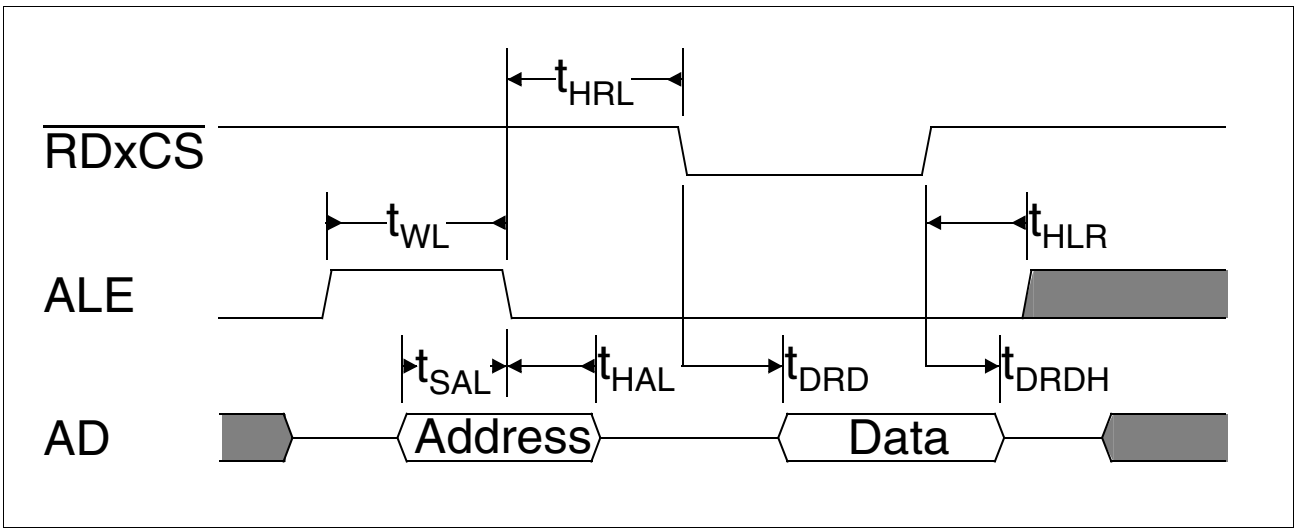


Figure 9-6 Read Cycle in Intel/Infineon Multiplexed Mode

9.3 Interrupt Acknowledge Cycle Timing

The IREQ (Interrupt REQuest) output signal of the DELIC is activated upon a DSP write operation to the OCMD register (OAK Mailbox command register). This operation sets the OAK Mailbox busy bit (OBUSY), which drives directly the IREQ output signal. The IREQ signal may be masked, by programming the MASK bit within the µP interface Control Register (UPCR).

The microprocessor may force the DELIC to drive the interrupt vector over the data bus by activation of the interrupt acknowledge input signal ($\overline{\text{IACK}}$).

In Motorola mode, an interrupt acknowledge cycle consists of one $\overline{\text{IACK}}$ pulse, during which the interrupt vector is issued by the DELIC. In Intel/Infineon mode, an interrupt acknowledge cycle consists of two $\overline{\text{IACK}}$ pulses. Note that the interrupt vector is issued as a response to the second pulse. The source of the vector is the OAK Mailbox interupt vector register (IVEC). The DSP determines the value stored in this register by a write operation.

IREQ is not deactivated by the $\overline{\text{IACK}}$ pulses directly, but by a µP write access to OBUSY.

Table 9-7 Interrupt Acknowledge Cycle Timing

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
D-bus valid after $\overline{\text{IACK}}$ falling edge	t_{DADV}	0	20	ns	Output load capacity of 50 pF
D-bus float after $\overline{\text{IACK}}$ rising edge	t_{DADT}	0	15	ns	
$\overline{\text{IACK}}$ pulse width	t_{WA}	25		ns	
Interval between two $\overline{\text{ACK}}$ pulses	t_{HA}	10[1)]		ns	

1) Valid only for Intel/Infineon mode.

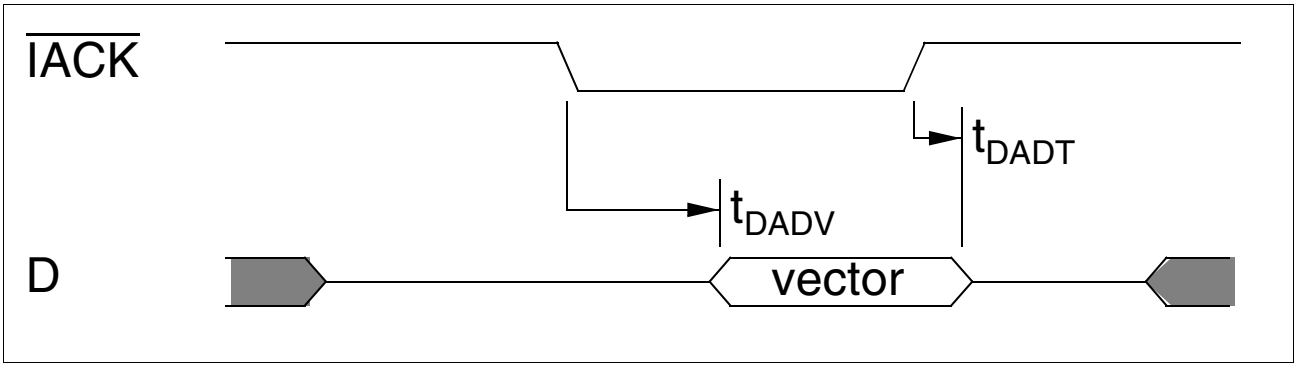


Figure 9-7 Interrupt Acknowledge Cycle Timing in Motorola Mode

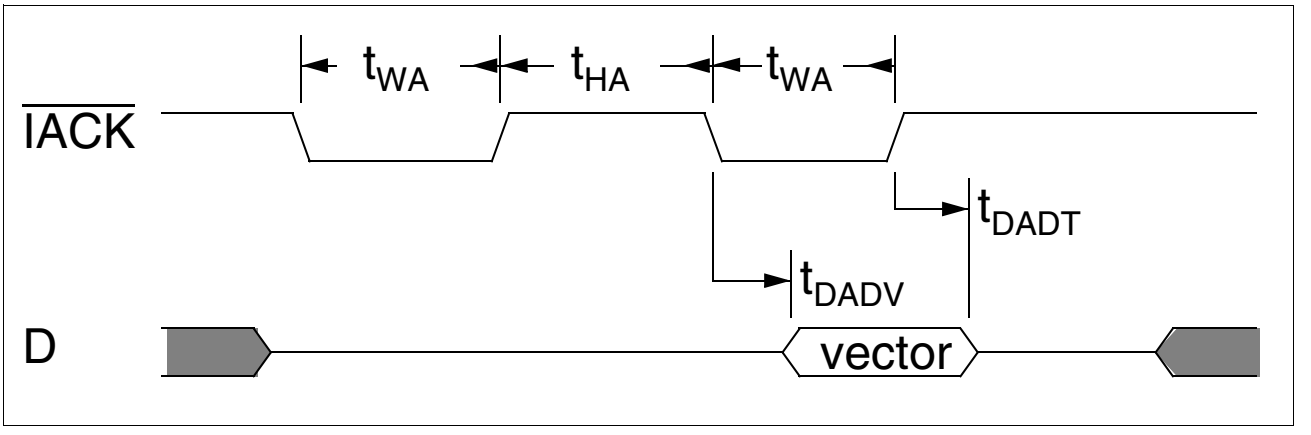


Figure 9-8 Interrupt Acknowledge Cycle Timing in Intel/Infineon Mode

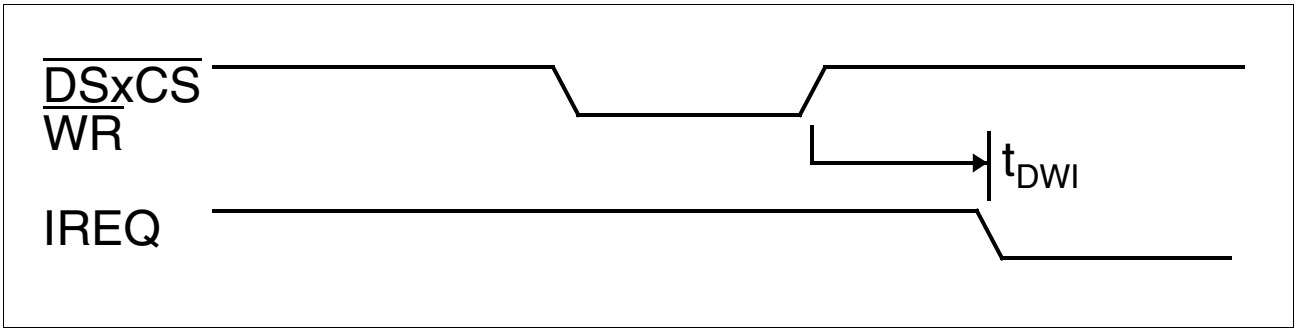


Figure 9-9 IREQ Deactivation Timing

Note: IREQ is deactivated due to µP write operation to OBUSY register. In Motorola mode DS and CS together time the write access. In Intel mode WR alone times the write access. For more details regarding the timing required during write access to the DELIC, refer to section 9.2. The other signals required for a write operation to OBUSY in each mode, are assumed to be driven.

9.4 DMA Access Timing

The exact behavior required from the µP interface signals during a DMA access depends on the following modes:

- Motorola or Intel Mode: Determined by the MODE input pin.
- Normal or 'fly-by' Mode: Programmable in the control register of the µP interface.

In any mode, the DACK input is used to indicate that this is a DMA transaction, and to select the DMA Mailbox. An activation via the CS signal is not required in such cases.

9.4.1 DMA Access Timing In Motorola Mode

In this mode DS is used for timing the access, while R/W is used to distinguish between DMA read transactions and DMA write transactions. The R/W input signal is used differently in normal mode and in fly-by mode. The next table shows how R/W should be used in each mode during DMA transactions:

Table 9-8 R/W Behavior During DMA Transactions in Normal and Fly-By Mode

Mode	R/W = '0'	R/W = '1'
Normal (Non-Fly-By)	Write DMA transaction. (A response to DMA transmitter request)	Read DMA transaction. (A response to DMA receiver request)
Fly-By	Read DMA transaction. (A response to DMA receiver request)	Write DMA transaction. (A response to DMA transmitter request)

In fly-by mode R/$\overline{W}$ is used inverted to the normal mode, since the same signal, R/$\overline{W}$, is required for concurrent accesses of an external memory device.

Table 9-9 DMA Transaction timing in Mototrola Mode

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
$\overline{DACK}$ setup time to $\overline{DS}$ falling edge	t_{SAS}	7		ns	Output load capacity of 50 pF
$\overline{DACK}$ hold time after $\overline{DS}$ rising edge	t_{HSA}	5		ns	
D-bus setup time to $\overline{DS}$ rising edge	t_{SDS}	5		ns	
D-bus hold time after $\overline{DS}$ rising edge	t_{HSD}	10		ns	
DREQT/DREQR delay after $\overline{DS}$ falling edge	t_{DSR}	0	36	ns	
R/$\overline{W}$ setup time to $\overline{DS}$ falling edge	t_{SRWS}	7		ns	
R/$\overline{W}$ hold time after $\overline{DS}$ rising edge	t_{HSRW}	5		ns	
$\overline{DS}$ pulse width and interval between $\overline{DS}$ pulses	t_{WS}	30		ns	
D-bus valid after $\overline{DS}$ falling edge	t_{DSDV}	0	22		
D-bus float (high impedance) after $\overline{DS}$ rising edge	t_{DSDT}	0	15		

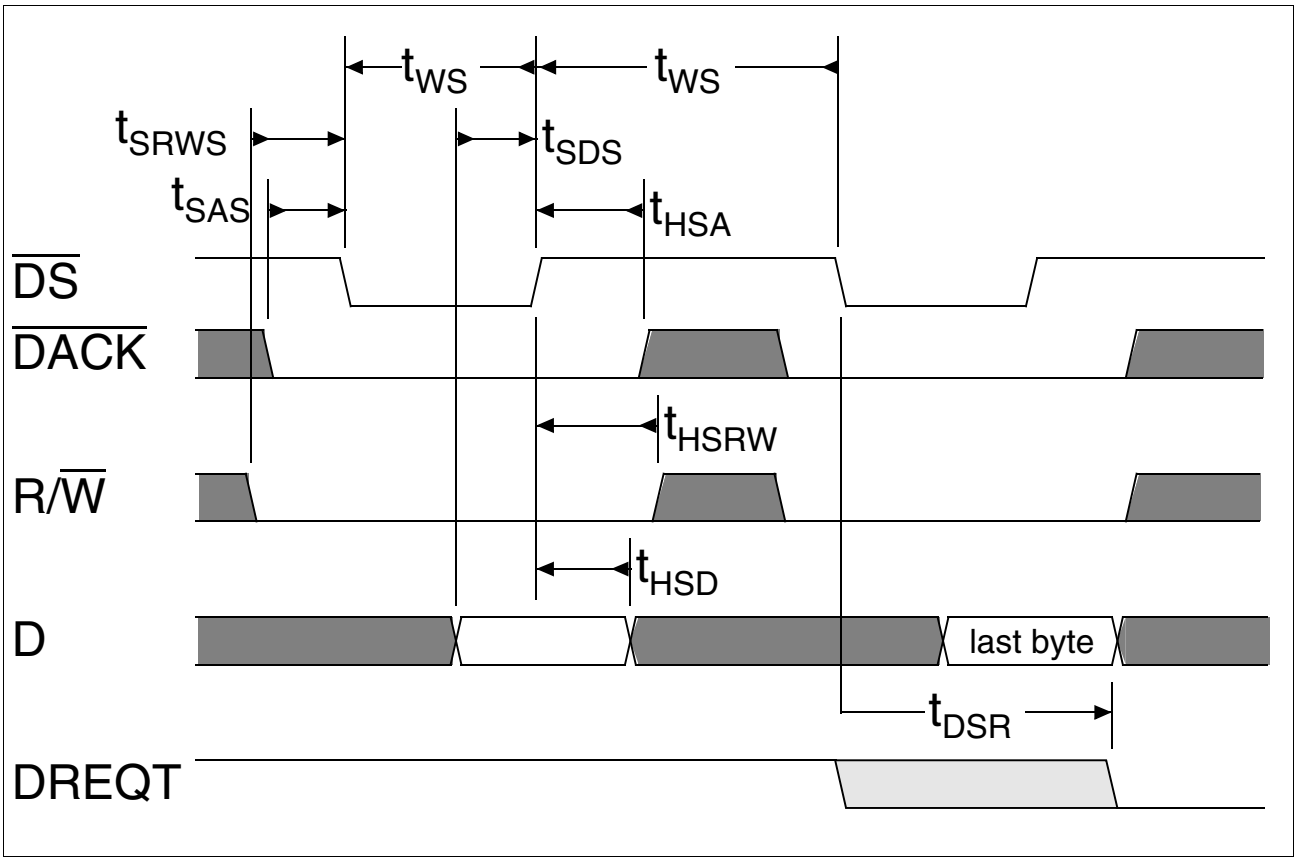


Figure 9-10 DMA Write Transaction Timing in Motorola Mode

Note: R/W is shown for normal mode. In Fly-by mode, R/W should be high during DMA write transactions.

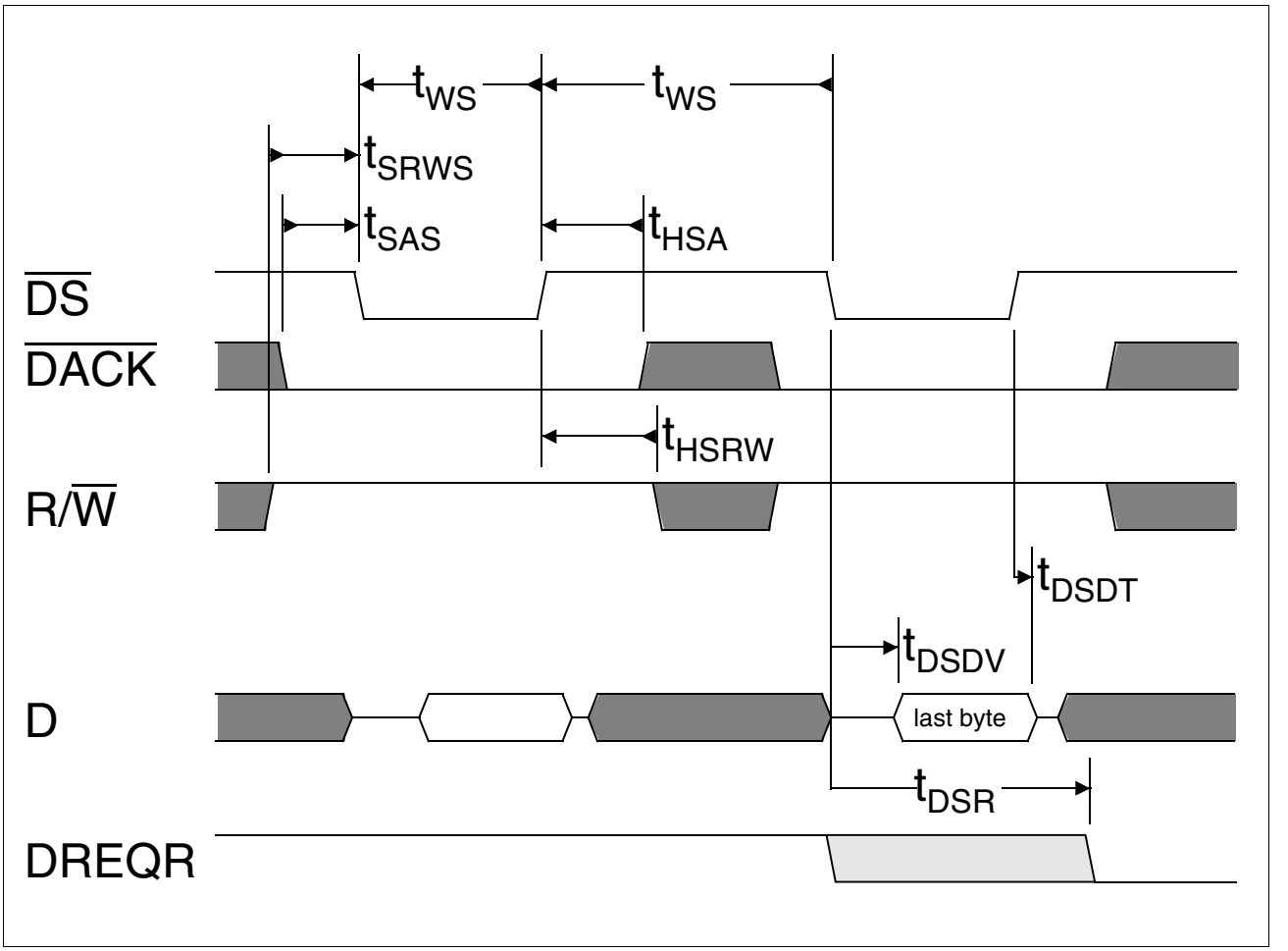


Figure 9-11 DMA Read-Transaction Timing in Motorola Mode

Note: R/W is shown for normal mode. In Fly-by mode, R/W should be low during DMA read transactions.

9.4.2 DMA Access Timing in Intel/Infineon Mode

In this mode, R and W are used for timing the access and to determine whether a DMA read cycle or DMA write cycle has occured. R and W input signals are used in opposite ways in normal mode and in fly-by mode.

The next table shows how R and W should be used in each mode during DMA transactions:

Table 9-10 R/$\overline{W}$ Behavior During DMA Transactions in Normal and Fly-By Mode

Mode	$\overline{R}$ = '1', $\overline{W}$ = '0'	$\overline{R}$ = '0', $\overline{W}$ = '1'
Normal (Non-Fly-By)	Write DMA transaction. (A response to DMA transmitter request)	Read DMA transaction. (A response to DMA receiver request)
Fly-By	Read DMA transaction. (A response to DMA receiver request)	Write DMA transaction. (A response to DMA transmitter request)

In Fly-By mode $\overline{R}$ and $\overline{W}$ are used inverted to the normal mode, because these signals are required also for concurrent accesses of an external memory device.

Table 9-11 DMA Transaction Timing in Intel/Infineon Mode

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
$\overline{DACK}$ setup time to $\overline{W}$ or $\overline{R}$ falling edge	t_{SAW} t_{SAR}	7		ns	Output load capacity of 50 pF
$\overline{DACK}$ hold time after $\overline{W}$ or $\overline{R}$ rising edge	t_{HWA} t_{HRA}	5		ns	
D-bus setup time to $\overline{W}$ rising edge	t_{SDW}	5		ns	
D-bus hold time after $\overline{W}$ rising edge	t_{HWD}	10		ns	
DREQT/DREQR delay after $\overline{W}$ or $\overline{R}$ falling edge	t_{DWR} t_{DRR}	0	36	ns	
$\overline{W}$ pulse width and interval between $\overline{W}$ pulses	t_{WW}	30		ns	
$\overline{R}$ pulse width and interval between $\overline{R}$ pulses	t_{WR}	30		ns	
D-bus valid after $\overline{R}$ falling edge	t_{DRDV}	0	22		
D-bus float (high impedance) after $\overline{R}$ rising edge	t_{DRDT}	0	15		

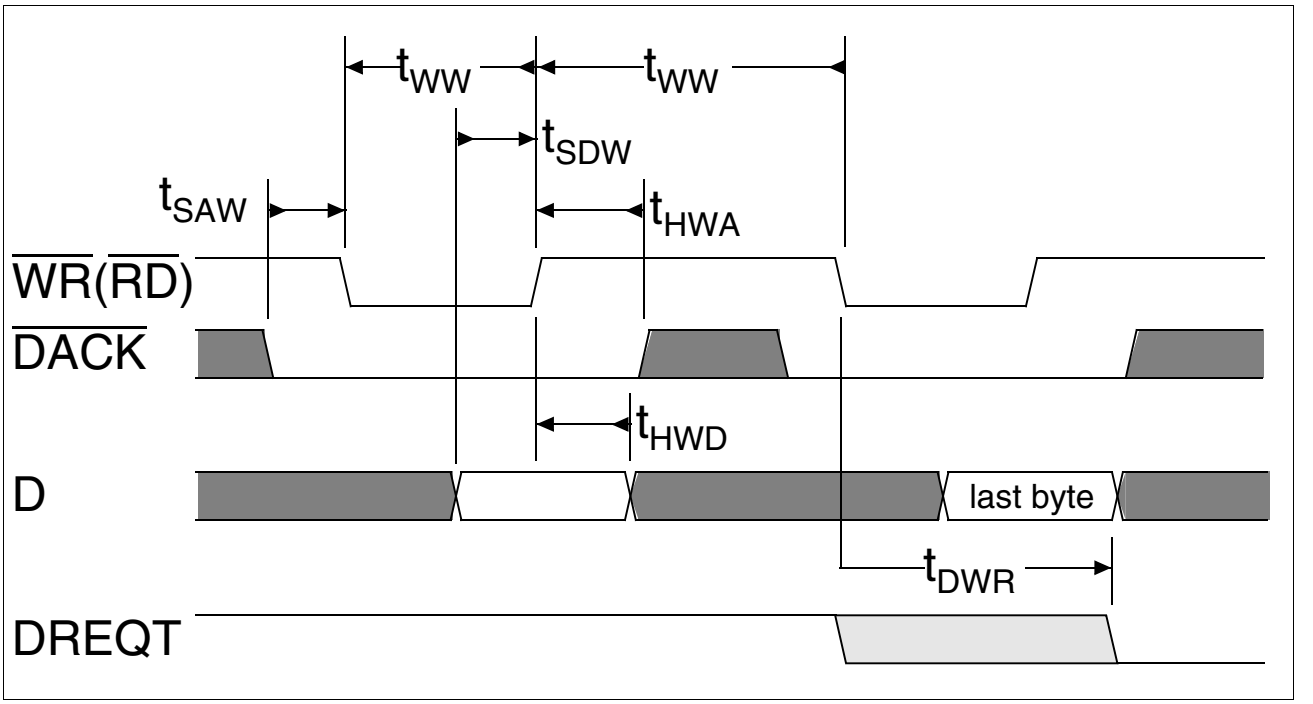


Figure 9-12 DMA Write Transaction Timing in Intel/Infineon Mode

Note: The figure shows a transaction in normal mode. In Fly-by mode, $\overline{RD}$ is used during DMA write transactions, instead of $\overline{WR}$

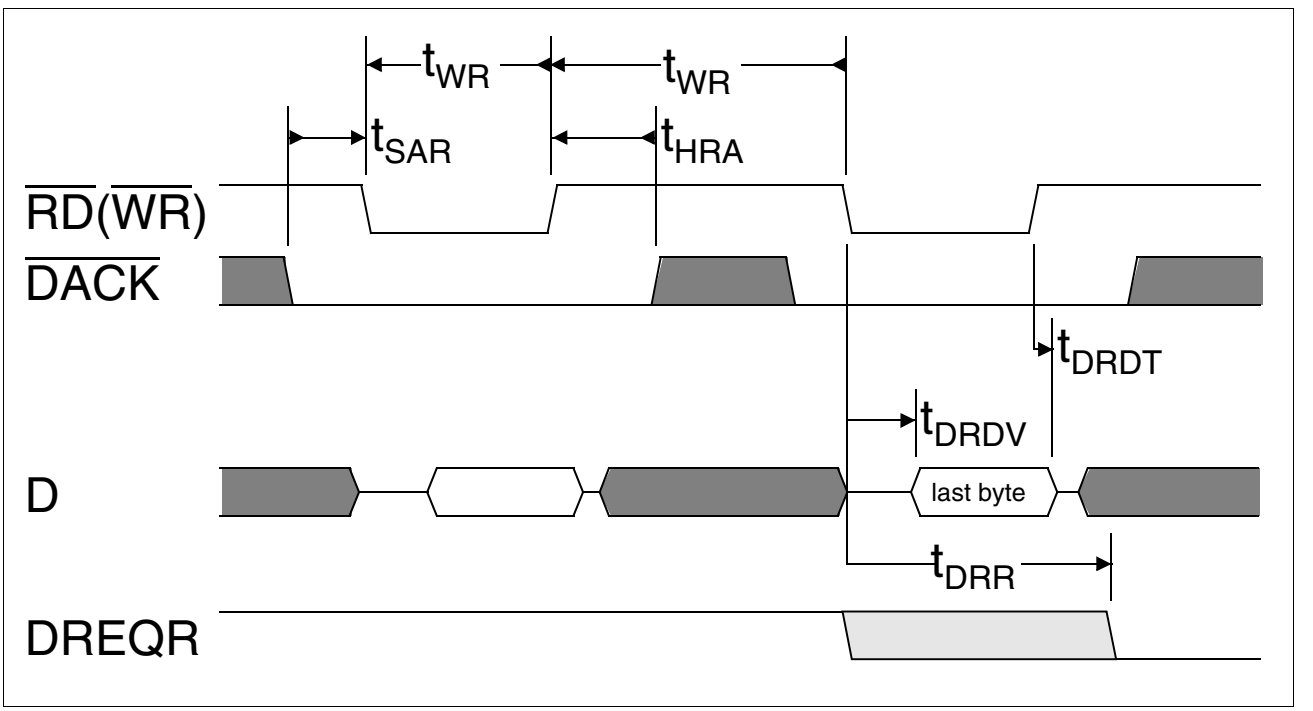


Figure 9-13 DMA Read Transaction Timing in Intel/Infineon Mode

Note: The figure shows a transaction in normal mode. In Fly-by mode, $\overline{WR}$ is used during DMA read-transactions, instead of $\overline{RD}$.

9.5 IOM®-2 Interface Timing

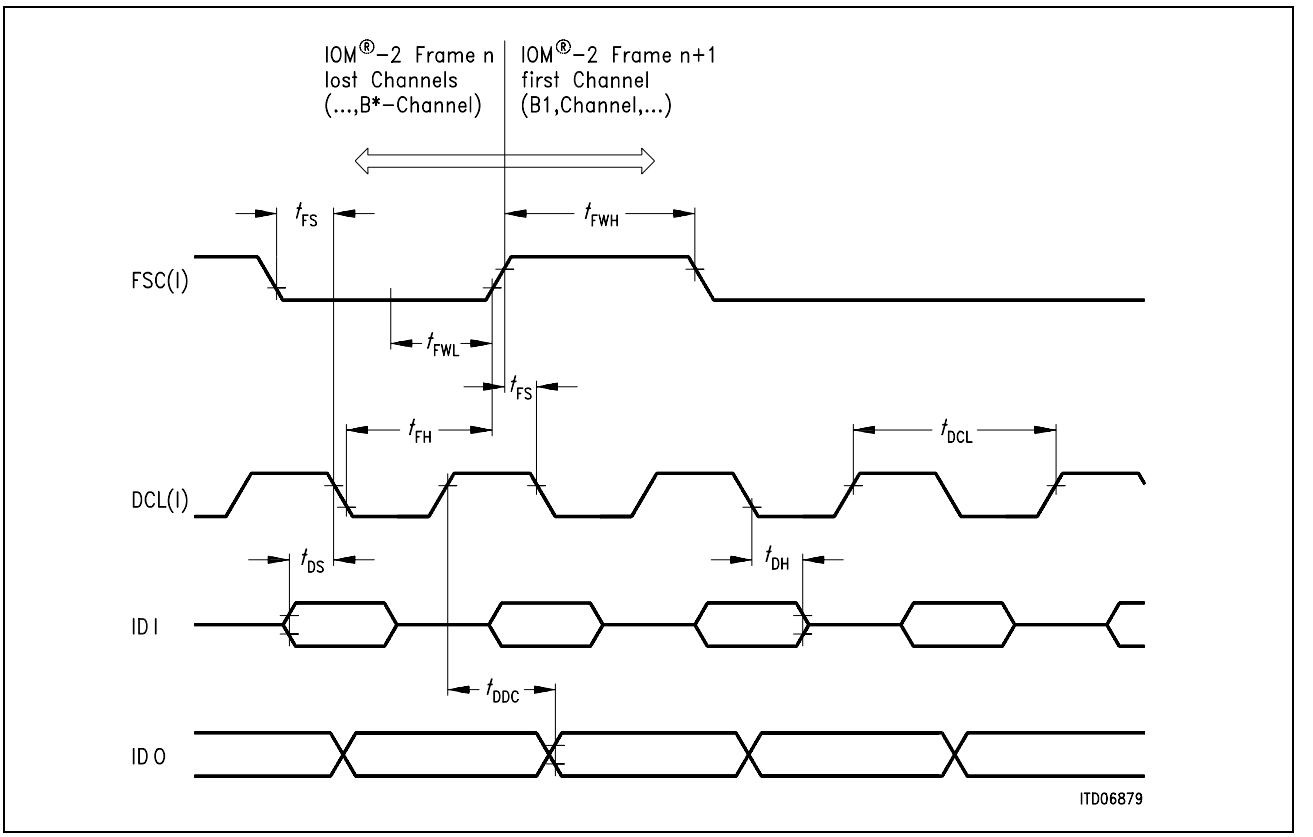


Figure 9-14 IOM®-2 Interface Timing with Single Data Rate DCL

Table 9-12 Timing Characteristics of the IOM®-2

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Frame sync. hold	t_{FH}	30			ns	
Frame sync. setup	t_{FS}	70			ns	
Frame sync. high	t_{FWH}	130			ns	
Frame sync. low	t_{FWL}	t_{DCL}				
Data delay to clock	t_{DDC}			100	ns	
Data delay to frame[1)]	t_{DDF}			150	ns	
Data setup	t_{DS}	20			ns	
Data hold	t_{DH}	50			ns	

Note: 1) $t_{DDF} = 0.5\, t_{DCL} + t_{DDC} - t_{FH}$

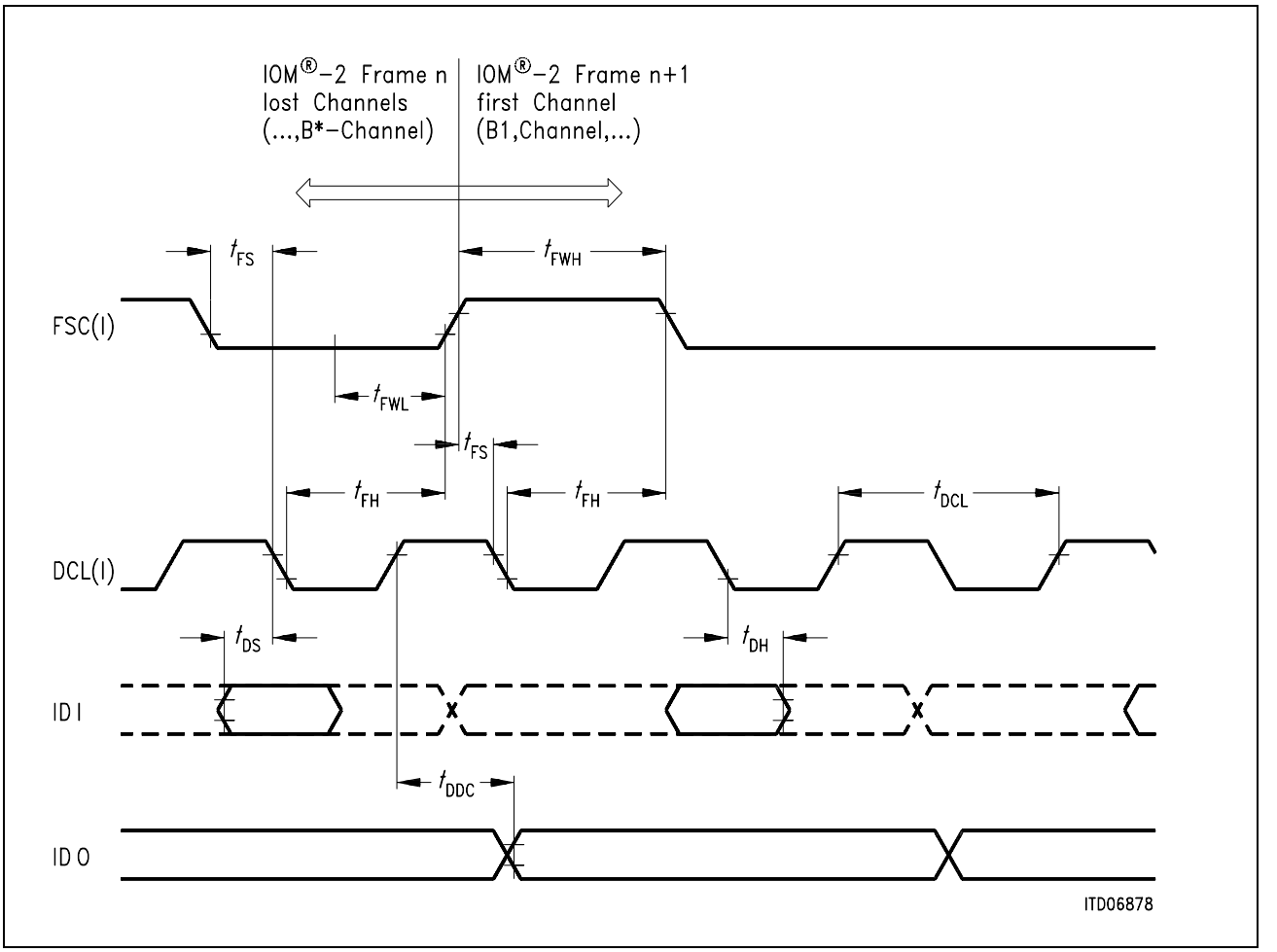


Figure 9-15 Timing of the IOM®-2 Interface with Double Data Rate DCL

Table 9-13 Timing Characteristics of the IOM®-2

Parameter	Symbol	Limit Values			Unit	Conditions
		min.	typ.	max.		
Frame sync hold	t_{FH}	30			ns	
Frame sync setup	t_{FS}	70			ns	
Frame sync high	t_{FWH}	130			ns	
Frame sync low	t_{FWL}	t_{DCL}				
Data delay to clock	t_{DDC}			100	ns	
Data delay to frame[1)]	t_{DDF}			150	ns	
Data setup	t_{DS}	20			ns	
Data hold	t_{DH}	50			ns	

Note: [1)] $t_{DDF} = 0.5\ t_{DCL} + t_{DDC} - t_{FH}$

10 Application Hints

10.1 DELIC Connection to External Microprocessors

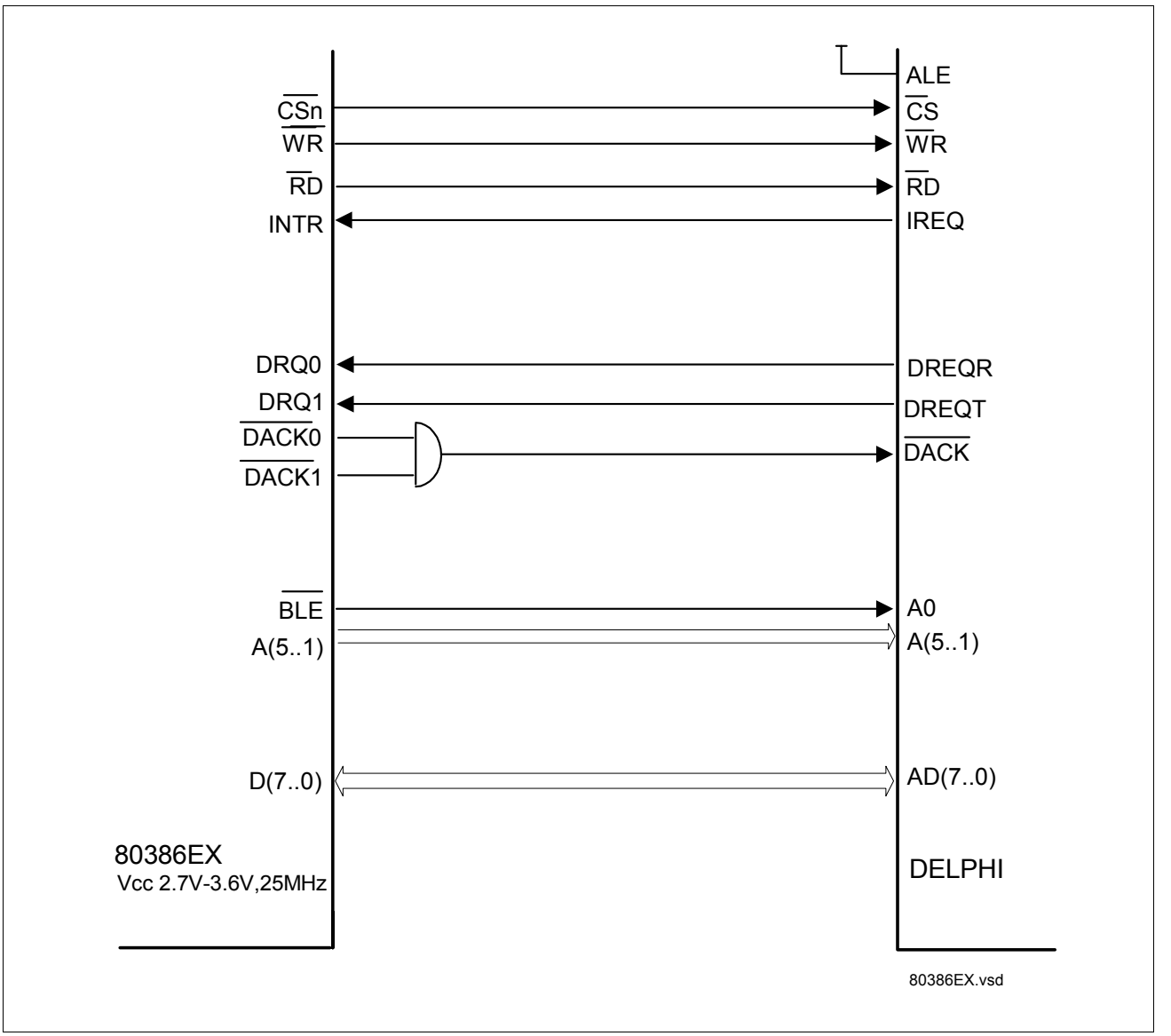


Figure 10-1 DELIC Connection to Intel 80386EX (Demuxed Configuration)

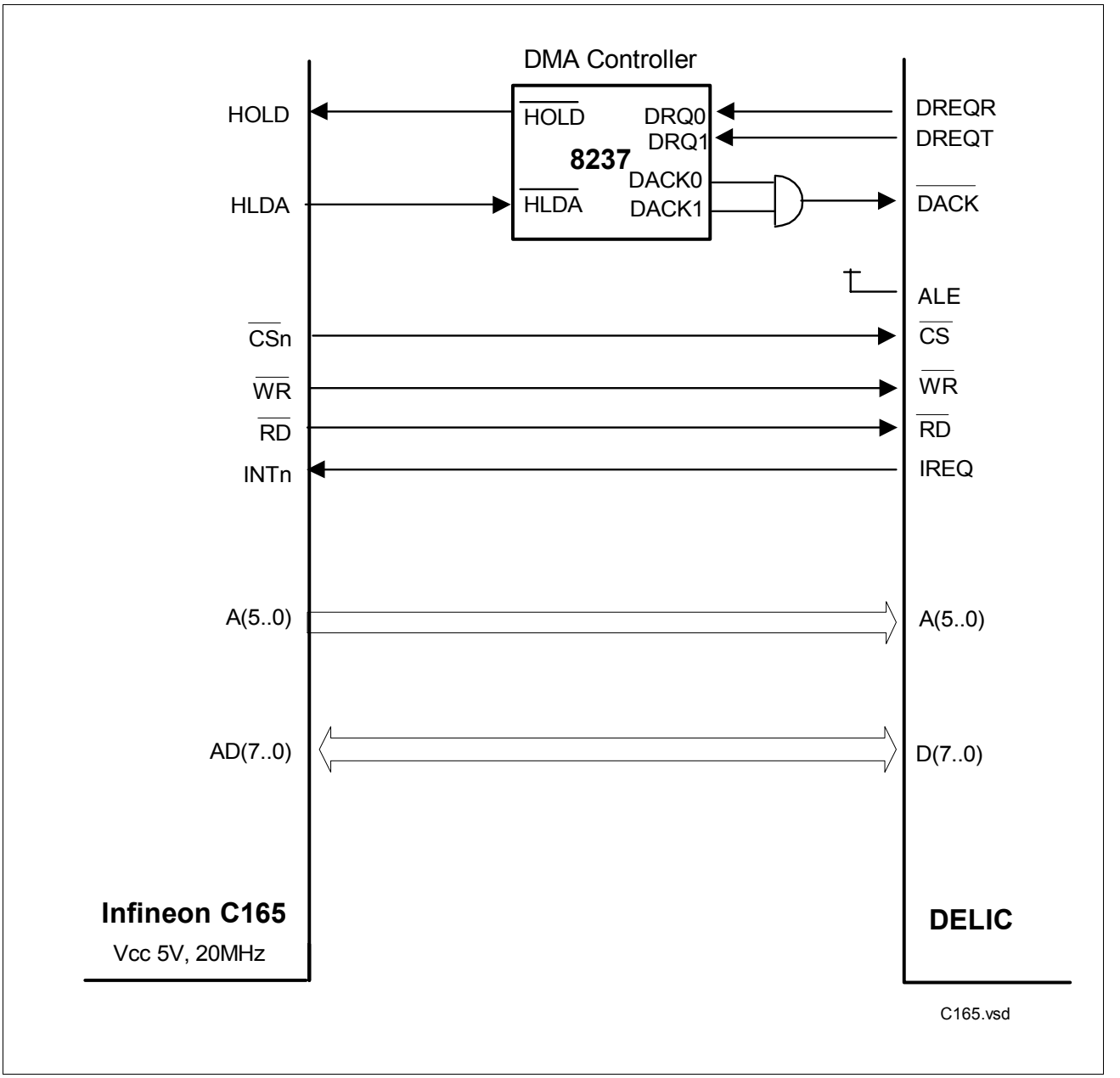


Figure 10-2 DELIC Connection to Siemens C165 (Demuxed Configuration)

10.2 DELIC Worksheets

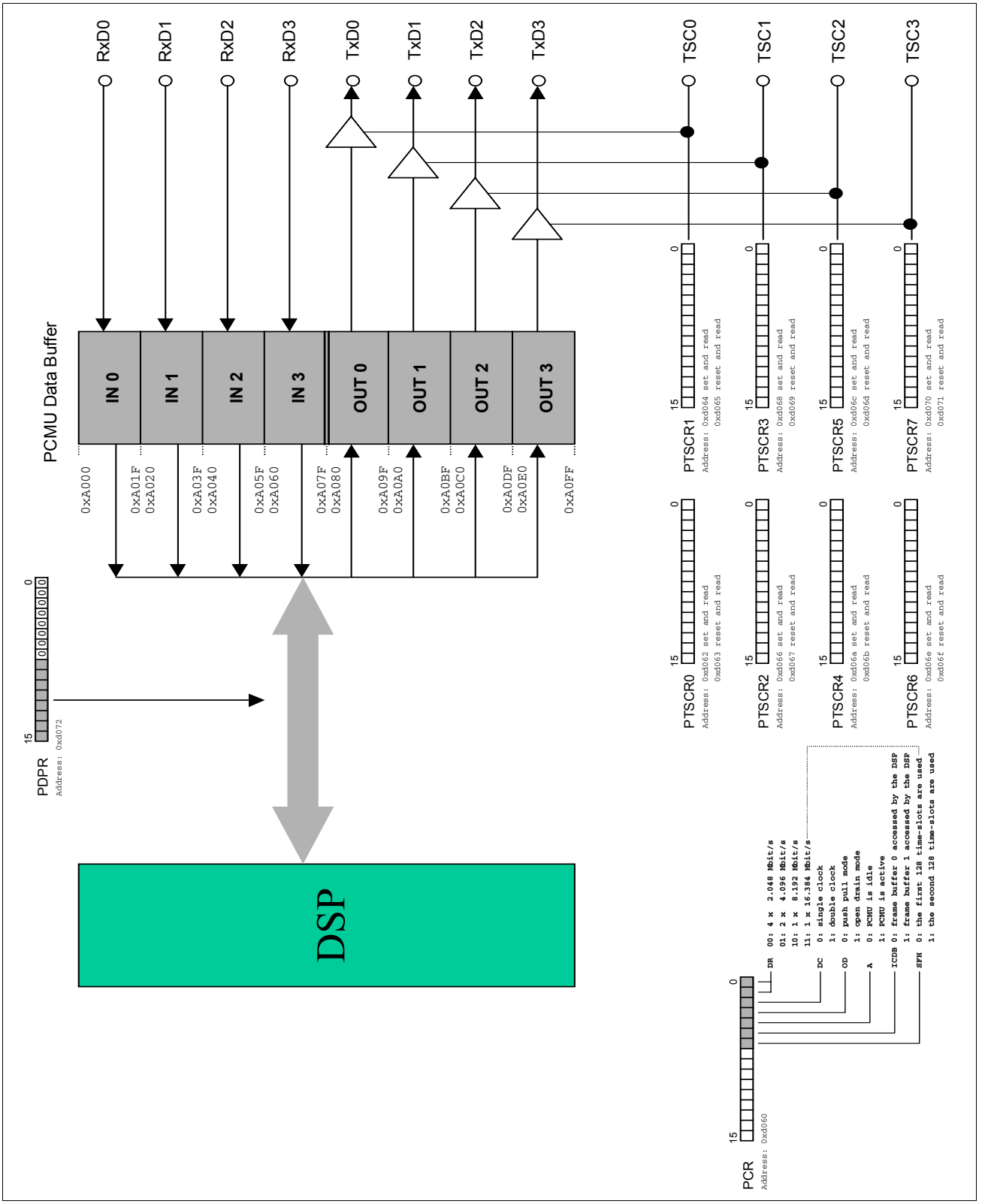


Figure 10-3 DELIC-LC PCM unit mode 0 (4 ports with 2 MBit/s)

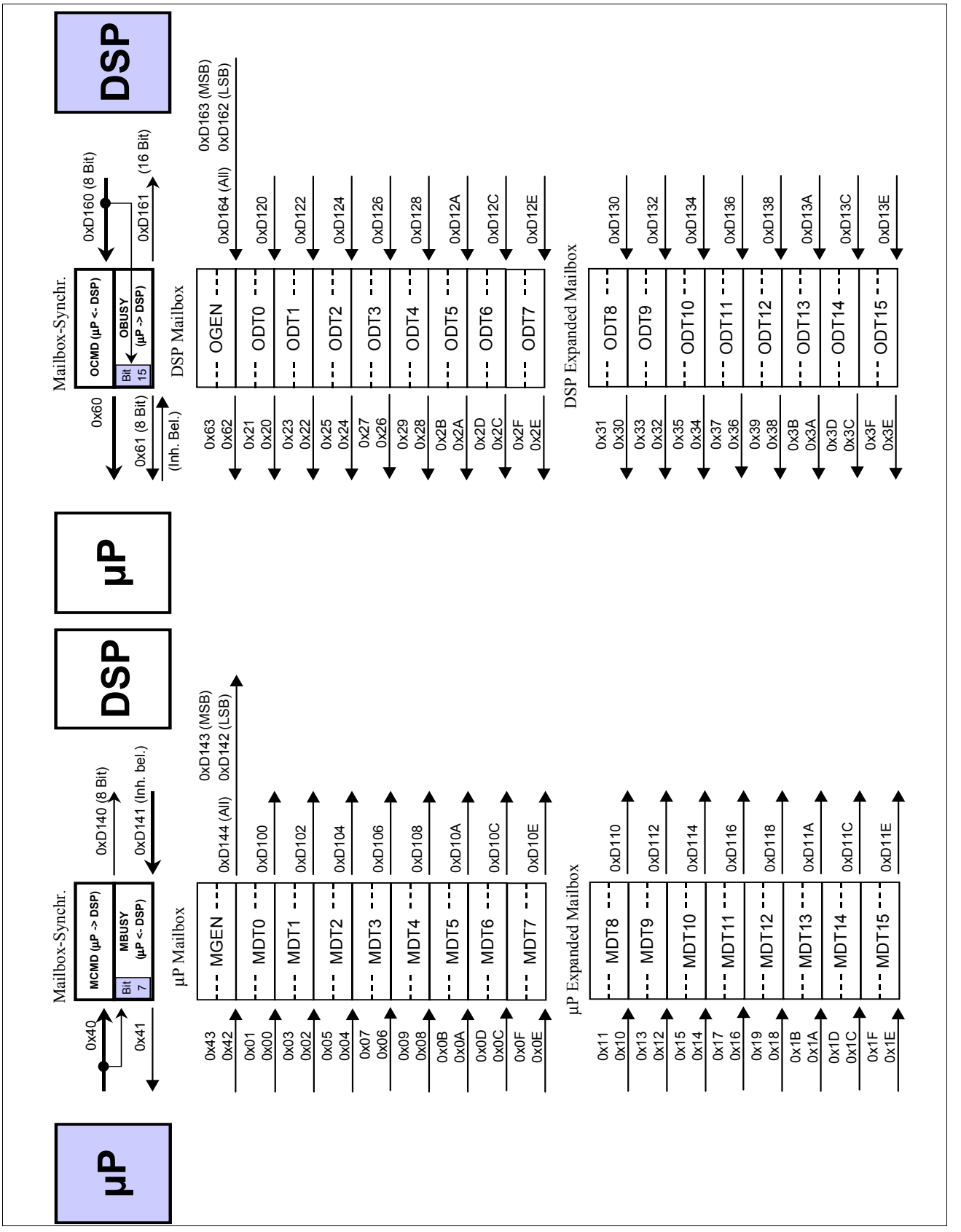


Figure 10-4 Command/ Indication handshake of general mailbox

11 Mailbox Protocol Description

The following chapters describe the way of communication between DELIC and an external µP via the mailbox. If no DMA is used the general mailbox contains 32 data registers. If DMA is used there are actually two different mailboxes. In this case the DMA mailbox consists of 16 data registers and the general mailbox also contains 16 data registers.

For more details especially initialization of the different units refer to the provided application notes.

Note: As a reference, ELIC registers with similar functionality are appended in brackets.

11.1 Mailbox Access

11.1.1 Mailbox Access Transmit Direction (µP->DELIC)

The general mailbox for transmit direction (**Figure 11-1**) consists of 20 (36) registers. One register (MCMD) contains the command to be processed by the DELIC. Another register (MBUSY) just consists of a Busy Bit indicating whether the mailbox is free to be written to or not. Two other registers (MGEN Low and MGEN High) serve for general parameters. A block of 16 (32) parameter registers contains data. Writing to the command register sets the Busy Bit and thereby an interrupt in the DELIC. If the DELIC has processed the command it clears the Busy Bit to release the mailbox.

11.1.2 Mailbox Access Receive Direction (DELIC->µP)

The mailbox for receive direction (**Figure 11-2**) consists of 20 (36) registers. One register (OCMD) contains the indication to be processed by the µP. Another register (OBUSY) just consists of a Busy Bit which has to be cleared by the µP after processing the indication in order to release the mailbox. Two other registers (OGEN Low and OGEN High) serve as general parameters. A block of 16 (32) parameter registers contains data associated with the indication.

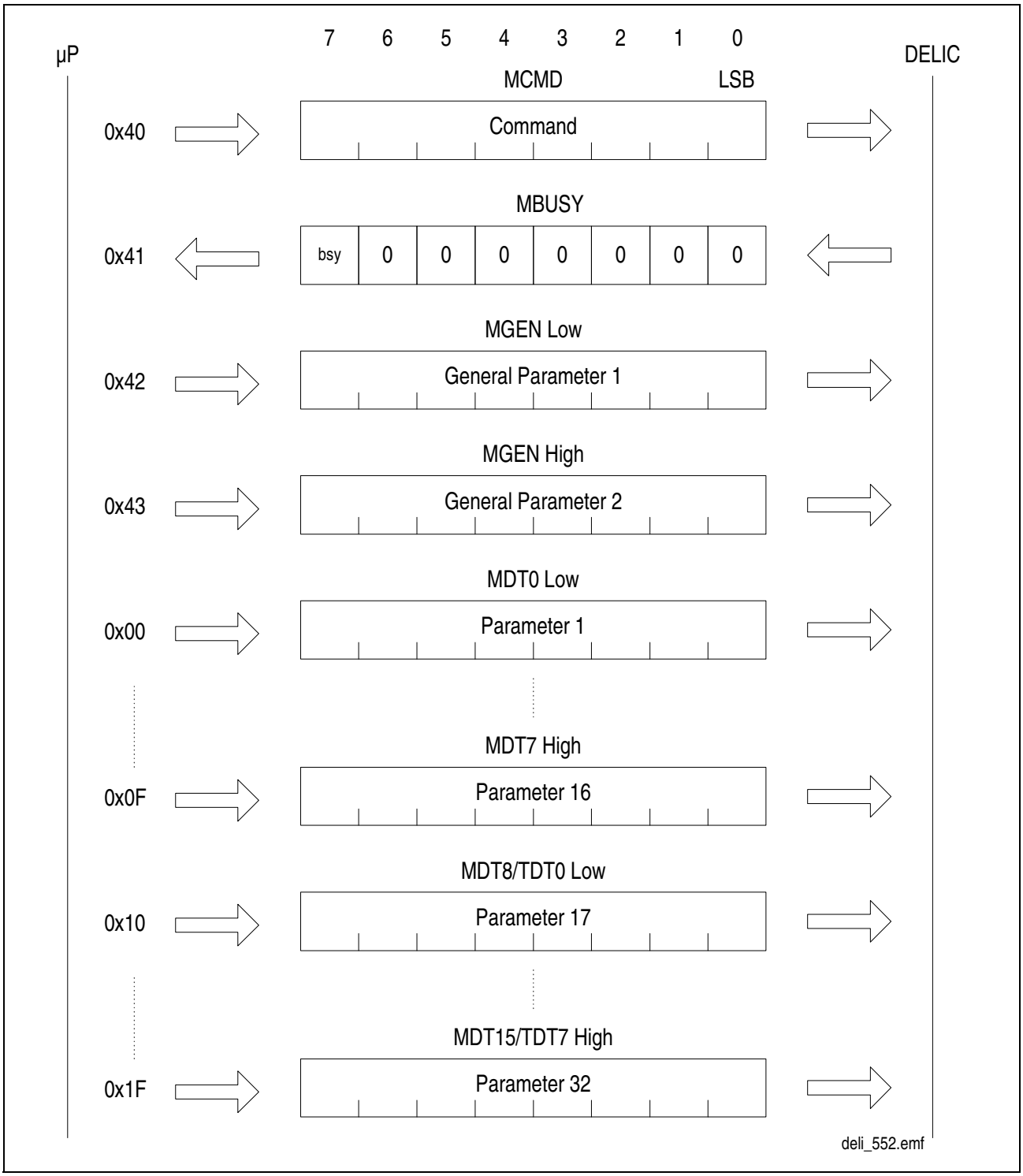


Figure 11-1 Transmit Mailbox Structure

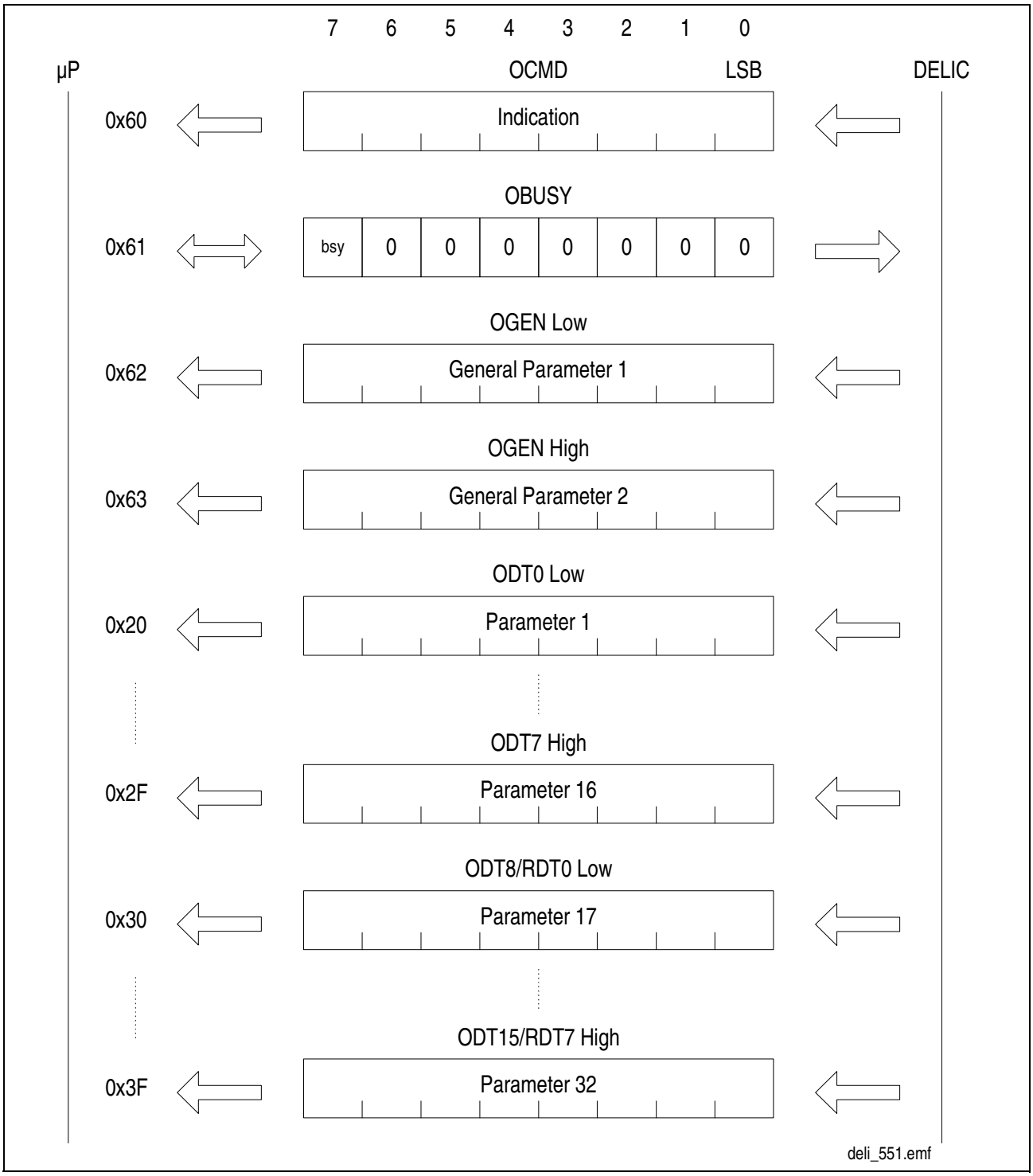


Figure 11-2 Receive Mailbox Structure

Both sides, µP and DELIC, use the same procedure to perform write accesses to the mailbox. If one side wants to put a message into the mailbox it has to check whether the mailbox is free. If the mailbox is free the parameters have to be written first than the command (**Figure 11-3**).

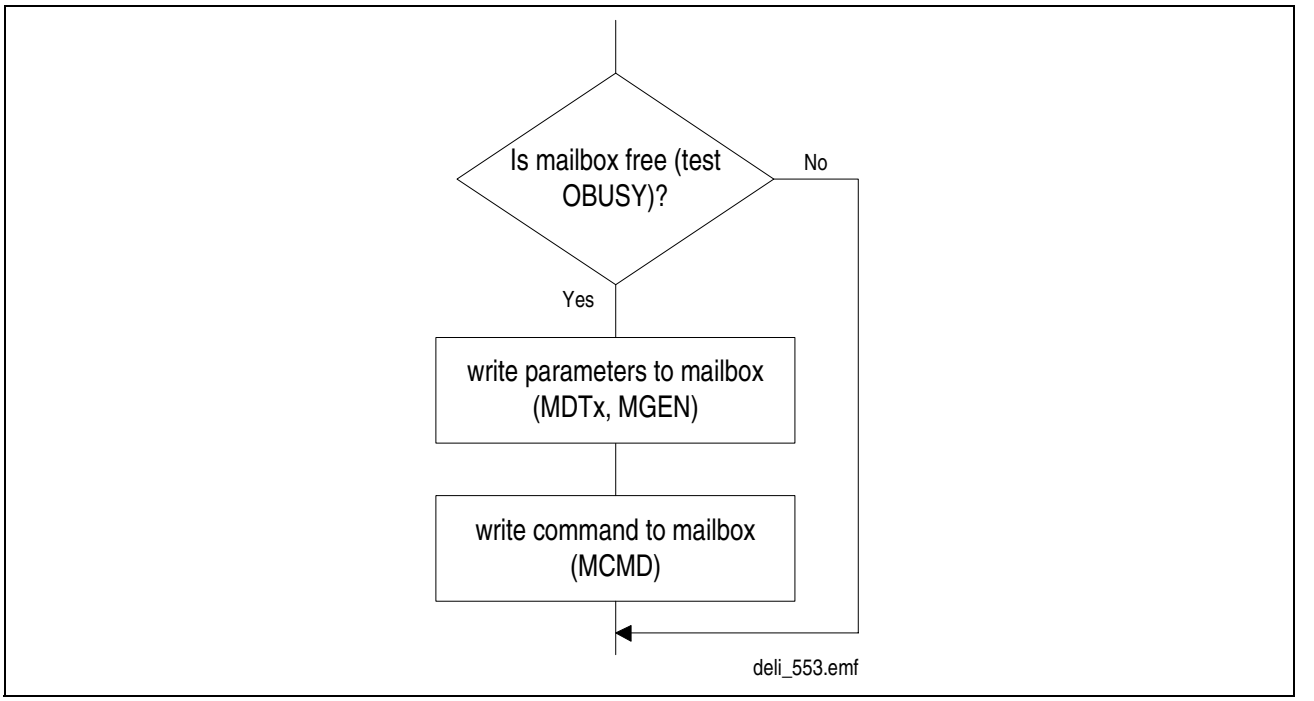


Figure 11-3 Flow Diagram: Mailbox Write Access

11.2 Subscriber Address (SAD) Interpretation

In this chapter SAD is used commonly for the subscriber address. There are two possibilities to interpret SAD

11.2.1 SAD as IOM-2 Port and Channel Number

The DELIC has two IOM-2 ports. The subscriber address has to be interpreted as follows.

bit	7	6	5	4	3	2	1	0
					SAD3	SAD2	SAD1	SAD0

SAD3 IOM-2 port number (2.048 Mbit/s)

0 = IOM-2 port 0 is addressed

1 = IOM-2 port 1 is addressed

SAD2..0 IOM-2 channel number (range: 0..7) (2.048 Mbit/s)

SAD3..0 IOM-2 channel number (range: 0..15) (4.096 Mbit/s)

11.2.2 SAD as IOM-2000 VIP and Channel Number

It is possible to connect up to 3 VIPs to the DELIC via the IOM-2000 interface. Each VIP contains up to 8 channels. The subscriber address has to be interpreted as follows.

bit	7	6	5	4	3	2	1	0
				SAD4	SAD3	SAD2	SAD1	SAD0

SAD4..3 VIP number

00 = VIP 0 is addressed

01 = VIP 1 is addressed

10 = VIP 2 is addressed

11 = reserved

SAD2..0 IOM-2000 channel number (range: 0..7)

11.3 Overview of Commands and Indications

The following tables give an overview of all commands and indications according name, code value, parameters and the referring page where the detailed description can be found.

11.3.1 Commands and Indications for Boot Sequence

Table 11-1 Boot Commands

Name	MCMD	MDT0	MDT1..15	Page
Start Boot	0x55			11-13
Write Program Memory	0xAn n = Amount	Start Address	Data	11-13
Write Data Memory	0xEn n = Amount	Start Address	Data	11-14
Finish Boot	0x1F			11-13

Table 11-2 Boot Indications

Name	OCMD	ODT0	Page
Start Loading Program RAM	0x1F		11-15
Start Loading Data RAM	0xEF		11-15
Error	0b011100XX XXX=Error Code		11-15
Firmware Version Indication	0x00	Version Number	11-15

11.3.2 General Commands and Indications

Table 11-3 General Commands

Name	OCMD	OGEN Low	OGEN High	ODTx	Page
Write Register	0x01	Size		MDT0: Destination address MDTx: Register value(s)	11-16
Read Register	0x02	Size		MDT0: Start address for read	11-17

Table 11-4 General Indications

Name	OCMD	OGEN Low	OGEN High	ODTx	Page
Read Register	0x01	Size		Value(s) read from register	11-18

11.3.3 Commands and Indications for Configuration

Table 11-5 Configuration Commands

Name	MCMD	MGEN Low	MGEN High	MDTx	Page
IOM-2000 Reference Channel Select	0x05	IOM-2000 VIP and channel no.			11-20
IOM-2000 Delay Measurement	0x04	IOM-2000 VIP and channel no.			11-21
IOM-2000 VIP Channel Configuration	0x03			MDT0 H= TICCMR[31..24] MDT0 L= TICCMR[23..16] MDT1 H= TICCMR[15..8] MDT1 L= TICCMR[7..0]	11-22
GHDLC Configuration	0x14	GHDLC no.		MDT0 L = Mode Information MDT1 = Normal Address MDT2 = Broadcast Address	11-22
Finish Initialization	0x06				11-24

Table 11-6 Configuration Indications

Name	OCMD	OGEN Low	OGEN High	ODTx	Page
IOM-2000 Far-end Code Violation	0x07		Size	IOM-2000 VIP and channel no. FECV	11-24
IOM-2000 Delay	0x04	Delay Value			11-25
Finish VIP Channel Configuration[1)]	0x02	Delay Value		ODT0 H= TICSTR[31..24] ODT0 L= TICSTR[23..16] ODT1 H= TICSTR[15..8] ODT1 L= TICSTR[7..0]	11-26

1) *this indication is only sent if the read bit of TICCMR has been set in IOM-2000 VIP Channel Configuration Command*

11.3.4 Commands and Indications for IOM-2 C/I Channels

Table 11-7 IOM-2 C/I Command

Name	MCMD	MGEN High	MDTx	Page
Write C/I Value	0x23	Size	IOM-2 port and channel no. C/I value	11-27

Table 11-8 IOM-2 C/I Indication

Name	OCMD	OGEN High	ODTx	Page
Change Detected	0x41	Size	IOM-2 port and channel no. new C/I value	11-27

11.3.5 Commands and Indications for IOM-2 Monitor Channel

Table 11-9 IOM-2 Monitor Commands

Name	MCMD	MGEN Low	MGEN High	MDTx	Page
Search On	0x2B				11-29
Search Reset	0x2C				11-30
Monitor Reset	0x2D				11-30
Transmit Continuous	0x29	IOM-2 port and channel no.	Size	Data	11-30
Transmit	0x28	IOM-2 port and channel no.	Size	Data	11-30
Transmit&Receive/ Receive Only	0x2A	IOM-2 port and channel no.	Size	Data	11-30

Table 11-10 IOM-2 Monitor Indications

Name	OCMD	OGEN Low	OGEN High	ODTx	Page
Transfer Ready	0x53				11-31
Receive Continuous	0x52		Size	Data	11-31
Receive	0x51		Size	Data	11-31
Transmit Abort	0x55				11-32
Monitor Active	0x54	IOM-2 port and channel no.			11-32

11.3.6 Commands and Indications for IOM-2000 C/I Channels

Table 11-11 IOM-2000 C/I Command

Name	MCMD	MGEN High	MDTx	Page
Write C/I Value	0x0B	Size	IOM-2000 VIP and channel no. C/I value	11-38

Table 11-12 IOM-2000 C/I Indication

Name	OCMD	OGEN High	ODTx	Page
Change Detected	0x11	Size	IOM-2000 VIP and channel no. new C/I value	11-38

11.3.7 Commands and Indications for HDLC Channel

Table 11-13 HDLC Commands

Name	MCMD	MGEN Low	MGEN High	MDTx	Page
Reset	0x1F		Size	HDLC No. Receiver or Transmitter or both	11-40
Transmit	0x1D	HDLC No.	Size	Data	11-41
Transmit Continuous	0x1E	HDLC No.	Size	Data	11-41
Activation/ Deactivation	0x20		Size	HDLC No. and activation information	11-41

Table 11-14 HDLC Indications

Name	OCMD	OGEN Low	OGEN High	ODTx	Page
Error	0x34	HDLC No.	0x01	ODT0 L: Error Code	11-42
Transmit Ready	0x33	HDLC No.			11-43
Receive	0x31	HDLC No.	Size	Data	11-44
Receive Continuous	0x32	HDLC No.	Size	Data	11-44

11.3.8 Commands and Indications for GHDLC Channel

Table 11-15 GHDLC Commands

Name	MCMD	MGEN Low	MGEN High	MDTx	Page
Reset	0x15		Size	GHDLC No.	11-46
Transmit	0x11	GHDLC No.	Size	Data	11-47
Transmit Continuous	0x12	GHDLC No.	Size	Data	11-48

Table 11-16 GHDLC Indications

Name	OCMD	OGEN Low	OGEN High	ODTx	Page
Error	0x24	GHDLC No.	0x01	ODT0 L: Error Code	11-48
Fatal Error	0x25	GHDLC No.	0x02	ODT0: Status Word	11-48
Transmit Ready	0x23	GHDLC No.			11-49
Receive	0x21	GHDLC No.	Size	Data	11-49
Receive Continuous	0x22	GHDLC No.	Size	Data	11-49

11.3.9 Switching

Table 11-17 Switching Commands

Name	MCMD	MGEN High	MDTx	Page
Connect	0x17	Size	Connection Identifier Source/Destination Interface Type Source Time Slot No. Destination Time Slot No.	11-50
Disconnect	0x18	Size	Connection Identifier	11-52

11.4 Boot Procedure

After reset the DELIC jumps into the boot routine and waits for downloading a program via the µP-Mailbox. **Figure 11-4** shows the handshake.

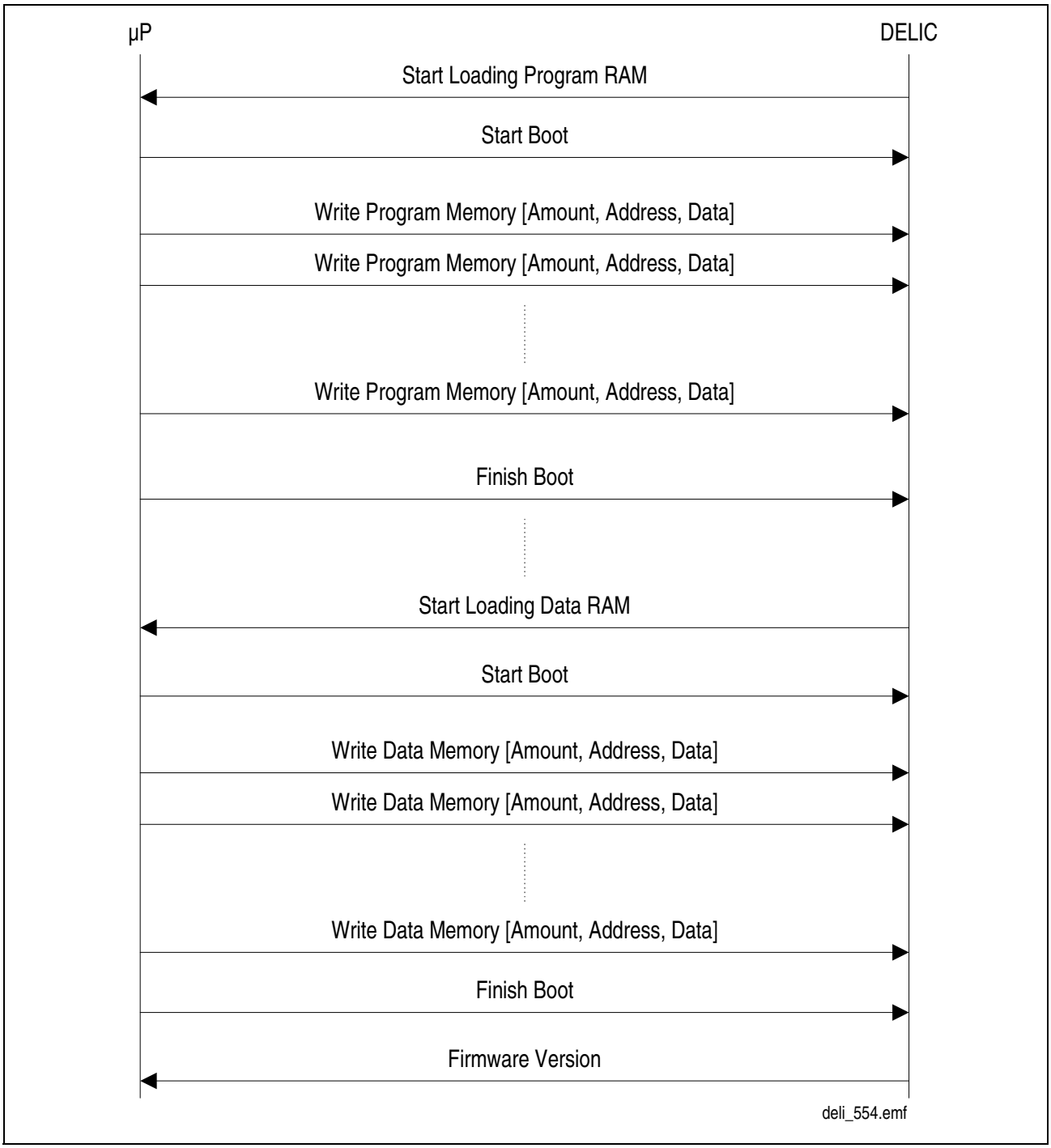


Figure 11-4 Boot Sequence

The range for Amount must be between 1 and 15. In case of an verification failure or if an amount of zero has been used the Start Boot Command has to be issued again before continuing the download. After issuing Start Boot any invalid command is ignored.

11.4.1 Boot Commands

After reset the DELIC waits for downloading a program from the processor via the mailbox indicated by the Start Loading Program RAM Indication (0x1F) (**Figure 11-4**).

11.4.1.1 Start Boot Command (0x55)

This command has to be issued before using the Write Program Memory Command (0xAn) and Write Data Memory Command (0xEn) directly after receiving the Start Loading Program RAM Indication (0x1F) or the Start Loading Data RAM Indication (0xEF).

Mailbox Register (MCMD) µP-write Address: 40_H

bit	7	6	5	4	3	2	1	0
	0	1	0	1	0	1	0	1

11.4.1.2 Finish Boot Command (0x1F)

First usage of this command finishes filling of the program memory. The second usage finishes filling of the data memory and let the DELIC wait for initialization commands.

Mailbox Register (MCMD) µP-write Address: 40_H

bit	7	6	5	4	3	2	1	0
	0	0	0	1	1	1	1	1

11.4.1.3 Write Program Memory Command (0xAn)

After issuing the Start Boot Command (0x55) the first time the program memory can be filled with this command. The filling has to be finished with the Finish Boot Command (0x1F).

Mailbox Register (MCMD) µP-write Address: 40_H

bit	7	6	5	4	3	2	1	0
	1	0	1	0	N3	N2	N1	N0

N3..0 Amount of 16-bit data words within MDT1 to MDT15 (range: 1..15)

Mailbox Register (MDT0) µP-write Address: $00+01_H$

bit	7	6	5	4	3	2	1	0
High	AD(15:8)							

bit	7	6	5	4	3	2	1	0
Low	AD(7:0)							

AD15..0 Start Address (DELIC Address Space)

11.4.1.4 Write Data Memory Command (0xEn)

After issuing the Start Boot Command (0x55) the second time the data memory can be filled with this command. The filling has to be finished with the Finish Boot Command (0x1F).

Mailbox Register (MCMD) µP-write Address: 40_H

bit	7	6	5	4	3	2	1	0
	1	1	1	0	N3	N2	N1	N0

N3..0 Amount of 16-bit data words within MDT1 to MDT15 (range: 1..15)

Mailbox Register (MDT0) µP-write Address: $00+01_H$

bit	7	6	5	4	3	2	1	0
High	AD(15:8)							

bit	7	6	5	4	3	2	1	0
Low	AD(7:0)							

AD15..0 Start Address (DELIC Address Space)

11.4.2 Boot Indications

11.4.2.1 Error Indication (0b011100XX)

Mailbox Register (OCMD) µP-read Address: 60_H

bit	7	6	5	4	3	2	1	0
	0	1	1	1	0	0	EN1	EN0

EN1..0 Error Code

00 = Wrong command error

01 = Data verification failure

10 = Incorrect amount of data (zero size)

Note: After an zero size error and after a verification failure the Start Boot Command (0x55) has to be issued again.

11.4.2.2 Start Loading Program RAM Indication (0x1F)

This indication is issued after reset to inform the processor that program download can begin.

Mailbox Register (OCMD) µP-read Address: 60_H

bit	7	6	5	4	3	2	1	0
	0	0	0	1	1	1	1	1

11.4.2.3 Start Loading Data RAM Indication (0xEF)

This indication is issued after issuing the Finish Boot Command (0x1F) the first time to inform the processor that data download can begin.

Mailbox Register (OCMD) µP-read Address: 60_H

bit	7	6	5	4	3	2	1	0
	1	1	1	0	1	1	1	1

11.4.2.4 Firmware Version Indication (0x00)

This indication is sent after the last Finish Boot Command (0x1F) to confirm the correct program and daa boot.

Mailbox Register (ODT0) µP-read Address: $20+21_H$

bit	7	6	5	4	3	2	1	0
High	FVNO(15:8)							

bit	7	6	5	4	3	2	1	0
Low	FVNO(7:0)							

FVNO15..0 Firmware Version Number

11.5 General Commands and Indications

The following commands and indications are used during initialization and during normal operation.

11.5.1 General Commands

11.5.1.1 Write Register Command (0x01)

The command writes any 16-bit value(s) to DELIC's register(s), starting from the specified destination address (and continuing to the consecutive address(es)).

Parameter:

– Number of values to be written
– Destination address for write
– Register value(s) to be written

Mailbox Register (MGEN Low) µP-write Address: 42_H

bit	7	6	5	4	3	2	1	0
					(SIZE3)	SIZE2	SIZE1	SIZE0

SIZE3..0 Number of valid 16-bit values within MDT1..7(15) (range: 1..7(15))

Mailbox Register (MDT0) µP-write Address: $00+01_H$

bit	7	6	5	4	3	2	1	0
High	DAD(15:8)							

bit	7	6	5	4	3	2	1	0
Low	DAD(7:0)							

DAD15..0 Destination Address (DELIC Address Space)

Mailbox Register (MDT1..7(15)) µP-write

bit	7	6	5	4	3	2	1	0
High	WRV(15:8)							

bit	7	6	5	4	3	2	1	0
Low	WRV(7:0)							

WRV15..0 MDT1: Write Value to Destination Address DAD
MDT2: Write Value to Destination Address DAD+1
..
MDT7(15): Write Value to Destination Address DAD+6(14)

11.5.1.2 Read Register Command (0x02)

The command initiates read access(es) to DELIC's register(s), starting from the specified base address (and continuing to the consecutive address(es)).

Parameter:

– Number of values to be read
– Base address for read

Mailbox Register (MGEN Low) µP-write Address: 42_H

bit	7	6	5	4	3	2	1	0
				(SIZE4)	SIZE3	SIZE2	SIZE1	SIZE0

SIZE4..0 Amount of 16-bit values to be read from the base address (range: 1..8(16))

Mailbox Register (MDT0) µP-write Address: $00+01_H$

bit	7	6	5	4	3	2	1	0
High	BAD(15:8)							

bit	7	6	5	4	3	2	1	0
Low	BAD(7:0)							

BAD15..0 Base address from which register value is to be read

11.5.2 General Indication

11.5.2.1 Read Register Indication (0x01)

The indication returns the values read from DELIC's register(s) as specified in the Read Register Command (0x02).

Parameter:

– Number of read values
– Read register values

Mailbox Register (OGEN Low) µP-read Address: 62_H

bit	15	14	13	12	11	10	9	8
				(SIZE4)	SIZE3	SIZE2	SIZE1	SIZE0

SIZE4..0 Number of valid 16-bit values that have been read (range: 1..8(16))

Mailbox Register (ODT0..7(14)) µP-read

bit	7	6	5	4	3	2	1	0
High	RRV(15:8)							

bit	7	6	5	4	3	2	1	0
Low	RRV(7:0)							

RRV15..0 ODT0: Read Register Value from Base Address BAD
ODT1: Read Register Value from Base Address BAD+1
..
ODT7(15): Read Register Value from Base Address BAD+7(15)

11.6 Initialization/Configuration

After issuing the last Finish Boot Command (0x1F) the DELIC waits for the Finish Initialization Command (0x06) before it starts all tasks. Here the device can be configured according the application requirements.

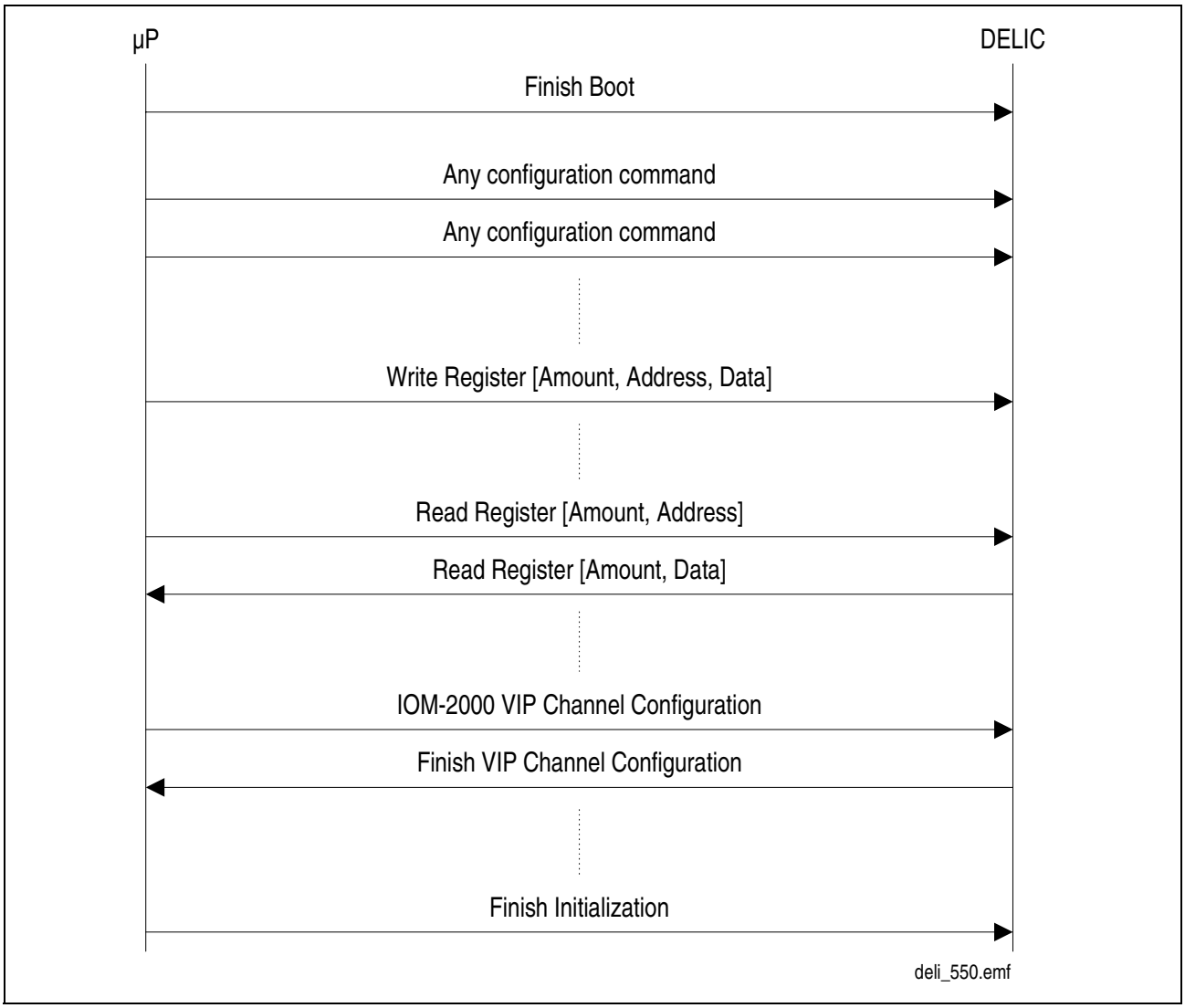


Figure 11-5 Initialization Flow Diagram: Configuration Example

11.6.1 Configuration Commands

11.6.1.1 IOM-2000 Reference Channel Select Command (0x05)

The command selects the VIP channel which provides the reference clock.

Parameter:

– IOM-2000 VIP and channel number
– External reference source

Mailbox Register (MGEN Low) µP-write Address: 42_H

bit	7	6	5	4	3	2	1	0
			EXREF	SAD4	SAD3	SAD2	SAD1	SAD0

SAD4..0 Subscriber Address i.e. IOM-2000 VIP and channel number

EXREF External Reference Clock Selection (LT-T)

0 = No external reference clock source. Reference clock is generated from internal VIP_n channel specified in REFCLK(2:0) and passed on via REFCLK pin to VIP_n-1 or directly to DELIC.

1 = Reference clock is generated from external source via pin INCLK and passed on via REFCLK pin to VIP_n-1 or directly to DELIC. The internal reference clock generation logic is disabled.

Note: VIP_0 has the highest priority in terms of clock selection

Note: This command is only applicable for channels in LT-T Mode

11.6.1.2 IOM-2000 Delay Measurement Command (0x04)

This command selects the VIP channel in which the line delay is to be measured. The delay is reported with the IOM-2000 Delay Indication (0x04).

Parameter:

– IOM-2000 VIP and channel number

Mailbox Register (MGEN Low) µP-write Address: 42_H

bit	7	6	5	4	3	2	1	0
				SAD4	SAD3	SAD2	SAD1	SAD0

SAD4..0 Subscriber Address i.e. IOM-2000 VIP and channel number

Note: This command is only applicable for channels in U_{PN} Mode

11.6.1.3 IOM-2000 VIP Channel Configuration Command (0x03)

The command initializes or re configures the channel register in the TRANSIU for the specified VIP channel.

Parameter:

– Initialization values of VIP Channel Command Register TICCR (4 bytes including VIP and channel number)

Mailbox Register (MDT0 High) µP-write Address: 01_H

bit	15	14	13	12	11	10	9	8
	x	VIPADR(1:0)		CHADR(2:0)			FIL	EXLP

Mailbox Register (MDT0 Low) µP-write Address: 00_H

bit	7	6	5	4	3	2	1	0
	PLLS	PD	DHEN	x	x	PDOWN	LOOP	TX_EN

Mailbox Register (MDT1 High) µP-write Address: 03_H

bit	15	14	13	12	11	10	9	8
	PLLINT	AAC(1:0)		BBC(1:0)		OWIN(2:0)		

Mailbox Register (MDT1 Low) µP-write Address: 02_H

bit	7	6	5	4	3	2	1	0
	MF_EN	MODE(2:0)			MOSEL(1:0)		RD	WR

Note: For the meaning of the bits, refer to "TRANSIU Initialization Channel Command Register" on page 6-15. 'x'=unused

11.6.1.4 GHDLC Configuration Command (0x14)

Mailbox Register (MGEN Low) µP-write Address: 42_H

bit	7	6	5	4	3	2	1	0
							GCA1	GCA0

GCA1..0 GHDLC Channel Address

00 = GHDLC Channel 0 (all other combinations are reserved)

Mailbox Register (MDT0 Low) µP-write Address: 00_H

bit	7	6	5	4	3	2	1	0
							ADM	AUTO

AUTO Auto Mode Enable

0 = Disable Auto Mode

1 = Enable Auto Mode

ADM Address Mode

0 = 8-bit address mode

1 = 16-bit address mode

Mailbox Register (MDT1) µP-write Address: $02+03_H$

bit	7	6	5	4	3	2	1	0
High	AAD(15:8)							

bit	7	6	5	4	3	2	1	0
Low	AAD(7:0)							

AAD15..0 Address for address recognition **(ELIC reg. RAL1 and RAH1)**

Note: If ADM is set to 0 (8-bit address) only the low part is considered

Mailbox Register (MDT2) µP-write Address: $04+05_H$

bit	7	6	5	4	3	2	1	0
High	BAD(15:8)							

bit	7	6	5	4	3	2	1	0
Low	BAD(7:0)							

BAD15..0 Broadcast address **(ELIC reg. RAL2 and RAH2)**

Note: If ADM is set to 0 (8-bit address) only the low part is considered

11.6.1.5 Finish Initialization Command (0x06)

This command has to be issued after downloading program and data and configuring the DELIC correctly. It forces the DELIC to start with all tasks.

Mailbox Register (MCMD) µP-write Address: 40_H

bit	7	6	5	4	3	2	1	0
	0	0	0	0	0	1	1	0

11.6.2 Configuration Indications

11.6.2.1 IOM-2000 Far-end Code Violation Indication (0x07)

This indication reports a far-end code violation (FECV) in the specified VIP channel.

Parameter:

– IOM-2000 VIP and channel number

Mailbox Register (OGEN High) µP-read Address: 63_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of entries in ODT0..7(15) (range: 1..16(32))

For every entry (one byte per entry):

Mailbox Register (ODT0..7(15)) µP-read

bit	7	6	5	4	3	2	1	0
	FECV			SAD4	SAD3	SAD2	SAD1	SAD0

SAD4..0 Subscriber Address i.e. IOM-2000 VIP and channel number

FECV Far-end Code Violation

0 = No far-end code violation detected

1 = Far-end code violation (bit error) detected

11.6.2.2 IOM-2000 Delay Indication (0x04)

This indication returns the measured line delay value of an U_{PN} channel. This indication is the answer to the IOM-2000 Delay Measurement Command (0x04).

Parameter:

– IOM-2000 VIP and channel number
– Delay Value

Mailbox Register (OGEN High) µP-read Address: 63_H

bit	15	14	13	12	11	10	9	8
				SAD4	SAD3	SAD2	SAD1	SAD0

SAD4..0 Subscriber Address i.e. IOM-2000 VIP and channel number

Mailbox Register (OGEN Low) µP-read Address: 62_H

bit	7	6	5	4	3	2	1	0
	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0

DV7..0 Delay Value

Note: This command is only applicable for channels in U_{PN} Mode

11.6.2.3 Finish VIP Channel Configuration Indication (0x02)

After issuing the IOM-2000 VIP Channel Configuration Command (0x03) with set read bit the DELIC confirms the command by this indication.

Mailbox Register (ODT0 High) µP-read Address: 21_H

bit	15	14	13	12	11	10	9	8
	x	VIPADR(1:0)		CHADR(2:0)			FIL	EXLP

Mailbox Register (ODT0 Low) µP-read Address: 20_H

bit	7	6	5	4	3	2	1	0
	PLLS	PD	DHEN	x	x	PDOWN	LOOP	TX_EN

Mailbox Register (ODT1 High) µP-read Address: 23_H

bit	15	14	13	12	11	10	9	8
	PLLINT	AAC(1:0)		BBC(1:0)		OWIN(2:0)		

Mailbox Register (ODT1 Low) µP-read Address: 22_H

bit	7	6	5	4	3	2	1	0
	MF_EN	MODE(2:0)			MOSEL(1:0)		RD	WR

Note: For the meaning of the bits, refer to "TRANSIU Initialization Channel Status Register (TICSTR)" on page 6-20. 'x'=unused

11.7 IOM-2 C/I Handling

Purpose of the C/I handler is to transmit C/I values and to receive C/I value changes on the C/I channels. The C/I values itself are not interpreted.

A new C/I value will be considered if it is detected for at least two consecutive frames (double last look).

The DELIC considers all channels affected by at least one C/I value change. After detecting the first change the DELIC reports it to the µP. As soon as the mailbox is free the DELIC sends the current C/I values of the affected channels, together with their addresses, to the µP. If the µP is fast enough to serve the interrupts every change will be reported. But if the µP is not as fast preceding changes according to the same channel will be lost (**Figure 11-6**).

11.7.1 IOM-2 C/I Command

The following command is sent from the µP to the DELIC.

11.7.1.1 Write C/I Value Command (0x23)

(ELIC Reg.: MACR, MADR, MAAR)
This command provides the DELIC with new C/I values to be sent on the specified channels. It can be issued any time.

Parameter:

– Amount of following entries

For every entry:

- IOM-2 port and channel number
- C/I value

See "Common Mailbox Parameter Structure" on page 11-27

11.7.2 IOM-2 C/I Indication

The following indication is sent from the DELIC to the µP.

11.7.2.1 Change Detected Indication (0x41)

If at least one change is detected this indication will be issued. The amount of entries depends on the mailbox size and the amount of used IOM-2 channels. Maximum values of 8 entries (if DMA is used) or 16 (if DMA is not used) are possible.

Parameter:

– Amount of following entries

For every entry:

- IOM-2 port and channel number
- C/I value

See "Common Mailbox Parameter Structure" on page 11-27

11.7.3 Common Mailbox Parameter Structure

Both command and indication have the same structure.

Mailbox Register (MGEN High) µP-write Address: 43_H

Mailbox Register (OGEN High) µP-read Address: 63_H

bit	7	6	5	4	3	2	1	0
				(SIZE4)	SIZE3	SIZE2	SIZE1	SIZE0

SIZE4..0 Amount of valid entries in MDT0..7(15) or ODT0..7(15) (range: 1..8(16))

For every entry (two bytes per entry):

Mailbox Register (MDT0..7(15) Low) µP-write

Mailbox Register (ODT0..7(15) Low) µP-read

bit	7	6	5	4	3	2	1	0
					SAD3	SAD2	SAD1	SAD0

SAD3..0 Subscriber Address i.e. IOM-2 port and channel number

Mailbox Register (MDT0..7(15) High) µP-write

Mailbox Register (ODT0..7(15) High) µP-read

bit	7	6	5	4	3	2	1	0
			CI5	CI4	CI3	CI2	CI1	CI0

CI5..0 6-bit C/I value

CI3..0 4-bit C/I value

11.7.4 Flow Diagram

The following diagram describes the way of handling C/I value changes. It is assumed that the mailbox is not free as the first change was detected. After releasing the mailbox by the µP the DELIC sends the C/I values and their IOM-2 channel addresses. The preceding change on channel 6 will not be reported.

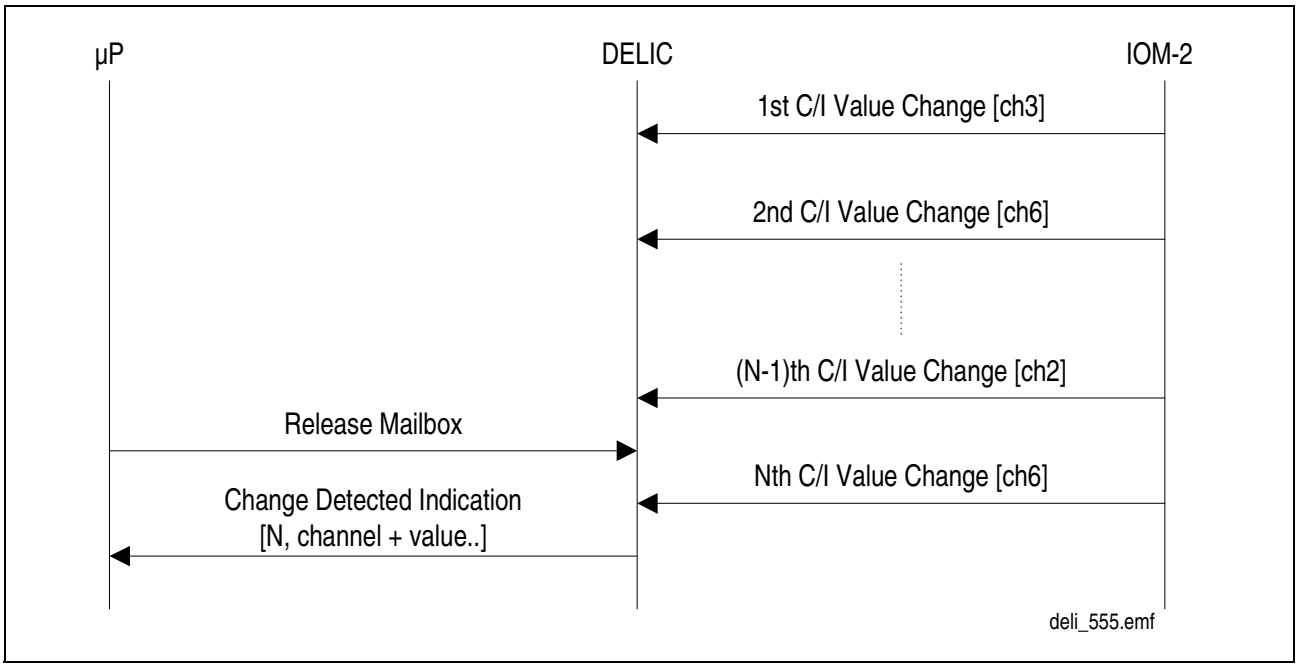


Figure 11-6 C/I Flow Diagram: Receiving C/I Value Changes

11.8 IOM-2 Monitor Handling

According to the monitor channels the DELIC has to manage the data exchange between IOMU and mailbox. Only one of all possible channels is served at the same time. The main task of the DELIC is to transform an acknowledged block stream from and to the mailbox to an acknowledged byte stream from and to the IOMU. If the µP issues a command it has to wait for the related indication before the next command can be issued.

11.8.1 IOM-2 Monitor Commands

The following commands are sent from the µP to the DELIC:

11.8.1.1 Search On Command (0x2B)

(ELIC bit: MFSO)
By this command the DELIC is instructed to search for an active monitor channel. After finding an active channel the search mechanism is stopped and the event is reported with Monitor Active Indication. This command can be issued any time. If there is a transmission command in progress the Search Mode is started after transmission was terminated.

11.8.1.2 Search Reset Command (0x2C)

(ELIC bit: OMSO)
By this command the Search Mode is stopped. This command can be issued any time. It will not stop a running transmission.

11.8.1.3 Monitor Reset Command (0x2D)

(ELIC bit: MFFR)
By this command the execution of the current transfer command is stopped immediately.

11.8.1.4 Transmit Continuous Command (0x29)

(ELIC bits: MFT1..0)
This command starts transmission of one of more blocks. The Search Mode is suspended until transmission was terminated. After acknowledging the last sent byte Transfer Ready is issued to ask for a new block. The size of the blocks is variable. The last block is sent with Transmit or Transmit & Receive. Only with the first appearance of this command the first parameter will be considered.

Parameter:

– IOM-2 port and channel number
– Size of data block
– Data block

See "Common Mailbox Parameter Structure" on page 11-32

11.8.1.5 Transmit Command (0x28)

(ELIC bits: MFT1..0)
This command starts transmission of a single/last block. The Search Mode is suspended until transmission was terminated. After transmission was completed (rising edge of MR) Transfer Ready is issued. If this command follows after Transmit Continuous the first parameter will be ignored.

Parameter:

– IOM-2 port and channel number
– Size of data block
– Data block

See "Common Mailbox Parameter Structure" on page 11-32

11.8.1.6 Transmit&Receive/Receive Only Command (0x2A)

(ELIC bits: MFT1..0)
This command starts transmission of a single/last block and waits for reception on the same channel. The Search Mode is suspended during transmission and reception. If this

command follows after Transmit Continuous the first parameter will be ignored. Received blocks are reported with Receive and/or Receive Continuous. If size of data is zero the command has the meaning of Receive Only i.e. reception on the specified channel is activated.

Parameter:

– IOM-2 port and channel number
– Size of data block
– Data block

See "Common Mailbox Parameter Structure" on page 11-32

11.8.2 IOM-2 Monitor Indications

The following indications are sent from the DELIC to the µP.

11.8.2.1 Transfer Ready Indication (0x53)

(ELIC bit: MFFI)
Indicates end of Transmit or end of Transmit Broadcast or asks for a new block after Transmit Continuous.

11.8.2.2 Receive Continuous Indication (0x52)

(ELIC bit: MFFI)
This indication reports one of more received blocks to the µP. The reception has not been terminated yet.

Parameter:

– Size of data block
– Data block

Mailbox Register (OGEN High) µP-read Address: 63_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of following data bytes within ODT0..7(15) (range: 1..16(32))

11.8.2.3 Receive Indication (0x51)

(ELIC bits: MFFI, MFFE)
The only/last received block is reported to the µP.

Parameter:

– Size of data block
– Data block

Mailbox Register (OGEN High) µP-read Address: 63_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of following data bytes within ODT0..7(15) (range: 1..16(32))

11.8.2.4 Transmit Abort Indication (0x55)

(ELIC bit: MFAB)
The remote receiver aborted reception of a locally issued Transmit Command.

11.8.2.5 Monitor Active Indication (0x54)

(ELIC bit: MAC)
Informs the µP that an active monitor channel has been found. The µP may issues Receive Only to activate the receiver.

Parameter:

– IOM-2 port and channel number

Mailbox Register (OGEN Low) µP-read Address: 62_H

Reset value: unchanged

bit	7	6	5	4	3	2	1	0
					SAD3	SAD2	SAD1	SAD0

SAD3..0 Subscriber Address i.e. IOM-2 port and channel number (up to 16 channels)

11.8.3 Common Mailbox Parameter Structure

This structure is valid for Transmit Continuous Command (0x29), Transmit Command (0x28), Transmit&Receive/Receive Only Command (0x2A).

Mailbox Register (MGEN Low) µP-write Address: 42_H

bit	7	6	5	4	3	2	1	0
					SAD3	SAD2	SAD1	SAD0

SAD3..0 Subscriber Address i.e. IOM-2 port and channel number (up to 16 channels)

Mailbox Register (MGEN High) µP-write Address: 43_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of following data bytes within MDT0..7(15) (range: 1..16(32))

11.8.4 Flow Diagrams

The following flow diagrams describe the way the DELIC transforms the protocols. N and M are always less or equal the mailbox size and less or equal the buffer size.

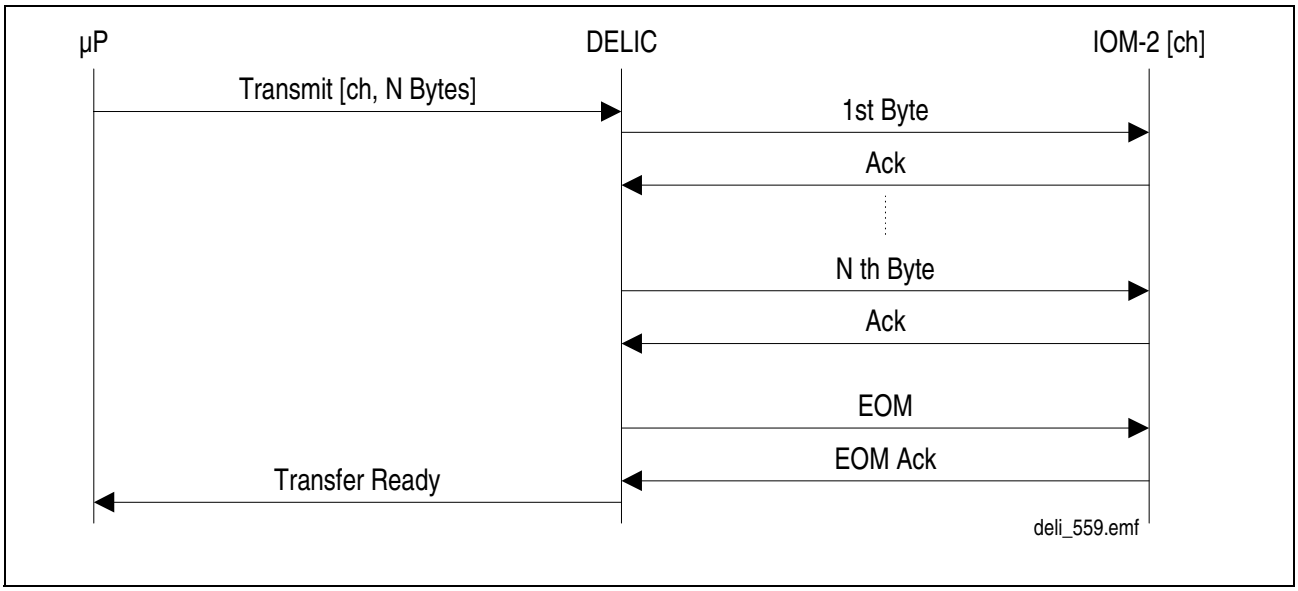


Figure 11-7 Monitor Flow Diagram: Transmit

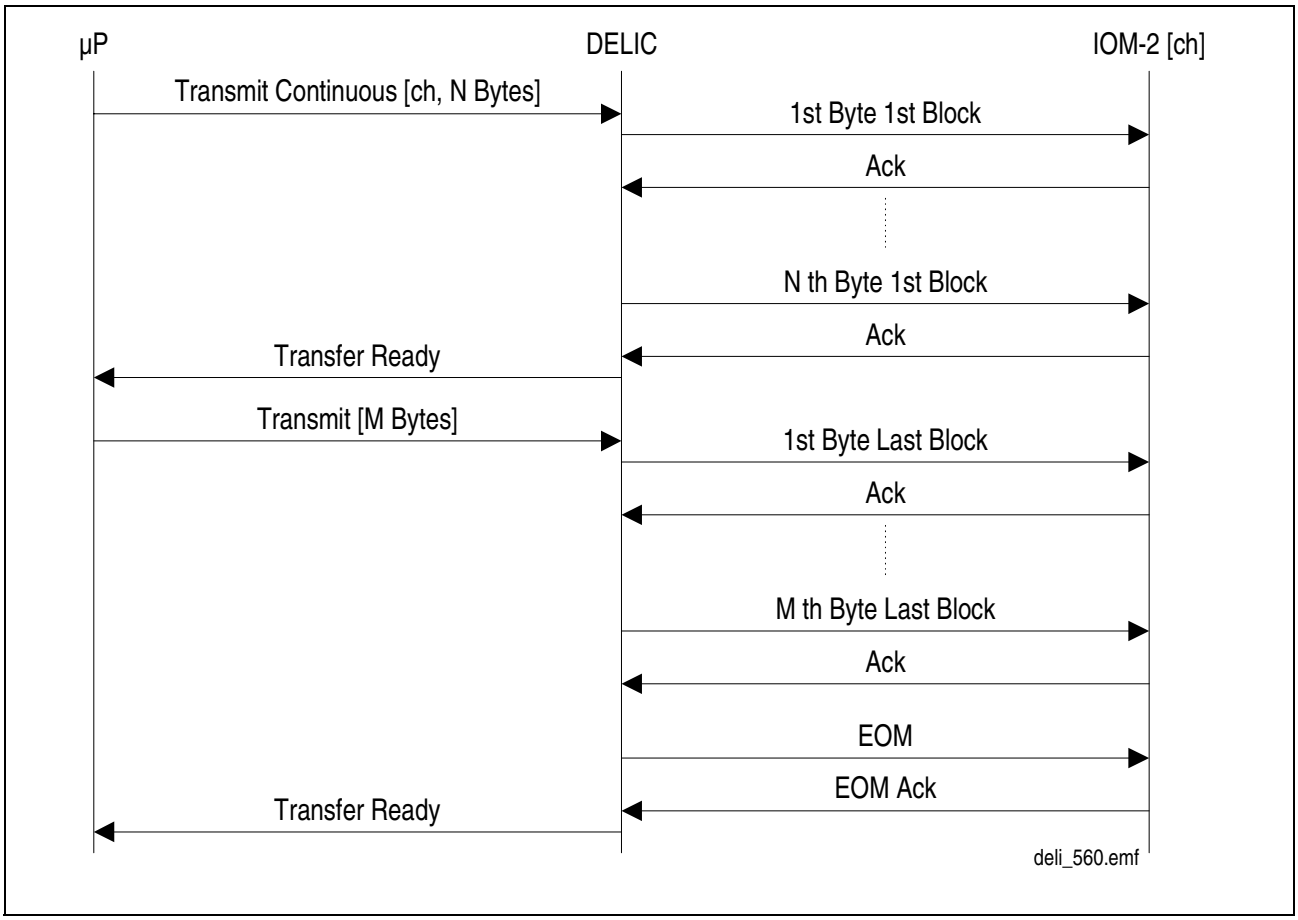


Figure 11-8 Monitor Flow Diagram: Transmit Continuous

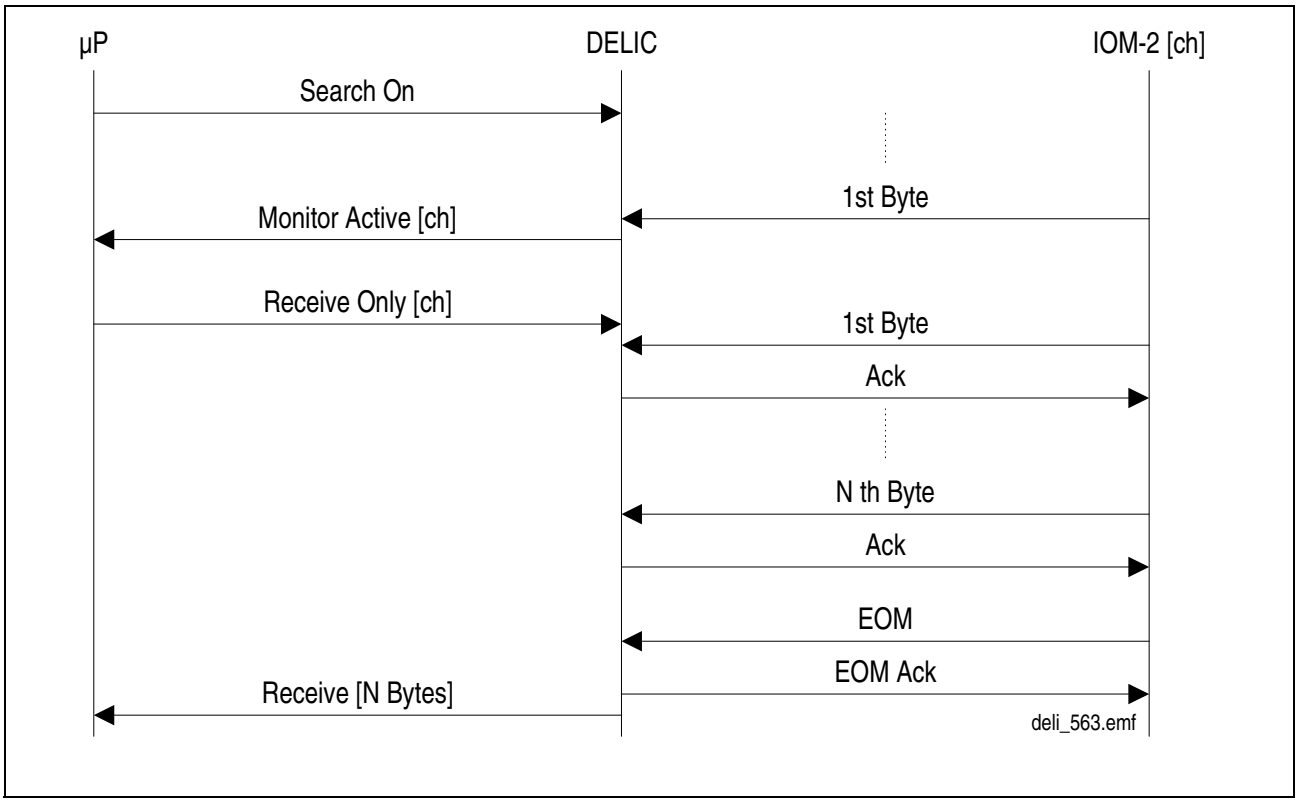


Figure 11-9 Monitor Flow Diagram: Search Mode

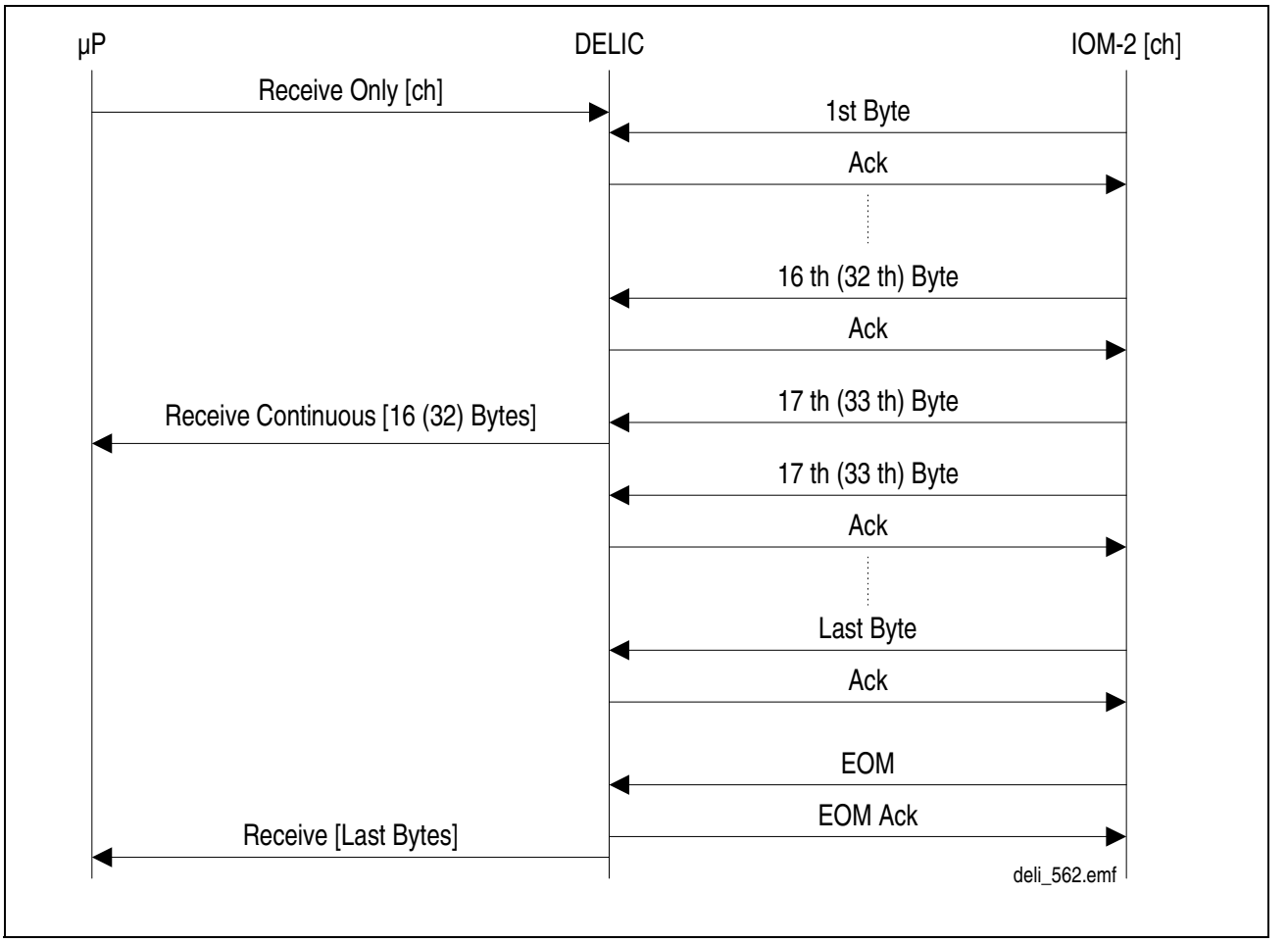


Figure 11-10 Monitor Flow Diagram: Receive Only with Receive Continuous

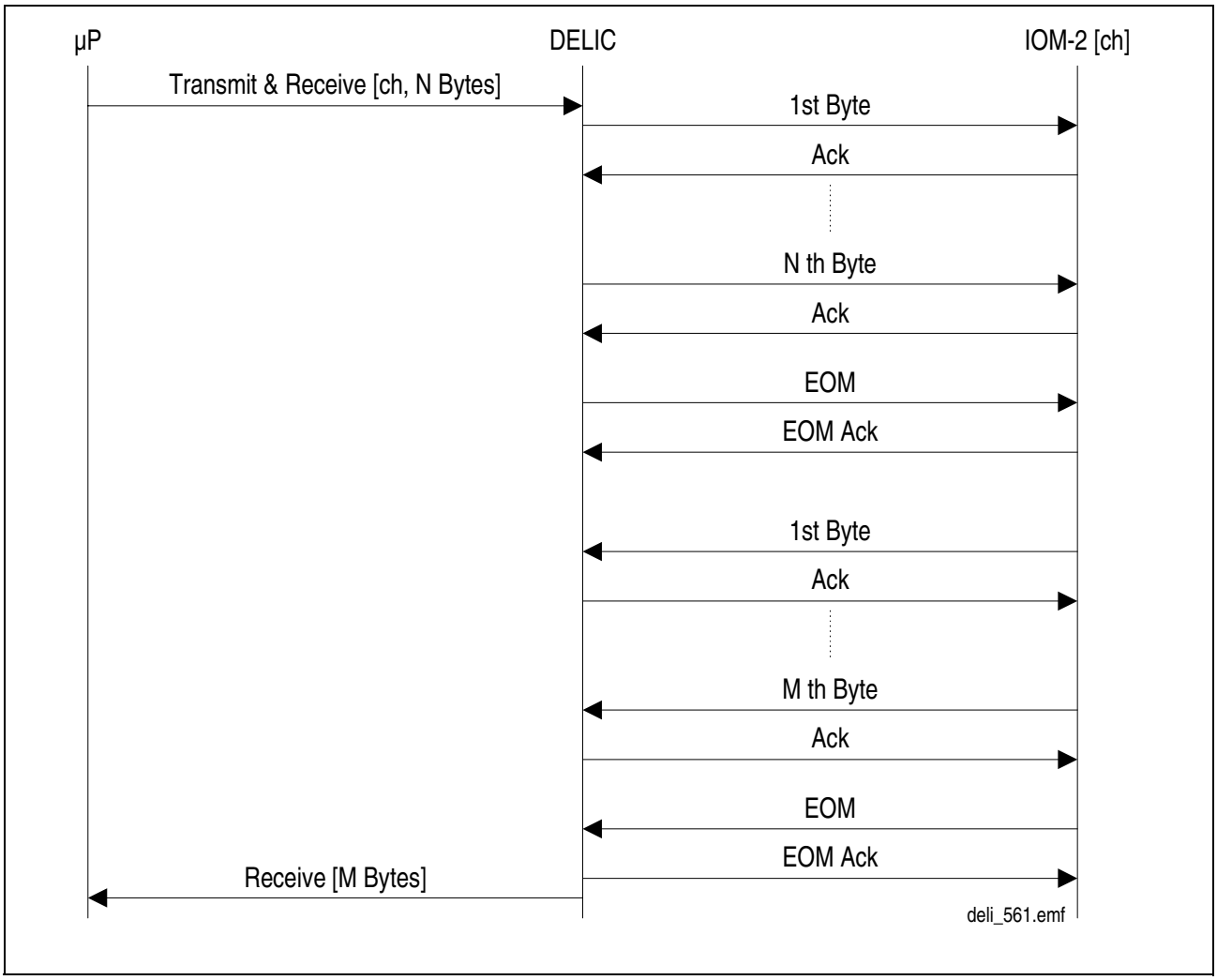


Figure 11-11 Monitor Flow Diagram: Transmit & Receive

11.9 IOM-2000 C/I Handling

The layer 1 state machine is accessed the same way as the C/I channels.

11.9.1 IOM-2000 C/I Command

The following command is sent from the µP to the DELIC:

11.9.1.1 Write C/I Value Command (0x0B)

This command provides the DELIC with new C/I values to be sent on the specified channels. It can be issued any time.

Parameter:

– Amount of following entries

For every entry:

– IOM-2000 VIP and channel number
– C/I value

See "Common Mailbox Parameter Structure" on page 11-38

11.9.2 IOM-2000 C/I Indication

The following indication is sent from the DELIC to the µP.

11.9.2.1 Change Detected Indication (0x11)

If at least one change is detected this indication will be issued. The amount of entries depends on the mailbox size and the amount of used IOM-2000 channels. Maximum values of 8 entries (if DMA is used) or 16 (if DMA is not used) are possible.

Parameter:

– Amount of following entries

For every entry:

– IOM-2000 VIP and channel number
– C/I value

See "Common Mailbox Parameter Structure" on page 11-38

11.9.3 Common Mailbox Parameter Structure

Both command and indication use the same structure.

Mailbox Register (MGEN High) µP-write Address: 43_H

Mailbox Register (OGEN High) µP-read Address: 63_H

bit	7	6	5	4	3	2	1	0
				(SIZE4)	SIZE3	SIZE2	SIZE1	SIZE0

SIZE4..0 Amount of valid entries in MDT0..7(15) or ODT0..7(15) (range: 1..8(16))

For every entry (two bytes per entry):

Mailbox Register (MDT0..7(15) Low) µP-write

Mailbox Register (ODT0..7(15) Low) µP-read

bit	7	6	5	4	3	2	1	0
				SAD4	SAD3	SAD2	SAD1	SAD0

SAD4..0 Subscriber Address i.e. IOM-2000 VIP and channel number

Mailbox Register (MDT0..7(15) High) µP-write

Mailbox Register (ODT0..7(15) High) µP-read

bit	7	6	5	4	3	2	1	0
					CI3	CI2	CI1	CI0

CI3..0 C/I value

11.10 HDLC Handling

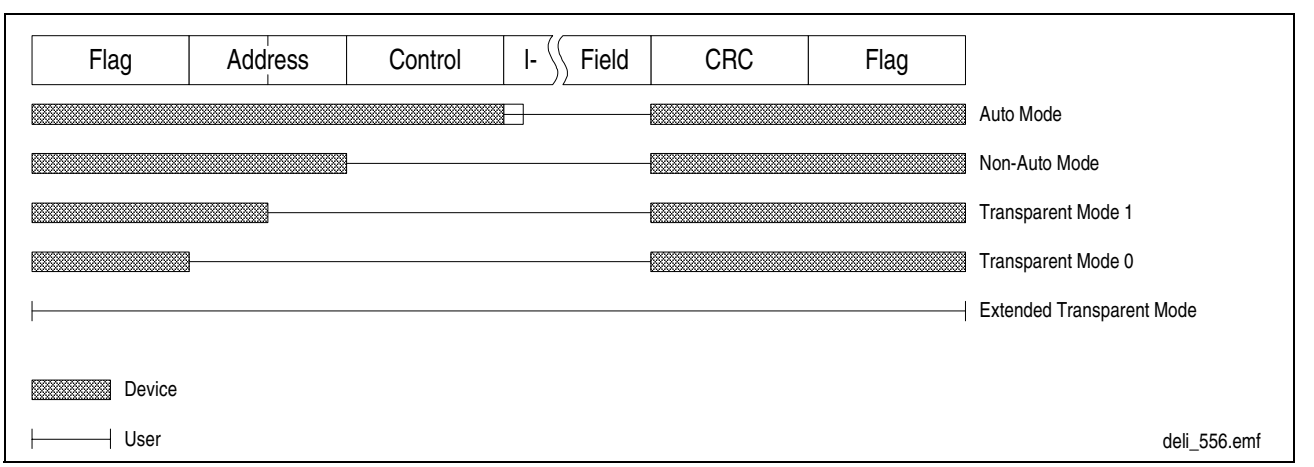


Figure 11-12 HDLC Frame Structure

11.10.1 HDLC Commands

The following commands are sent from the µP to the DELIC.

11.10.1.1 Reset Command (0x1F)

This command resets the specified HDLC controllers.

Parameter:

– Amount of following entries

For every entry:

– HDLC channel address
– Receiver or transmitter or both

Mailbox Register (MGEN High) µP-write Address: 43_H

bit	7	6	5	4	3	2	1	0
				(SIZE4)	SIZE3	SIZE2	SIZE1	SIZE0

SIZE4..0 Amount of following entries within MDT0..7(15) (range: 1..8(12))

For every entry (two bytes per entry):

Mailbox Register (MDT0..7(15) Low) µP-write

bit	7	6	5	4	3	2	1	0
				HCA4	HCA3	HCA2	HCA1	HCA0

HCA4..0 HDLC Channel Address

Mailbox Register (MDT0..7(15) High) µP-write

bit	7	6	5	4	3	2	1	0
				RX				TX

TX Transmitter will be reset **(ELIC bit XRES)**

0 = No action

1 = Reset

RX Receiver will be reset **(ELIC bit RHR)**

0 = No action

1 = Reset

11.10.1.2 Transmit Command (0x1D)

(ELIC bits: XTF, XME)
This command initiates sending of a single message or the last block of a long message. After transmission Transmit Ready will be issued.

Parameter:

– HDLC channel address
– Amount of data bytes
– Data bytes

See "Common Mailbox Parameter Structure" on page 11-44

11.10.1.3 Transmit Continuous Command (0x1E)

(ELIC bit: XTF)
This command allows sending of one of more blocks. The last block has to be sent with the Transmit Command. The next block is requested by Transmit Ready Indication.

Parameter:

– HDLC channel address
– Amount of data bytes
– Data bytes

See "Common Mailbox Parameter Structure" on page 11-44

11.10.1.4 Activation/Deactivation Command (0x20)

(ELIC bit: RAC)
The command activates or deactivates the specified HDLC channel.

Parameter:

– Amount of following entries

For every entry:

– HDLC channel address

Mailbox Register (MGEN High) µP-write Address: 43_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of following bytes within MDT0..7(15) (range: 1..16(32))

For every entry (one byte per entry):

Mailbox Register (MDT0..7(15)) µP-write

bit	7	6	5	4	3	2	1	0
	D			HCA4	HCA3	HCA2	HCA1	HCA0

HCA4..0 HDLC Channel Address

D Activation/Deactivation bit

0 = Activate HDLC channel

1 = Deactivate HDLC channel

Note: Both receiver and transmitter are activated/deactivated

11.10.2 HDLC Indications

The following indications are sent from the DELIC to the µP.

11.10.2.1 Error Indication (0x34)

This indication reports HDLC errors to the µP.

Parameter:

– HDLC channel address
– Error code

According to the receiver following errors can occur: Abort, CRC-Check failure, byte not complete, address recognition error, receive buffer overflow, extended HDLC frame (i.e. neither a RR nor an I frame in Auto Mode).

According to the transmitter following errors can occur: underflow of the transmit buffer, repeat request according to long messages (long frame polled twice, collision after first block).

Mailbox Register (OGEN Low) µP-read Address: 62_H

bit	7	6	5	4	3	2	1	0
				HCA4	HCA3	HCA2	HCA1	HCA0

HCA4..0 HDLC Channel Address

Mailbox Register (ODT0 Low) µP-read Address: 20_H

bit	7	6	5	4	3	2	1	0
		TXE2	TXE1	TXE0		RXE2	RXE1	RXE0

RXE2..0 Receiver Error Codes

001 = Abort **(ELIC bits VFR, RAB)**

010 = CRC check failure **(ELIC bit CRC)**

011 = Non octet **(ELIC bit VFR)**

100 = Address recognition error **(ELIC bits HA1..0)**

101 = Frame too short **(ELIC bit VFR)**

110 = Receive buffer overflow **(ELIC bits RFO, RDO)**

111 = Extended HDLC frame (Auto Mode: neither RR nor I frame) **(ELIC bit EHC)**

TXE2..0 Transmitter Error Codes

001 = Transmit buffer underflow **(ELIC bits XDU, EXE)**

010 = Repeat Request **(ELIC bit XMR)**

011 = Transmit buffer overflow

100 = Collision Detected

11.10.2.2 Transmit Ready Indication (0x33)

(ELIC bit XPR)
This indication informs the µP which HDLC controller finished the last transmit command.

Parameter:

– HDLC channel address

Mailbox Register (OGEN Low) µP-read Address: 62_H

bit	7	6	5	4	3	2	1	0
				HCA4	HCA3	HCA2	HCA1	HCA0

HCA4..0 HDLC Channel Address

11.10.2.3 Receive Indication (0x31)

(ELIC bit RME)
This indication reports a single or the last received block to the µP.

Parameter:

– HDLC channel address
– Amount of data bytes
– Data bytes

See "Common Mailbox Parameter Structure" on page 11-44

11.10.2.4 Receive Continuous Indication (0x32)

(ELIC bit RPF)
This indication sends a received block to the µP. More data follows. The last block will be sent with Receive Indication.

Parameter:

– HDLC channel address
– Amount of data bytes
– Data bytes

See "Common Mailbox Parameter Structure" on page 11-44

11.10.3 Common Mailbox Parameter Structure

The following structure is valid for following commands or indications respectively:

Transmit Command (0x1D), Transmit Continuous Command (0x1E), Receive Indication (0x31), Receive Continuous Indication (0x32).

Mailbox Register (MGEN Low) µP-write Address: 42_H

Mailbox Register (OGEN Low) µP-read Address: 62_H

bit	7	6	5	4	3	2	1	0
				HCA4	HCA3	HCA2	HCA1	HCA0

HCA4..0 HDLC Channel Address

Mailbox Register (MGEN High) µP-write Address: 43_H

Mailbox Register (OGEN High) µP-read Address: 63_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of following data bytes within MDT0..7(15) or ODT0..7(15)

Note: A SIZE value of '0' stands for a byte count of zero data bytes. Thus the width of SIZE is 5 bits to include a mailbox transfer of 16 data bytes, or 6 bits to include a mailbox transfer of 32 data bytes.

11.10.4 Flow Diagrams

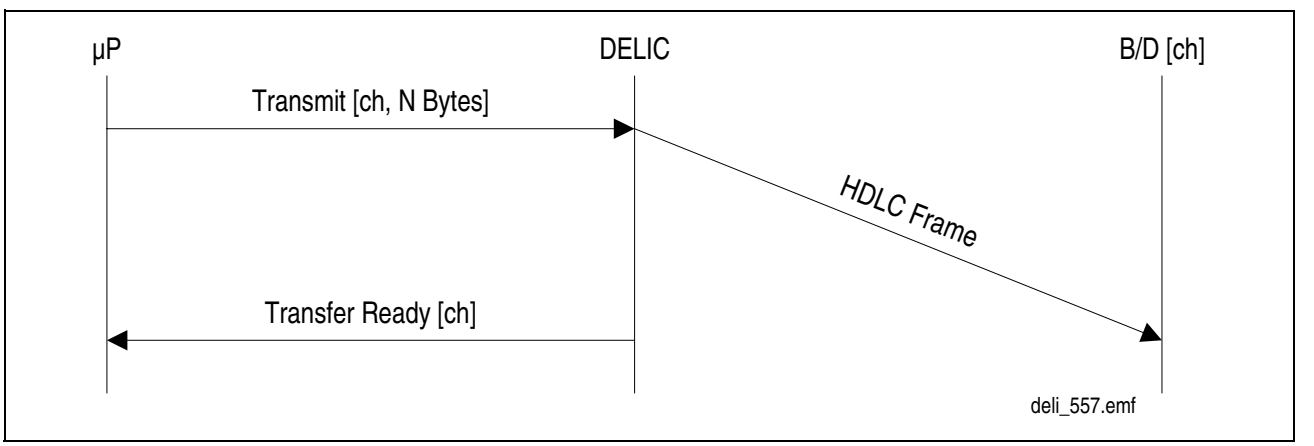


Figure 11-13 HDLC Flow Diagram: Transmit

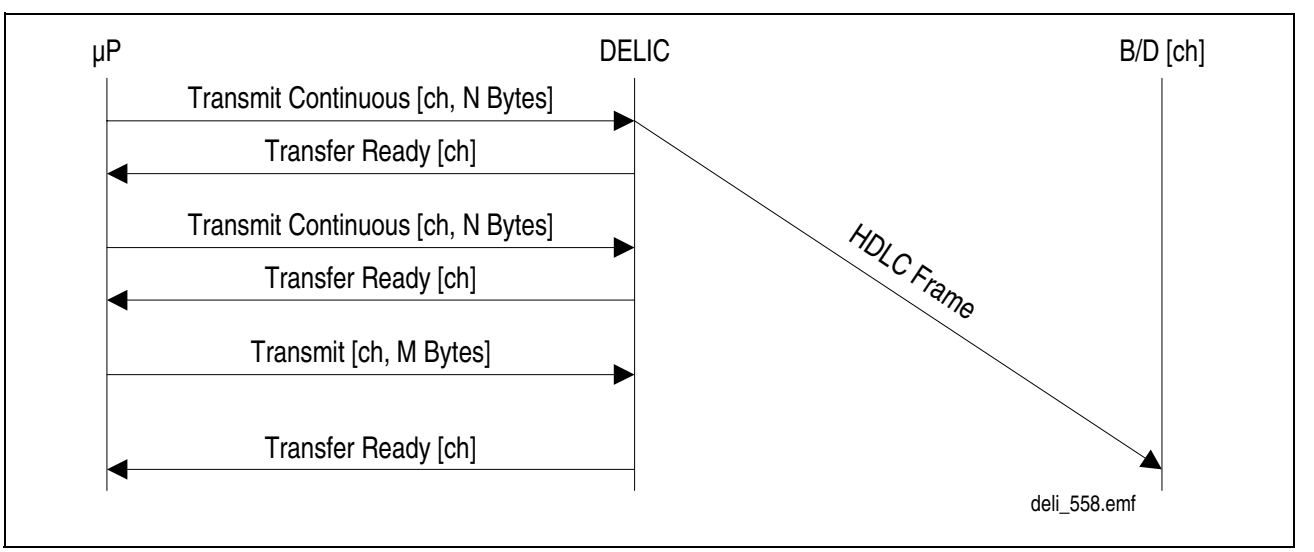


Figure 11-14 HDLC Flow Diagram: Transmit Continuous

11.11 GHDLC Handling

According to the commands and indications the same parameter structure as in HDLC handling is used. The only difference is that HCA4..0 (HDLC channel address) is called GCA1..0 (GHDLC channel address).

11.11.1 GHDLC Commands

11.11.1.1 Reset Command (0x15)

This command resets the specified GHDLC channel.

Parameter:

– Amount of following entries

For every entry:

– GHDLC channel address

Mailbox Register (MGEN High) µP-write Address: 43_H

bit	7	6	5	4	3	2	1	0
							SIZE1	SIZE0

SIZE1..0 Amount of following bytes within MDT0..7(15)

For every entry (one byte per entry):

Mailbox Register (MDT0 and MDT1) µP-write

bit	7	6	5	4	3	2	1	0
							GCA1	GCA0

GCA1..0 GHDLC Channel Address

11.11.1.2 Transmit Command (0x11)

Parameter:

- GHDLC channel address
- Transmit prepared or direct data
- Enable/Disable auto repeat
- Amount of data bytes
- Data bytes

Mailbox Register (MGEN Low) µP-write Address: 42_H

bit	7	6	5	4	3	2	1	0
	XPD/ XDD	AREP					GCA1	GCA0

XPD/XDD Transmit prepared or direct data (Auto Mode only)

0 = Transmit direct data

1 = Transmit prepared data

AREP Auto Repeat Enable

0 = Disable Auto Repeat

1 = Enable Auto Repeat

GCA1..0 GHDLC Channel Address

00= GHDLC Channel 0 (all other combinations are reserved)

Mailbox Register (MGEN High) µP-write Address: 43_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of data bytes within MDT0..7(15) (range: 1..16(32))

11.11.1.3 Transmit Continuous Command (0x12)

Parameter:

– GHDLC channel address
– Amount of data bytes
– Data bytes

Mailbox Register (MGEN Low) µP-write Address: 42_H

bit	7	6	5	4	3	2	1	0
							GCA1	GCA0

GCA1..0 GHDLC Channel Address

00= GHDLC Channel 0 (all other combinations are reserved)

Mailbox Register (MGEN High) µP-write Address: 43_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of data bytes within MDT0..7(15) (range: 1..16(32))

11.11.2 GHDLC Indications

11.11.2.1 Error Indication (0x24)

For the structure see "Error Indication (0x34)" on page 11-42 and replace HCA4..0 (HDLC channel address) with GCA1..0 (GHDLC channel address).

11.11.2.2 Fatal Error Indication (0x25)

This indication reports the status of the GHDLC unit to the µP in case of an error.

Parameter:

– GHDLC channel address
– Status of GHDLC channel

Mailbox Register (OGEN Low) µP-read Address: 62_H

bit	7	6	5	4	3	2	1	0
							GCA1	GCA0

GCA2..0 GHDLC Channel Address

Mailbox Register (ODT0 High) µP-read Address: 21_H

bit	7	6	5	4	3	2	1	0
	x	x	x	x	x	x	COLLD	UNDER

Mailbox Register (ODT0 Low) µP-read Address: 20_H

bit	7	6	5	4	3	2	1	0
	EMPTY	OVER	FULL	RBFILL(4:0)				

Note: For the meaning of the bits, refer to "GHDLC Receive Channel Status Registers 0..3" on page 6-40

11.11.2.3 Transmit Ready Indication (0x23)

For the structure see "Transmit Ready Indication (0x33)" on page 11-43 and replace HCA4..0 (HDLC channel address) with GCA1..0 (GHDLC channel address).

11.11.2.4 Receive Indication (0x21)

For the structure see "Receive Indication (0x31)" on page 11-44 and replace HCA4..0 (HDLC channel address) with GCA1..0 (GHDLC channel address).

11.11.2.5 Receive Continuous Indication (0x22)

For the structure see "Receive Continuous Indication (0x32)" on page 11-44 and replace HCA4..0 (HDLC channel address) with GCA1..0 (GHDLC channel address).

11.12 B-Channel Switching

(ELIC registers MAAR, MADR, MACR)
Purpose of the switching task is to manage connections between time slots i.e. to transfer data between memory locations. To every connection an identification is assigned in order to make fast disconnection possible and to avoid hole handling within the used connection table.

The connection information can be read back with the "Read Register Command (0x02)" on page 11-17. The internal connection table (base address t.b.d.) contains consecutive entries consisting of two consecutive 16-bit values each determining the source (first word) and destination (second word) time slot address. The actual time slot can be recalculated with the following table.

Table 11-18 Time Slot Address Ranges

Unit	Direction	Address Range	Time Slot Range
IOM-2	Receive Transmit	0x8000..0x803F 0x8040..0x807F	0..63 0..63
IOM-2000	Receive Transmit	0x6000..0x607F 0x6080..0x80FF	0..127 0..127
PCM	Receive Transmit	0xA000..0xA07F 0xA080..0xA0FF	0..127 0..127

11.12.1 Switching Commands

The following commands are sent from the µP to the DELIC:

11.12.1.1 8-bit Connect Command (0x17)

This command creates or overwrites a connection between two time slots.

Parameter:

– Amount of following entries

For every entry:

– Connection Identifier
– Source unit
– Source TS
– Destination unit
– Destination TS

Mailbox Register (MGEN High) µP-write Address: 43_H

bit	7	6	5	4	3	2	1	0
					(SIZE3)	SIZE2	SIZE1	SIZE0

SIZE3..0 Amount of following entries within MDT0..7(15) (range: 1..4(8))

For every entry (four bytes per entry):

Mailbox Register (MDT[x] Low) µP-write

bit	7	6	5	4	3	2	1	0
	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7..0 Connection Identification

Mailbox Register (MDT[x] High) µP-write

bit	7	6	5	4	3	2	1	0
		DIT2	DIT1	DIT0		SIT2	SIT1	SIT0

SIT2..0 Source Interface Type

001 = IOM-2

010 = IOM-2000

100 = PCM

DIT2..0 Destination Interface Type

001 = IOM-2

010 = IOM-2000

100 = PCM

Mailbox Register (MDT[x+1] Low) µP-write

bit	7	6	5	4	3	2	1	0
	STSN7	STSN6	STSN5	STSN4	STSN3	STSN2	STSN1	STSN0

STSN7..0 Source Time Slot Number

Mailbox Register (MDT[x+1] High) µP-write

bit	7	6	5	4	3	2	1	0
	DTSN7	DTSN6	DTSN5	DTSN4	DTSN3	DTSN2	DTSN1	DTSN0

DTSN7..0 Destination Time Slot Number

Note: Values for x are 0, 2, 4, 6, (8, 10, 12, 14)

11.12.1.2 8-bit Disconnect Command (0x18)

This command deactivates a connection between two time slots.

Parameter:

– Amount of following entries

For every entry:

– Connection Identifier

Mailbox Register (MGEN High) µP-write Address: 43_H

bit	7	6	5	4	3	2	1	0
			(SIZE5)	SIZE4	SIZE3	SIZE2	SIZE1	SIZE0

SIZE5..0 Amount of following bytes within MDT0..7(15) (range: 1..16(32))

For every entry (one byte per entry):

Mailbox Register (MDT0..7(15)) µP-write

bit	7	6	5	4	3	2	1	0
	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

ID7..0 Connection Identification

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13 Glossary

AHV-SLIC PEB 4165	High voltage part of SLIC
CMOS	Complementary Metal Oxide Semiconductor
CO	Central Office
CODEC	Coder Decoder
DC	Direct Current
DECT	Digital European Cordless Telecommunication
DELIC	DSP Embedded Line and Port Interface Controller (PEB 20570, PEB 20571)
DSL	Digital Subscriber Line
DSP	Digital signal processor
HDLC	High-level Data Link Control
IEEE	Institute of Electrical and Electronic Engineers
INFO	U- and S-interface signal as specified by ANSI/ETSI
I/O	Input/Output
IOM-2	ISDN-Oriented Modular 2nd generation
IOM-2000	Proprietary ISDN inferface for S/T and U_P
ISDN	Integrated services Digital Network
ITU	International Telecommunications Union
MUBIC PEB22521	MDSL transceiver
MuPP PEB 31665	16-channel CODEC digital front end part
µP	Micro Processor
OCTAT-P	OCTAl Transceiver for U_{PN}-Interfaces (PEB 2096)
LT-S	Line Termination-Subscriber
LT-T	Line Termination-Trunk
PLL	Phase-Locked Loop
PBX	Private Branch Exchange
QUAD-U PEB 2491	4-channel U-transceiver

QAP PEB 3465	Equivalent 4-channel analog front end part for MuPP
QUAT-S	QUAdrupleTransceiver for S/T-Interface (PEB 2084)
SLICOFI-2 PEB 3265	Dual channel CODEC + low voltage part of SLIC
S/T	Two-wire pair ISDN interface
TAP	Test Access Port
TBD	To Be Defined