



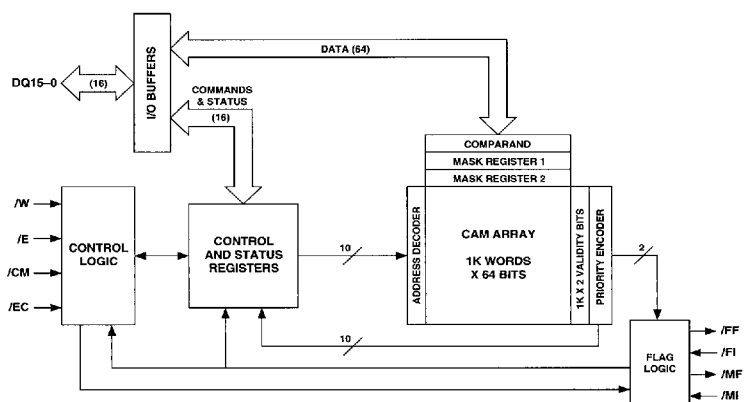
# MU9C1640 CacheCAM™

## DATA SHEET

### DISTINCTIVE CHARACTERISTICS

- 1024 X 64-bit Content-addressable Memory (CAM)
- Architecture similar to the industry standard MU9C1480 LANCAM® for ease of use
- Patented Associated Data feature allows storage of related data with each CAM entry that is immediately available after a match
- 64-bit internal data path multiplexed over a 16-bit I/O interface
- Simple four-wire synchronous control directly usable in conventional memory subsystems
- Memory Array width can be configured as a mixture of CAM and RAM on 16-bit boundaries
- Memory operations allow random access, associative access, and write-at-next-free-address cycles
- Extensive instruction set adds control flexibility
- Two Mask registers allow masking of individual bits for both writing and comparing
- Vertical cascading and system flag generation require no external logic
- Priority encoder returns Highest-priority Match address
- Device updates status information after each compare
- Two validity bits per entry for increased flexibility
- Manufactured in CMOS technology with TTL-compatible inputs and outputs
- Packaged in an industry-standard 44-pin PLCC package
- Also available on a CAMLAB™ board product that contains from one to four CacheCAMs with all the necessary support logic to allow direct use in any compatible PC with either an ISA or VL Bus

### BLOCK DIAGRAM



### GENERAL DESCRIPTION

Content-addressable Memories (CAMs), also known as Associative Memories, operate in the converse way to the much more familiar Random Access Memories. In a Random Access Memory, an address is an input to the device, and the output are the data stored at that address. In a CAM, data are an input and the output is a flag to indicate a match and the address of the matching data. This results in a device that can search large data bases for matching data in a short and identical time, no matter how many entries are in the data base. The fact that the data words to be searched can be up to 64 bits wide means that incredibly large address spaces can be searched rapidly and efficiently. A key feature of MUSIC's CacheCAM is a patented architecture that links associated data to the data entry which is available for use after a successful compare operation.

The MU9C1640 CacheCAM is a 1K X 64-bit CMOS Content-addressable Memory (CAM) that is configurable on 16-bit boundaries into CAM segments to support fully-associative data searches or look-ups such as might be required for virtual memories, optical and magnetic disk caches, data compressors, data base accelerators, or image processors. Additionally, the memory unused for CAM is configured as Random Access Memory (RAM.) This RAM memory is linked to the CAM memory entries so that it can be used for storage of associated data which can be easily retrieved.

A CAM operates by comparing simultaneously the data in all CAM memory locations to a data sample. It then returns an indication of whether or not one or more of the CAM locations contained data that matched the data sample. The data

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### GENERAL DESCRIPTION (CONT'D)

sample is loaded into the Comparand register by the user and is automatically compared to all valid CAM locations. Status of each CAM location is determined by two validity bits at each memory location. These two bits are encoded to render four validity conditions: Valid, Skip, Empty, and Random Access. The memory can be partitioned into CAM and a RAM segments on 16-bit boundaries, and by using one of the two available mask registers, the CAM/RAM partitioning can effectively be set at any arbitrary size between 0 and 64 bits.

The CacheCAM's internal data path is 64 bits wide for rapid internal comparison and data movement, with an external 16-bit multiplexed interface for low cost. Four

control signals and commands loaded into the Instruction register control device operation. CAM memory depth can be extended for large data bases by vertical cascading additional CacheCAMs in a daisy-chain fashion. No external logic is required for cascading. Both automatic and forced compares can be made with the CAM data with the corresponding RAM data immediately available. The Status register gives the results of Compares including all flags and addresses. Two mask registers are available which can be used in two different ways: to mask comparisons or to mask data writes. By the use of the random access validity flags, additional masks can be stored in the CacheCAM.

### PIN DESCRIPTIONS

Note that signal names that start with a slash ("/") are active low. All signals are TTL level signals implemented in CMOS technology. Never leave inputs floating. Due to its CAM architecture, large currents are drawn during compare operations, which mandate the use of good layout and bypassing techniques during design. Refer to the Electrical Characteristics section for more information.

#### **(DQ15–DQ0) (Data Bus, Common I/O, TTL)**

The DQ15–DQ0 lines convey data, commands and status to and from the MU9C1640. The direction and nature of the information that flows to or from the device is controlled by the states of /CM and /W.

#### **/E (Chip Enable, Input, TTL)**

The /E input enables the CacheCAM while LOW, registers the control signals /W, /CM, /EC on its falling edge and releases them on the rising edge, and clocks the Destination or Source Segment counter on its rising edge.

#### **/W (Write Enable, Input, TTL)**

The /W input selects the direction of data flow during a memory cycle. /W LOW selects a Write cycle, and /W HIGH selects a Read cycle.

#### **/CM (Data/Command Select, Input, TTL)**

The /CM input selects whether the input signals on DQ15–DQ0 are data or commands. /CM LOW selects Command cycles and /CM HIGH Data cycles.

#### **/EC (Enable Comparison, Input, TTL)**

The /EC signal performs two functions: The /EC input enables the /MF output to show the results of a comparison. If /EC is LOW at the falling edge of /E in a given cycle, the /MF output is enabled. Otherwise, the /MF output is held HIGH. The /EC signal also enables the /MF-/MI daisy-chain, which serves to select the Highest-priority Matching device in a string of CacheCAMs. Table 5 explains the effect the /EC signal on a device with and without a match. /EC must be HIGH during initialization.

#### **/MF (Match Flag, Output, TTL)**

If enabled in the control register, the /MF output goes LOW when one or more valid match(s) occurs during a Comparison cycle if the /EC line was registered LOW by the falling edge of /E at the start of the cycle. Valid match(s) can also be in higher priority devices in a daisy-chain. If disabled in the control register, the /MF output only depends on the /MI input of the device (/MF=/MI.)

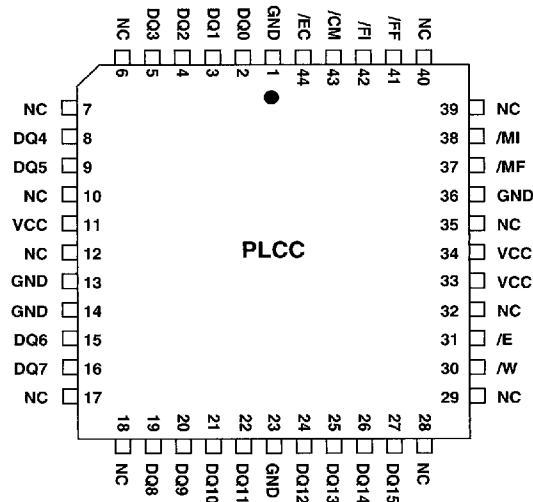
#### **/MI (Match Input, Input, TTL)**

The /MI input is used in vertically cascaded systems to prioritize devices. In a daisy-chained system, the /MF output of one device is connected to the /MI input of the next lower-priority device in the chain. The /MI of the highest priority device must be tied HIGH.

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### PINOUT DIAGRAM



### PIN DESCRIPTIONS (CONT'D)

#### /FF (Full Flag, Output, TTL)

If enabled in the control register, the /FF output indicates that no empty memory locations exist within the device (or daisy-chain above the device.) /FF LOW indicates Full. If disabled in the control register, the /FF output only depends on the /FI input (/FF = /FI.)

#### /FI (Full Input, Input, TTL)

The /FI input is used in vertically cascaded systems to generate a CAM-Memory-System-Full indication. In a

daisy-chained system, the /FF output of one device is connected to the /FI input of the next-lower priority device in the chain. The /FI of the highest priority device must be tied LOW.

#### VCC, GND (Positive Power Supply and Ground)

These pins are the power supply connections to the MU9C1640. VCC must meet the requirements in the Operating Conditions Section relative to the GND pin, which is at 0 Volts (system reference potential,) for correct operation of the device.

### FUNCTIONAL DESCRIPTION

The MU9C1640 CacheCAM is a 1K x 64-bit Content-addressable Memory (CAM) for virtual memory, cache, and table look-up applications, including data base machines, data compressors and image processors. The MU9C1640 contains 65,536 bits of static CAM, organized as 1024 64-bit Data fields. Each Data field can be partitioned into a CAM and a RAM subfield on 16-bit boundaries. The contents of the memory can be randomly accessed or associatively accessed by the use of a compare. During automatic Comparison cycles, data in the Comparand register is automatically compared with the "Valid" CAM section of the memory array.

The MU9C1640 is designed to minimize the external logic needed for expansion and control. It is controlled by four synchronous control signals, and by commands loaded into an Instruction decoder. The /CM signal is used to indicate whether information present on the 16-bit input bus is to be interpreted as a Data or a Command field. To access a specific memory location, the Address field is loaded into the Address register during a second Command Write cycle. While internal data moves and compares are done on a 64-bit basis, the data inputs and outputs of the MU9C1640 are multiplexed four ways over a 16-bit I/O bus for low cost.

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### FUNCTIONAL DESCRIPTION (CONT'D)

Appended to each 64-bit data field are two bits of CAM storage to indicate the validity of the location. These two bits are encoded to render four validity conditions: Valid data, Skip, Empty, and Random Access only. Automatic compares are performed between the contents of the Comparand register and the entire contents of the CAM entries marked as Valid data. Forced compares can be performed against any of the Validity bit conditions. An opaque mask can be used to find all the entries marked with a particular Validity condition (an opaque mask is automatic for CMP E instructions, which compare against all “empty” entries.) The Validity bits can then be modified on all matching entries simultaneously.

Two Mask registers on the device can be selected to mask Compares or Data writes. For comparison masking, data stored in the selected Mask register determine which bits of the Comparand are compared against CAM entries. During a Write cycle (including Move instructions,) data in the designated Mask register determines which bits in the destination are written.

The Match line associated with each location is fed into a Priority encoder where multiple matches are resolved, and the address of the Highest-priority match (lowest numbered physical address) is generated. In some applications, knowledge of the existence of multiple matches may be useful and is indicated by the /MM flag in the Status register.

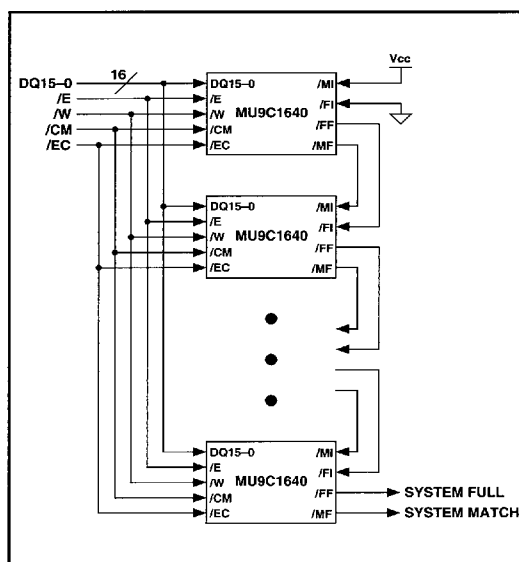
After a Compare cycle, the Status register contains the address of the highest-priority responding location, along with flags indicating Match, Multiple Match, and Full. The Match and Full flags are also available directly as output signals. These flags can be daisy-chained independently to provide system Match and Full indications without external logic.

The Page Address register simplifies vertical expansion in systems using more than one MU9C1640. This register is loaded with address information during system initialization. During a Compare cycle, the ten bits of the Match address are fed to the Status register from the Priority encoder and are concatenated with the Page Address register value. The Device Select register is used to select a particular device in a vertically cascaded CacheCAM array by setting the Device Select equal to the desired Page address. Setting DS = FFFFH will enable all devices for writing, while allowing only the device with a match to read, after /EC has been asserted.

The Control register sets up operating conditions within the MU9C1640, including Reset, enable or disable Match Flag, enable or disable Full Flag, CAM/RAM partitioning, disable or select masking conditions, and disable or select address auto-increment or auto-decrement.

Source and Destination Segment counters within the MU9C1640 separately control reading and writing data. A Segment Control register sets the count limits and start values for both the Source and Destination Segment counters.

Figure 1 shows expansion using a daisy-chain. Note that system flags are generated without the need for external logic. The Page Address register allows each device in the vertically cascaded chain to supply its own address in the event of a match eliminating the requirement for an external Priority encoder to calculate the complete Match address. The Full flag daisy-chaining allows use of Associative writes which do not use a specific address. Thus a Write at Next Free address operates globally.



### Figure 1: Vertical Cascading

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### OPERATIONAL CHARACTERISTICS

Throughout the following, "aaaH" represents a three-digit hexadecimal number "aaa," while "bbB" represents a two-digit binary number "bb." All registers and memory locations are broken into 16-bit segments. The lowest order bits (bits 15-0) are in segment zero, while the higher segments labeled 1, 2, and 3 contain bits 31-16, 47-32, and 63-48, respectively.

#### THE CONTROL BUS

Refer to the Block Diagram for the following discussion. The primary control mechanism for the MU9C1640 is the Control bus which comprises the Chip Enable (/E), the Write Enable (/W), the Command Enable (/CM), and the Enable Comparison (/EC) inputs. The /EC input of the Control bus is responsible for enabling the Match flag output when LOW, and controlling the daisy-chain operation. The secondary control mechanism of the MU9C1640 is by instructions which are decoded by the Instruction decoder. Logical combinations of the Control Bus inputs, coupled with the execution of Select Persistent Source (SPS), Select Persistent Destination (SPD), and Temporary Command Override (TCO) instructions, allow the I/O operations to and from the DQ15-DQ0 lines to the internal resources, as shown in Table 1.

The default source and destination for Data Read and Write cycles is the Comparand register. This default state can be overridden independently by executing a Select Persistent Source or Select Persistent Destination instruction, selecting a different source or destination for data. Subsequent Data Read or Data Write cycles will access that source or destination until another SPS or SPD instruction is executed. The currently selected persistent source or destination can be read back via a TCO PS or PD instruction. The sources and destinations available for persistent access are those resources on the 64-bit bus: Comparand register, Mask Register 1, Mask Register 2, and the Memory array.

The default destination for Command Write cycles is the Instruction decoder, while the default source for Command Read cycles is the Status register.

Access to the Control register, the Page Address register, the Segment Control register, the Address register, the Next Free Address register, and Device Select register is by Temporary Command Override (TCO) instructions which are only active for one Command Read or Write cycle after being loaded into the Instruction decoder.

The data and control interfaces to the MU9C1640 are synchronous. During a Write cycle, the Control and

Data inputs are registered by the falling edge of /E. When writing to the persistently selected data destination, the Destination Segment counter is clocked by the rising edge of /E. During a Read cycle, the Control inputs are registered by the falling edge of /E, and the Data outputs are enabled while /E is LOW. When reading from the persistently selected data source, the Source Segment counter is clocked by the rising edge of /E.

#### THE REGISTER SET

Worksheets to assist in decoding the CacheCAM Control register, Segment Control register, and Status registers are included as Tables 2, 4, and 6.

#### Instruction Decoder

The Instruction decoder is the write-only decode logic for instructions and is the default destination for Command Write cycles. The lower-order 12 bits comprise the instruction, as shown in the Instruction Set Description. Bit 11 is a flag that notifies the CacheCAM that the instruction is a two-cycle instruction and requires an absolute address to be loaded in the next cycle.

If the Address flag is set in the instruction, the address at which the Memory is to be accessed is loaded by a second Command Write cycle after the Select Persistent Source Memory Array at Address instruction. If the Address flag is not set, the memory access occurs at the address currently contained in the Address register. Addresses can be generated in two additional ways. A new address can be forced into the Address register by a TCO instruction that targets the Address register and supplies an absolute address on the immediately following Command Write cycle. Alternatively, by correctly setting Control register bits CT3 and CT2, the Address register auto-increments or -decrements during Data writes or reads to Memory at Address register when either of the Segment counters reaches its end count, after Moves to Memory at Address register, or after VBC Instructions at Address register.

#### Control Register (CT)

The Control register is composed of a number of switches that configure the CacheCAM, as shown in Table 2. It is written to or read from using a TCO CT instruction. If bit 15 of the value written following the TCO CT is a "0", the device is Reset (and all other bits are ignored.) See Table 3 for the reset state. A write to the Control register causes an automatic compare to occur (except in case of a Reset.)

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OPERATIONAL CHARACTERISTICS (CONT'D)									
CycleType	/E	/CM	/W	I/O Status	SPS	SPD	TCO	Operation	Notes
Com Write	L	L	L	IN				Load Instruction decoder	1
				IN			✓	Load Address register	2, 3
				IN			✓	Load Control register	3
				IN			✓	Load Page Address register	3
				IN			✓	Load Segment Control register	3
				IN			✓	Load Device Select register	3
Com Read	L	L	H	OUT			✓	Read Next Free Address register	3
				OUT			✓	Read Address register	3
				OUT				Read Status Register bits 0-15	4
				OUT				Read Status Register bits 16-31	5
				OUT			✓	Read Control Register	3
				OUT			✓	Read Page Address Register	3
				OUT			✓	Read Segment Control Register	3
				OUT			✓	Read Device Select Register	3
				OUT			✓	Read Current Persistent Source or Destination	3, 11
Data Write	L	H	L	IN		✓		Load Comparand Register	6, 9
				IN		✓		Load Mask Register 1	7, 9
				IN		✓		Load Mask Register 2	7, 9
				IN		✓		Write Memory Array at Address	7, 9
				IN		✓		Write Memory Array at Next Free Address	7, 9
				IN		✓		Write Memory Array at Highest-priority Match	7, 9
Data Read	L	H	H	OUT	✓			Read Comparand Register	6, 9
				OUT	✓			Read Mask Register 1	8, 9
				OUT	✓			Read Mask Register 2	8, 9
				OUT	✓			Read Memory Array at Address	8, 9
				OUT	✓			Read Memory Array at Highest-priority Match	8, 9
	H	X	X	HIGH-Z				Deselected	
Com Write	L	L	L	IN				Deselected if DS=PA or DS=FFFFH	10
<b>Notes</b> 1. Default Command Write cycle destination. 2. Command Write cycle destination on the consecutive Command Write cycle if Address flag was set in bit IR11 of the instruction loaded in the previous cycle. 3. Loaded or read on the consecutive Command Write or Read cycle after a TCO instruction has been loaded. Active for one Command Write or Read cycle only. NFA register cannot be loaded this way. 4. Default Command Read cycle source. 5. Command Read cycle source on the consecutive Command Read cycle. If next cycle is not a Command Read cycle, it accesses the Status register low-order 16-bits. 6. Default persistent source and destination on power-up and after Reset. If other resources were sources or destinations, SPD CR or SPS CR restores the Comparand register as the destination or source. 7. Selected by executing a Select Persistent Destination. 8. Selected by executing a Select Persistent Source Instruction. 9. May require multiple 16-bit Read or Write cycles. Segment Control register used to control selection of desired 16-bit segment(s) by establishing Segment counters' limits and start values. 10. Device is also deselected if contents of Device Select register do not match contents of Page Address register except when Device Select register contains all 1's (FFFFH). All Device Select registers in a vertically cascaded device array are written in a Command Write cycle immediately following a TCO with the Device Select register as the destination. 11. TCO PS or TCO PD read back the Instruction decoder bits that were last set to select a source or destination on the next cycle which must be a Command Read cycle.									
<b>Table 1: Input/Output Operations</b>									

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### OPERATIONAL CHARACTERISTICS (CONT'D)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	Match Flag	Full Flag	Reserved	Reserved	CAM/RAM Part.	Comp. Mask	AR Inc/Dec	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
R	Enable	Enable	Reserved	Reserved	64 CAM = "000"	None = "00"	Increment	Set to "00"							
E	= "00"	= "00"	= "00"		48 CAM = "001"	MR1 = "01"	= "00"								
S	Disable	Disable			32 CAM = "010"	MR2 = "10"	Decrement								
E	= "01"	= "01"			16 CAM = "011"	No Change	= "01"								
T	No Change	No Change			0 CAM = "100"	= "11"	Disable								
=	= "11"	= "11"			No Change = "111"		= "10"								
"0"							No Change	= "11"							

**Table 2: Control Register Bit Assignments**

CAM Status	After Power-on Reset	Software Reset
Validity bits at all memory locations	Skip = 0, Empty = 1	Same
Match and Full Flag outputs	Enabled	Same
CAM/RAM Partitioning	64 bits CAM, 0 bits RAM	Same
Comparison Masking	Disabled	Same
Address register auto-increment or -decrement	Disabled	Same
Source and Destination Segment Counters Count Ranges	00B to 11B; loaded with 00B	Same
Address register	Contains all "0"s	Same
Page Address and Device Select registers	Contains all "0"s	Unchanged
Control register after reset (Including CT15)	Contains 0008H	Same
Persistent Destination for Command Writes	Instruction decoder	Same
Persistent Source for Command Reads	Status register	Same
Persistent Source and Destination for Data Reads and Writes	Comparand register	Same

**Table 3: Device Control State after Reset Command**

If the Match Flag is disabled, the internal match condition for the device is forced HIGH (Internal /MA = 1 in Table 5: Device Select Response.), so that Case 6 is not possible, effectively removing the device from the daisy-chain. With the Match Flag disabled, /MF=/MI for that device and operations directed to Highest-priority Match locations are ignored. Normal operation of the device is with the /MF enabled.

If the Full Flag is disabled, the device thinks that it is full and ignores instructions to Next Free Address. All other instructions operate normally. Additionally, with the /FF disabled, /FF=/FI. Normal operation of the device is with the /FF enabled.

#### Segment Control Register (SC)

The Segment Control register contains dual independent incrementing counters with limits. One counter controls which segments data are written to,

while the other counter controls which segments data are read from. Destinations for data writes and sources for data reads (called the persistent destination and source) are set independently with TCO Instructions.

Each of the two counters consists of a start segment, the end segment, and the current segment pointer. Numbers are be set independently for writing or reading. The current segment pointer can be set to any segment, even a segment outside the range set by the start and end segments. A TCO SC instruction writes a configuration value to the Segment Control register, as shown in Table 4. After a Reset, both Source and Destination counters are set to count from Segment 0 to Segment 3.

#### Page Address Register (PA)

The Page Address register is loaded using a TCO PA instruction with a user selected 16-bit value (not FFFFH.) The entry in this register is used to give a

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### OPERATIONAL CHARACTERISTICS (CONT'D)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Set Dest. Seg. Limits = "0"	Destination Count Start Limit "00-11"	Destination Count End Limit "00-11"	Set Source Seg. Limits = "0"	Source Count Start Limit "00-11"	Source Count End Limit "00-11"	Load Dest. Seg. Count = "0"	Destination Segment Count Value "00-11"	Load Source Seg. Count = "0"	Source Segment Count Value "00-11"						

**Table 4: Segment Control Register Bit Assignments**

unique address to the different devices in a daisy-chain. In a daisy-chain, the PA value of each device is loaded using the SFF instruction to advance to the next device. A Reset does not affect the Page Address register. This register must be initialized even if only one device is used.

#### Device Select Register (DS)

The Device Select register is used to select a specific (target) device using the TCO DS instruction by setting the 16-bit DS value equal to the target's PA value. In a daisy-chain, setting DS = FFFFH will select all devices. However, in this case, the ability to read information out of the device is restricted as shown in Table 5. A software Reset (using the Control register) does not affect the Device Select register.

#### Address Register (AR)

The Address register points to the CAM Memory location to be operated upon with a M@[AR] or M@aaaH instruction. It can be loaded with a value by using a TCO AR instruction followed by an absolute address value, or by using an instruction requiring an

absolute address, such as MOV aaaH,CR,V, after which the Address register will increment or decrement from that value according to the setting of bits CT3 and CT2 of the Control register. A Reset sets the Address register to zero.

#### Next Free Address Register (NF)

The Next Free Address register can be read using a TCO NF instruction. It stores the address of the first empty location in the CAM memory, and is used as a pointer for M@NF operations. After a Reset, the Next Free Address register is set to zero.

#### Status Register

The 32-bit Status register is the default source for Command Read cycles. The first Command Read cycle will return bits 15-0 of the Status register, and the second Command Read cycle, if issued immediately after the first, will return bits 31-16. Bit 0 is the internal Match flag and will go LOW if a match was found in this particular device. Bits 9-1 give the match address of the Highest-priority match. Bits 11-26 give the Page Address of the device. Bit 30 is the internal Multiple

Case	Internal /EC	Internal /MA	External /MI	Device Select Reg.	Command Write*	Data Write	Command Read	Data Read
1	1	X	X	DS = FFFFH	YES	YES	NO	NO
2	1	X	X	DS = PA	YES	YES	YES	YES
3	1	X	X	DS ≠ FFFFH and DS ≠ PA	NO	NO	NO	NO
4	0	X	0	X	NO	NO	NO	NO
5	0	1	1	X	NO	NO	NO	NO
6	0	0	1	X	YES	YES	YES	YES

\*Note: Exceptions are 1) Write to Device Select register is always active in all devices; 2) Write to Page Address register is active in the device with /FI LOW and /FF HIGH; 3) the Set Full Flag (SFF) instruction is active in the device with /FI LOW and /FF HIGH.; and, 4) if /MF is disabled in the Control Register, /MA (Internal) is forced HIGH preventing a Case 6 response.

**Table 5: Device Select Response**

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### OPERATIONAL CHARACTERISTICS (CONT'D)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
/FL	/MM	Rsvd	Rsvd	Rsvd	Page Address Bits, PA15–PA5										
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PA4–PA0					Rsvd	Match Address, AM8–AM0									/MA

Note: The Status register is read by performing Command Read cycles. On the first cycle, bits 15–0 will be output, and if a second Command Read cycle is issued immediately after the first Command Read cycle, bits 31–16 will be output. Reserved bits will read as "0"s, except for bit 10, which will read as a "0" if there was a match, and a "1" if there was not a match.

**Table 6: Status Register Bit Assignments**

Match flag and goes LOW if a Multiple match was detected. Bit 31 is the internal Full flag, and goes LOW if the particular device has no empty memory locations. Table 6 shows the Status register bit assignments.

#### Comparand Register (CR)

The 64-bit Comparand register is the default destination for Data Writes and Reads, using the Segment Control register to select the segment of the Comparand register to be loaded or read out. The Persistent Source and Destination for Data Writes and Reads can be changed to the Mask registers or Memory by SPS and SPD instructions. During an automatic or forced compare, the Comparand register is compared against the CAM portion of all memory locations with the correct validity condition simultaneously. Automatic compares always compare against Valid Memory locations, while forced compares, using CMP instructions, can compare against Memory locations tagged with any specific validity condition.

#### Mask Registers (MR1, MR2)

The Mask registers can be used in two different ways, either to mask compares or to mask data writes and moves. Either Mask register can be selected in the Control register to mask every compare, or selected by instructions to participate in data writes or moves to and from Memory. If a bit in a 64-bit Mask register is set to a "0", the corresponding bit in the Comparand register will enter into a masked compare operation. If a Mask bit is a "1", the corresponding bit in the Comparand register will not enter into a masked compare operation. Bits set to "0" in the Mask register cause corresponding bits in the destination register or memory location to be updated when masking data writes or moves, while a bit set to "1" will prevent that bit in the destination from being changed.

#### THE MEMORY ARRAY

##### Memory Organization

The Memory array is organized as 1024 64-bit locations, each having two Validity bits, the Skip bit and Empty bit. By default all locations are configured to be 64 CAM cells. However, the array can be reconfigured in the Control register to divide each location into a CAM field and a RAM field. The RAM field is assigned to the lower-order segments, starting with Segment 0. The CAM/RAM partitioning is allowed on 16-bit boundaries, permitting selections of 64 CAM bits, 0 RAM bits; 48 CAM bits, 16 RAM bits; 32 CAM bits, 32 RAM bits; 16 CAM bits, 48 RAM bits; 0 CAM bits, 64 RAM bits. Memory Array bits designated to be RAM bits can be used to store and retrieve Associated data (data associated with a CAM content).

##### Memory Access

There are two general ways to get data into and out of the memory array, directly or by moving the data via the Comparand or Mask registers.

The first way, through direct reads or writes, is set up by issuing a Set Persistent Destination (SPD) or Set Persistent Source (SPS) command. The addresses for the direct access can be directly supplied, supplied from the address register, supplied from the Next Free Address Register, or supplied as the Highest-priority Match address. Additionally, all the direct writes can be masked by either mask register.

The second way to move data to or from the Comparand or Mask registers into or out of the memory array is accomplished by Data Move commands (MOV). Moves using the Comparand register can also be masked by either of the Mask registers.

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### OPERATIONAL CHARACTERISTICS (CONT'D)

#### I/O CYCLES

The MU9C1640 supports four basic I/O cycles: Data Read, Data Write, Command Read, and Command Write. The type of cycle is determined by the states of the /W and /CM control inputs. These signals are registered at the beginning of a cycle by the falling edge of /E. Table 7 shows how the /W and /CM lines select the cycle type.

/W	/CM	Cycle Type
LOW	LOW	Command Write Cycle
LOW	HIGH	Data Write Cycle
HIGH	LOW	Command Read Cycle
HIGH	HIGH	Data Read Cycle

**Table 7: I/O Cycles**

During Read cycles, the outputs are enabled after /E goes LOW. During Write cycles, the data or command to be written is captured at the beginning of the cycle by the falling edge of /E. Figures 2 and 3 show Read and Write cycles respectively. Figure 4 shows typical cycle-to-cycle timing with the Match flag valid at the end of the third load cycle if /EC is LOW at the start of the third cycle. The Compare operation automatically occurs when the segment counter reaches the end count set in the Segment Control register (for Data writes to the Comparand or Mask registers). If there was a match, the fourth cycle reads status or associated data, depending on the state of /CM. For cascaded devices, /EC is held LOW for the fourth cycle to continue the locked daisy-chain until the second read cycle is complete. If there was not a match, the output buffers go Hi-Z, and the daisy-chain must be unlocked by taking /EC HIGH. Figure 5 shows how the internal /EC timing holds the daisy-chain locking effect over into the next cycle. In a single-chip system with DS=PA, taking /EC HIGH for the fourth cycle will allow Status reads with a match, while a NOP taking /EC HIGH must be inserted to read Status without a match.

The minimum timings for the /E control signal are given in the Electrical Characteristics section. Note that at minimum timings the /E signal is non-symmetrical, and that different cycle types have different timing requirements.

#### COMPARE OPERATIONS

All compare operations available in the CacheCAM are similar in that the data in the Comparand register are compared to all locations in the Memory array simultaneously. There are two ways compares are initiated: Automatic and Forced compares. Mask registers to be used for compares are selected in the Control register.

Automatic compares perform a compare of the contents of the Comparand register against Memory locations that are tagged as "Valid", and occur whenever the following happens:

1. The Destination Segment counter in the Segment Control register reaches its end limit during writes to the Comparand or Mask registers.
2. After the second command write of a TCO CT command is executed, i.e. a compare is executed with the new Control register settings.

Forced compares are initiated by CMP instructions using one of the four validity conditions. The forced compare against "Empty" locations automatically masks all 64 bits of data to find all locations with the validity bits set to "Empty", while the other forced compares are only masked as selected in the Control register.

#### VERTICAL CASCADING

The MU9C1640 can be vertically cascaded to increase system depth. Through the use of flag daisy-chaining, multiple CacheCAMs will respond as an integrated system. The daisy-chain of flags allows all commands to operate globally. For example, operations at the Next Free address or at the Highest-priority Match address will only operate in the device in a string that actually has the first empty location or the first matching location, respectively. When connected in a daisy-chain, the last device's Full flag and Match flag accurately report the condition for the whole string. By setting the Page Address and Device Select registers to the same value, individual devices in a daisy-chain can be addressed. The ripple delay of the flags when connected in a daisy-chain requires the extension of the /E HIGH time until the logic in all devices has settled out. In a string of "n" devices, the /E HIGH time should be greater than  $t_{EHMFV} + (n-1) \cdot t_{MIVMFV}$ . A system in which MU9C1640s are vertically cascaded using daisy-chaining of the flags is shown in Figure 1.

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### OPERATIONAL CHARACTERISTICS (CONT'D)

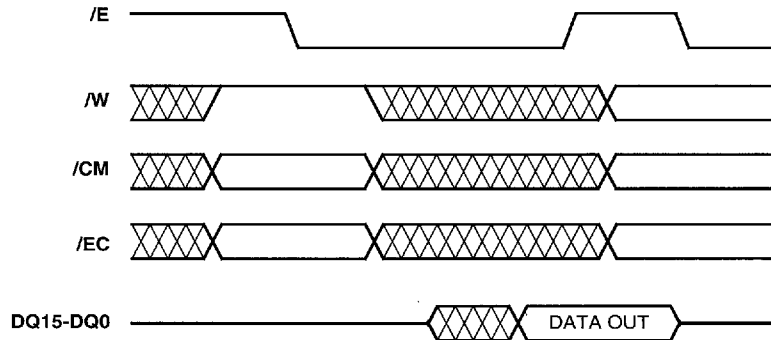


Figure 2: Read Cycle

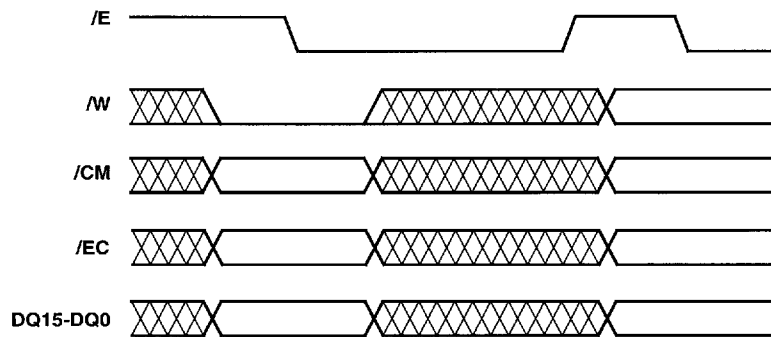


Figure 3: Write Cycle

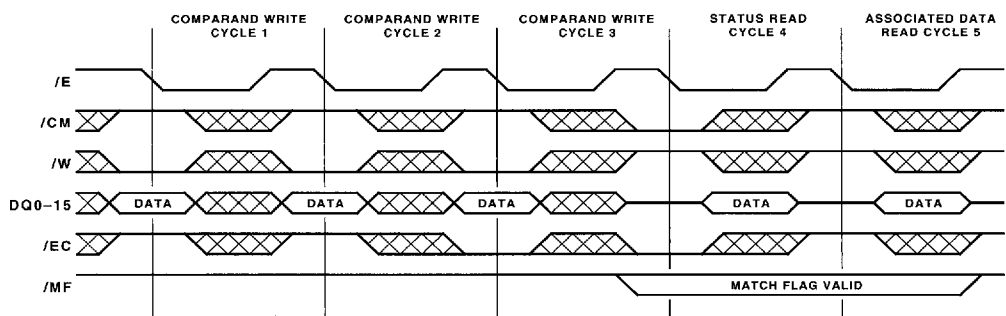


Figure 4: Example Cycle to Cycle Timing

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### OPERATIONAL CHARACTERISTICS (CONT'D)

#### LOCKED DAISY-CHAIN

In a locked daisy chain, the highest priority device is the one with /MI HIGH and /MF LOW. Only this device will respond to command and data reads and writes, until the daisy chain has been unlocked by taking /EC HIGH, with the exceptions noted in Table 5. This allows reading from the associated data field of the Highest-priority Match location anywhere in a string of devices, or the Match address from the Status register of the device with the match. It also permits updating the entry stored at the Highest-priority Match location.

Table 5 shows when a CacheCAM will respond to reads or writes and when it won't based on the state of /EC(int), the internal match condition, and other control inputs. /EC(int) is registered from the external /EC pin off the rising edge of /E, so it controls what happens in the next cycle, as shown in Figure 5. When you first take /EC LOW in a string of CacheCAM devices (and assuming the Device Select registers are set to FFFFH), all devices will respond to that command write or data write. (When DS=FFFFH, none of the devices will respond to a Command Read cycle or a Data Read cycle to prevent data bus contention. See Case 1 of Table 5.) The daisy-chain will remain locked on subsequent cycles as long as /EC is held LOW on the falling edge of /E. When a daisy-chain is locked, only the Highest-priority Match device will respond (See Case 6 of Table 5). If, for example, all of the CAM memory locations were empty, there would be no match, and /MF would stay HIGH. Since none of the devices could then be the Highest-priority Match device, none will respond to reads or writes until the daisy chain is unlocked by taking /EC HIGH.

If there is a match between the data in the Comparand register and a location or locations in memory, then only the Highest-priority Match device will respond to a Status read. If there isn't a match, then a NOP (or any other instruction) with /EC HIGH needs to be inserted before issuing a Write to Next Free Address instruction. Since Next Free operations are controlled by the /FI-/FF daisy-chain, only the device with the first empty location will respond. If an instruction is used to unlock the daisy-chain it will work only on the Highest-priority Match device, if one exists. If none exists, the instruction will have no effect except to unlock the daisy-chain. To read the Status registers of specific devices when there is no match requires the use of the TCO DS command to set DS=PA of each device.

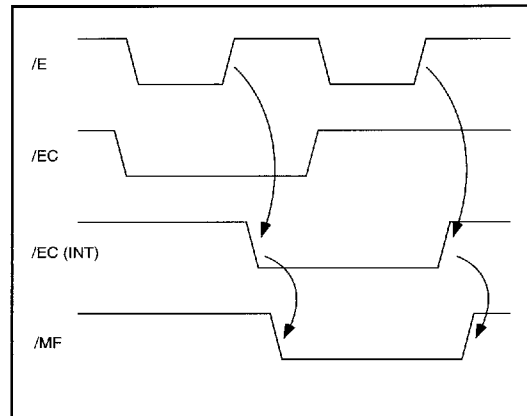


Figure 5: /EC(Int) Timing Diagram

#### Full Flag Cascading

The Full Flag daisy-chain cascading is used for three purposes: First, to allow instructions that address Next Free locations to operate globally, second, to provide a system wide Full flag, and third, to allow the loading of the Page Address registers during initialization using the SFF instruction. The full flag logic causes only the device containing the first empty location to respond to Next Free instructions such as "MOV NF,CR,V", which will move the contents of the Comparand register to the first empty location in a string of devices and set that location Valid, so it will be available for the next automatic compare. With devices connected as in Figure 1, the /FF output of the last device in a string provides a full indication for the entire string.

#### Match Flag Cascading

The Match Flag daisy-chain cascading is used for three purposes: First, to allow operations on Highest Priority Match addresses to operate globally over the whole string, second, to provide a system wide match flag, and third, to lock out all devices except the one with the Highest-priority match for instructions such as Status reads after a match. The Match flag logic causes the only the highest priority device to operate on its Highest-priority Match location and lower priority devices to ignore operations on Highest-priority Match locations. With devices connected as in Figure 1, the /MF output of the last device provides a system match indication for the entire string. The lock out feature is enabled by the match flag cascading and the use of the /EC control signal as shown in Table 5.

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### OPERATIONAL CHARACTERISTICS (CONT'D)

#### Global vs. Local Access for Cascaded Systems

The Device Select register controls access to devices in the daisy-chain once the Page Address registers have been initialized. Local access into a daisy-chained system works by sending a Device Select value to all the Device Select registers which equals the Page Address of the target device using the TCO DS instruction. Once this is done, only the device which has a match between its Page Address register and its Device Select register will respond to Read or Write cycles.

Loading the value "FFFFH" into the Device Select registers of a string will restore global access as shown in Table 5, with Read cycles being restricted to devices with the Highest-priority Match to eliminate bus contention.

#### INITIALIZING THE CacheCAM

Since the MU9C1640 is controlled by a combination of input signals and instructions, initialization is required to configure the device. Since a Control register reset establishes the operating conditions shown in Table 2, restoration of operation conditions better suited for the application may be required after a reset.

#### Setting Page Address Register Values

In a vertically cascaded system, the user must set the individual Page Address registers to unique values by using the Page Address initialization mechanism. Each Page Address register must contain a unique value to prevent bus contention. This process allows individual device selection. The Page Address register initialization works as follows: Writes to Page Address registers are only active for devices with /FI LOW and /FF HIGH. At initialization, all devices are empty, thus the top device in the string will respond to a TCO PA instruction, and load its PA register. To advance to the next device in the string, a Set Full Flag (SFF) instruction is used, which is also only active for the device with /FI LOW and /FF HIGH. The SFF instruction changes the first device's /FF to LOW, although the device really is empty, which allows the next device in the string to respond to the TCO PA instruction and load its PA register. The initialization proceeds through the chain in a similar manner filling

all the PA registers in turn. Each device must have a unique Page Address value stored in its PA register, or contention will result. After all the PA registers are filled, the entire string is reset through the Control register, which does not change the values stored in the individual PA registers. After the reset, the Device Select registers are usually set to FFFFH to enable operation as shown in Case 1 of Table 5. The Control registers and the Segment Control registers are now also set to their normal operating values for the application.

#### Vertically Cascaded System Initialization

Table 8 shows an example of code that initializes a daisy-chained string of CacheCAM devices. The Initialization example shows how to set the Page Address registers of each of the devices in the chain through the use of the Set Full Flag instruction, and how the Control registers and Segment counters of all the CacheCAM devices are set for a typical application. Each Page Address register must contain a unique value (not FFFFH) to prevent bus contention. The first Command Write of 0000H is provided to take care of the situation of an anomalous power-up state caused by a too slow rise of the voltage on /E relative to VCC, and will place the device in a known initial state by resetting the internal two-cycle state machines.

For typical daisy-chain operation, data are loaded into the Comparand registers of all the devices in a string simultaneously by setting DS=FFFFH. Since reading is prohibited when DS=FFFFH except for the device with a match, for a diagnostic operation you need to select a specific device by setting DS=PA for the desired device to be able to read from it. Refer to Table 5 for pre-conditions for reading and writing.

Initialization for a single CacheCAM is similar. The Page Address register must still be initialized to a known value. The Device Select register in this case is usually set to equal the Page Address register for normal operations. If the hardware match flag, /MF, is not needed by this single device application, the compare results can be read out of the Status register. Because /MF isn't monitored, the /EC signal is also not needed and can be kept HIGH, which will eliminate the need to insert a NOP after a no-match, often speeding up the application.

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OPERATIONAL CHARACTERISTICS (CONT'D)						
Cycle Type	Opcode or Data on Data Bus	Control Bus				Notes
		/E	/CM	/W	/EC	
Command Write	0000H	L	L	L	H	Accounts for Power-up anomalies
Command Write	TCO DS	L	L	L	H	Target Device Select register to disable local device selection
Command Write	FFFFH	L	L	L	H	Disables Device Select feature
Command Write	TCO CT	L	L	L	H	Target Control register for reset
Command Write	0000H	L	L	L	H	Causes reset
Command Write	TCO PA	L	L	L	H	Target Page Address register to set page for cascaded operation
Command Write	nnnnH	L	L	L	H	Page Address value
Command Write	SFF • •	L	L	L	H	Set Full flag; allows access to next device (repeat previous 2 instructions plus this one for each device in chain)
Command Write	TCO CT	L	L	L	H	Target Control register for reset of Full flags, but not Page Address.
Command Write	0000H	L	L	L	H	Causes Reset
Command Write	TCO CT	L	L	L	H	Target Control register for initial values
Command Write	8040H	L	L	L	H	Control register value
Command Write	TCO SC	L	L	L	H	Target Segment Counter Control register
Command Write	39C9H	L	L	L	H	Set both Segment Counters to load segments 1, 2, and 3 (48 bits), starting with segment 1.
<p style="text-align: center;"><b>Notes</b></p> <ol style="list-style-type: none"> <li>1. The TCO CT immediate field bit assignments translate to 0000H for the Reset operation. The default power-up condition generates the same effect, but good programming practice dictates a software reset for initialization to account for all possible conditions.</li> <li>2. This instruction may be omitted for a single MU9C1640 application. The last SFF will cause the /MF pin in the last chip in a daisy chain to go LOW. In a daisy chain, DS needs to be set equal to PA to read out of a particular chip prior to a match condition.</li> <li>3. Typical CacheCAM control environment:            Enable match flag            Enable full flag            48 CAM bits, 16 RAM bits            Disable comparison masking            Enable address increment             This example translates to 8040H. See Table 2 for Control register bit assignments.</li> <li>4. Use Worksheets to help determine Segment Counter and Control register values.</li> </ol>						
<b>Table 8: Example Initialization Routine</b>						

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■ 6411817 0000173 595 ■

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### INSTRUCTION SET DESCRIPTION

#### Instruction: Select Persistent Source (SPS)

**Binary Op Code:** 0000 f000 0000 0sss  
**f** Address Field Flag (†)  
**sss** Selected Source

This instruction selects a persistent source for Data Reads, which remains the source for Data Reads until another SPS instruction or a Reset occurs. The Comparand register is the default persistent source after power-up or Reset.

#### Instruction: Select Persistent Destination (SPD)

**Binary Op Code:** 0000 f001 mmdd dvvv  
**f** Address Field Flag (†)  
**mm** Mask Register Select  
**ddd** Selected Destination  
**vvv** Validity Setting for memory location destinations

This instruction selects a persistent destination for Data Writes, which remains the destination for Data Writes until another SPD instruction or a Reset occurs. The Comparand register is the default destination for Data Writes after power-up or Reset. When the destination is the Comparand register or the Memory array, the writing of data may be masked by either Mask Register 1 or 2. In this case, only those bits in the destination that correspond to "0s" in the Mask register will be modified. An automatic compare will occur after writing to the Comparand or Mask registers, but not after writing to Memory.

#### Instruction: Temporary Command Override (TCO)

**Binary Op-Code:** 0000 0010 00dd d000  
**ddd** Register selected as source or destination for only the next Command Read or Write cycle.

The TCO instruction selects a register to become the source or destination for only the next Command Read or Write cycle, so a value can be loaded or read out. Subsequent Command Read or Write cycles revert to reading the Status register and writing to the Instruction register. The TCO PS and TCO PD instructions allow the user to read which persistent source or destination has been selected. A TCO AR permits access to the Address register for flexible memory addressing. The Next Free Address register can be read by a TCO NF instruction. Writing to the Page Address register sets the particular device address. A TCO DS can select a particular device if DS = PA, or all devices in a string if DS = FFFFH.

† If f=1, the instruction requires an absolute address to be supplied, which updates the Address register to the "aaaH" value supplied in the second cycle of the instruction. During instructions involving M@[AR] or M@aaaH, the Address register will be incremented or decremented depending on the setting in the Control register.

#### Instruction: Data Move (MOV)

**Binary Op-code:** 0000 f011 mmdd dsss or 0000 f011 mmdd dvss  
**f** Address Field Flag (†)  
**mm** Mask Register select  
**ddd** Destination of Data  
**sss** Source of Data  
**v** Validity setting if destination is a memory location

The MOV instruction performs a 64-bit move of the data in the selected source to the selected destination. Data transfers between the Memory array and the Comparand register may be masked by either Mask Register 1 or Mask Register 2, in which case, only those bits in the destination which correspond to bits containing 0's in the selected Mask register will be changed. A Memory location used as a destination for a MOV instruction will be set to Valid or left unchanged, depending on the setting of the "v" bit. If the source and destination are the same register, no net change occurs (a No-Op).

#### Instruction: Validity Bit Control (VBC)

**Binary Op-code:** 0000 f100 00dd dvvv  
**f** Address Field Flag (†)  
**ddd** Destination of data  
**vvv** Validity setting for Memory location

The VBC instruction sets the Validity bits at the selected memory location to the selected state. This feature can be used in finding multiple matches, for example, by using a repetitive sequence of CMP V through a Mask of all "1s", followed by a VBC HM, S.

#### Instruction: Compare (CMP)

**Binary Op-code:** 0000 0101 0000 0vvv  
**vvv** Validity condition

A CMP V, S, or R instruction forces a Comparison of Valid, Skipped, or Random entries against the Comparand register through a Mask register, if one is selected. During a CMP E instruction, the compare is only done on the Validity bits.

#### Instruction: Set Full Flag (SFF)

**Binary Op-code:** 0000 0111 0000 0000

The SFF instruction is a special instruction used to force the Full flag LOW to permit setting the Page Address register in vertically cascaded systems.

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## CacheCAM™

### INSTRUCTION SET SUMMARY

#### MNEMONIC FORMAT

INS dst,src[msk],val

**INS:** Instruction mnemonic.  
**dst:** Destination of the data.  
**src:** Source of the data.  
**msk:** Mask register used.  
**val:** Validity condition set at the location written.

#### Instruction: Select Persistent Source

Operation	Mnemonic	Op Code
Comparand Register	SPS CR	0000H
Mask Register 1	SPS MR1	0001H
Mask Register 2	SPS MR2	0002H
Memory Array at Address Reg	SPS M@[AR]	0004H
Memory Array at Address	SPS M@aaaH	0804H
Memory at Highest-priority Match	SPS M@HM	0005H

#### Instruction: Select Persistent Destination

Operation	Mnemonic	Op Code
Comparand Register	SPD CR	0100H
Masked by MR1	SPD CR[MR1]	0140H
Masked by MR2	SPD CR[MR2]	0180H
Mask Register 1	SPD MR1	0108H
Mask Register 2	SPD MR2	0110H
Memory at Address Reg set Valid	SPD M@[AR],V	0124H
Masked by MR1	SPD M@[AR][MR1],V	0164H
Masked by MR2	SPD M@[AR][MR2],V	01A4H
Memory at Address Reg set Empty	SPD M@[AR],E	0125H
Masked by MR1	SPD M@[AR][MR1],E	0165H
Masked by MR2	SPD M@[AR][MR2],E	01A5H
Memory at Address Reg set Skip	SPD M@[AR],S	0126H
Masked by MR1	SPD M@[AR][MR1],S	0166H
Masked by MR2	SPD M@[AR][MR2],S	01A6H
Memory at Address Reg set Random	SPD M@[AR],R	0127H
Masked by MR1	SPD M@[AR][MR1],R	0167H
Masked by MR2	SPD M@[AR][MR2],R	01A7H
Memory at Address set Valid	SPD M@aaaH,V	0924H
Masked by MR1	SPD M@aaaH[MR1],V	0964H
Masked by MR2	SPD M@aaaH[MR2],V	09A4H
Memory at Address set Empty	SPD M@aaaH,E	0925H
Masked by MR1	SPD M@aaaH[MR1],E	0965H
Masked by MR2	SPD M@aaaH[MR2],E	09A5H
Memory at Address set Skip	SPD M@aaaH,S	0926H
Masked by MR1	SPD M@aaaH[MR1],S	0966H
Masked by MR2	SPD M@aaaH[MR2],S	09A6H
Memory at Address set Random	SPD M@aaaH,R	0927H
Masked by MR1	SPD M@aaaH[MR1],R	0967H
Masked by MR2	SPD M@aaaH[MR2],R	09A7H
Memory at Highest-prio. Match, Valid	SPD M@HM,V	012CH
Masked by MR1	SPD M@HM[MR1],V	016CH
Masked by MR2	SPD M@HM[MR2],V	01ACH
Memory at Highest-prio. Match, Emp.	SPD M@HM,E	012DH
Masked by MR1	SPD M@HM[MR1],E	016DH
Masked by MR2	SPD M@HM[MR2],E	01ADH
Memory at Highest-prio. Match, Skip	SPD M@HM,S	012EH
Masked by MR1	SPD M@HM[MR1],S	016EH
Masked by MR2	SPD M@HM[MR2],S	01AEH

#### Instruction: Select Persistent Destination (Cont'd)

Operation	Mnemonic	Op Code
Memory at High-prio. Match, Random	SPD M@HM,R	012FH
Masked by MR1	SPD M@HM[MR1],R	016FH
Masked by MR2	SPD M@HM[MR2],R	01AFH
Memory at Next Free Addr., Valid	SPD M@NF,V	0134H
Masked by MR1	SPD M@NF[MR1],V	0174H
Masked by MR2	SPD M@NF[MR2],V	01B4H
Memory at Next Free Addr., Empty	SPD M@NF,E	0135H
Masked by MR1	SPD M@NF[MR1],E	0175H
Masked by MR2	SPD M@NF[MR2],E	01B5H
Memory at Next Free Addr., Skip	SPD M@NF,S	0136H
Masked by MR1	SPD M@NF[MR1],S	0176H
Masked by MR2	SPD M@NF[MR2],S	01B6H
Memory at Next Free Addr., Random	SPD M@NF,R	0137H
Masked by MR1	SPD M@NF[MR1],R	0177H
Masked by MR2	SPD M@NF[MR2],R	01B7H

#### Instruction: Temporary Command Override

Operation	Mnemonic	Op Code
Control Register	TCO CT	0200H
Page Address Register	TCO PA	0208H
Segment Control Register	TCO SC	0210H
Read Next Free Address	TCO NF	0218H
Address Register	TCO AR	0220H
Device Select Register	TCO DS	0228H
Read Persistent Source	TCO PS	0230H
Read Persistent Destination	TCO PD	0238H

#### Instruction: Data Move

Operation	Mnemonic	Op Code
Comparand Register from:		
No Operation	NOP	0300H
Mask Register 1	MOV CR,MR1	0301H
Mask Register 2	MOV CR,MR2	0302H
Memory at Address Reg	MOV CR,[AR]	0304H
Masked by MR1	MOV CR,[AR][MR1]	0344H
Masked by MR2	MOV CR,[AR][MR2]	0384H
Memory at Address	MOV CR,aaaH	0B04H
Masked by MR1	MOV CR,aaaH[MR1]	0B44H
Masked by MR2	MOV CR,aaaH[MR2]	0B84H
Memory at Highest-prio Match	MOV CR,HM	0305H
Masked by MR1	MOV CR,HM[MR1]	0345H
Masked by MR2	MOV CR,HM[MR2]	0385H
Mask Register 1 from:		
Comparand Register	MOV MR1,CR	0308H
No Operation	NOP	0309H
Mask Register 2	MOV MR1,MR2	030AH
Memory at Address Reg	MOV MR1,[AR]	030CH
Memory at Address	MOV MR1,aaaH	0B0CH
Memory at Highest-prio Match	MOV MR1,HM	030DH
Mask Register 2 from:		
Comparand Register	MOV MR2,CR	0310H
Mask Register 1	MOV MR2,MR1	0311H
No Operation	NOP	0312H
Memory at Address Reg	MOV MR2,[AR]	0314H
Memory at Address	MOV MR2,aaaH	0B14H
Memory at Highest-prio Match	MOV MR2,HM	0315H

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### INSTRUCTION SET SUMMARY (CONT'D)

#### Instruction: Data Move (Cont'd)

Operation	Mnemonic	OpCode
Memory at Address Register, No Change to Validity bits, from:		
Comparand Register	MOV [AR],CR	0320H
Masked by MR1	MOV [AR],CR[MR1]	0360H
Masked by MR2	MOV [AR],CR[MR2]	03A0H
Mask Register 1	MOV [AR],MR1	0321H
Mask Register 2	MOV [AR],MR2	0322H
Memory at Address Register, Location set Valid, from:		
Comparand Register	MOV [AR],CR,V	0324H
Masked by MR1	MOV [AR],CR[MR1],V	0364H
Masked by MR2	MOV [AR],CR[MR2],V	03A4H
Mask Register 1	MOV [AR],MR1,V	0325H
Mask Register 2	MOV [AR],MR2,V	0326H
Memory at Address, No Change to Validity bits, from:		
Comparand Register	MOV aaH,CR	0B20H
Masked by MR1	MOV aaH,CR[MR1]	0B60H
Masked by MR2	MOV aaH,CR[MR2]	0BA0H
Mask Register 1	MOV aaH,MR1	0B21H
Mask Register 2	MOV aaH,MR2	0B22H
Memory at Address, Location set Valid, from:		
Comparand Register	MOV aaH,CR,V	0B24H
Masked by MR1	MOV aaH,CR[MR1],V	0B64H
Masked by MR2	MOV aaH,CR[MR2],V	0BA4H
Mask Register 1	MOV aaH,MR1,V	0B25H
Mask Register 2	MOV aaH,MR2,V	0B26H
Memory at Highest-priority Match, No Change to Validity bits, from:		
Comparand Register	MOV HM,CR	0328H
Masked by MR1	MOV HM,CR[MR1]	0368H
Masked by MR2	MOV HM,CR[MR2]	03A8H
Mask Register 1	MOV HM,MR1	0329H
Mask Register 2	MOV HM,MR2	032AH
Memory at Highest-priority Match, Location set Valid, from:		
Comparand Register	MOV HM,CR,V	032CH
Masked by MR1	MOV HM,CR[MR1],V	036CH
Masked by MR2	MOV HM,CR[MR2],V	03ACH
Mask Register 1	MOV HM,MR1,V	032DH
Mask Register 2	MOV HM,MR2,V	032EH
Memory at Next Free Address, No Change to Validity bits, from:		
Comparand Register	MOV NF,CR	0330H
Masked by MR1	MOV NF,CR[MR1],V	0370H
Masked by MR2	MOV NF,CR[MR2],V	03B0H
Mask Register 1	MOV NF,MR1	0331H
Mask Register 2	MOV NF,MR2	0332H

#### Instruction: Data Move (Cont'd)

Operation	Mnemonic	Op Code
Memory at Next Free Address, Location set Valid, from:		
Comparand Register	MOV NF,CR,V	0334H
Masked by MR1	MOV NF,CR[MR1],V	0374H
Masked by MR2	MOV NF,CR[MR2],V	03B4H
Mask Register 1	MOV NF,MR1,V	0335H
Mask Register 2	MOV NF,MR2,V	0336H

#### Instruction: Validity Bit Control

Operation	Mnemonic	Op Code
Set Validity bits at Address Register		
Set Valid	VBC [AR],V	0424H
Set Empty	VBC [AR],E	0425H
Set Skip	VBC [AR],S	0426H
Set Random Access	VBC [AR],R	0427H
Set Validity bits at Address		
Set Valid	VBC aaH,V	0C24H
Set Empty	VBC aaH,E	0C25H
Set Skip	VBC aaH,S	0C26H
Set Random Access	VBC aaH,R	0C27H
Set Validity bits at Highest-priority Match		
Set Valid	VBC HM,V	042CH
Set Empty	VBC HM,E	042DH
Set Skip	VBC HM,S	042EH
Set Random Access	VBC HM,R	042FH
Set Validity bits at All Matching Locations		
Set Valid	VBC ALM,V	043CH
Set Empty	VBC ALM,E	043DH
Set Skip	VBC ALM,S	043EH
Set Random Access	VBC ALM,R	043FH

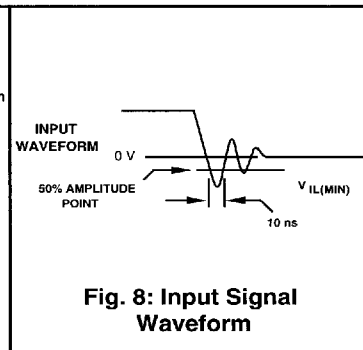
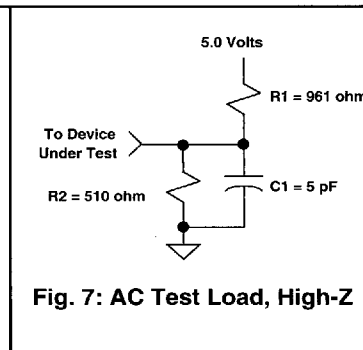
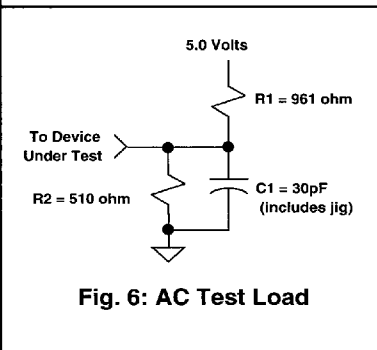
#### Instruction: Compare

Operation	Mnemonic	Op Code
Compare Valid Locations	CMP V	0504H
Compare Empty Locations	CMP E	0505H
Compare Skipped Locations	CMP S	0506H
Compare Random Access Locations	CMP R	0507H

#### Instruction: Special Instructions

Operation	Mnemonic	Op Code
Set Full Flag	SFF	0700H

### SWITCHING TEST FIGURES



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### ABSOLUTE MAXIMUM RATINGS

Supply Voltage	-0.5 to 7.0 Volts
Voltage on all Other Pins	-0.5 to VCC+0.5 Volts (-2.0 Volts for 10 ns, measured at the 50% point)
Temperature Under Bias	-40°C to +85°C
Storage Temperature	-55°C to +125°C
DC Output Current	20 mA (per Output, one at a time, one second duration)

Stresses exceeding those listed under Absolute Maximum Ratings may induce failure. Exposure to absolute maximum ratings for extended periods may reduce reliability. Functionality at or above these conditions is not implied.

All voltages are referenced to GND.

### OPERATING CONDITIONS (voltages referenced to GND at the device pin)

Symbol	Parameter	Min	Typical	Max	Units	Notes
V <sub>CC</sub>	Operating Supply Voltage	4.5	5.0	5.5	Volts	3
V <sub>IH</sub>	Input Voltage Logic "1"	2.2		V <sub>CC</sub> +0.5	Volts	
V <sub>IL</sub>	Input Voltage Logic "0"	-0.5		0.8	Volts	1, 2
T <sub>A</sub>	Ambient Operating Temperature	0		70	°C	Still Air

### ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typical	Max	Units	Notes
I <sub>CC</sub>	Average Power Supply Current			200	mA	
V <sub>OH</sub>	Output Voltage Logic "1"	2.4			Volts	I <sub>OH</sub> = -2.0 mA
V <sub>OL</sub>	Output Voltage Logic "0"			0.4	Volts	I <sub>OL</sub> = 4.0 mA
I <sub>Iz</sub>	Input Leakage Current	-2		2	μA	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>
I <sub>OZ</sub>	Output Leakage Current	-10		10	μA	V <sub>SS</sub> ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> ; DQ <sub>n</sub> = High Impedance

### CAPACITANCE

Symbol	Parameter	Max	Units	Notes
C <sub>IN</sub>	Input Capacitance	6	pF	f = 1 MHz, V <sub>IN</sub> = 0 V.
C <sub>OUT</sub>	Output Capacitance	7	pF	f = 1 MHz, V <sub>OUT</sub> = 0 V.

### AC TEST CONDITIONS

Input Signal Transitions	0.0 to 3.0 volts
Input Signal Rise Time	< 3 ns
Input Signal Fall Time	< 3 ns
Input Timing Reference Level	1.5 volts
Output Timing Reference Level	1.5 volts

### NOTES

- 1.0V for a duration of 10 ns measured at the 50% amplitude points for Input-only lines (Figure 8).
- Common I/O lines are clamped, so that signal transients cannot fall below -0.5V.
- At 5.0 ± 0.5 volts and 0-70° C, except for the -40 part which is 5.0 ± 0.25 volts.
- Applies to a Data Write to the Comparand or Mask registers (without a Compare), or a Command Write to a Register (except a Control register Reset), a TCO instruction, or a MOV between registers (e.g., a NOP).
- Applies to a Command Write of a VBC instruction, a MOV to the Comparand or Mask registers from Memory, or a Control register Reset, a Command Read from a register (e.g., a Status Read), a Data Read from the Comparand or Mask registers, or a Data Write to Memory.
- Applies to any Compare Cycle (a Data Write to the last segment of the Comparand or Mask registers, a Command Write of a CMP instruction or a non-resetting value to the Control register), a Data Read from Memory, or a Command Write of a MOV to Memory from the Comparand or Mask registers.
- Applies to a Command Read from a register (e.g., a Status Read), or a Data Read from the Comparand or Mask registers.
- Applies to a Data Read from Memory.
- Control signals are /W, /CM and /EC.
- With load specified in Figure 6.
- With load specified in Figure 7.

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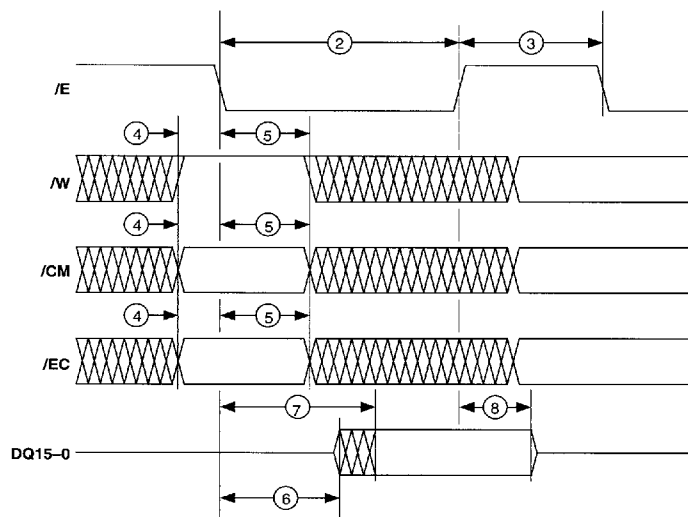
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### SWITCHING CHARACTERISTICS (see Note 3 under AC Test Conditions)

No	Symbol	Parameter (all times in nanoseconds)	-40		-55		Notes
			Min	Max	Min	Max	
1	t <sub>ELEL</sub>	Chip Enable Data Write (w/o Compare) Cycle Time	40		55		
2	t <sub>ELEH</sub>	Chip Enable LOW Pulse Width	25		35		4
			50		75		5
			75		100		6
3	t <sub>EHHL</sub>	Chip Enable HIGH Pulse Width	15		20		
4	t <sub>CVEL</sub>	Control Input to Chip Enable LOW Set-up Time	0		0		9
5	t <sub>ELCX</sub>	Control Input from Chip Enable LOW Hold Time	10		15		9
6	t <sub>ELQX</sub>	Chip Enable LOW to Outputs Active	3		3		10
7	t <sub>ELQV</sub>	Chip Enable LOW to Outputs Valid		50		70	7, 10
				75		85	8, 10
8	t <sub>EHQZ</sub>	Chip Enable HIGH to Outputs High-Z	3	15	3	20	11
9	t <sub>DVEL</sub>	Data to Chip Enable LOW Set-up Time	0		0		
10	t <sub>ELDX</sub>	Data from Chip Enable LOW Hold Time	10		15		
11	t <sub>FIVEL</sub>	Full In Valid to Chip Enable LOW Set-up Time	0		0		
12	t <sub>FIVFFV</sub>	Full In Valid to Full Flag Valid		7		8	
13	t <sub>ELFFV</sub>	Chip Enable LOW to Full Flag Valid		75		90	
14	t <sub>MIVEL</sub>	Match In Valid to Chip Enable LOW Set-up Time	0		0		
15	t <sub>EHMFV</sub>	Chip Enable HIGH to Match Flag Invalid	0		0		
16	t <sub>MIVMFV</sub>	Match In Valid to Match Flag Valid		7		8	
17	t <sub>EHMFV</sub>	Chip Enable HIGH to Match Flag Valid		25		30	

### TIMING DIAGRAMS

#### READ CYCLE

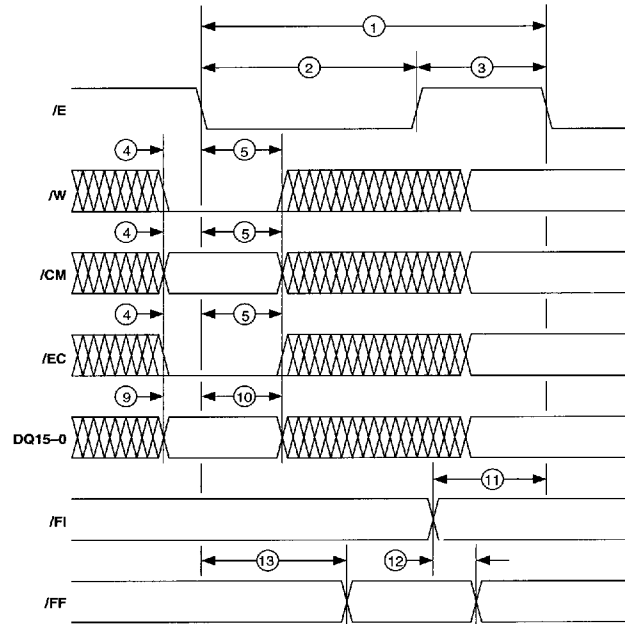


# MU9C1640

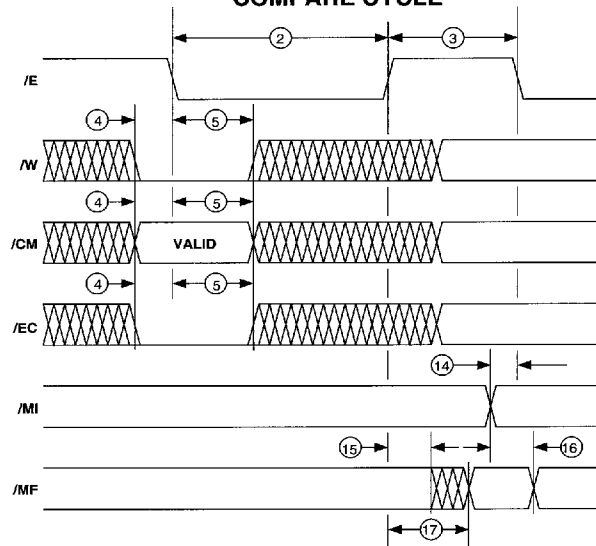
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### TIMING DIAGRAMS (CONT'D)

#### WRITE CYCLE



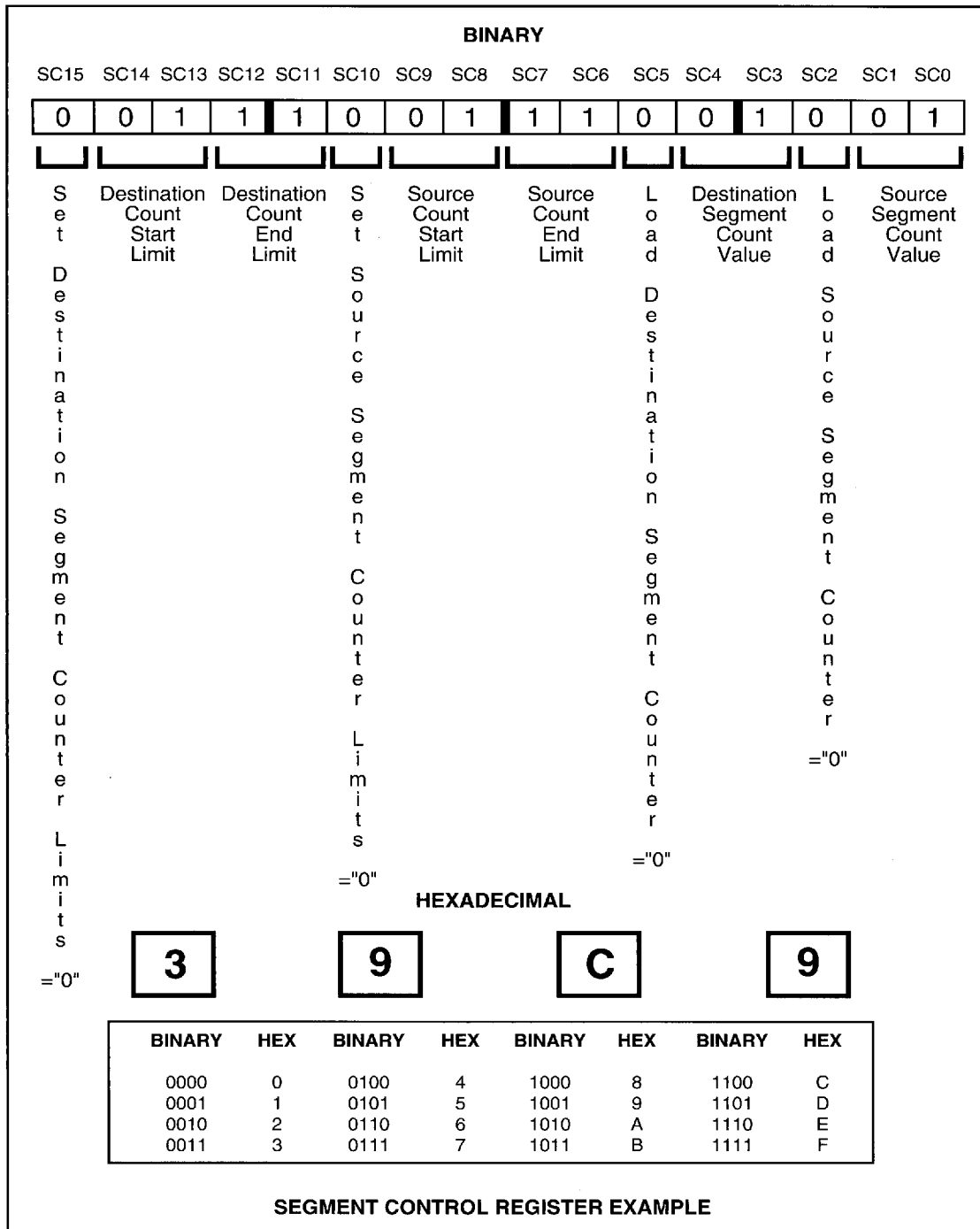
#### COMPARE CYCLE



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BINARY															
SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>		<input type="checkbox"/>	
S e t	Destination Count Start Limit		Destination Count End Limit		S e t	Source Count Start Limit		Source Count End Limit		L o a d	Destination Segment Count Value		L o a d	Source Segment Count Value	
D e s t i n a t i o n S e g m e n t C o u n t e r L i m i t s					S o u r c e S e g m e n t C o u n t e r L i m i t s					D e s t i n a t i o n S e g m e n t C o u n t e r L i m i t s			S o u r c e S e g m e n t C o u n t e r L i m i t s		
= "0"					= "0"					= "0"			= "0"		
HEXADECIMAL															
<input type="text"/>		<input type="text"/>		<input type="text"/>		<input type="text"/>		<input type="text"/>		<input type="text"/>		<input type="text"/>		<input type="text"/>	

BINARY	HEX	BINARY	HEX	BINARY	HEX	BINARY	HEX
0000	0	0100	4	1000	8	1100	C
0001	1	0101	5	1001	9	1101	D
0010	2	0110	6	1010	A	1110	E
0011	3	0111	7	1011	B	1111	F

**SEGMENT CONTROL REGISTER**

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### BINARY

CT15	CT14	CT13	CT12	CT11	CT10	CT9	CT8	CT7	CT6	CT5	CT4	CT3	CT2	CT1	CT0
					0	0								0	0

Res	Match Flag	Full Flag	Must be Set to "0"	CAM/RAM Partitioning	Masking	Address Inc/Dec	Must be Set to "0"
	Enable ="00"	Enable ="00"		0 RAM ="000"	Off ="00"	Increment ="00"	
	Disable ="01"	Disable ="01"		16 RAM ="001"	MR1 ="01"	Decrement ="01"	
= "0"	No change ="11"	No change ="11"		32 RAM ="010"	MR2 ="10"	Disable ="10"	
				48 RAM ="011"	No change ="11"	No change ="11"	
				64 RAM ="100"			
				No Change ="111"			

### HEXADECIMAL

BINARY	HEX	BINARY	HEX	BINARY	HEX	BINARY	HEX
0000	0	0100	4	1000	8	1100	C
0001	1	0101	5	1001	9	1101	D
0010	2	0110	6	1010	A	1110	E
0011	3	0111	7	1011	B	1111	F

### CONTROL REGISTER

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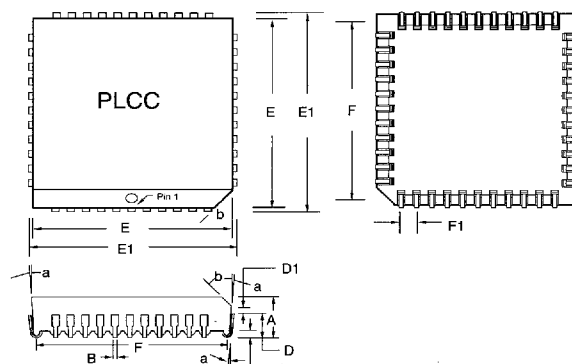
# MU9C1640

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### ORDERING INFORMATION

PART NUMBER	CYCLE TIME	PACKAGE	TEMPERATURE RANGE	VOLTAGE
MU9C1640-40DC	40ns	44-PIN PLCC	0-70°C	5.0 ± 0.25
MU9C1640-55DC	55ns	44-PIN PLCC	0-70°C	5.0 ± 0.5

### PACKAGE OUTLINE



Dimensions are in inches.

44-pin PLCC	Dim. A	Dim. B	Dim. C	Dim. D	Dim. E	Dim. E1	Dim. F	Dim. F1	Dim. a	Dim. b	
(in.)	.170 .180	.017 TYP	.018 .032	.100 TYP	.650 .656	.685 .695	.590 .630	.050 TYP	3° 6°	.045±.002 x 45°±2°	

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