16 x 16 multiplier-accumulators

LMA1010/1043

general information

The LMA1010/1043 are high speed, low power CMOS multiplier-accumulators (MACs). The LMA1010/LMA1043 are pin and functionally compatible with the TRW TDC1010/1043 and AMD Am29510 in DIP packages. The LOGIC Devices LMA2010/2043 offer compatible pinouts for surface mount packages.

The LMA1010/1043 produce the 32-bit product of two 16-bit numbers. The results of a series of multiplications may be accumulated to form a sum of products. Accumulation is performed to 35-bit precision with the multiplier product sign extended as appropriate.

Data present at the A and B input registers is latched in on the rising edges of CLK A and CLK B respectively, RND, TC, ACC, and SUB controls are latched on the rising edge of the logical OR of CLK A and CLK B. The TC control specifies the inputs as two's complement (TC high) or unsigned magnitude (TC low). RND, when high, adds 1 to the most significant bit position of the least significant half of the product. Subsequent truncation of the 16 least significant bits produces a result correctly rounded to 16-bit precision.

The ACC and SUB inputs control accumulator operation. Assertion of ACC results in addition of the multiplier result and the accumulator contents, with the result stored in the accumulator register at the rising edge of CLK R. ACC and SUB high results in subtraction of the accumulator contents from the multiplier product, with the result again stored in the accumulator register. With ACC low, no accumulation occurs and the next product is loaded directly into the output register.

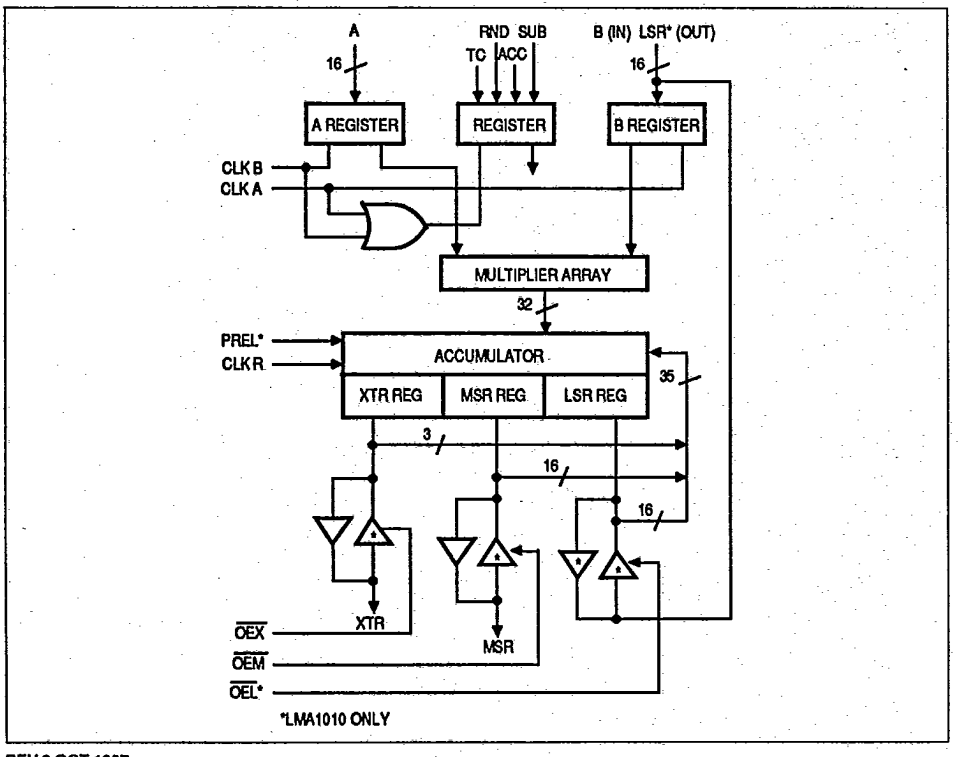
The LMA1010/1043 output (accumulator) register is divided into three independently controlled sections. The least significant result (LSR) and the most significant result (MSR) registers are 16 bits in length. The extended result register (XTR) is three bits long. In the LMA1010, the LSR output pins are multiplexed with the B inputs.

Each output register has an independent output enable control. In addition to providing three state control of the output buffers, when $\overline{OEX}$, $\overline{OEM}$, or $\overline{OEL}$ are high and PREL is high data can be preloaded via the bidirectional output pins into the appropriate output registers (LMA1010 only). Data present on the output pins is loaded in on the rising edge of CLK R. The interrelation of the PREL and the enable controls is summarized in the preload truth table.

features

- High-speed (45ns), low-power CMOS Multiplier-Accumulator
- Replaces TRW TDC1010/TDC1043 and AMD Am29510
- 16 x 16 bit multiplication and 35 bit product accumulation
- TTL compatible inputs and outputs
- Three-state outputs
- Two's complement and unsigned magnitude operands
- Accumulator performs accumulation, subtraction, and rounding
- Accumulator can be preloaded from external source (LMA1010 only)
- Available with full High-Rel screening

functional diagram



PRELOAD TRUTH TABLE
(LMA 1010 ONLY)

PREL	$\overline{OEX}$	$\overline{OEM}$	$\overline{OEL}$	XTR	MSR	LSR
L	L	L	L	OUT	OUT	OUT
L	L	L	H	OUT	OUT	Z
L	L	H	L	OUT	Z	OUT
L	L	H	H	OUT	Z	Z
L	H	L	L	Z	OUT	OUT
L	H	L	H	Z	OUT	Z
L	H	H	L	Z	Z	OUT
L	H	H	H	Z	Z	Z
H	L	L	L	Z	Z	Z
H	L	L	H	Z	Z	PREL
H	L	H	L	Z	PREL	Z
H	L	H	H	Z	PREL	PREL
H	H	L	L	PREL	Z	Z
H	H	L	H	PREL	Z	PREL
H	H	H	L	PREL	PREL	Z
H	H	H	H	PREL	PREL	PREL

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device pinouts

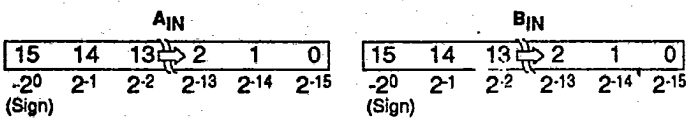
PIN P,D[1]	PIN G[2]	Function LMA1010/1043
1	F02	A6
2	F01	A5
3	E02	A4
4	E01	A3
5	D02	A2
6	D01	A1
7	C02	A0
8	C01	R0, B0
9	B02	R1, B1
10	A02	R2, B2
11	B03	R3, B3
12	A03	R4, B4
13	B04	R5, B5
14	A04	R6, B6
15	B05	R7, B7
16	A05	GND
17	B06	R8,B8
18	A06	R9,B9
19	B07	R10,B10
20	A07	R11,B11
21	B08	R12,B12
22	A08	R13,B13
23	B09	R14,B14
24	A09	R15,B15
25	B10	R16
26	B11	R17
27	C10	R18
28	C11	R19
29	D10	R20
30	D11	R21
31	E10	R22
32	E11	R23
33	F10	R24
34	F11	R25
35	G10	R26
36	G11	R27
37	H10	R28
38	H11	R29
39	J10	R30
40	J11	R31
41	K10	R32
42	L10	R33
43	K09	R34
44	L09	CLKR
45	K08	$\overline{OEM}$
46	L08	PREL/GND
47	K07	$\overline{OEX}$
48	L07	TC
49	K06	V_{CC}
50	L06	CLKB
51	K05	CLKA
52	L05	ACC
53	K04	SUB
54	L04	RND
55	K03	$\overline{OEL}$/NC
56	L03	A15
57	K02	A14
58	K01	A13
59	J02	A12
60	J01	A11
61	H02	A10
62	H01	A9
63	G02	A8
64	G01	A7
	A10	NC
	K11	NC
	L02	NC
	B01	NC

NC= No Connection
1) Pins are sequenced counterclockwise from the pin 1 indicator in the top view
2) See mechanical data section of LOGIC DEVICES PRODUCT CATALOG for pin number to pin location correspondence

INPUT FORMATS

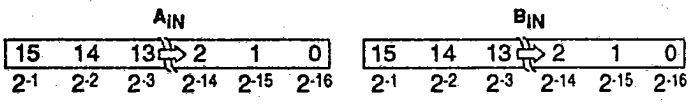
Fractional Two's Complement

TC=1



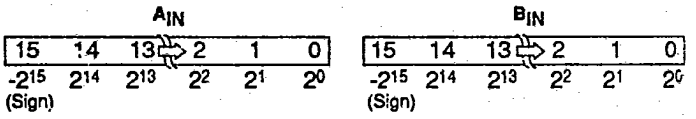
Unsigned Fractional

TC=0



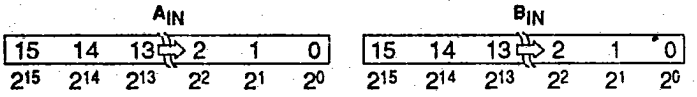
Integer Two's Complement

TC=1



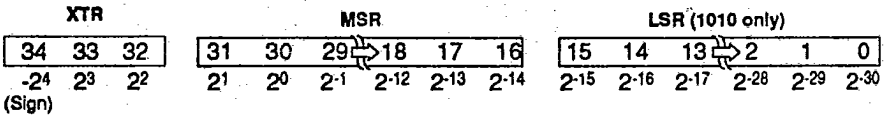
Unsigned Integer

TC=0

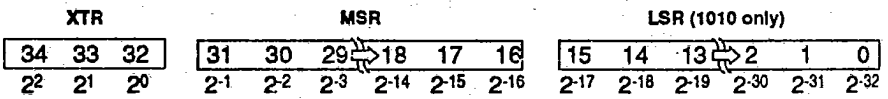


OUTPUT FORMATS

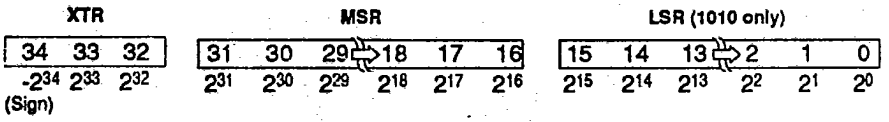
Fractional Two's Complement



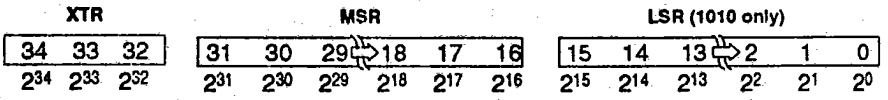
Unsigned Fractional



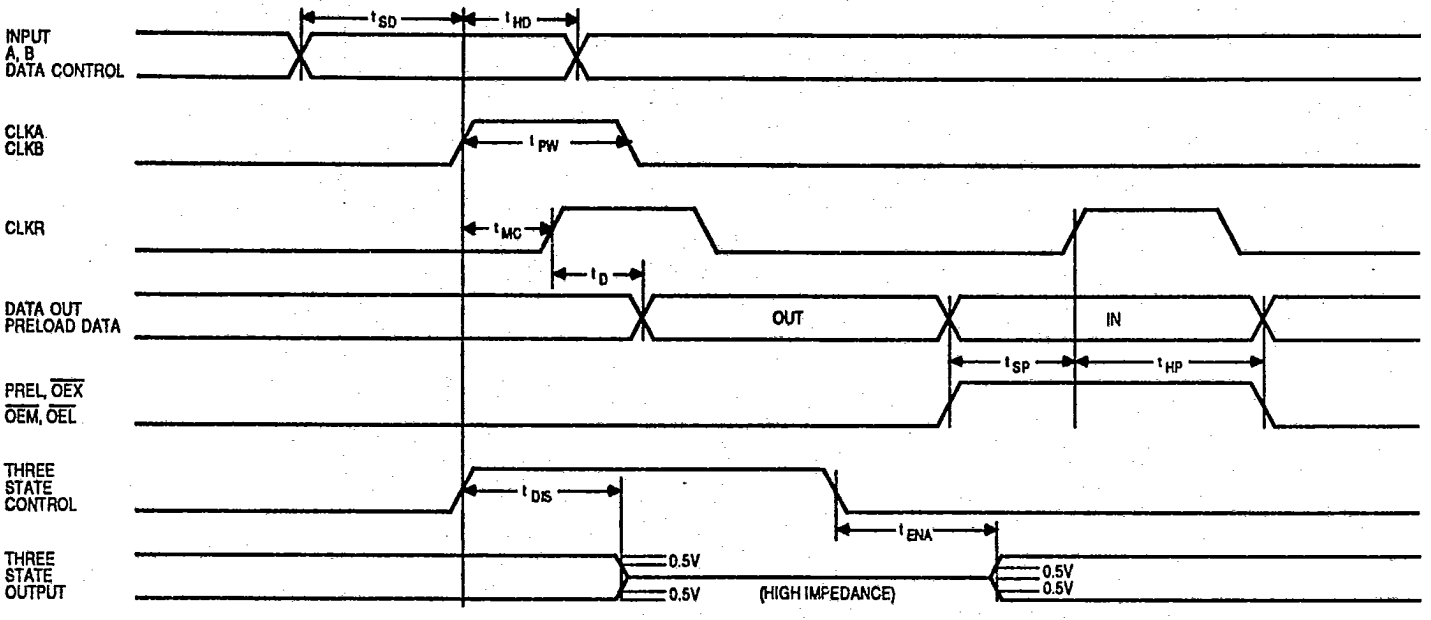
Integer Two's Complement



Unsigned Integer



timing diagram



switching characteristics

I. LMA1010/1043 Guaranteed Performance - Commercial Range

	Suffix:	None		65		55		45		units
PARAMETER	DESCRIPTION	min	max	min	max	min	max	min	max	
t_{MC}	Clocked Multiply-Accumulate Time		120		65		55		45	ns
t_D	Clock to Output Time		35		30		25		25	
t_{ENA}	Output Enable Time		35		30		30		30	
t_{DIS}	Output Disable Time		32		30		25		25	
t_{HD}	Data/Control Hold Time	3		0		0		0		
t_{HP}	Preload Hold Time	2		0		0		0		
t_{SD}	Data/Control Set-Up Time	20		15		15		10		
t_{SP}	Preload Set-Up Time	20		15		15		10		
t_{PW}	A, B, C, Clock Pulse Width	20		15		15		15		

AC TEST CONDITIONS: Input levels: 0 to 3V | Output timing reference level: 1.5V | Output load: 1.0KΩ to 5V, 820Ω to GND, 60pF to GND

II. LMA1010/1043 Guaranteed Performance - Military Range

	Suffix:	None		75		65		55		units
PARAMETER	DESCRIPTION	min	max	min	max	min	max	min	max	
t_{MC}	Clocked Multiply-Accumulate Time		140		75		65		55	ns
t_D	Clock to Output Time		45		35		30		30	
t_{ENA}	Output Enable Time		40		35		30		30	
t_{DIS}	Output Disable Time		40		35		25		25	
t_{HD}	Data/Control Hold Time	3		0		0		0		
t_{HP}	Preload Hold Time	3		0		0		0		
t_{SD}	Data/Control Set-Up Time	25		20		15		10		
t_{SP}	Preload Set-Up Time	25		20		15		10		
t_{PW}	A, B, C, Clock Pulse Width	25		20		15		15		

AC TEST CONDITIONS: Input levels: 0 to 3V | Output timing reference level: 1.5V | Output load: 1.0KΩ to 5V, 820Ω to GND, 60pF to GND

16 x 16 multiplier-accumulators absolute maximum ratings

Supply Voltage	-0.5V to 7.0V
Input Voltage	0V to 5.5V
Output Voltage	0V to 5.5V
Operating Temperature (Ambient)	-55°C to 125 °C
Storage Temperature	-65°C to 150°C

recommended operating conditions

PARAMETER	DESCRIPTION		min	typ	max	unit
V_{CC}	Supply Voltage	Commercial	4.75	5.0	5.25	V
		Military	4.50	5.0	5.5	V
I_{OL}	Low Level Output Current				4.0	mA
I_{OH}	High Level Output Current				-2.0	mA
T_{AMB}	Operating Temperature	Commercial	0	25	70	°C
		Military	-55	25	125	°C

electrical characteristics

PARAMETER	DESCRIPTION		min	typ	max	unit
V_{IL}	Low level Input Voltage				0.8	V
V_{IH}	High Level Input Voltage		2.0			V
V_{OL}	Low Level Output Voltage (I_{OL} = 8 mA)				0.5	V
V_{OH}	High Level Output Voltage (I_{OH} = -2 mA)		3.5			V
I_{IL}	Low Level Input Current (V_{IL} = 0.4 V)				20	µA
I_{IH}	High Level Input Current (V_{IH} = 2.4 V)				20	µA
I_{OZ}	Output Current (High-Impedance State)				20	µA
I_{CC}	Supply Current	(Quiescent)			1.0	mA
		(Dynamic)		12[1]	25[2]	mA

1) 5 MHz clock rate, TTL Input levels; V_{CC} = 5V; T_A = 25° C; random input patterns; no load.
2) 5 MHz clock; V_{IH} = 2.0V, V_{IL} = 0.8V, V_{CC} = 5.5V, T_A = -55°C, all outputs toggling every cycle; no load.

LMA1010/1043 ordering information

Ordering Code	Speed (NS)	Package Type	Operating Range
LMA1010 PC-45	45	P4	Commer-
LMA1010 DC-45		D6	cial
LMA1010 GC-45		G2	
LMA1010 PCR-45		P4	
LMA1010 DCR-45		D6	
LMA1010 GCR-45		G2	
LMA1010 PC-55	55	P4	Commer-
LMA1010 DC-55		D6	cial
LMA1010 GC-55		G2	
LMA1010 PCR-55		P4	
LMA1010 DCR-55		D6	
LMA1010 GCR-55		G2	
LMA1010 DM-55	55	D6	Military
LMA1010 DMB-55		D6	
LMA1010 GM-55		G2	
LMA1010 GMB-55		G2	
LMA1010 PC-65	65	P4	Commer-
LMA1010 DC-65		D6	cial
LMA1010 GC-65		G2	
LMA1010 PCR-65		P4	
LMA1010 DCR-65		D6	
LMA1010 GCR-65		G2	
LMA1010 DM-65	65	D6	Military
LMA1010 DMB-65		D6	
LMA1010 GM-65		G2	
LMA1010 GMB-65		G2	
LMA1010 DM-75	75	D6	Military
LMA1010 DMB-75		D6	
LMA1010 GM-75		G2	
LMA1010 GMB-75		G2	
LMA1010 PC	120	P4	Commer-
LMA1010 DC		D6	cial
LMA1010 GC		G2	
LMA1010 PCR		P4	
LMA1010 DCR		D6	
LMA1010 GCR		G2	
LMA1010 DM	140	D6	Military
LMA1010 DMB		D6	
LMA1010 GM		G2	
LMA1010 GMB		G2	

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