

DESCRIPTION

The HY5118160B is the new generation and fast dynamic RAM organized 1,048,576 x 16-bit. The HY5118160B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY5118160B to be packaged in a standard 42/42 pin plastic SOJ, 44/50 pin TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of $5V \pm 10\%$ tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. battery back-up 1.9mW (SL-part)
Max. CMOS standby 1.7mW (SL-part)
5.5mW
Max. TTL standby 11.0mW
Max. operating

Speed	Power
60	880mW
70	825mW
80	770mW

- Single power supply of $5V \pm 10\%$
- TTL compatible inputs and outputs
- Fast access and cycle time

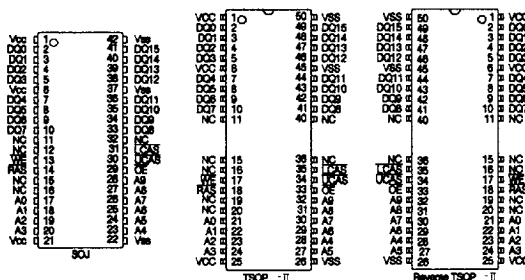
Speed	t _{TRC}	t _{CAC}	t _{PC}
60	60ns	15ns	40ns
70	70ns	20ns	45ns
80	80ns	20ns	50ns

- Fast Page mode operation
- 2CAS Inputs for upper and lower byte control
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self Refresh capability
- 1024 refresh cycles / 256ms (SL-part)
1024 refresh cycles / 16ms

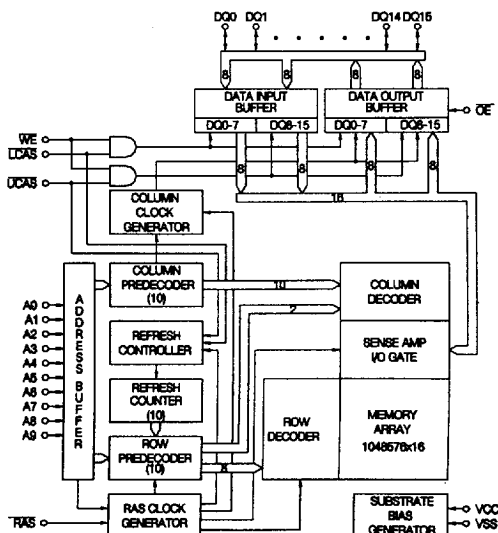
PIN DESCRIPTION

RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A9	Address input
DQ0-DQ15	Data Input/Output
Vcc	Power (+5V)
Vss	Ground

PIN CONNECTION



BLOCK DIAGRAM



4675088 0004752 T75

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1AD54-10-MAY95

ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
T _A	Ambient Temperature	0 to 70	°C
T _{STG}	Storage Temperature	- 55 to 150	°C
V _{IN} , V _{OUT}	Voltage on Any Pin Relative to V _{SS}	- 1.0 to 7.0	V
V _{CC}	Voltage on V _{CC} Relative to V _{SS}	- 1.0 to 7.0	V
I _{OS}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	1.0	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
V _{SS}	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.4	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-1.0	-	0.8	V

NOTE: All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=5V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	$V_{SS} \leq V_{IN} \leq V_{CC}+1.0V$ All other pins not under test= V_{SS}		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	$V_{SS} \leq V_{OUT} \leq V_{CC}$ RAS & CAS at V_{IH}		-10	10	μA	
ICC1	Vcc Supply Current, Operating	trc = trc (min.)	60 70 80	- - -	160 150 140	mA	1,2,3
ICC2	Vcc Supply Current, TTL Standby	RAS & CAS at V_{IH} , other inputs V_{SS}	SL-Part	- -	2 1	mA	
ICC3	Vcc Supply Current, RAS-only Refresh	trc = trc (min.)	60 70 80	- - -	160 150 140	mA	1,3
ICC4	Vcc Supply Current, Fast Page mode	tpc = tpc (min.)	60 70 80	- - -	110 100 90	mA	1,2,3
ICC5	Vcc Supply Current, CMOS Standby	RAS & CAS $\geq V_{CC}-0.2V$	SL-part	- -	1 300	mA μA	5
ICC6	Vcc Supply Current, CAS-before- RAS Refresh	trc = trc (min.)	60 70 80	- - -	160 150 140	mA	1,2
ICC7	Vcc Supply Current, Battery Back up (SL-part only)	trc = 250 μs , CAS = CBR cycling or 0.2V OE & WE= $V_{CC}-0.2V$ or 0.2V A0-A9 = $V_{CC}-0.2V$ or 0.2V DQ0 -DQ15= -0.2V, $V_{CC}-0.2V$ or open	trAS $\leq$ 300ns trAS $\leq$ 1 μs	- -	350 450	μA	4,5
ICC8	Vcc Supply Current, Self Refresh (SL-part only)	RAS & CAS $\leq 0.2V$ other pins same as ICC7		-	350	μA	5
VOL	Output Low Voltage	IOL = 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH = -5.0mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rate.
2. ICC1, ICC3, ICC4 and ICC6 are dependent on output loading. Specified values are obtained with the output open.
3. ICC is specified as an average current. ICC1, ICC3, ICC6, Address can be changed maximum two times while $\overline{RAS} = V_{IL}$. ICC4, Address can be changed maximum once while $\overline{CAS} = V_{IH}$.
4. Only trAS(max.)=1 μs is applied to refresh of battery backup but trAS(max.)=10 μs is applied to normal functional operation .
5. ICC5(max.) =300 μA , ICC7 and ICC8 are applied to SL-part only.

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=5V ± 10%, VSS=0V, unless otherwise noted.) NOTE3,7,8

#	SYMBOL	PARAMETER	HY5118160BJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			- 60		- 70		- 80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	170	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	95	-	105	-	ns	
5	tRAC	Access Time from $\overline{\text{RAS}}$	-	60	-	70	-	80	ns	8,9,10
6	tCAC	Access Time from $\overline{\text{CAS}}$	-	15	-	20	-	20	ns	8,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	
8	tCPA	Access Time from $\overline{\text{CAS}}$ Precharge		35		35		45	ns	8,15
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	8
10	tOFF	Output Buffer Turn-off Delay from $\overline{\text{CAS}}$	0	15	0	15	0	15	ns	11
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	6
12	tRP	$\overline{\text{RAS}}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{\text{RAS}}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	$\overline{\text{RAS}}$ Hold Time	15	-	20	-	20	-	ns	
16	tCSH	$\overline{\text{CAS}}$ Hold Time	40	-	50	-	60	-	ns	
17	tCAS	$\overline{\text{CAS}}$ Pulse width	15	10K	15	10K	20	10K	ns	
18	tRCD	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	15	45	20	50	20	60	ns	9
19	tRAD	$\overline{\text{RAS}}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	$\overline{\text{CAS}}$ Precharge Time	10	-	10	-	10	-	ns	20
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	15
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	15
26	tRAL	Column Address to $\overline{\text{RAS}}$ Lead Time	30	-	35	-	40	-	ns	
27	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	15
28	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	13,15
29	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	15
30	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	15
31	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
32	tRWL	Write Command to $\overline{\text{RAS}}$ Lead Time	20	-	20	-	20	-	ns	
33	tCWL	Write Command to $\overline{\text{CAS}}$ Lead Time	20	-	20	-	20	-	ns	22
34	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	15,25
35	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	15,25
36	tREF	Refresh Period (1024 cycles)		16		16		16	ms	18
		SL-part		256		256		256	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	15,16
38	tCWD	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	45	-	50	-	50	-	ns	16
39	tRWD	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	85	-	95	-	105	-	ns	16
40	tAWD	Column Address to $\overline{\text{WE}}$ Delay Time.	55	-	60	-	65	-	ns	16

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	5118160BJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			- 60		- 70		- 80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time(CBR Cycle)	5	-	5	-	5	-	ns	15
42	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15,23
43	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	15,24
44	tCPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	20
45	tROH	RAS Hold Time Reference to OE	10	-	10	-	10	-	ns	
46	tOEA	OE Access Time	-	15	-	20	-	20	ns	
47	tOED	OE to Data Delay	15	-	20	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time	0	15	0	15	0	15	ns	11
49	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	
50	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	16
51	tRHCP	RAS Hold Time from CAS Precharge	40	-	40	-	50	-	ns	
52	tWRP	WE to RAS Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	
53	tWRH	WE to RAS Hold Time(CBR Cycle)	10	-	10	-	10	-	ns	
54	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	μs	
55	tRPS	RAS Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	
56	tCHS	CAS Hold Time (Self Refresh Cycle)	50	-	50	-	50	-	ns	

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NOTE:

1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages referenced to Vss.
3. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles are required.
4. Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$. In case of changed once or less during a fast page mode cycle (tPC).
5. AC measurements assume $t_t = 3\text{ns}$.
6. $\text{VIH}(\text{min.})$ and $\text{VIL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL .
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_A = 0$ to 70°C) is assured.
8. Measured at $\text{VOH}=2.4\text{V}$ and $\text{VOL}=0.4\text{V}$ with a load equivalent to 2TTL load and 100pF.
9. Operation within the $\text{tRCD}(\text{max.})$ limit insures that $\text{tRAC}(\text{max.})$ can be met.
 $\text{tRCD}(\text{max.})$ is specified as a reference point only. If tRCD is greater than the specified $\text{tRCD}(\text{max.})$ limit, then access time is controlled by tCAC .
10. Operation within the $\text{tRAD}(\text{max.})$ limit insures that $\text{tRAC}(\text{max.})$ can be met.
 $\text{tRAD}(\text{max.})$ is specified as a reference point only. If tRAD is greater than the specified $\text{tRAD}(\text{max.})$ limit, then access time is controlled by tAA .
11. $\text{tOFF}(\text{max.})$, $\text{tREZ}(\text{max.})$, $\text{tWEZ}(\text{max.})$, $\text{tOEZ}(\text{max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. The tCRP requirement should be applicable for $\overline{\text{RAS}} / \overline{\text{CAS}}$ cycles preceded by any cycle.
13. Either tRCH or tRRH must be satisfied for a read cycle.
14. Parameter tWP is applicable for a late write cycle. For early write cycle, tWCH must be met.
15. These parameters are referenced to $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
16. twCS , trWD , tcWD , tAWD , and tcpWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $\text{twCS} \geq \text{twCS}(\text{min.})$, the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) through the entire cycle; If $\text{trWD} \geq \text{trWD}(\text{min.})$, $\text{tcWD} \geq \text{tcWD}(\text{min.})$, $\text{tAWD} \geq \text{tAWD}(\text{min.})$, and $\text{tcpWD} \geq \text{tcpWD}(\text{min.})$ (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell: If neither of the above sets of condition of the data out (at access time) is interminate.
17. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
18. 1024 cycles of Burst refresh must be excuted within 16ms after exiting Self Refresh.
19. tASC , tCAH are referenced to the earlier $\overline{\text{CAS}}$ falling edge.
20. tcp and tcPT are measured when both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ are high state.
21. tcWD is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
22. tcWL must be satisfied by both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ for 16-bits access cycles.
23. tCSR is referenced to the earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
24. tCHR is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.
25. tDS , tDH is independetly specified for lower byte DQ(0-7), upper byte DQ(8-15).

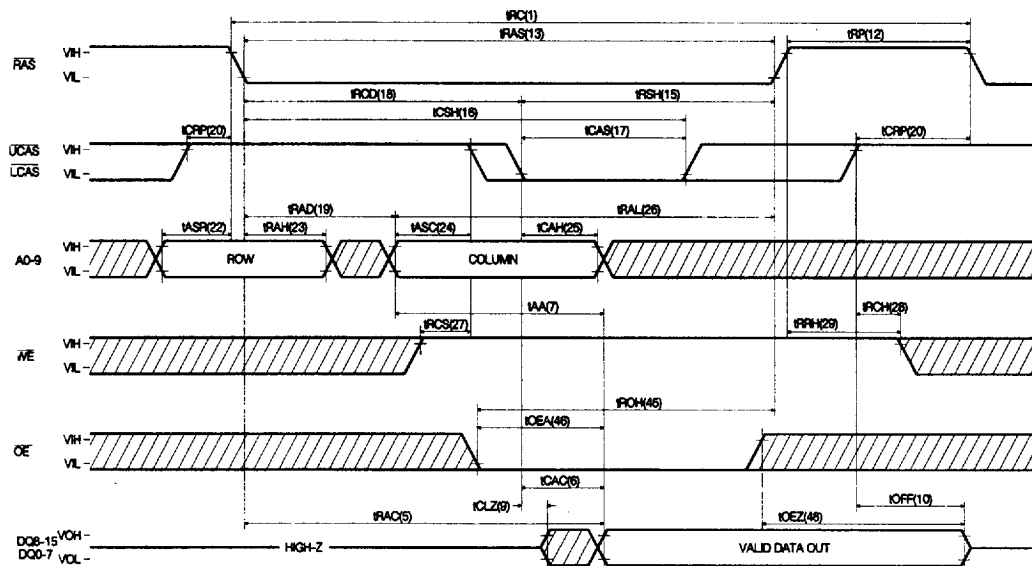
CAPACITANCE

($T_A=25^\circ\text{C}$, $\text{Vcc}=5\text{V}\pm 10\%$, $\text{Vss}=0\text{V}$, $f=1\text{MHz}$, unless otherwise noted.)

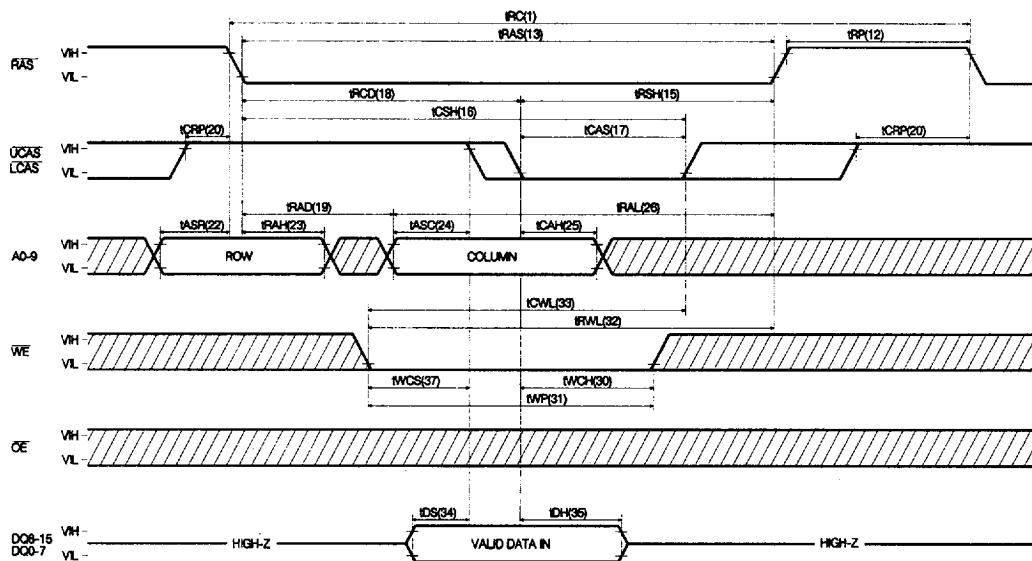
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A9)	-	5	pF
CIN2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, OE)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0 - DQ15)	-	7	pF

TIMING DIAGRAM

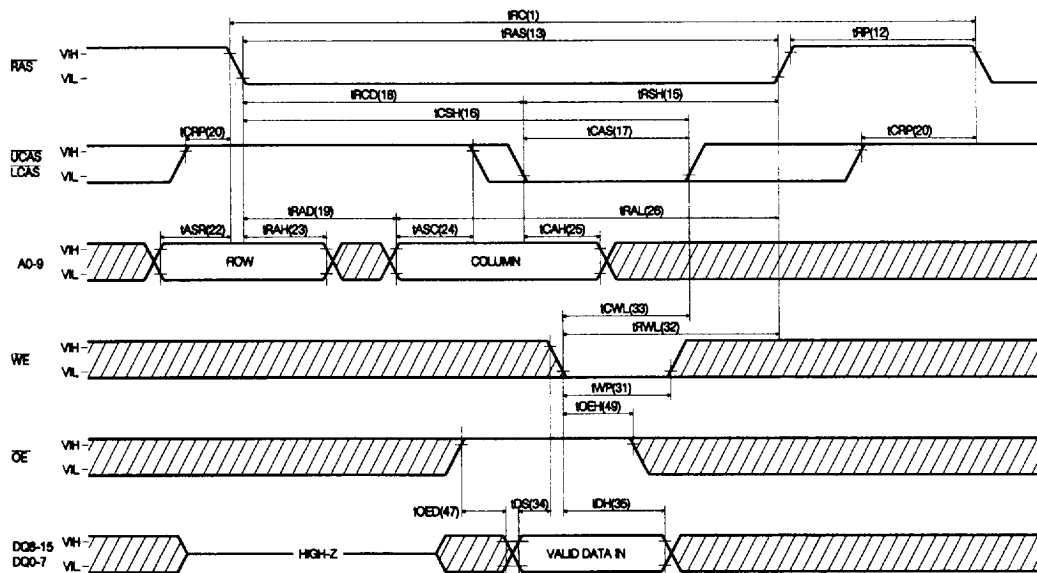
READ CYCLE



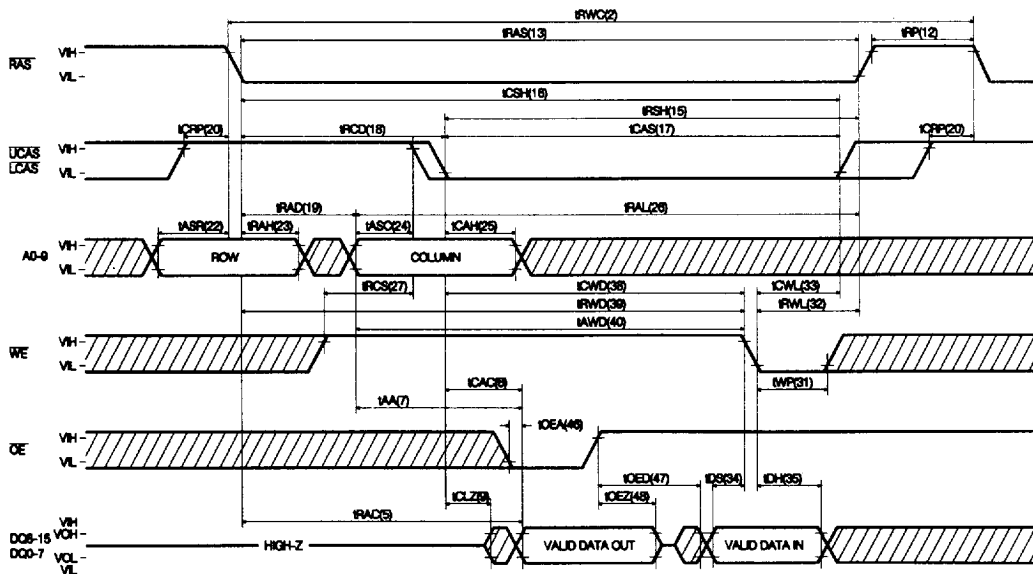
EARLY WRITE CYCLE



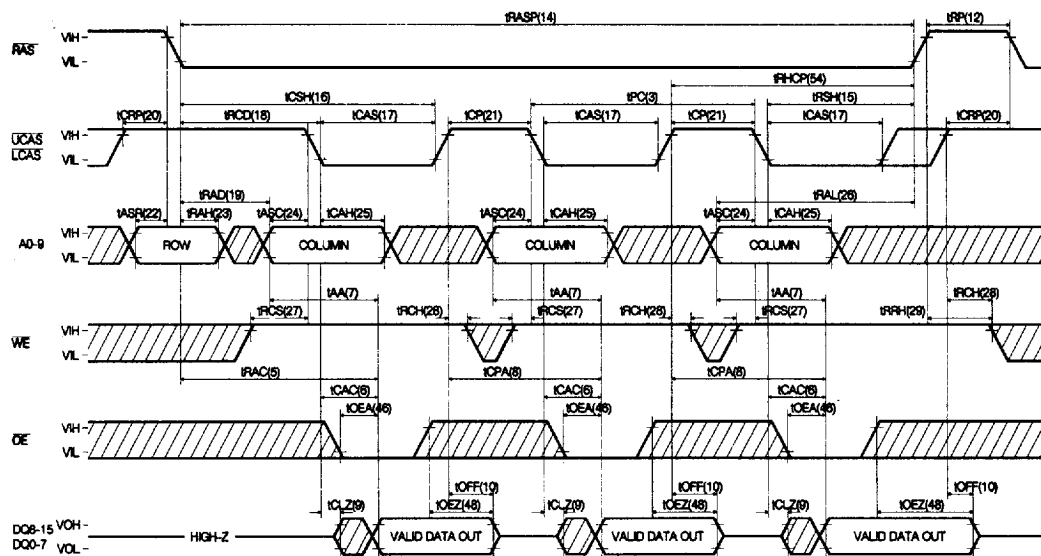
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



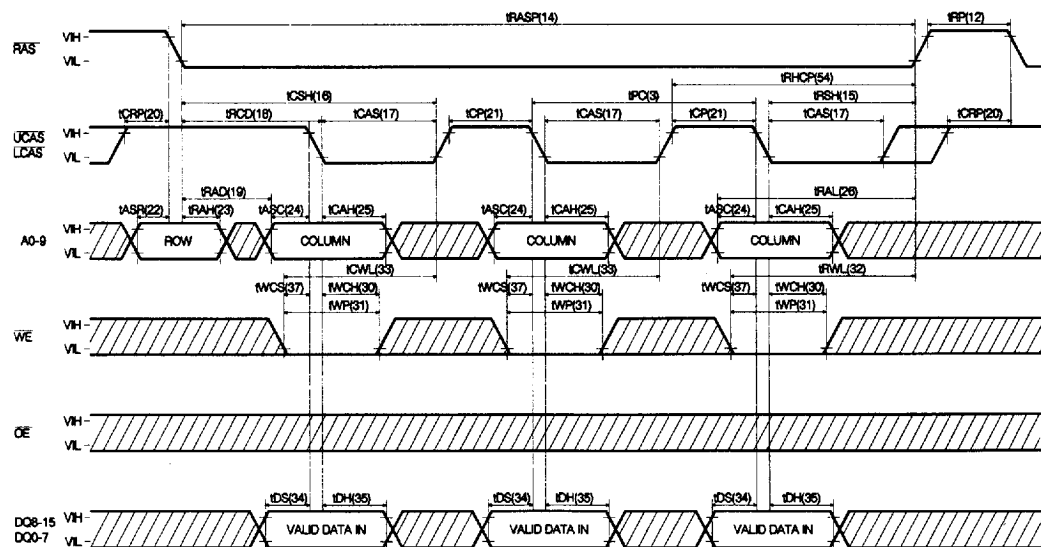
READ-MODIFY-WRITE CYCLE



FAST PAGE MODE READ CYCLE

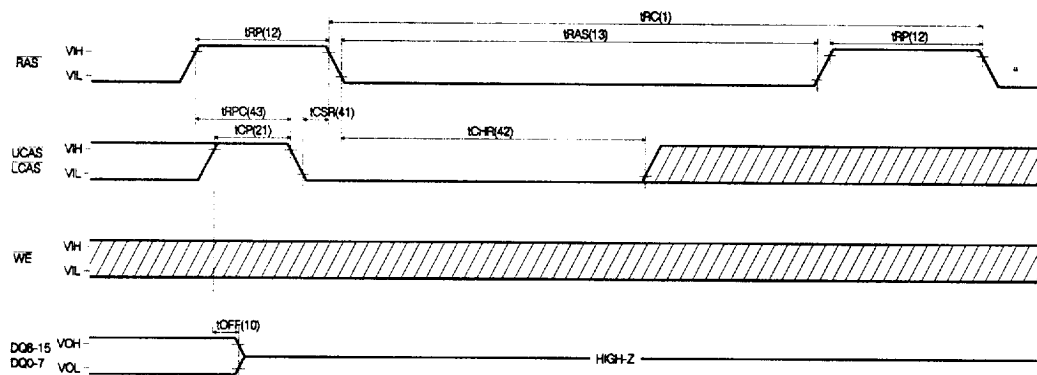


FAST PAGE MODE EARLY WRITE CYCLE



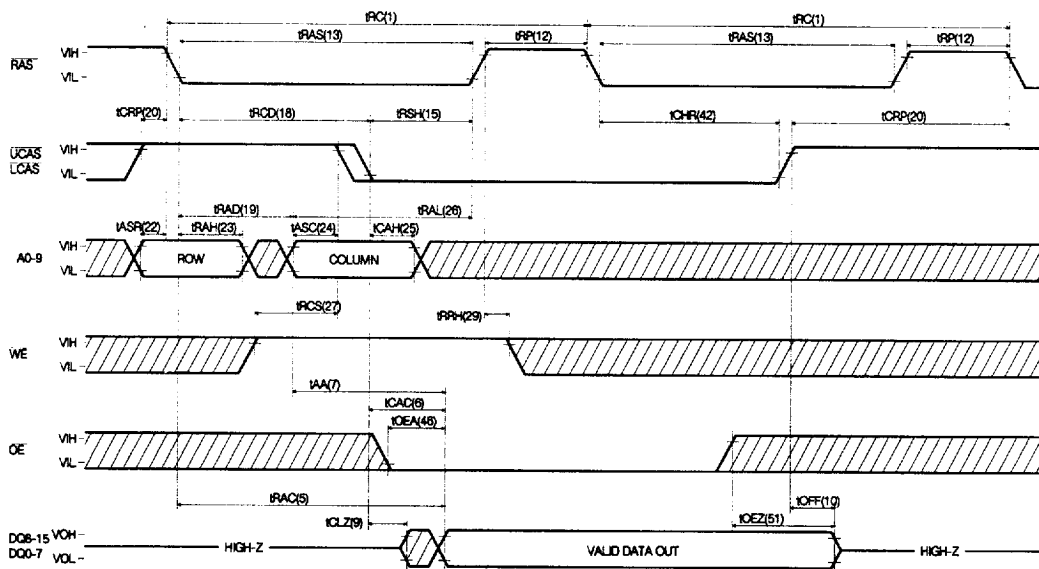
NOTE : OE and WE ="H" or "L"

CAS-BEFORE-RAS REFRESH CYCLE

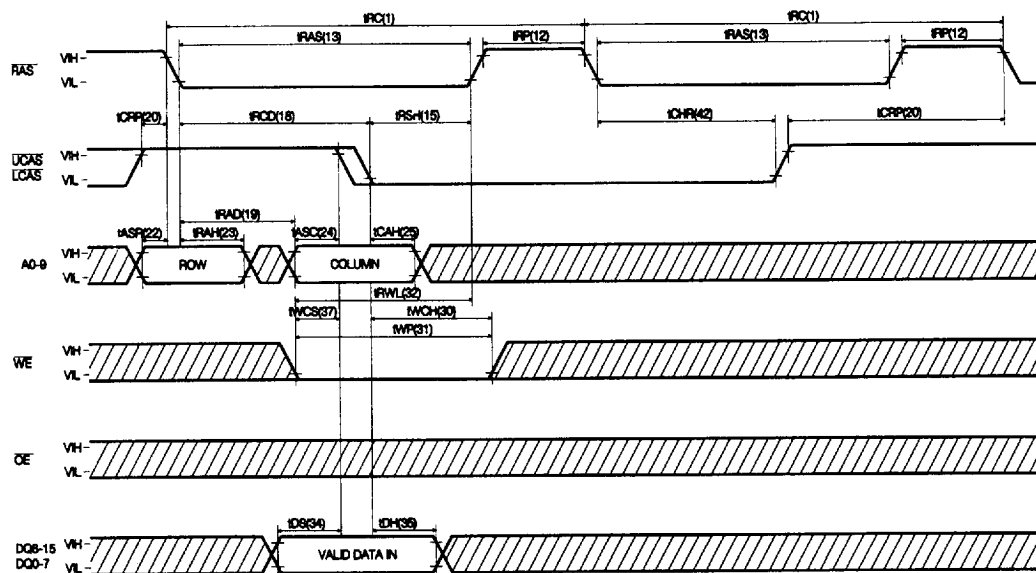


NOTE : A0-9 and OE = "H" or "L"

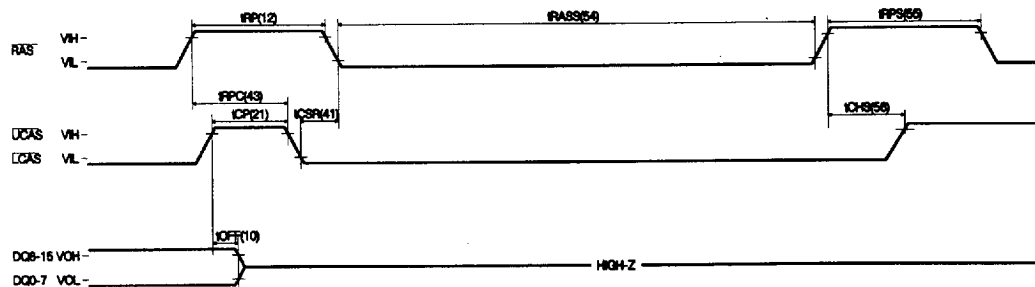
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



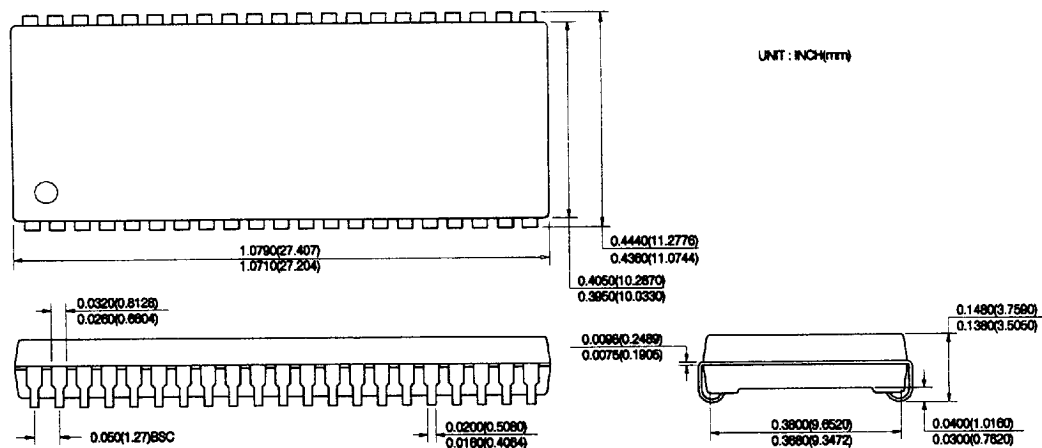
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



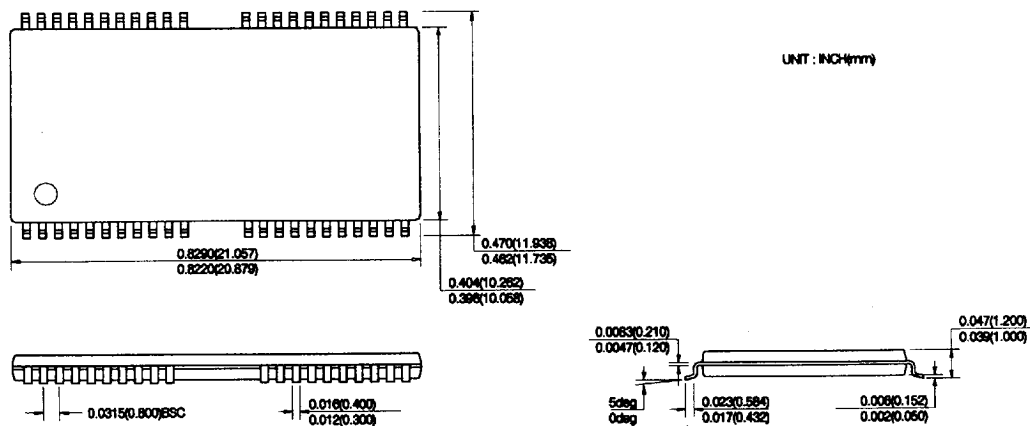
NOTE : A0-9 OE and WE = "H" or "L"

PACKAGE INFORMATION

400 mil 42/42 pin Small Outline J-form Package (JC)



400 mil 44/50 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAG6E
HY5118160BJC	60/70/80		SOJ
HY5118160BSLJC	60/70/80	SL-part	SOJ
HY5118160BTC	60/70/80		TSOP-II
HY5118160BSLTC	60/70/80	SL-part	TSOP-II
HY5118160BRC	60/70/80		TSOP-II(R)
HY5118160BSLRC	60/70/80	SL-part	TSOP-II(R)