10-Bit, 125/60 MSPS, High Speed D/A Converter

Features

- **Throughput Rate** . . . . **125 MSPS**

- **Low Power** . . . . **165mW at 5V, 27mW at 3V**

- **Power Down Mode** . . . . **23mW at 5V, 10mW at 3V**

- **Integral Linearity Error** . . . . **±1 LSB**

- **Adjustable Full Scale Output Current** . . **2mA to 20mA**

- **SFDR to Nyquist at 40MHz Output** **52dBc**

- **Internal 1.2V Temperature Compensated Bandgap Voltage Reference**

- **Single Power Supply from +5V to +3V**

- **CMOS Compatible Inputs**

- **Excellent Spurious Free Dynamic Range**

Applications

- **Cable Modems**

- **Set Top Boxes**

- **Wireless Communications**

- **Direct Digital Frequency Synthesis**

- **Signal Reconstruction**

- **Test Instrumentation**

- **High Resolution Imaging Systems**

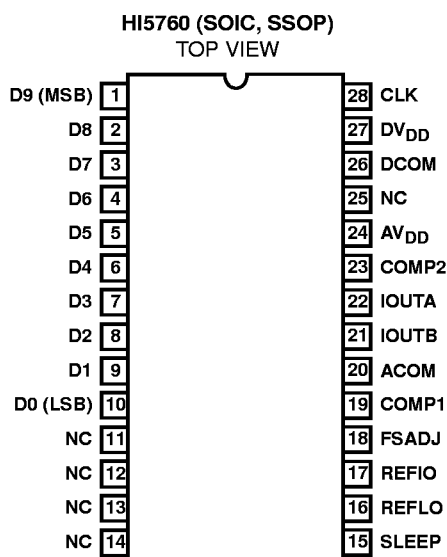- **Arbitrary Waveform Generators**

Description

The HI5760 is a 10-bit, 125 MSPS, high speed, low power, D/A converter which is implemented in an advanced CMOS process. Operating from a single +3V to +5V supply, the converter provides 20mA of full scale output current and includes edge-triggered CMOS input data latches. Low glitch energy and excellent frequency domain performance are achieved using a segmented current source architecture. For an equivalent performance dual version, see the HI5728. For lower speed applications, a 60 MSPS version is available.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.	CLOCK SPEED
HI5760BIB	-40 to 85	28 Ld SOIC	M28.3	125MHz
HI5760IA	-40 to 85	28 Ld SSOP	M28.15	125MHz
HI5760/6IB†	-40 to 85	28 Ld SOIC	M28.3	60MHz
HI5760/6IA†	-40 to 85	28 Ld SSOP	M28.15	60MHz
HI5760EVAL1	25	Evaluation Platform		125MHz

† Contact factory for availability.

Pinout

HI5760 (SOIC, SSOP)
TOP VIEW

D9 (MSB) [1]	[28] CLK
D8 [2]	[27] DV$_{DD}$
D7 [3]	[26] DCOM
D6 [4]	[25] NC
D5 [5]	[24] AV$_{DD}$
D4 [6]	[23] COMP2
D3 [7]	[22] IOUTA
D2 [8]	[21] IOUTB
D1 [9]	[20] ACOM
D0 (LSB) [10]	[19] COMP1
NC [11]	[18] FSADJ
NC [12]	[17] REFIO
NC [13]	[16] REFLO
NC [14]	[15] SLEEP

File Number **4320.2**

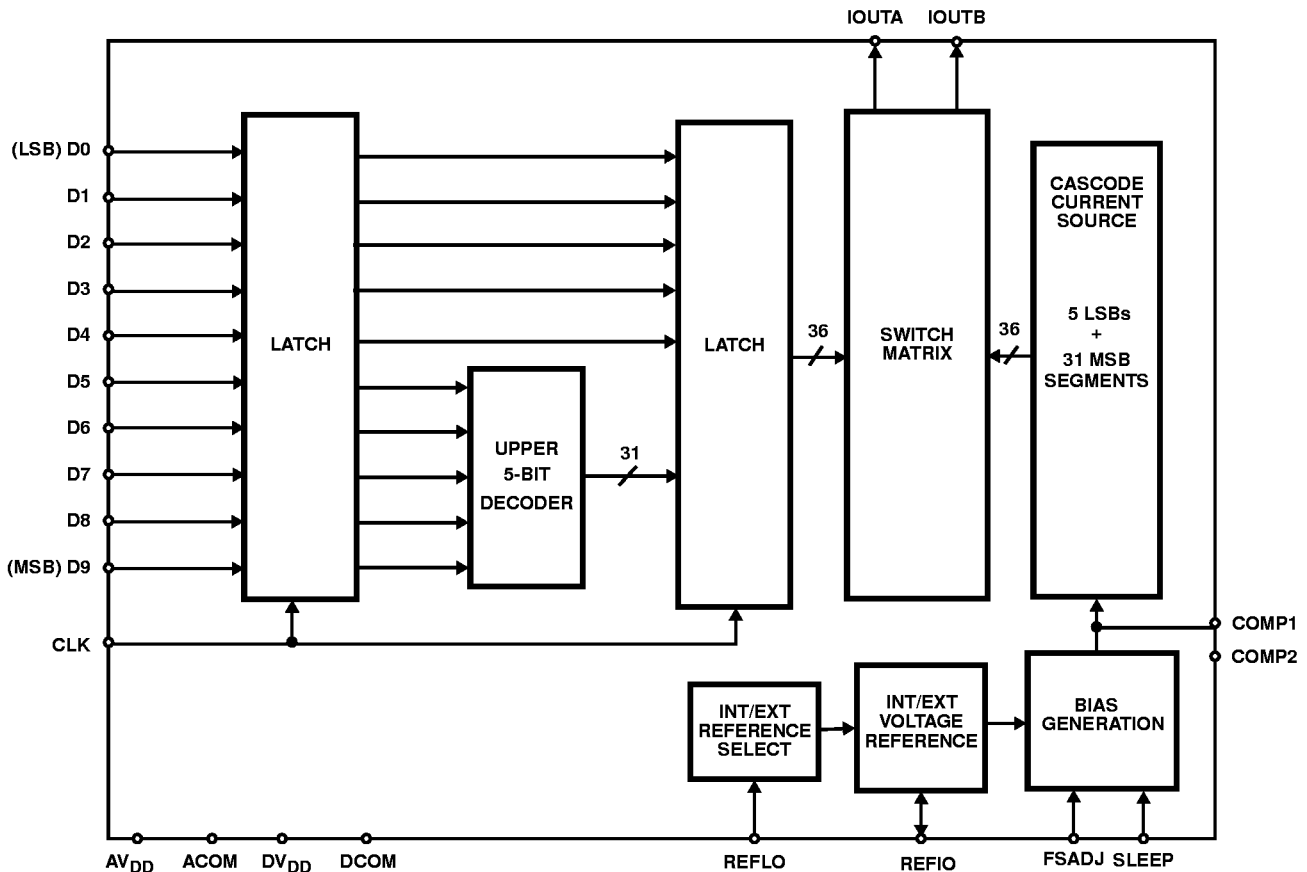## Typical Applications Circuit

NOTE: This schematic demonstrates the single supply, single ground plane method of using the DAC. Separate analog and digital grounds can also be used, in which case they should be tied together near the DAC.

HI5760

NC — (11-14, 25)	(15) SLEEP
	(16) REFLO
D9 — D9 (MSB) (1)	(17) REFIO
D8 — D8 (2)	
D7 — D7 (3)	0.1µF
D6 — D6 (4)	
D5 — D5 (5)	(18) FSADJ
D4 — D4 (6)	R_{SET} 2kΩ
D3 — D3 (7)	(22) IOUTA — D/A OUT
D2 — D2 (8)	50Ω
D1 — D1 (9)	50Ω
D0 — D0 (LSB) (10)	(21) IOUTB — $\overline{D/A\ OUT}$
CLK (28)	(23) COMP2 (OR)
50Ω	(19) COMP1 0.1µF
DCOM (26)	(20) ACOM
	0.1µF
DV_{DD} (27)	(24) AV_{DD}
0.1µF	FERRITE BEAD +5V or +3V (V_{DD})
	10µH 10µF
	0.1µF
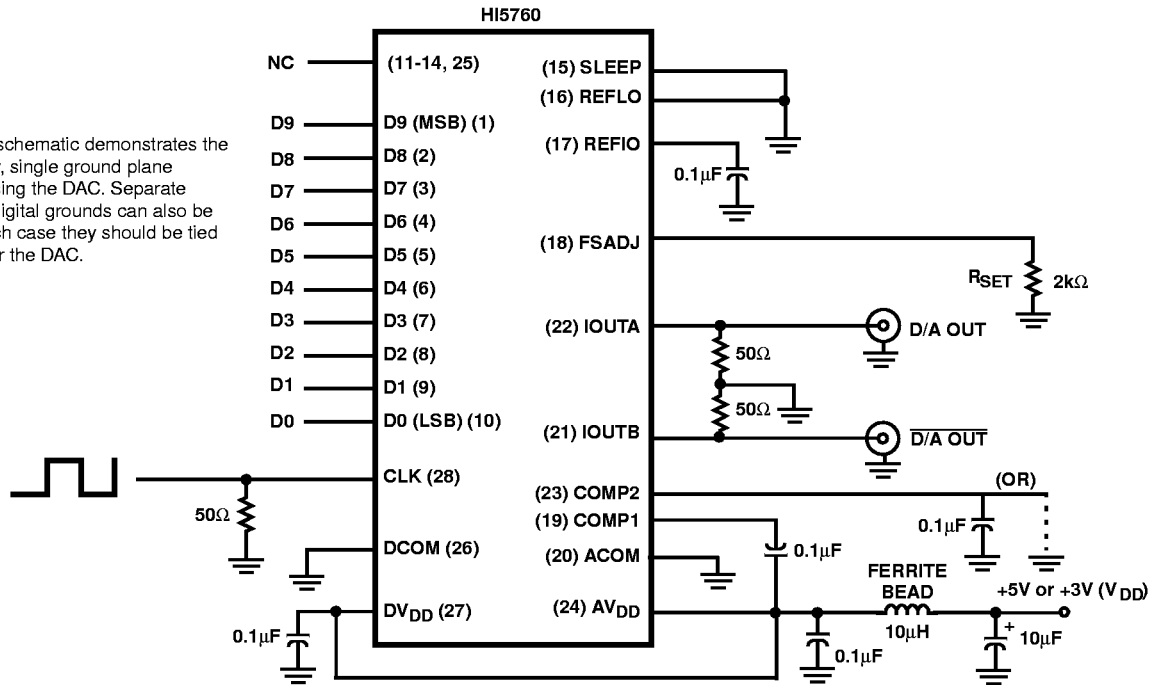
Functional Block Diagram

IOUTA   IOUTB

(LSB) D0				CASCODE CURRENT SOURCE
D1			SWITCH MATRIX	
D2				5 LSBs + 31 MSB SEGMENTS
D3	LATCH	LATCH		
D4		36	36	
D5				
D6				
D7	UPPER 5-BIT DECODER			
D8	31			
(MSB) D9				
CLK				COMP1
				COMP2

INT/EXT REFERENCE SELECT → INT/EXT VOLTAGE REFERENCE → BIAS GENERATION

AV_{DD} ACOM DV_{DD} DCOM   REFLO   REFIO   FSADJ SLEEP

2

HI5760

Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DCOM . . . . +5.5V
Analog Supply Voltage AV_{DD} to ACOM . . . . +5.5V
Grounds, ACOM TO DCOM . . . . -0.3V To + 0.3V
Digital Input Voltages (D9-D0, CLK, SLEEP) . . . . DV_{DD} + 0.3V
Internal Reference Output Current . . . . $\pm50\mu A$
Reference Input Voltage Range . . . . AV_{DD} + 0.3V
Analog Output Current (I_{OUT}) 24mA

Operating Conditions

Temperature Range . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA}(°C/W)
    SOIC Package   70
    SSOP Package   117
Maximum Junction Temperature
  HI5760 . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C
  (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications
$AV_{DD} = DV_{DD}$ = +5V, V_{REF} = Internal 1.2V, IOUTFS = 20mA, T_A = 25°C for All Typical Values

PARAMETER	TEST CONDITIONS	HI5760 T_A = -40°C TO 85°C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	"Best Fit" Straight Line (Note 7)	-1	±0.5	+1	LSB
Differential Linearity Error, DNL	(Note 7)	-0.5	±0.25	+0.5	LSB
Offset Error, I_{OS}	(Note 7)	-0.025		+0.025	% FSR
Offset Drift Coefficient	(Note 7)	-	0.1	-	ppm FSR/°C
Full Scale Gain Error, FSE	With External Reference (Notes 2, 7)	-10	±2	+10	% FSR
	With Internal Reference (Notes 2, 7)	-10	±1	+10	% FSR
Full Scale Gain Drift	With External Reference (Note 7)	-	±50	-	ppm FSR/°C
	With Internal Reference (Note 7)	-	±100	-	ppm FSR/°C
Full Scale Output Current, I_{FS}		2	-	20	mA
Output Voltage Compliance Range	(Note 3)	0	-	1.25	V
DYNAMIC CHARACTERISTICS					
Maximum Clock Rate, f_{CLK}	(Note 3)	-	125	-	MHz
Output Settling Time, (t_{SETT})	0.1% (±1 LSB, equivalent to 9 Bits) (Note 7)	-	20	-	ns
	0.05% (±1/2 LSB, equivalent to 10 Bits) (Note 7)	-	35	-	ns
Singlet Glitch Area (Peak Glitch)	R_L = 25Ω (Note 7)	-	35	-	pV•s
Output Rise Time	Full Scale Step	-	1.0	-	ns
Output Fall Time	Full Scale Step	-	1.5	-	ns
Output Capacitance			10		pF
Output Noise	IOUTFS = 20mA	-	50	-	pA/√Hz
	IOUTFS = 2mA	-	30	-	pA/√Hz

Electrical Specifications $AV_{DD} = DV_{DD} = +5V$, V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values

PARAMETER	TEST CONDITIONS	HI5760 $T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
AC CHARACTERISTICS - HI5760BIB, HI5760IA - 125MHz					
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 125 MSPS, f_{OUT} = 32.9MHz, 10MHz Span (Notes 4, 7)	-	75	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 5.04MHz, 4MHz Span (Notes 4, 7)	-	76	-	dBc
	f_{CLK} = 60 MSPS, f_{OUT} = 10.1MHz, 10MHz Span (Notes 4, 7)	-	75	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 5.02MHz, 2MHz Span (Notes 4, 7)	-	76	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 1.00MHz, 2MHz Span (Notes 4, 7)	-	78	-	dBc
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 100 MSPS, f_{OUT} = 2.00MHz (Notes 4, 7)	-	71	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 2.00MHz (Notes 4, 7)	-	71	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 1.00MHz (Notes 4, 7)	-	76	-	dBc
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 125 MSPS, f_{OUT} = 32.9MHz, 62.5MHz Span (Notes 4, 7)	-	54	-	dBc
	f_{CLK} = 125 MSPS, f_{OUT} = 10.1MHz, 62.5MHz Span (Notes 4, 7)	-	64	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 40.4MHz, 50MHz Span (Notes 4, 7)	-	52	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 20.2MHz, 50MHz Span (Notes 4, 7)	-	60	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 5.04MHz, 50MHz Span (Notes 4, 7)	-	68	-	dBc
	f_{CLK} = 100 MSPS, f_{OUT} = 2.51MHz, 50MHz Span (Notes 4, 7)	-	74	-	dBc
	f_{CLK} = 60 MSPS, f_{OUT} = 10.1MHz, 30MHz Span (Notes 4, 7)	-	63	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 20.2MHz, 25MHz Span (Notes 4, 7)	-	55	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 5.02MHz, 25MHz Span (Notes 4, 7)	-	68	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 2.51MHz, 25MHz Span (Notes 4, 7)	-	73	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 1.00MHz, 25MHz Span (Notes 4, 7)	-	73	-	dBc
AC CHARACTERISTICS - HI5760/6IB, HI5760/6IA - 60MHz					
Spurious Free Dynamic Range, SFDR Within a Window	f_{CLK} = 60 MSPS, f_{OUT} = 10.1MHz, 10MHz Span (Notes 4, 7)	-	75	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 5.02MHz, 2MHz Span (Notes 4, 7)	-	76	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 1.00MHz, 2MHz Span (Notes 4, 7)	-	78	-	dBc
Total Harmonic Distortion (THD) to Nyquist	f_{CLK} = 50 MSPS, f_{OUT} = 2.00MHz (Notes 4, 7)	-	71	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 1.00MHz (Notes 4, 7)	-	76	-	dBc
Spurious Free Dynamic Range, SFDR to Nyquist	f_{CLK} = 60 MSPS, f_{OUT} = 20.2MHz, 30MHz Span (Notes 4, 7)	-	56	-	dBc
	f_{CLK} = 60 MSPS, f_{OUT} = 10.1MHz, 30MHz Span (Notes 4, 7)	-	63	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 20.2MHz, 25MHz Span (Notes 4, 7)	-	55	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 5.02MHz, 25MHz Span (Notes 4, 7)	-	68	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 2.51MHz, 25MHz Span (Notes 4, 7)	-	73	-	dBc
	f_{CLK} = 50 MSPS, f_{OUT} = 1.00MHz, 25MHz Span (Notes 4, 7)	-	73	-	dBc
	f_{CLK} = 25 MSPS, f_{OUT} = 5.02MHz, 25MHz Span (Notes 4, 7)	-	71	-	dBc
VOLTAGE REFERENCE					
Internal Reference Voltage, V_{REF}		-	1.2	-	V
Internal Reference Voltage Drift		-	±60	-	ppm/^oC
Internal Reference Output Current Sink/Source Capability		-	±50	-	µA

Electrical Specifications $AV_{DD} = DV_{DD} = +5V$, V_{REF} = Internal 1.2V, IOUTFS = 20mA, $T_A = 25^oC$ for All Typical Values

PARAMETER	TEST CONDITIONS	HI5760 $T_A = -40^oC$ TO 85^oC			UNITS
		MIN	TYP	MAX	
Reference Input Impedance		-	1	-	MΩ
Reference Input Multiplying Bandwidth	(Note 7)	-	1.4	-	MHz
DIGITAL INPUTS D9-D0, CLK					
Input Logic High Voltage with 5V Supply, V_{IH}	(Note 3)	3.5	5	-	V
Input Logic High Voltage with 3V Supply, V_{IH}	(Note 3)	2.1	3	-	V
Input Logic Low Voltage with 5V Supply, V_{IL}	(Note 3)	-	0	1.3	V
Input Logic Low Voltage with 3V Supply, V_{IL}	(Note 3)	-	0	0.9	V
Input Logic Current, I_{IH}		-10	-	+10	μA
Input Logic Current, I_{IL}		-10	-	+10	μA
Digital Input Capacitance, C_{IN}		-	5	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 3 (Note 3)	3	-	-	ns
Data Hold Time, t_{HLD}	See Figure 3 (Note 3)	3	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 3	-	1	-	ns
CLK Pulse Width, t_{PW1}, t_{PW2}	See Figure 3 (Note 3)	4	-	-	ns
POWER SUPPLY CHARACTERISITICS					
AV_{DD} Power Supply	(note 8)	2.7	5.0	5.5	V
DV_{DD} Power Supply	(note 8)	2.7	5.0	5.5	V
Analog Supply Current (I_{AVDD})	(5V or 3V, IOUTFS = 20mA)	-	23	30	mA
	(5V or 3V, IOUTFS = 2mA)	-	4	-	mA
Digital Supply Current (I_{DVDD})	(5V, IOUTFS = Don't Care) (Note 5)	-	3	5	mA
	(3V, IOUTFS = Don't Care) (Note 5)	-	1.5	-	mA
Supply Current (I_{AVDD}) Sleep Mode	(5V or 3V, IOUTFS = Don't Care)	-	1.6	3	mA
Power Dissipation	(5V, IOUTFS = 20mA) (Note 6)	-	165	-	mW
	(5V, IOUTFS = 2mA) (Note 6)	-	70	-	mW
	(3V, IOUTFS = 20mA) (Note 6)	-	85	-	mW
	(3V, IOUTFS = 2mA) (Note 6)	-	27	-	mW
Power Supply Rejection	Single Supply (Note 7)	-0.2	-	+0.2	% FSR/V

NOTES:

2. Gain Error measured as the error in the ratio between the full scale output current and the current through R_{SET} (typically 625μA). Ideally the ratio should be 31.969.
3. Parameter guaranteed by design or characterization and not production tested.
4. Spectral measurements made with differential coupled transformer.
5. Measured with the clock at 50 MSPS and the output frequency at 1MHz.
6. Measured with the clock at 100 MSPS and the output frequency at 40MHz.
7. See 'Definition of Specifications'.
8. It is recommended that the output current be reduced to 12mA or less to maintain optimum performance for operation below 3V. Also, the intended operating voltage is $AV_{DD} = DV_{DD}$.

Definition of Specifications

Integral Linearity Error, INL, is the measure of the worst case point that deviates from a best fit straight line of data values along the transfer curve.

Differential Linearity Error, DNL, is the measure of the step size output deviation from code to code. Ideally the step size should be 1 LSB. A DNL specification of 1 LSB or less guarantees monotonicity.

Output Settling Time, is the time required for the output voltage to settle to within a specified error band measured from the beginning of the output transition. In the case of the HI5760, the measurement was done by switching from code 0 to 256, or quarter scale. Termination impedance was 25Ω due to the parallel resistance of the output 50Ω and the oscilloscope's 50Ω input. This also aids the ability to resolve the specified error band without overdriving the oscilloscope.

Singlet Glitch Area, is the switching transient appearing on the output during a code transition. It is measured as the area under the overshoot portion of the curve and is expressed as a Volt-Time specification. This is tested under the same conditions as 'Output Settling Time.'

Full Scale Gain Error, is the error from an ideal ratio of 32 between the output current and the full scale adjust current (through R_{SET}).

Full Scale Gain Drift, is measured by setting the data inputs to all ones and measuring the output voltage through a known resistance as the temperature is varied from Tmin to Tmax. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either Tmin or Tmax. The units are ppm of FSR (full scale range) per degree C.

Total Harmonic Distortion, THD, is the ratio of the DAC output fundamental to the RMS sum of the first five harmonics.

Spurious Free Dynamic Range, SFDR, is the amplitude difference from the fundamental to the largest harmonically or non-harmonically related spur within the specified window.

Output Voltage Compliance Range, is the voltage limit imposed on the output. The output impedance load should be chosen such that the voltage developed does not violate the compliance range.

Offset Error, is measured by setting the data inputs to all zeros and measuring the output voltage through a known resistance. Offset error is defined as the maximum *deviation* of the output current from a value of 0mA.

Offset Drift, is measured by setting the data inputs to all zeros and measuring the output voltage through a known resistance as the temperature is varied from Tmin to Tmax. It is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either Tmin or Tmax. The units are ppm of FSR (full scale range) per degree C.

Power Supply Rejection, is measured using a single power supply. Its nominal +5V is varied ±10% and the change in the DAC full scale output is noted.

Reference Input Multiplying Bandwidth, is defined as the 3dB bandwidth of the voltage reference input. It is measured by using a sinusoidal waveform as the external reference with the digital inputs set to all 1s. The frequency is increased until the amplitude of the output waveform is 0.707 of its original value.

Internal Reference Voltage Drift, is defined as the maximum *deviation* from the *value* measured at room temperature to the *value* measured at either Tmin or Tmax. The units are ppm per degree C.

Detailed Description

The HI5760 is a 10-bit, current out, CMOS, digital to analog converter. Its maximum update rate is 125MSPS and can be powered by either single or dual power supplies in the recommended range of +3V to +5V. It consumes less than 165mW of power when using a +5V supply with the data switching at 100MSPS. The architecture is based on a segmented current source arrangement that reduces glitch by reducing the amount of current switching at any one time. The five MSBs are represented by 31 major current sources of equivalent current. The five LSBs are comprised of binary weighted current sources. Consider an input waveform to the converter which is ramped through all the codes from 0 to 1023. The five LSB current sources would begin to count up. When they reached the all high state (decimal value of 31) and needed to count to the next code, they would all turn off and the first major current source would turn on. To continue counting upward, the 5 LSBs would count up another 31 codes, and then the next major current source would turn on and the five LSBs would all turn off. The process of the single, equivalent, major current source turning on and the five LSBs turning off each time the converter reaches another 31 codes greatly reduces the glitch at any one switching point. In previous architectures that contained all binary weighted current sources or a binary weighted resistor ladder, the converter might have a substantially larger amount of current turning on and off at certain, worst-case transition points such as mid-scale and quarter scale transitions. By greatly reducing the amount of current switching at certain 'major' transitions, the overall glitch of the converter is dramatically reduced, improving settling times and transient problems.

Digital Inputs and Termination

The HI5760 digital inputs are guaranteed to CMOS levels. However, TTL compatibility can be achieved by lowering the supply voltage to 3V due to the digital threshold of the input buffer being approximately half of the supply voltage. The internal register is updated on the rising edge of the clock. To minimize reflections, proper termination should be implemented. If the lines driving the clock and the digital inputs are 50Ω lines, then 50Ω termination resistors should be placed as close to the converter inputs as possible to the digital ground plane (if separate grounds are used).

Ground Plane(s)

If separate digital and analog ground planes are used, then all of the digital functions of the device and their corresponding components should be over the digital ground plane and terminated to the digital ground plane. The same is true for the analog components and the analog ground plane. The converter will function properly with a single ground plane, as the Evaluation Board is configured in this matter. Refer to the AppNote on the HI5760 Evaluation Board for further discussion of the ground plane(s) upon availability.

Noise Reduction

To minimize power supply noise, 0.1μF capacitors should be placed as close as possible to the converter's power supply pins, AV_{DD} and DV_{DD}. Also, should the layout be designed

using separate digital and analog ground planes, these capacitors should be terminated to the digital ground for DV_{DD} and to the analog ground for AV_{DD}. Additional filtering of the power supplies on the board is recommended. See the AppNote on the HI5760 Evaluation Board for more information upon availability.

Voltage Reference

The internal voltage reference of the device has a nominal value of +1.2V with a $\pm$60 ppm/^{o}C drift coefficient over the full temperature range of the converter. It is recommended that a 0.1μF capacitor be placed as close as possible to the REFIO pin. The REFLO pin (16) selects the reference. The internal reference can be selected if pin 16 is tied low (ground) or if it is left disconnected due to an active pull-down circuit. If an external reference is desired, then pin 16 should be tied high (the supply voltage) and the external reference driven into REFIO, pin 17. The external reference should be +1.2V nominal, with amplitude attenuation to 150mV possible. The output current of the converter, IOUTA and IOUTB, is a function of the voltage reference used and the value of R_{SET}. I_{OUT} should be within the 2mA to 20mA range.

$$I_{OUT}(\text{Full Scale}) = V_{FSADJ}/R_{SET} \times (1023/32),$$

where V_{FSADJ} is defined as the voltage at pin 18.

Outputs

IOUTA and IOUTB are complementary current outputs. The sum of the two currents is always equal to the full scale output current minus one LSB. These outputs can be used in a differential-to-single-ended arrangement to achieve better harmonic rejection. The SFDR measurements in this datasheet were performed with a 1:1 transformer on the output of the DAC. If single ended use is desired, a load resistor can be used to convert the output current to a voltage. It is recommended that the unused output be either grounded or equally terminated. The voltage developed at the output must not violate the output voltage compliance range of 0V to 1.25V. R_{LOAD} should be chosen so that the desired output voltage is produced in conjunction with the output full scale current, which is described above in the 'Reference' section. If a known line impedance is to be driven, then the output load resistor should be chosen to match this impedance. The output voltage equation is:

$$V_{OUT} = I_{OUT} \times R_{LOAD}$$

If the full scale output current is set to 20mA by using the internal voltage reference and a 1.91kΩ R_{SET} resistor, then the input coding to output current will resemble the following:

TABLE 1. INPUT CODING VS. OUTPUT CURRENT

INPUT CODE (D9-D0)	IOUTA (mA)	IOUTB (mA)
11111 11111	20	0
10000 00000	10	10
00000 00000	0	20

Timing Diagrams
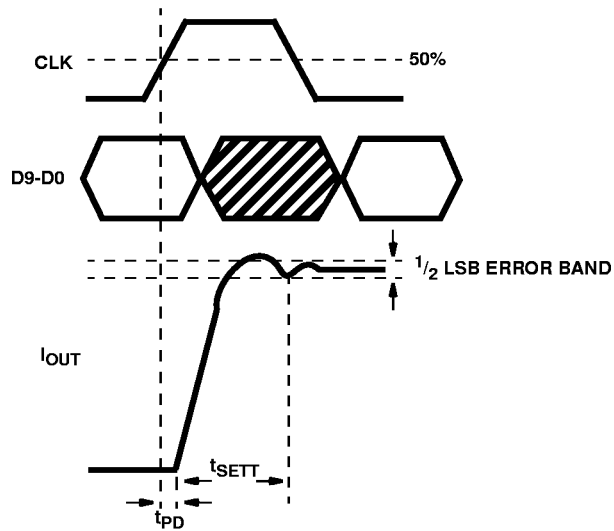

FIGURE 1. OUTPUT SETTLING TIME DIAGRAM
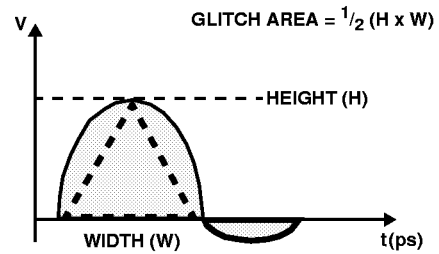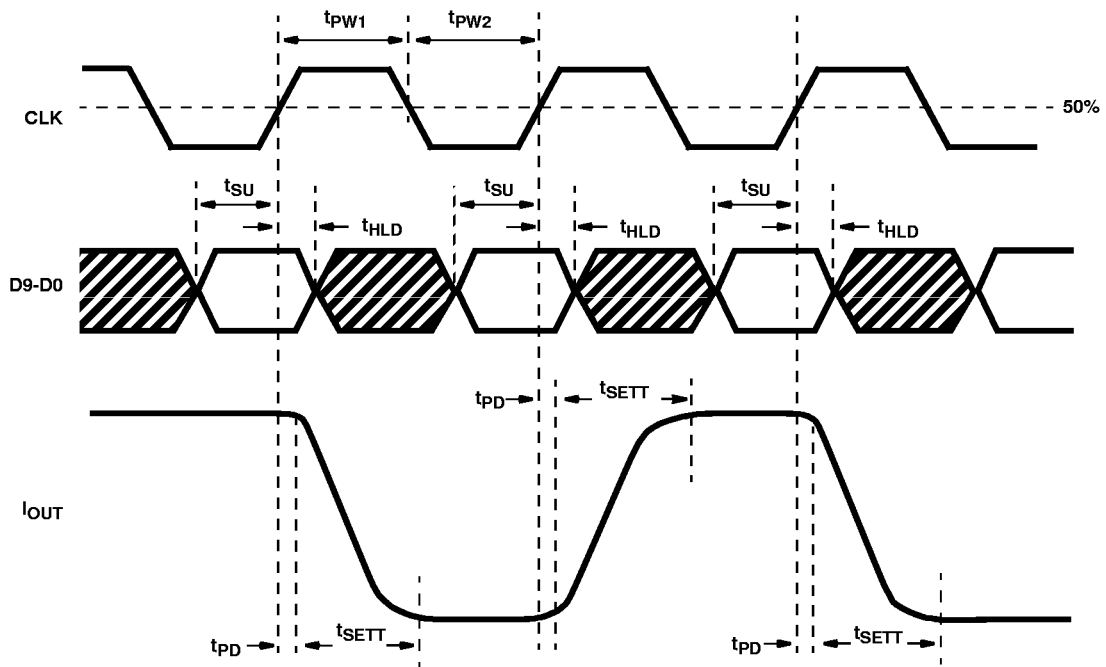

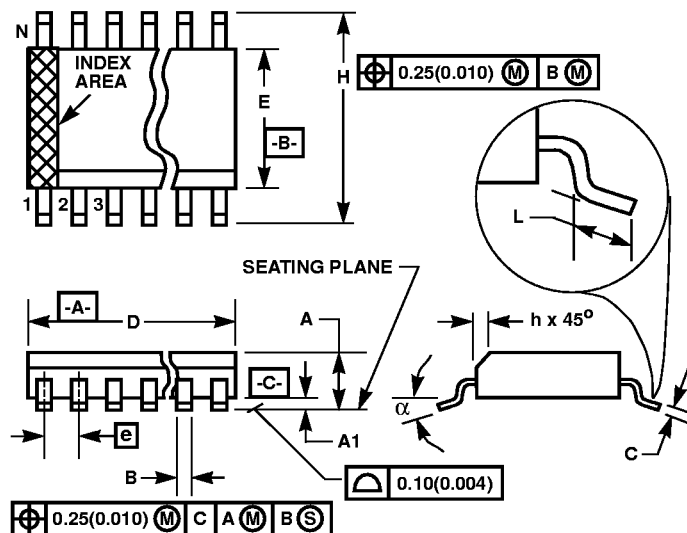FIGURE 2. PEAK GLITCH AREA (SINGLET) MEASUREMENT METHOD

GLITCH AREA = $^1/_2$ (H x W)

FIGURE 3. PROPAGATION DELAY, SETUP TIME, HOLD TIME AND MINIMUM PULSE WIDTH DIAGRAM

Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-10	D9 (MSB) Through D0 (LSB)	Digital Data Bit 9, (Most Significant Bit) through Digital Data Bit 0, (Least Significant Bit).
11-14	NC	No Connect. Recommend ground.
15	SLEEP	Control Pin for Power-Down mode. Sleep Mode is active high; Connect to ground for Normal Mode. Sleep pin has internal 20μA active pull-down current.
16	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV_{DD} to disable internal reference.
17	REFIO	Reference voltage input if internal reference is disabled. Reference voltage output if internal reference is enabled. Use 0.1μF cap to ground when internal reference is enabled.
18	FSADJ	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full Scale Output Current = 32 x V_{FSADJ}/R_{SET}.
19	COMP1	For use in reducing bandwidth/noise. Recommended: connect 0.1μF to AV_{DD}.
20	ACOM	Analog Ground.
21	IOUTB	The complimentary current output of the device. Full scale output current is acheived when all input bits are set to binary 0.
22	IOUTA	Current output of the device. Full scale output current is acheived when all input bits are set to binary 1.
23	COMP2	Connect to ACOM directly or through a 0.1μF capacitor.
24	AV_{DD}	Analog Supply (+3V to +5V).
25	NC	No Connect.
26	DCOM	Digital Ground.
27	DV_{DD}	Digital Supply (+3V to +5V).
28	CLK	Input for clock. Positive edge of clock latches data.

Small Outline Plastic Packages (SOIC)

M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

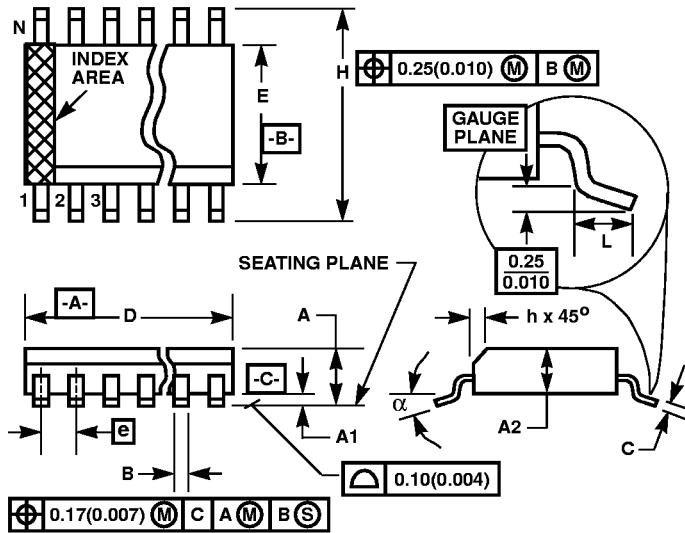| SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline Plastic Packages (SSOP)

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.

10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

M28.15
28 LEAD SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
A2	-	0.061	-	1.54	-
B	0.008	0.012	0.20	0.30	9
C	0.007	0.010	0.18	0.25	-
D	0.386	0.394	9.81	10.00	3
E	0.150	0.157	3.81	3.98	4
e	0.025 BSC		0.635 BSC		-
H	0.228	0.244	5.80	6.19	-
h	0.0099	0.0196	0.26	0.49	5
L	0.016	0.050	0.41	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 2/95