



High Density FLASH Memory Card 16, 32, 48, 64, 80 MEGABYTE

General Description

WEDC’s Flash memory cards - FLF Series - offer high density linear Flash memory for code and data storage, high performance disk emulation, mobile PC and embedded applications.

The WEDC FLF series is based on Intel’s Multi Level Cell (MLC) Flash memory technology, providing high density Flash components at significantly lower cost per megabyte. MLC technology allows for two bits of information to be stored in a single cell. This leads to reduced die size and reduced cost per megabyte.

WEDC’s FLF series cards are built with Intel’s 64Mb components, 28F640J5, with manufacturer/device ID of 89/15_H. The FLF series is available in standard densities of 16, 32, 48 and 64MB.

Additionally, WEDC’s FLF series provides densities beyond the 64MB density, supported by PCMCIA standard. These higher densities are based on a “paging scheme”. By writing a page address to the Configuration Option Register (address 4000H), an additional page of memory could be access. The current FLF series supports densities to 80MB: total of 2 pages: page 0 := 64MB, page 1 := 16MB.

To provide a 16 bit word wide access and to support PCMCIA standard, devices are paired on the card. Therefore, the Flash array is structured in 128K word (256kB) blocks. Write, read and block erase operations can be performed as either a word or byte wide operation.

The FLF series cards conform with the PC Card 95 Standard supported by PCMCIA and JEIDA, providing electrical and physical compatibility. The PC Card form factor offers an industry standard pinout and mechanical outline, allowing density upgrades without system design changes.

WEDC’s standard cards are shipped with WEDC’s Flash Logo. Cards are also available with blank housings (no Logo). The blank housings are available in both, a recessed (for label) or flat housing. Please contact WEDC sales representative for further information on Custom artwork.

Features

- Low cost, high density Linear Flash Card
- Single 5V Supply
 - (3V/5V operation is available as option)
- Based on Intel 28F640J5 (MLC) Components
- Fast Read Performance
 - 250ns Maximum Access Time
 - (200ns optional)
- PCMCIA compatible
 - x8/ x16 Data Interface
- 32-Byte Write Buffer
 - 6µs per Byte Effective Write Time
- Cross-Compatible Command Support
 - Intel Basic Command Set
 - Common Flash Interface (CFI)
 - Scaleable Command Set
- Power-Down Mode
 - Reset, Power Down Registers
- 10,000 Erase Cycles per Block
- 128K word symmetrical Block Architecture
- PC Card Standard Type II Form Factor

Ordering Information

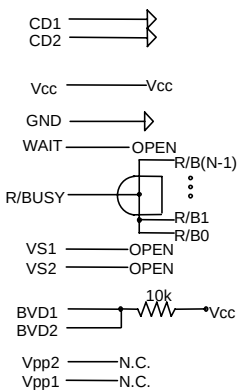
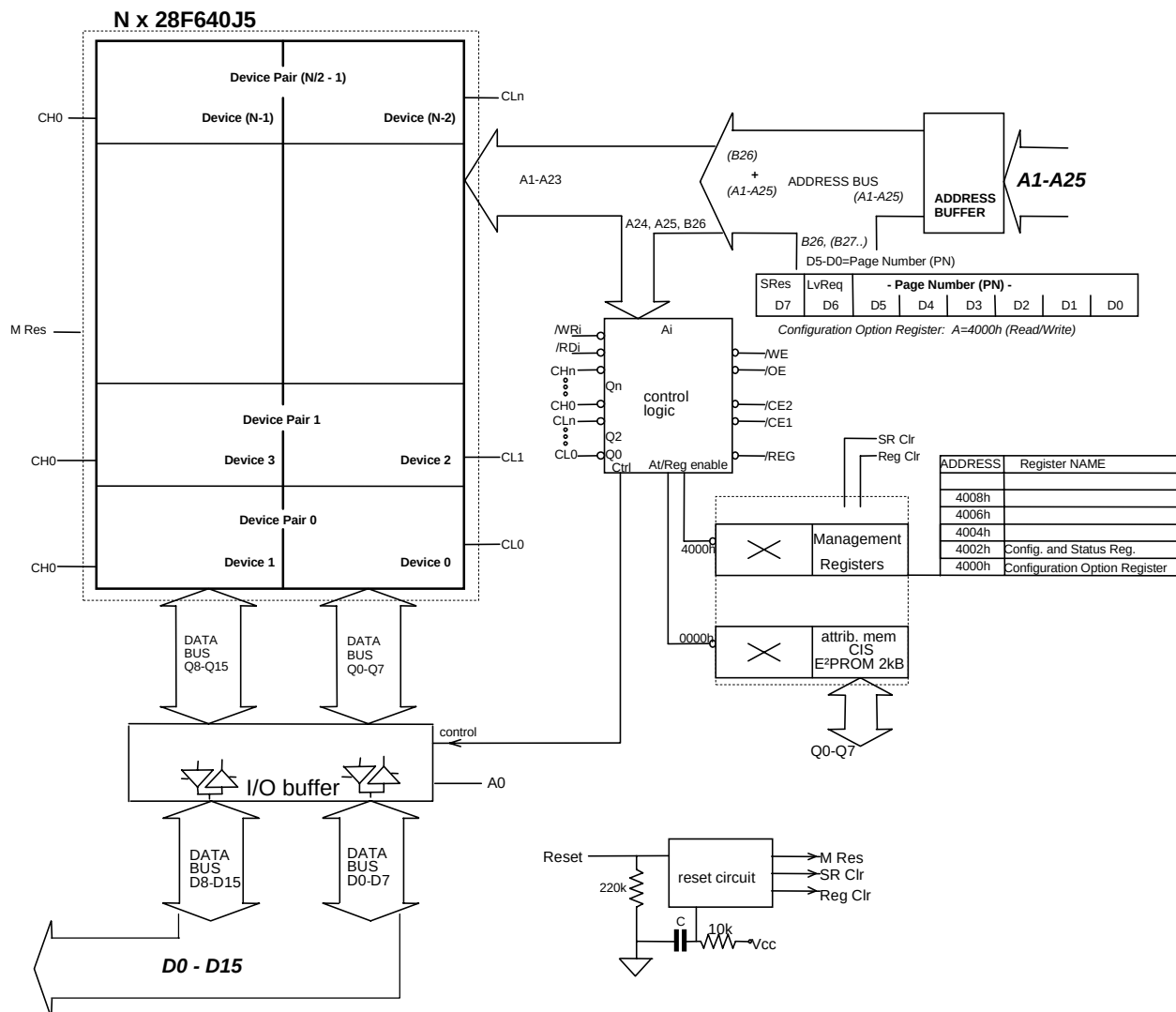
EDI 7P XXX FLF YY SS T ZZ

where

XXX:	016	16MB
	032	32MB
	048	48MB
	064	64MB
	080	80MB
YY:	02	based on 28F640J5 With Attribute Memory
SS:	03	WEDC Logo
	04	Blank Housing Type 2
	05	Blank Housing T 2 (Recessed)
T:	C	Commercial
ZZ:	20	200ns
	25	250ns



Block Diagram



/CE1, /CE2, /OE, /WE, /Reg: pull up typ 100k
 A0, A25, Reset: pull down typ 100k
 R/Busy - Open Drain output (require pull up on host)

Configuration Option Register: ADRS=4000h

Read/Write							
SRes	LvReq	- Page Number (PN) -					
D7	D6	D5	D4	D3	D2	D1	D0

- D7 Soft Reset, active High
 1=Reset State
 0=End Reset State
- D6 LevelReq (not supported)
- D5-D0 Configuration index
 D5-D1 reserved
 D0 Page Number Config. (PN) Power On default =0

Configuration Status Register: ADRS=4002h

Read/Write							
D7	reserved	D5	D4	D3	PwrDwn	reserved	D0
D2	D6	D5	D4	D3	D2	D1	D0

- D2 Power Down; active High
 1 = Place all memory devices in power down mode
 0 = normal operation Power On default=0

Manufacturer ID	Intel	89 _H
Device ID	28F640J5	15 _H

FLF Flash Card based on Strata Flash 28F640J5

Pinout

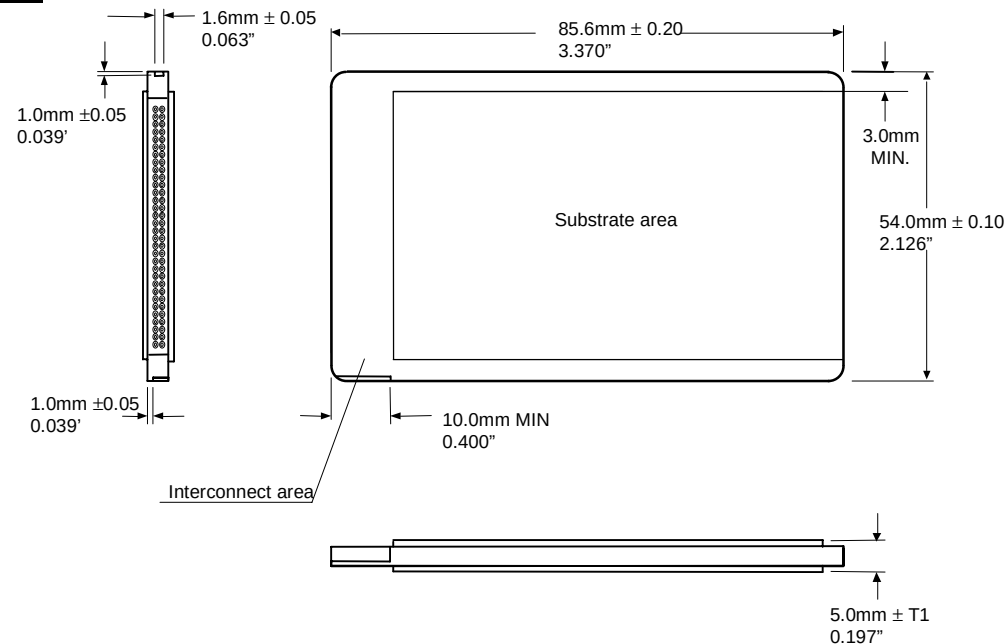
Pin	Signal name	I/ O	Function	Active
1	GND		Ground	
2	DQ3	I/O	Data bit 3	
3	DQ4	I/O	Data bit 4	
4	DQ5	I/O	Data bit 5	
5	DQ6	I/O	Data bit 6	
6	DQ7	I/O	Data bit 7	
7	CE1#	I	Card enable 1	LOW
8	A10	I	Address bit 10	
9	OE#	I	Output enable	LOW
10	A11	I	Address bit 11	
11	A9	I	Address bit 9	
12	A8	I	Address bit 8	
13	A13	I	Address bit 13	
14	A14	I	Address bit 14	
15	WE#	I	Write Enable	LOW
16	RDY/BSY#	O	Ready/Busy	LOW(1)
17	Vcc		Supply Voltage	
18	Vpp1		Prog. Voltage	N.C.
19	A16	I	Address bit 16	
20	A15	I	Address bit 15	
21	A12	I	Address bit 12	
22	A7	I	Address bit 7	
23	A6	I	Address bit 6	
24	A5	I	Address bit 5	
25	A4	I	Address bit 4	
26	A3	I	Address bit 3	
27	A2	I	Address bit 2	
28	A1	I	Address bit 1	
29	A0	I	Address bit 0	
30	DQ0	I/O	Data bit 0	
31	DQ1	I/O	Data bit 1	
32	DQ2	I/O	Data bit 2	
33	WP	O	Write Potect	HIGH
34	GND		Ground	

Pin	Signal name	I/ O	Function	Active
35	GND		Ground	
36	CD1#	O	Card Detect 1	LOW
37	DQ11	I/O	Data bit 11	
38	DQ12	I/O	Data bit 12	
39	DQ13	I/O	Data bit 13	
40	DQ14	I/O	Data bit 14	
41	DQ15	I	Data bit 15	
42	CE2#	I	Card Enable 2	LOW
43	VS1	O	Voltage Sense 1	NC (2)
44	RFU		Reserved	
45	RFU		Reserved	
46	A17	I	Address bit 17	
47	A18	I	Address bit 18	
48	A19	I	Address bit 19	
49	A20	I	Address bit 20	
50	A21	I	Address bit 21	
51	Vcc		Supply Voltage	
52	Vpp2		Prog. Voltage	N.C.
53	A22	I	Address bit 22	
54	A23	I	Address bit 23	
55	A24	I	Address bit 24	
56	A25	I	Address bit 25	
57	VS2	O	Voltage Sense 2	N.C.
58	RST	I	Card Reset	HIGH
59	Wait#	O	Extended Bus cycle	LOW(3)
60	RFU		Reserved	
61	REG#	I	Attrib Mem Select	
62	BVD2	O	Bat. Volt. Detect 2	(3)
63	BVD1	O	Bat. Volt. Detect 1	(3)
64	DQ8	I/O	Data bit 8	
65	DQ9	I/O	Data bit 9	
66	DQ10	O	Data bit 10	
67	CD2#	O	Card Detect 2	LOW
68	GND		Ground	

Notes:

- 1. RDY/BSY signal is an open drain type output, pull-up resistors are required on the host side.
- 2. VS1 is connected to GND for 3.3V/5V cards and N.C. for 5V only cards.
- 3. Wait#, BVD1 and BVD2 are internally connected to Vcc by resistors for compatibility.

Mechanical





Card Signal Description

Symbol	Type	Name and Function
A0 - A25	INPUT	ADDRESS INPUTS: A0 through A25 enable direct addressing of up to 64MB of memory on the card. Signal A0 is not used in word access mode. A25 is the most significant bit
DQ0 - DQ15	INPUT/OUTPUT	DATA INPUT/OUTPUT: DQ0 THROUGH DQ15 constitute the bi-directional databus. DQ15 is the MSB.
CE1#, CE2#	INPUT	CARD ENABLE 1 AND 2: CE1# enables even byte accesses, CE2# enables odd byte accesses. Multiplexing A0, CE1# and CE2# allows 8-bit hosts to access all data on DQ0 - DQ7 (see truth table).
OE#	INPUT	OUTPUT ENABLE: Active low signal gating read data from the memory card.
WE#	INPUT	WRITE ENABLE: Active low signal gating write data to the memory card.
RDY/BSY#	OUTPUT	READY/BUSY OUTPUT: Indicates status of internally timed erase or program algorithms. A high output indicates that the card is ready to accept accesses. A low output indicates that one or more devices in the memory card are busy with internally timed erase or write activities.
CD1#, CD2#	OUTPUT	CARD DETECT 1 and 2: Provide card insertion detection. These signals are internally connected to ground on the card. The host shall monitor these signals to detect card insertion. Pulled up on host side.
WP	OUTPUT	WRITE PROTECT: Write protect reflects the status of the Write Protect switch on the memory card. WP set to high = write protected, providing internal hardware write lockout to the Flash array. If card does not include optional write protect switch, this signal will be pulled low internally indicating write protect = "off".
VPP1, VPP2	N.C.	PROGRAMMING VOLTAGES: Not connected for 5V only card.
VCC		CARD POWER SUPPLY: 5.0V for all internal circuitry.
GND		CARD GROUND
REG#	INPUT	ATTRIBUTE MEMORY SELECT: Active low signal, enables access to attribute memory space, occupied by the Card Information Structure (CIS) and Card Registers.
RST	INPUT	RESET: Active high signal for placing card in Power-on default state. Reset can be used as a Power-Down control for the memory array.
WAIT#	OUTPUT	WAIT: This signal is pulled high internally for compatibility. No wait states are generated.
BVD1, BVD2	OUTPUT	BATTERY VOLTAGE DETECT: These signals are pulled high to maintain SRAM card compatibility.
VS1, VS2	OUTPUT	VOLTAGE SENSE: Notifies the host socket of the card's VCC requirements. VS1 and VS2 are open to indicate a 5V card.
RFU		RESERVED FOR FUTURE USE
N.C.		NO INTERNAL CONNECTION TO CARD: pin may be driven or left floating.

Functional Truth Table

READ function

Function Mode	/CE2	/CE1	A0	/OE	/WE
Standby Mode	H	H	X	X	X
Byte Access (8 bits)	H	L	L	L	H
	H	L	H	L	H
Word Access (16 bits)	L	L	X	L	H
Odd-Byte Only Access	L	H	X	L	H

Common Memory

	/REG	D15-D8	D7-D0
Standby Mode	X	High-Z	High-Z
Byte Access (8 bits)	H	High-Z	Even-Byte
	H	High-Z	Odd-Byte
Word Access (16 bits)	H	Odd-Byte	Even-Byte
Odd-Byte Only Access	H	Odd-Byte	High-Z

Attribute Memory

	/REG	D15-D8	D7-D0
Standby Mode	X	High-Z	High-Z
Byte Access (8 bits)	L	High-Z	Even-Byte
	L	High-Z	Not Valid
Word Access (16 bits)	L	Not Valid	Even-Byte
Odd-Byte Only Access	L	Not Valid	High-Z

WRITE function

Standby Mode	H	H	X	X	X
Byte Access (8 bits)	H	L	L	H	L
	H	L	H	H	L
Word Access (16 bits)	L	L	X	H	L
Odd-Byte Only Access	L	H	X	H	L

Standby Mode	X	X	X
Byte Access (8 bits)	H	X	Even-Byte
	H	X	Odd-Byte
Word Access (16 bits)	H	Odd-Byte	Even-Byte
Odd-Byte Only Access	H	Odd-Byte	X

Standby Mode	X	X	X
Byte Access (8 bits)	L	X	Even-Byte
	L	X	X
Word Access (16 bits)	L	X	Even-Byte
Odd-Byte Only Access	L	X	X



Card Interface

The FLF series flash card complies with PC Card standard (PCMCIA, March 1997). While maintaining PCMCIA compatibility, the FLF series card has integrated special features to extend functionality.

Card has built in 2 control registers:

- Configuration Option Register (COR) Address = 4000_h
- Configuration and Status Register (CSR) Address = 4002_h

COR register: provide a soft reset function (bit D7) and additional page register (bit D0) to extend card capacity beyond 64MB.

SReset

As defined by PCMCIA, setting the SReset bit to 1, places the card in the reset state. During this state all memory devices are place in power down mode, minimizing power consumption. Returning this bit to 0 leaves the reset cycle and place the card in the same condition as following a power up or hardware reset. This bit must be cleared to 0, to access any device on the card.

Complete soft reset cycle must consist of a 2 step write sequence to the SReset bit:

1. Initialization: write 1 to SReset

- reset cycle begin
- memory devices enters Power-Down mode aborting all operations and clearing all

registers.

2. Write 0 to SReset

- Reset cycle ends
- memory devices and registers enters power on default state

Card can be place in Power Down mode by activating Reset signal (pin58) or by controlling the bit D2 in CSR register.

LevlRequest

Not supported

Configuration Index

Configuration Index bits (D0 - D5) are defined to provide address extension bits -page address, to extend card capacity beyond 64MB.

Only bit D0 is supported:

- D0 set to 0 selects **page 0**
- D0 set to 1 selects: **page 1**

D0 is set to the value of 0, during power on or any reset.

CSR register: provide a power control of memory array. Only bit D2 is supported; all other bits are “don’t care”

PwrDwn

Writing 1 to PwrDwn bit (D2) forces each memory device on the card into a reset/power down mode by asserting all the devices RP# pins. Writing 0 to the bit returns the array to stand by mode.

Card Information Structure (CIS) contains information about Registers addressing and Memory structure.

Cards with memory capacity < 64MB do not support Configuration Index bits.

Notes:

1. Reading from undefined address location or unsupported bits will return random data.
2. Writing to undefined address location may result in card malfunctioning due to limited address decoding.
3. See block diagram for more details about control registers.



Absolute Maximum Ratings ⁽²⁾

Operating Temperature TA (ambient)	0°C to +60 °C
Commercial	-10°C to +70 °C
Storage Temperature	-0.5V to VCC+0.5V
Voltage on any pin relative to VSS	-0.5V to +7.0V
VCC supply Voltage relative to VSS	

Note:

Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Characteristics ⁽¹⁾

Symbol	Parameter	Density (Mbytes)	Notes	Typ ⁽³⁾	Max	Units	Test Conditions
ICCR	VCC Read Current	16,32,48,64,80		70	110	mA	VCC = VCCmax tcycle = 200ns
ICCW	VCC Program Current	16,32,48,64,80		70	120	mA	2 memory devices
ICCE	VCC Erase Current	16,32,48,64,80		70	140	mA	2 memory devices
ICCD	VCC Power-down Current	16	2	160	250	μA	VCC = VCCmax Control Signals = VCC Reset = VCC (active)
		32		320	500		
		48		480	750		
		64		650	1000		
		80		800	1250		
ICCS (CMOS)	VCC Standby Current	16	2	0.2	0.4	mA	VCC = VCCmax Control Signals = VCC Reset = 0V (not active)
		32		0.4	0.7		
		48		0.6	1.0		
		64		0.8	1.3		
		80		1.0	1.6		

CMOS Test Conditions: VCC = 5V ± 5%, VIL = VSS ± 0.2V, VIH = VCC ± 0.2V

Notes:

1. All currents are RMS values unless otherwise specified. ICCR, ICCW and ICCE are based on Word wide operations (2 memory devices activated).
2. Control Signals: CE₁#, CE₂#, OE#, WE#.
3. Typical: VCC = 5V, T = +25°C.

Symbol	Parameter	Notes	Min	Max	Units	Test Conditions
ILI	Input Leakage Current	1, 2		±20	μA	VCC = VCCMAX Vin = VCC or GND
ILO	Output Leakage Current	1		±20	μA	VCC = VCCMAX Vin = VCC or GND
VIL	Input Low Voltage	1	0	0.8	V	
VIH	Input High Voltage	1	0.7xVCC	VCC+0.5	V	
VOL	Output Low Voltage	1		0.4	V	IOL = 3.2mA
VOH	Output High Voltage	1	VCC-0.4	VCC	V	IOH = -2.0mA
VLKO	VCC Erase/Program Lock Voltage	1	3.25		V	

Notes:

1. Values are the same for byte and word wide modes for all card densities.
2. Exception: Leakage current on control signals with internal pull up resistors (see block diag) will be < 500μA when VIN=GND.



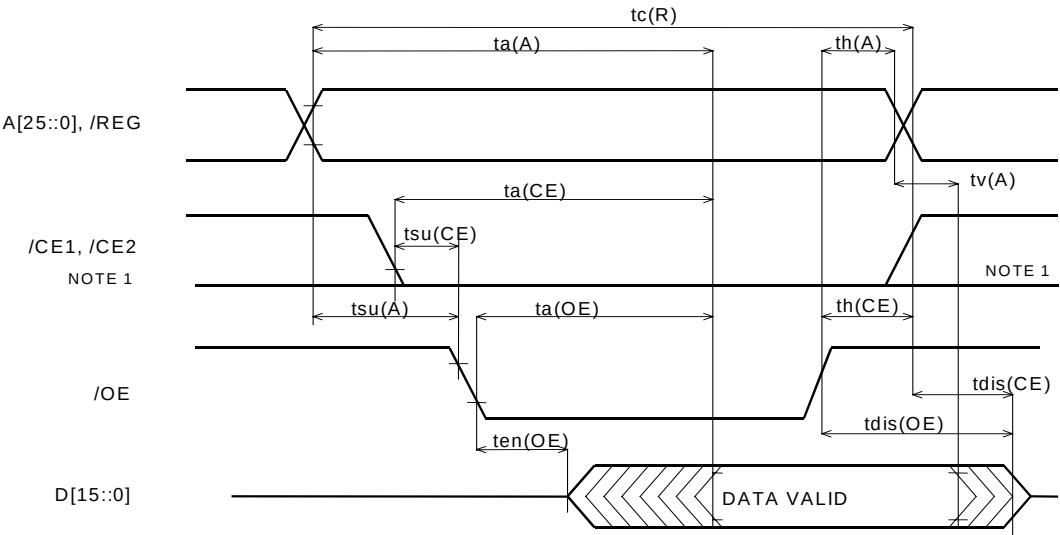
AC Characteristics

Read Timing Parameters

		200ns		250ns		
SYMBOL (PCMCIA)	Parameter	Min	Max	Min	Max	Unit
t _c (R)	Read Cycle Time	200		250		ns
t _a (A)	Address Access Time		200		250	ns
t _a (CE)	Card Enable Access Time		200		250	ns
t _a (OE)	Output Enable Access Time		90		100	ns
t _{su} (A)	Address Setup Time		20		30	ns
t _{su} (CE)	Card Enable Setup Time		0		0	ns
t _h (A)	Address Hold Time		20		20	ns
t _h (CE)	Card Enable Hold Time		20		20	ns
t _v (A)	Output Hold from Address Change		0		0	ns
t _{dis} (CE)	Output Disable Time from CE#		90		100	ns
t _{dis} (OE)	Output Disable Time from OE#		90		100	ns
t _{en} (CE)	Output Enable Time from CE#	5		5		ns
t _{en} (OE)	Output Enable Time from OE#	5		5		ns
t _{rec} (RST)	Power Down recovery to Output Delay. VCC = 5V		500		500	ns

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Read Timing Diagram



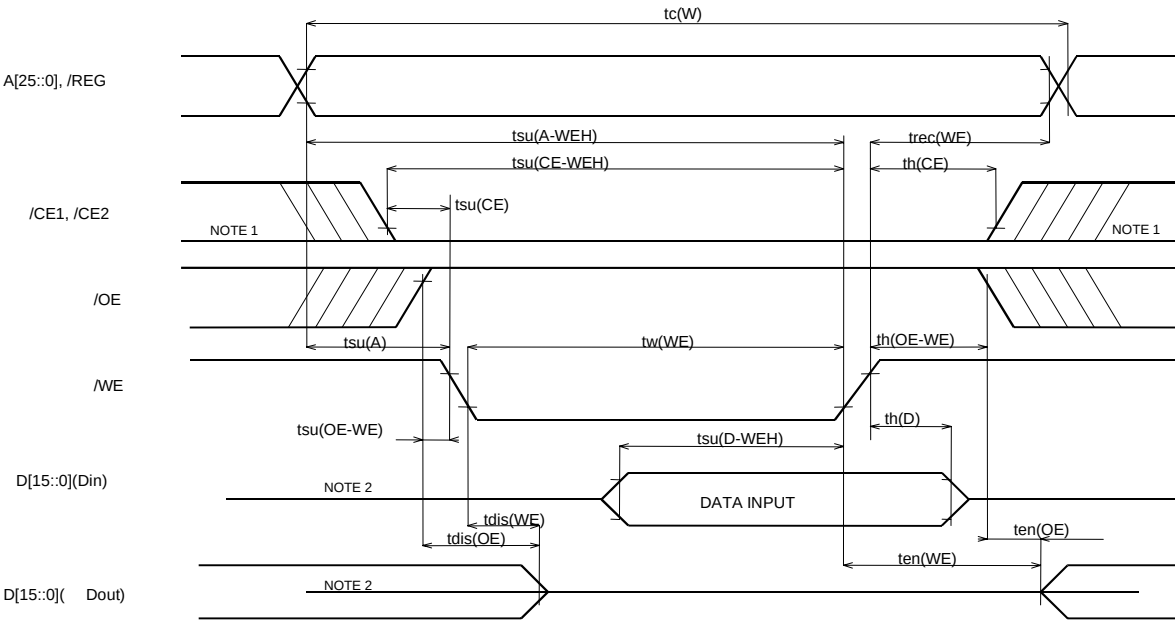


Write Timing Parameters

SYMBOL (PCMCIA)	Parameter	200ns		250ns		Unit
		Min	Max	Min	Max	
t _{CW}	Write Cycle Time	200		250		ns
t _w (WE)	Write Pulse Width	120		150		ns
t _{su} (A)	Address Setup Time	20		30		ns
t _{su} (A-WEH)	Address Setup Time for WE#	140		180		ns
t _{su} (CE-WEH)	Card Enable Setup Time for WE#	140		180		ns
t _{su} (D-WEH)	Data Setup Time for WE#	60		80		ns
t _h (D)	Data Hold Time	30		30		ns
t _{rec} (WE)	Write Recover Time/Address hold	30		30		ns
t _{dis} (WE)	Output Disable Time from WE#		90		100	ns
t _{dis} (OE)	Output Disable Time from OE#		90		100	ns
t _{en} (WE)	Output Enable Time from WE#	5		5		ns
t _{en} (OE)	Output Enable Time from OE#	5		5		ns
t _{su} (OE-WE)	Output Enable Setup from WE#	10		10		ns
t _h (OE-WE)	Output Enable Hold from WE#	50		50		ns
t _{su} (CE)	Card Enable Setup Time from OE#	0		0		ns
t _h (CE)	Card Enable Hold Time	20		20		ns
t _{rec} (WEL)	Reset recovery to WE going low	1		1		μS

Note: AC timing diagrams and characteristics are guaranteed to meet or exceed PCMCIA 2.1 specifications.

Write Timing Diagram



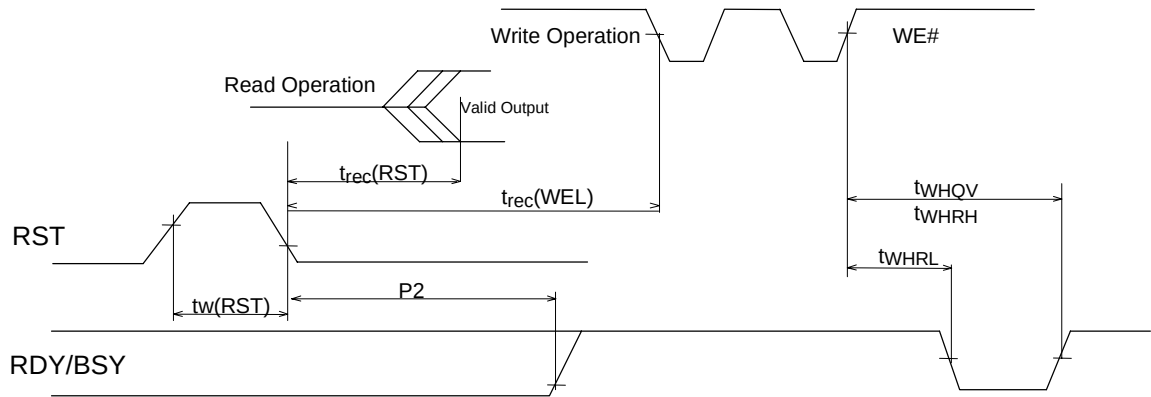
Data Write and Erase Performance ^(1,3)

VCC = 5V ± 5%, T_A = 0C to + 70C

SYM	Parameter	Notes	Min	Typ ⁽¹⁾	Max	Units	Test Conditions
t _{WHQV1}	Word/Byte Program time	2,4		6		µs	Effective time per Byte (using Write Buffer)
t _{WHQV3}	Byte Program Time (using Byte program command)			120		µs	
	Block Program Time (using write to buffer command)	2		0.8		sec	Word Program Mode
t _{WHQV4}	Block Erase Time	2		1.0		sec	
t _{WHRH}	Erase Suspend Latency Time to Read			25	35	µs	

- Notes:**
- 1. Typical: Nominal voltages and T_A = 25C.
 - 2. Excludes system overhead.
 - 3. Valid for all speed options.
 - 4. To maximize system performance RDY/BSY# signal should be polled.

Waveforms for Reset Operation

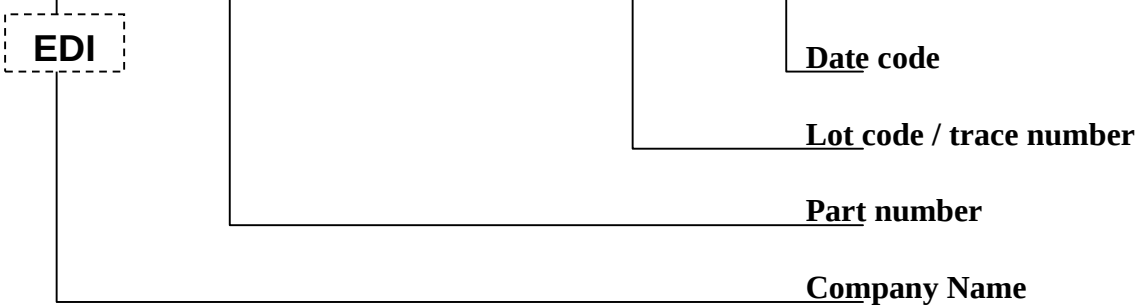


SYMBOL	Parameter	Min	Max	Unit
t _{w(RST)}	Reset pulse High time	35		µs
P2	RST Low to reset during Erase/Program/Lock-bit		100	ns
t _{rec(RST)}	Reset Low to output delay		500	ns
t _{rec(WEL)}	Reset Recovery to WE going Low	1		µs
t _{WHRL}	WE High to Rdy/Bsy going low		100	ns



PRODUCT MARKING

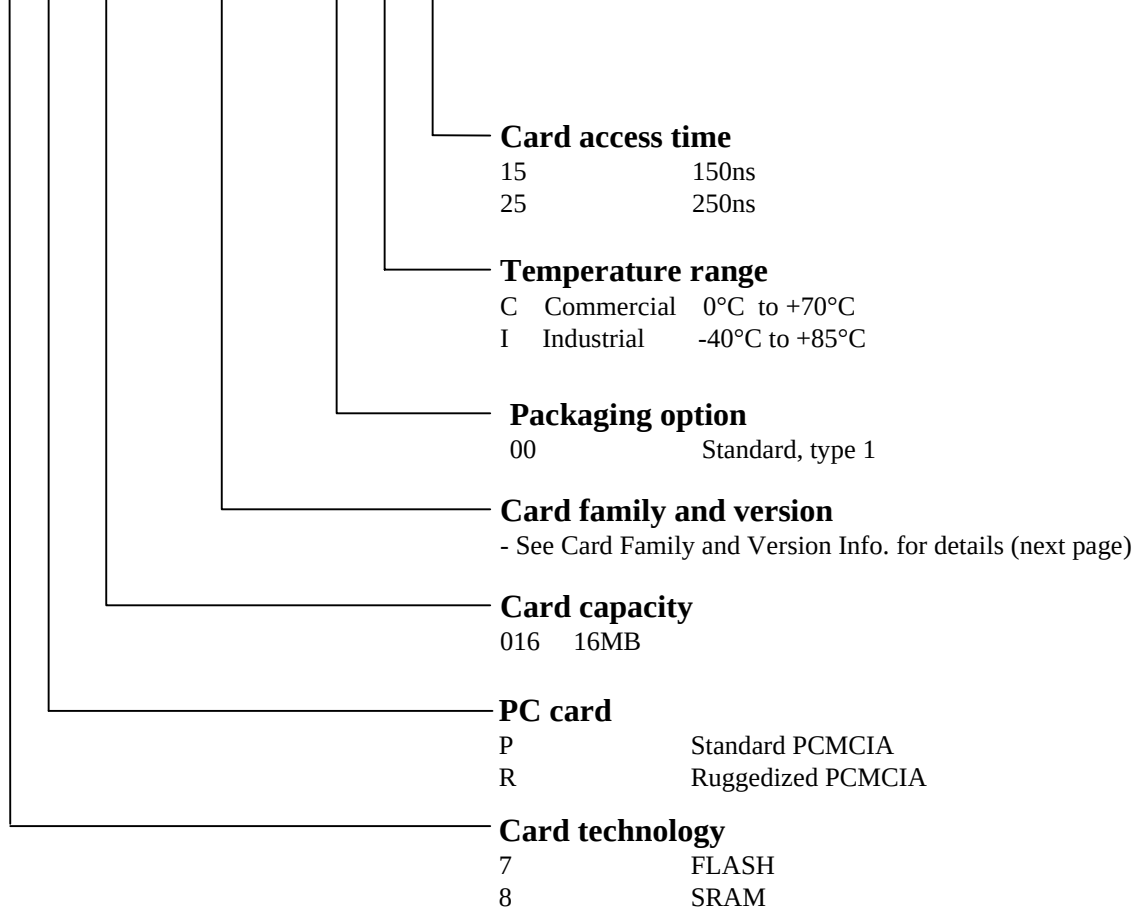
WED 7P016FLF0200C15 C995 9915



Note:
Some products are currently marked with our pre-merger company name/acronym (EDI). During our transition period, some products will also be marked with our new company name/acronym (WED). Starting October 2000 all PCMCIA products will be marked only with the WED prefix.

PART NUMBERING

7 P 016 FLF 02 00 C 15





CIS data for 16-64MB cards based on Intel 28F640J5

Address	Value	Description	Address	Value	Description	Address	Value	Description
00H	01H	CISTPL_DEVICE	4EH	1BH	CISTPL_CFTABLE_ENTRY	A4H	54H	T
02H	03H	TPL_LINK	50H	03H	TPL_LINK	A6H	52H	R
04H	51H	FLASH = 250ns (device writable)	52H	00H	TPCE_INDEX	A8H	4FH	O
06H	3EH	CARD SIZE: 16MB	54H	00H	TPCE_FS (no selection)	AAH	4EH	N
	7EH	32MB	56H	FFH	END OF TUPLE	ACH	49H	I
	BEH	48MB	58H	15H	CISTPL_VERS1	AEH	43H	C
	FEH	64MB	5AH	47H	TPL_LINK	B0H	20H	SPACE
08H	FFH	END OF TUPLE	5CH	05H	TPLL1V1_MAJOR	B2H	44H	D
0AH	18H	CISTPL_JEDEC_C	5EH	00H	TPLL1V1_MINOR	B4H	45H	E
0CH	03H	TPL_LINK	60H	45H	E	B6H	53H	S
0EH	89H	INTEL - ID	62H	44H	D	B8H	49H	I
10H	15H	INTEL 28F640J5 - ID	64H	49H	I	BAH	47H	G
12H	FFH	END OF TUPLE	66H	37H	7	BCH	4EH	N
14H	17H	CISTPL_DEVICE_A	68H	50H	P	BEH	53H	S
16H	03H	TPL_LINK	6AH	30H	0	C0H	20H	SPACE
18H	42H	EEPROM - 200ns	6CH	34H	4	C2H	49H	I
1AH	01H	Device Size = 2KBytes	6EH	38H	8	C4H	4EH	N
1CH	FFH	END OF TUPLE	70H	46H	F	C6H	43H	C
1EH	1EH	CISTPL_DEVICEGEO	72H	4CH	L	C8H	4FH	O
20H	07H	TPL_LINK	74H	46H	F	CAH	52H	R
22H	02H	DGTPL_BUS	76H	30H	0	CCH	50H	P
24H	12H	DGTPL_EBS	78H	32H	2	CEH	4FH	O
26H	01H	DGTPL_RBS	7AH	2DH	-	D0H	52H	R
28H	01H	DGTPL_WBS	7CH	2DH	-	D2H	41H	A
2AH	01H	DGTPL_PART	7EH	2DH	-	D4H	54H	T
2CH	01H	FLASH DEVICE NON-INTERLEAVED	80H	32H	2	D6H	45H	E
2EH	FFH	END OF TUPLE	82H	35H	5	D8H	44H	D
30H	20H	CISTPL_MANFID	84H	20H	SPACE	DAH	20H	SPACE
32H	05H	TPL_LINK(04H)	86H	00H	END TEXT	DCH	00H	END TEXT
34H	F6H	EDI TPLMID_MANF: LSB	88H	43H	C	DEH	31H	1
36H	01H	EDI TPLMID_MANF: MSB	8AH	4FH	O	E0H	39H	9
38H	00H	LSB: Number Not Assigned	8CH	50H	P	E2H	39H	9
3AH	00H	MSB: Number Not Assigned	8EH	59H	Y	E4H	38H	8
3CH	FFH	END OF TUPLE	90H	52H	R	E6H	00H	END TEXT
3EH	1AH	CISTPL_CONF	92H	49H	I	E8H	FFH	END OF LIST
40H	06H	TPL_LINK	94H	47H	G	EAH	FFH	
42H	01H	TPCC_SZ	96H	48H	H			
44H	00H	TPCC_LAST	98H	54H	T			
46H	00H	TPCC_RADR	9AH	20H	SPACE			
48H	40H	TPCC_RADR	9CH	45H	E			
4AH	03H	TPCC_RMSK	9EH	4CH	L			
			A0H	45H	E			



CIS data for 80MB card based on Intel 28F640J5

Address	Value	Description	Address	Value	Description	Address	Value	Description
00H	01H	CISTPL_DEVICE	50H	20H	CISTPL_MANFID	A0H	45H	E
02H	03H	TPL_LINK	52H	04H	TPL_LINK(04H)	A2H	4CH	L
04H	51H	FLASH = 250ns (device writable)	54H	F6H	EDI TPLMID_MANF: LSB	A4H	45H	E
06H	FEH	CARD SIZE: 64MB(1 st page)	56H	01H	EDI TPLMID_MANF: MSB	A6H	43H	C
08H	FFH	END OF TUPLE	58H	00H	LSB: Number Not Assigned	A8H	54H	T
0AH	09H	CISTPL_EXTDEVICE	5AH	00H	MSB: Number Not Assigned	AAH	52H	R
0CH	06H	TPL_LINK	5CH	15H	CISTPL_VERS1	ACH	4FH	O
0EH	04H	Mem Paging Info: 1bit/COR/64M	5EH	47H	TPL_LINK	AEH	4EH	N
10H	51H	FLASH = 250ns	60H	05H	TPLL1_MAJOR	B0H	49H	I
12H	07H	Device Size Extender	62H	00H	TPLL1_MINOR	B2H	43H	C
14H	01H	1x64MB	64H	45H	E	B4H	20H	SPACE
16H	3EH	+16MB	66H	44H	D	B6H	44H	D
18H	FFH	END OF TUPLE	68H	49H	I	B8H	45H	E
1AH	1AH	CISTPL_CONF	6AH	37H	7	BAH	53H	S
1CH	06H	TPL_LINK	6CH	50H	P	BCH	49H	I
1EH	01H	TPCC_SZ	6EH	30H	0	BEH	47H	G
20H	00H	TPCC_LAST(no index descript)	70H	38H	8	C0H	4EH	N
22H	00H	TPCC_RADR: LSByte	72H	30H	0	C2H	53H	S
24H	40H	TPCC_RADR: MSByte	74H	46H	F	C4H	20H	SPACE
26H	03H	TPCC_RMSK: 2 Reg	76H	4CH	L	C6H	49H	I
28H	FFH	END OF TUPLE	78H	46H	F	C8H	4EH	N
2AH	18H	CISTPL_JEDEC_C	7AH	30H	0	CAH	43H	C
2CH	03H	TPL_LINK	7CH	32H	2	CCH	4FH	O
2EH	89H	INTEL - ID	7EH	2DH	-	CEH	52H	R
30H	15H	INTEL 28F640J5 - ID	80H	2DH	-	D0H	50H	P
32H	FFH	END OF TUPLE	82H	2DH	-	D2H	4FH	O
34H	17H	CISTPL_DEVICE_A	84H	32H	2	D4H	52H	R
36H	03H	TPL_LINK	86H	35H	5	D6H	41H	A
38H	42H	EEPROM - 200ns	88H	20H	SPACE	D8H	54H	T
3AH	01H	Device Size = 2KBytes	8AH	00H	END TEXT	DAH	45H	E
3CH	FFH	END OF TUPLE	8CH	43H	C	DCH	44H	D
3EH	1EH	CISTPL_DEVICEGEO	8EH	4FH	O	DEH	20H	SPACE
40H	07H	TPL_LINK	90H	50H	P	E0H	00H	END TEXT
42H	02H	DGTPL_BUS	92H	59H	Y	E2H	31H	1
44H	12H	DGTPL_EBS	94H	52H	R	E4H	39H	9
46H	01H	DGTPL_RBS	96H	49H	I	E6H	39H	9
48H	01H	DGTPL_WBS	98H	47H	G	E8H	38H	8
4AH	01H	DGTPL_PART	9AH	48H	H	EAH	00H	END TEXT
4CH	01H	FLASH DEVICE NON-INTERLEAVED	9CH	54H	T	ECH	FFH	END OF LIST
4EH	FFH	END OF TUPLE	9EH	20H	SPACE	EEH	FFH	CISTPL_END
						D2H	FFH	



REVISION HISTORY		
Date of revision	Version	Description
20-Mar-98	-001	Initial release
27-May-99	-002	Logo change
5-Jun-00	-003	Added Page 10, changed page header
1-Aug-00	-004	Corrected timing errors on pgs. 7&8

White Electronic Designs Corporation

One Research Drive, Westborough, MA 01581, USA

tel: (508) 366 5151

fax: (508) 836 4850

www.whiteedc.com



WHITE ELECTRONIC DESIGNS