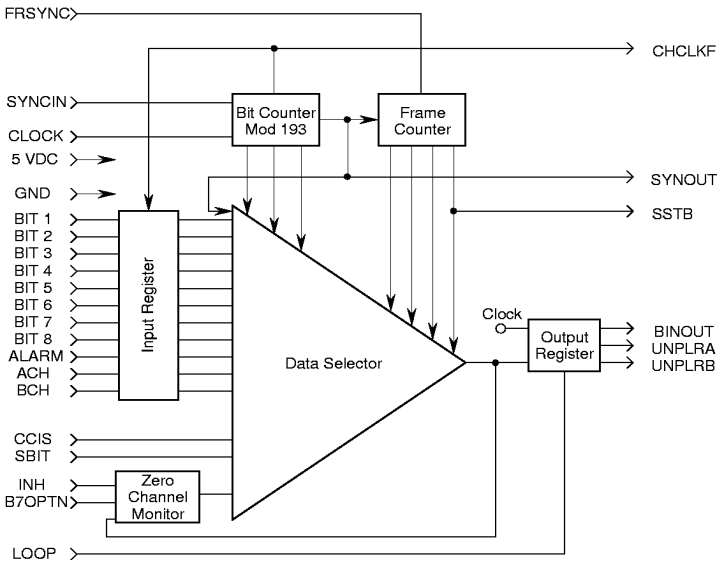
Bt8050

T-1 Serial Transmitter

Distinguishing Features

- Single 5 V Power Supply, Low-Power Schottky TTL Compatible
- Accepts Eight Bits of Parallel Data as Input
- Generates Output as 193-bit Serial Data Stream in T-1, D2, D3 or D4 Mode-3 Data Format
- Provides a Channel and Frame Timing Signal
- Provides Alternate Control for Alarm Reporting and Signalling
- Provides Automatic Bit Insertion for All-Zero Channel Samples

Functional Block Diagram



Product Description

The Brooktree T-1 Serial Transmitter formats data to be serially transmitted according to T-1 D2 or T-1 D3 specifications, inserting framing and signalling bits and 24 channels of 8-bit channel data. The T-1 Serial Transmitter also provides for alarm reporting via the bit 2 inhibit method, or with minimal external logic via the multiframe alignment signal (Fs) modification method.

The Mod-193 counter is driven by the clock at 1.544 MHz. The counter is either synchronized to the driving system by input signal SYNCIN or provides synchronization via output signal SYNOUT. Input signal FRSYNC applies synchronization to a Mod-12 counter, which identifies the frame of the 12-frame multiframe being processed.

The input data register latches data during each bit period, when bit 8 of a channel sample is being transmitted. The data selector outputs the proper sequence of bits as controlled by a bit count and frame count.

The zero channel monitor function causes bit 8 or bit 7 to be transmitted as a one if the channel data sample is all zeros. Input INH provides a means to inhibit the zero channel monitor function. Input B7OPTN controls the particulars of the insertion method.

Two types of transmit formats are provided, a binary output and a paired unipolar output. The unipolar pair provides a means to externally create a single bipolar output with minimal logic.

The T-1 Serial Transmitter operates on a single 5 V supply and is low-power Schottky TTL Compatible. The transmitter is packaged in a 28-Pin Dual In-Line Package (DIP) that is illustrated in Figure 1.

Brooktree Corporation • 9868 Scranton Rd. • San Diego, CA 92121-3707
(619) 452-7580 • (800) 2-BT-APPS • TLX: 383 596 • FAX: (619) 452-1249
L805001 Rev. A

Brooktree®

Interface Signals

T-1 Transmitter Inputs

Any input less than or equal to 0.8 V equals logical zero, low. Any input greater than or equal to 2.0 V equals logical one, high. The transition from a low level to a high level is called a "rising edge," while the converse is defined as a "falling edge."

Frame Synchronization (FRSYNC)

Frame sync allows external synchronization of the transmitter's internal frame counter. When FRSYNC becomes high, the frame counter is directly set to Frame 1, the first of the 12 frames. If FRSYNC is held high and does not return to zero before a rising edge of CLOCK, the subsequent states of BINOUT, UNPLRA, and UNPLRB are high and low, respectively, regardless of the states of any other inputs. The latter mechanism is useful for device and/or board testing only, and will cause bit errors and/or bipolar violations if used during field operations (see Figures 2 and 3).

Synchronization Input (SYNCIN)

SYNCIN allows external synchronization of the internal Modulo 193 bit per-channel counter. When SYNCIN becomes high, the Modulo 193 counter is directly set to the state corresponding to the output of the framing bit (F_T or F_S). The first bit of Channel 1 will be output on BINOUT (and UNPLRA or UNPLRB) as a result of the first rising edge of CLOCK following the return of SYNCIN to logical zero (see Figures 2 and 4).

Booktree Device Test Input (TEST)

This is used only for Booktree device testing. *Keep this input grounded.*

T-1 Clock (CLOCK)

Maximum frequency = 1.6 MHz

Minimum pulse width = 275 ns

The T-1 bit period is bounded by the rising edges of this input.

Inhibit Zero Channel Monitor (INH)

If INH is high, the zero channel monitor function is disabled and bits 7 and 8 are transmitted per corresponding inputs received (see Table 1).

For channels in signalling frames 6 or 12 in which the first six data bits and the signalling highway are all zeros, bit 7 will be forced to one if INH is low. For any frame except a signalling frame, bit 8 or bit 7 as selected by B70PTN will be transmitted as a one if the channel input data is zero and INH is low.

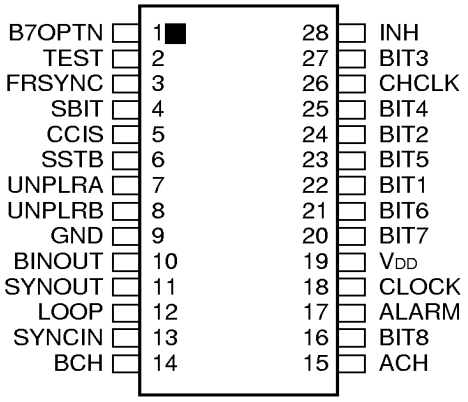


Figure 1. Pin Configuration.

Interface Signals *(continued)*

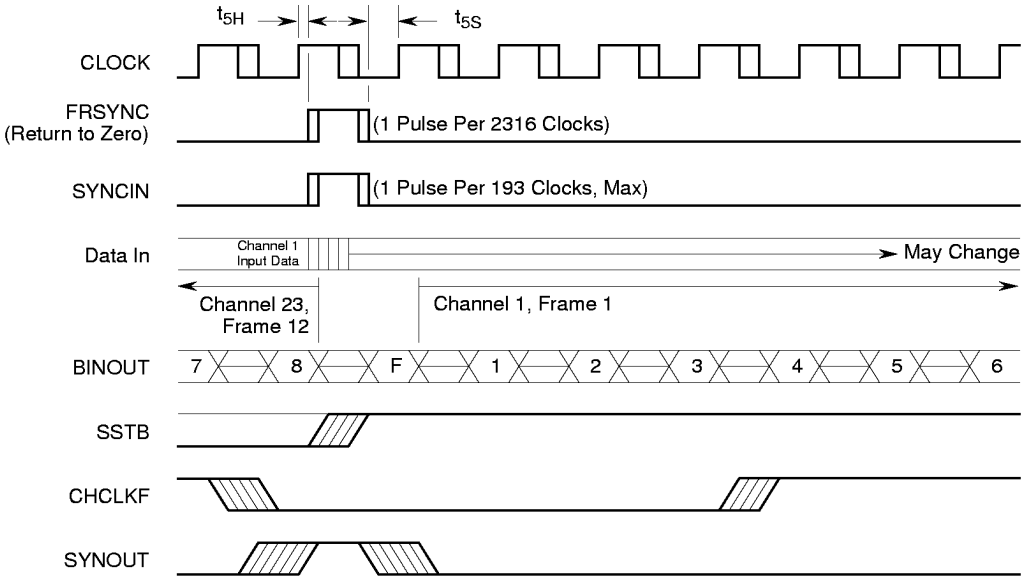


Figure 2. Transmitter External Synchronization (Return to Zero FRSYNC).

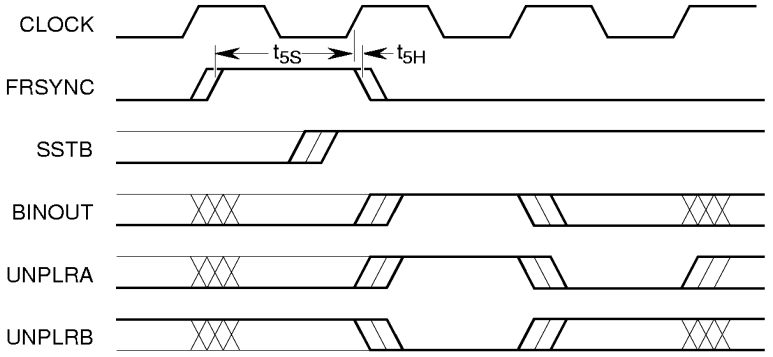


Figure 3. Non-Return to Zero FRSYNC Timing.

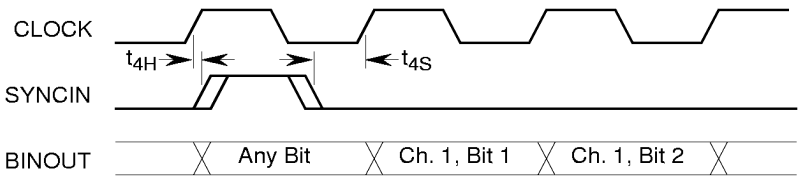


Figure 4. SYNCIN Timing Relationship.

Interface Signals *(continued)*

Inputs X = Don't Care													Current Frame Number	Binout Serial Output Channel Bit Position								Notes
ALARM	INH	B7OPTN	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	ACH	BCH		1	2	3	4	5	6	7	8	
1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
0	X	X	P	Q	R	S	T	U	V	X	A	X	6	P	Q	R	S	T	U	V	A	2
0	X	X	P	Q	R	S	T	U	V	X	X	B	12	P	Q	R	S	T	U	V	B	2
0	X	X	P	Q	R	S	T	U	V	W	X	X	Y	P	Q	R	S	T	U	V	W	2,3
0	1	X	0	0	0	0	0	0	0	X	A	X	6	0	0	0	0	0	0	0	A	
0	1	X	0	0	0	0	0	0	0	X	X	B	12	0	0	0	0	0	0	0	B	
0	1	X	0	0	0	0	0	0	0	W	X	X	Y	0	0	0	0	0	0	0	W	3
0	0	X	0	0	0	0	0	0	0	X	0	X	6	0	0	0	0	0	0	1	0	
0	0	X	0	0	0	0	0	0	0	X	X	0	12	0	0	0	0	0	0	1	0	
0	0	1	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	1	0	3
0	0	0	0	0	0	0	0	0	0	0	X	X	Y	0	0	0	0	0	0	0	1	3

Note 1: ALARM = has the same effect as BIT 2 = 0
Note 2: P,Q,R,S,T,U and V may not simultaneously be zero, unless A, B or W is 1
Note 3: Y is any frame # 6 and # 12 with CCIS = 0, or all frames with CCIS = 1

Table 1: Serial Channel Sample Output Data Truth Table.

Parallel Channel Data Input (BITS 1-8)

Bit 1, the sign bit, will be serially transmitted first, followed by bits 2 through 8. The falling edge of CHCLKF indicates input channel data has been clocked into the input register and always occurs during the transmission of the final bit (bit 8) of each channel data sample.

A-Channel Highway Signalling (ACH)

ACH allows the user to transmit one bit of signalling per channel as bit 8 of each channel data sample in Frame 6 only. ACH is clocked into the input register by the falling edge of CHCLKF (see Table 1 and Figure 5).

Interface Signals *(continued)*

B-Channel Highway Signalling (BCH)

BCH allows the user to transmit one bit of signalling per channel as bit 8 of each channel data sample in Frame 12 only. BCH is clocked into the input register by the falling edge of CHCLKF (see Table 1 and Figure 5).

Multiframe Signalling Bit (SBIT)

SBIT, in conjunction with CCIS, provides an alternate way to control the multiframe signalling bit (FS) transmission. The SBIT input is transmitted as the multiframe signalling bit (F_S) if CCIS is held high (see Table 2).

Local Alarm (ALARM)

ALARM is used to report alarm conditions. If the ALARM signal is high, bit 2 (the most significant bit) of every channel data sample of every frame is transmitting as a zero. This is commonly called "remote alarm signalling." ALARM is clocked into the input register at the falling edge of CHCLKF (see Table 1 and Figure 5).

Loop Strap (LOOP)

LOOP is provided to aid testing of user applications. When enabled to a high level, LOOP forces the unipolar outputs to transmit alternating ones and zeros, regardless of input conditions, while BINOUT continues to provide normal data outputs (see Figure 6).

Common Channel Interoffice Signalling Strap (CCIS)

CCIS provides optional control for replacing the automatic F_S pattern with a 4-KB common channel signalling path. When CCIS is high, the SBIT input replaces the FS pattern, and the insertion of ACH and BCH is suspended. CCIS input may also be used to provide the alternate method of alarm reporting (see Figure 5).

Bit 7 Option (B7OPTN)

P7OPTN provides bit 7 as an alternate bit position for "one stuffing," as programmed by the zero channel monitor function. (See Table 1.)

Ground And Power (VSS, VDD)

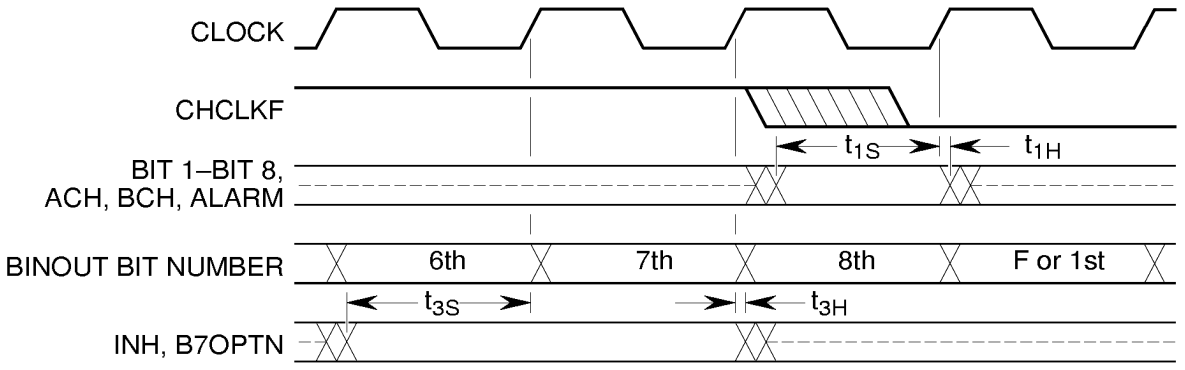
V_{SS} = Ground, 0 Vdc
V_{DD} = +5 ± 0.25 Vdc

Frame Number	Processed Bit	Binout	
		CCIS = 0	CCIS = 1
1	FT	1	1
2	FS	0	SBIT
3	FT	0	0
4	FS	0	SBIT
5	FT	1	1
6	FS	1	SBIT
7	FT	0	0
8	FS	1	SBIT
9	FT	1	1
10	FS	1	SBIT
11	FT	0	0
12	FS	0 (Note 1)	SBIT

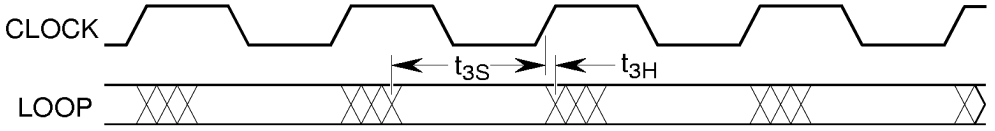
Note 1: Alternate remote alarm reporting may be accomplished by holding SBIT and CCIS both high just prior to initiation of Frame 12.
Note 2: F_t bit insertion is automatic and no optional control is provided.

Table 2: Framing Bit (F_t and F_s) Output Data.

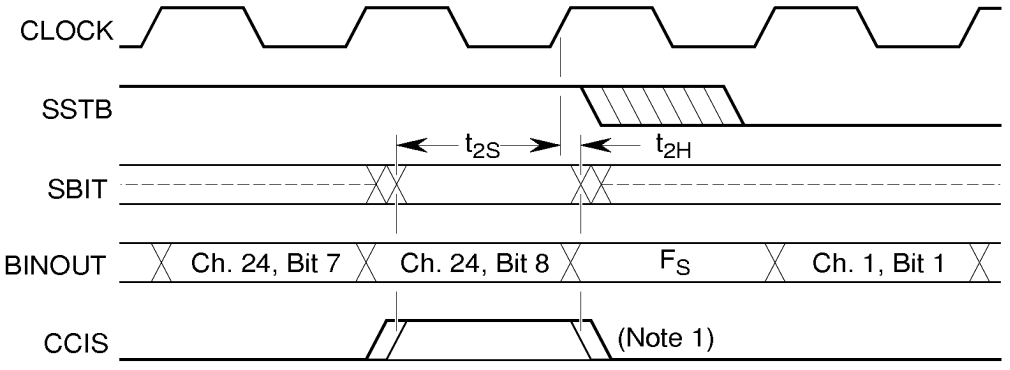
Interface Signals *(continued)*



a. Channel Input Timing



b. LOOP Input Timing



c. Control Input Timing

Note 1: CCIS waveform shown for alternate alarm reporting method. CCIS should be active just prior to Frame 12. Under these conditions, SBIT high would report the remote alarm.

Figure 5. a, b, c: Input Timing.

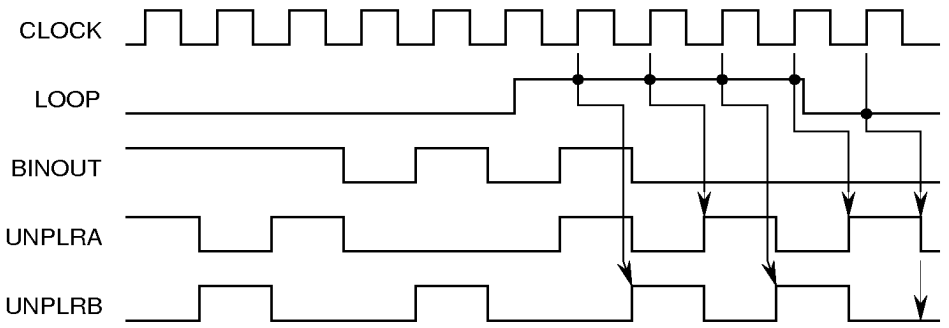


Figure 6. Transmitter Binary, Unipolar Outputs.

T-1 Transmitter Outputs

The transmitter outputs are low power, TTL Schottky compatible. 1 ≥ 2.4 Vdc, 0 ≤ 0.4 Vdc, and CMOS requires a 12k Ω pullup to V_{DD}.

4 kHz Signalling Channel Strobe (SSTB)

SSTB is the least significant bit of the frame counter. Unless SSTB is directly set by FRSYNC, SSTB will go high as each framing bit (F_T) is serially transmitted, and will return low as each multiframe alignment signal (F_S) is transmitted (see Figure 7).

Channel Sync Output (SYNOUT)

SYNOUT provides a means to synchronize to the internal bit counter (Mod 193). SYNOUT is high for one bit time, beginning just prior to the first data bit of a frame being serially transmitted (see Figure 2). SYNOUT is the only output determined by the falling edge of CLOCK.

Channel Clock False (CHCLKF)

The falling edge of CHCLKF, occurring while bit 8 of any channel is being serially transmitted, indicates input data has been clocked into the input register. With the exception of an extra bit period extending the low level duration at frame bit time, CHCLKF is a divide-by-8 of CLOCK (see Figure 7).

Serial Data Output, Binary Formatted (BINOUT)

BINOUT is the binary formatted serial conversion of the parallel input data. The programmed format of BINOUT is shown in Tables 1 and 2.

BINOUT is synchronously transmitted as a high level if FRSYNC remains high during the rising edge of CLOCK (see Figures 2 and 3).

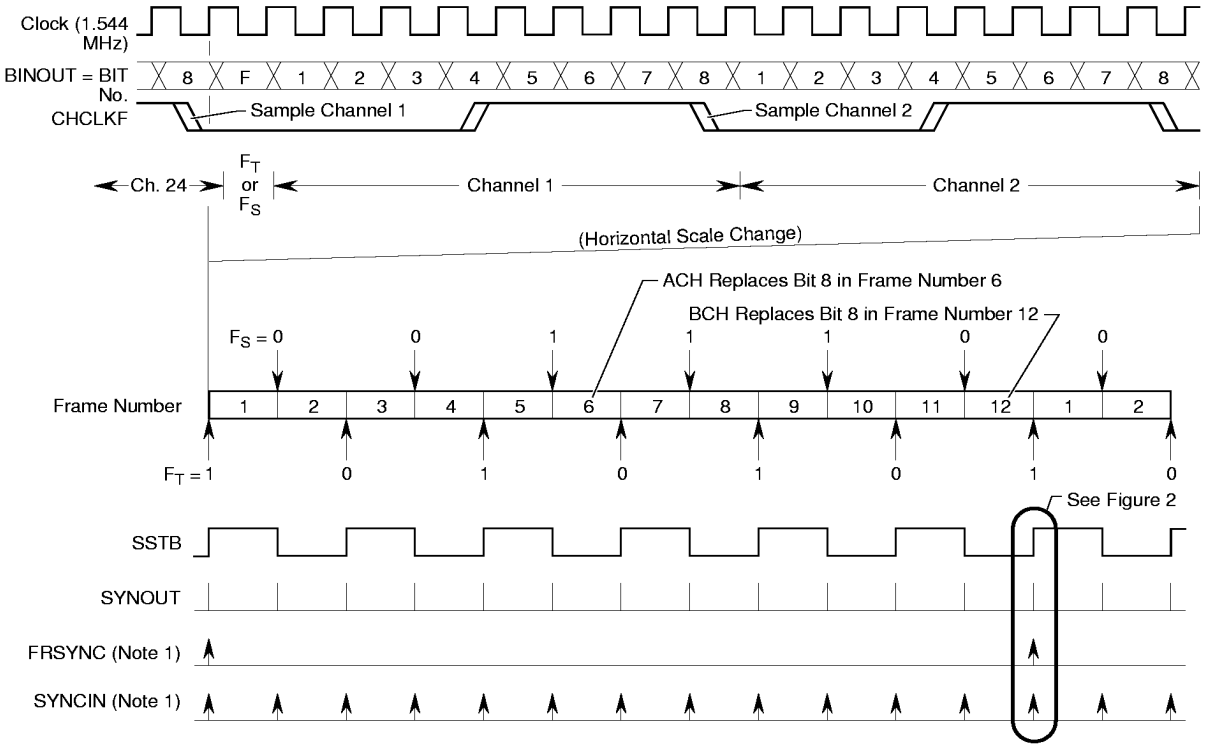
T-1 Serial Data Unipolar Outputs (UNPLRA, UNPLRB)

Two paired unipolar outputs are provided to create a single serial data output transmission in bipolar format. The unipolar output register toggle for each logical one bit to be serially transmitted. UNPLRA and UNPLRB are transmitted as complements for logical one data bits as low levels for logical zero data bits (see Figure 6).

If the input signal LOOP is high, the unipolar outputs are forced to toggle every bit time, regardless of input data.

FRSYNC perturbs the current bits being transmitted by UNPLRA and UNPLRB. If FRSYNC remains high during the rising edge of CLOCK, UNPLRA will be transmitted as a high level, and UNPLRB will be low (see Figures 2 and 3).

Interface Signals *(continued)*



Note 1: Possible positions to reinforce internal synchronization.

Figure 7. T-1 Serial Transmitter Input-Output Signal Relationships.

Interface Signals *(continued)*

Symbol	Parameter	Min	Max	Unit
t_{1S}	Buffered Data Setup Time	450		ns
t_{1H}	Buffered Data Hold Time	0		ns
t_{2S}	Control Input Setup Time	400		ns
t_{2H}	Control Input Hold Time	20		ns
t_{3S}	Asynchronous Control Input Setup Time	350		ns
t_{3H}	Asynchronous Control Input Hold Time	20		ns
t_{4S}	SYNCIN Setup Time	200		ns
t_{4H}	SYNCIN Hold Time	20		ns
	SYNCIN Pulse Width	100		ns
t_{5S}	Frame Sync Setup Time (Return to Zero)	250		ns
t_{5H}	Frame Sync Hold Time (Return to Zero)	20		ns
	Frame Sync Pulse Width	200		ns
t_{5S}	Frame Sync Setup Time (Non-Return to Zero)	525		ns
t_{5H}	Frame Sync Hold Time (Non-Return to Zero)	20		ns

Table 3. Input Timing.

Output	Max Delay	Unit
SSTB	500	ns
SYNOUT	500	ns
Ref from Falling Edge of Clock		
CHCLKF	500	ns
BINOUT	500	ns
UNPLRA	500	ns
UNPLRB	500	ns

Table 4. Output Propagation Delay, Worst Case.
Measured From Rising Edge of Clock Unless Stated Otherwise.

Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{DD}	+4.75 to +5.25	Vdc
Operating Temperature	T_{OP}	0 to +70	°C
Storage Temperature	T_{STG}	–55 to +150	°C

Note: Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

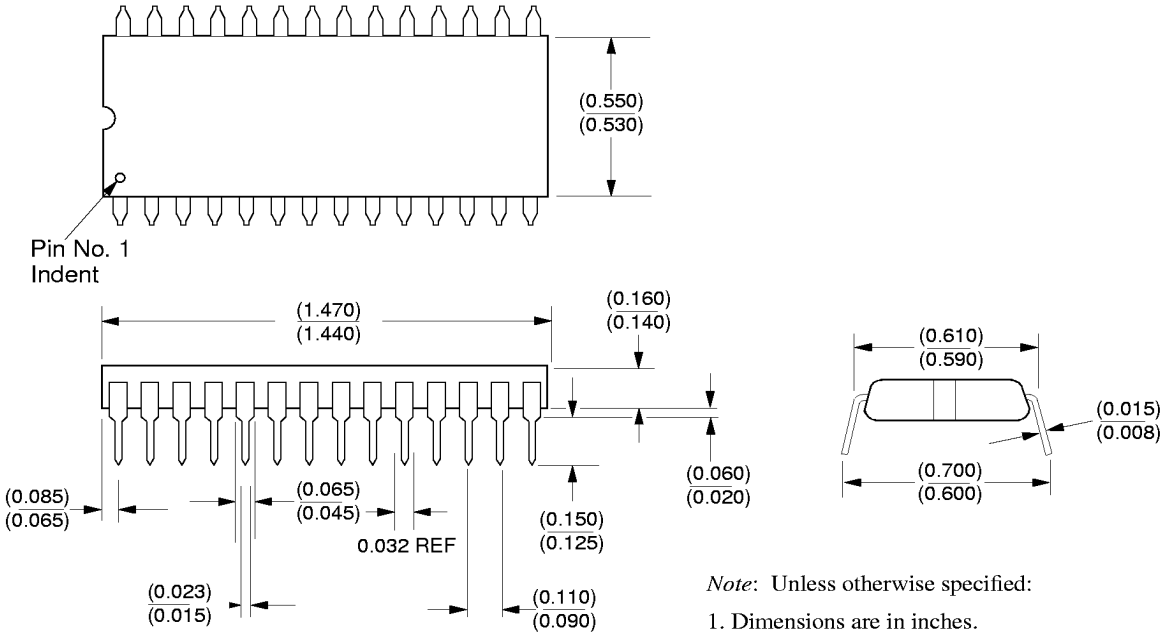
V_{DD} = +5.0 ± 5%

Parameter	Symbol	Min	Max	Unit
Logical 1 Input Voltage	V_{OH}	2.0	VDD + 0.3	V
Logical 0 Input Voltage	V_{IL}	-0.3	0.8	V
Logical l Output Voltage	V_{OH}	2.4	–	V
Logical 0 Output Voltage	V_{OL}	–	0.4	V
Output Source Current	I_{OH}	–100	–	µA
Output Sink Current	I_{OL}	400	–	µA
Capacitance Load (any output)	C	–	25	pF
Input Capacitance (any input)	C_{IN}	–	5	pF
Clock Frequency		–	1.6	MHz
Power Dissipation	P_D	–	250	mW

Ordering Information

Part Number	Package	Temperature Range
Bt8050KP	28-pin Plastic DIP	0°C to 70°C
Bt8050KC	28-pin Ceramic DIP	0°C to 70°C
Bt8050EP	28-pin Plastic DIP	–40°C to +85°C

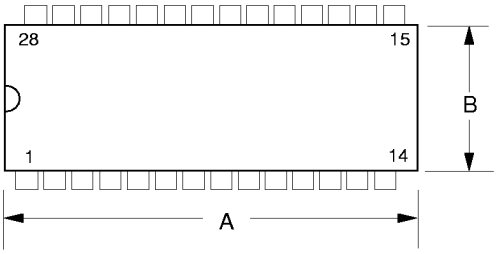
Package Dimensions



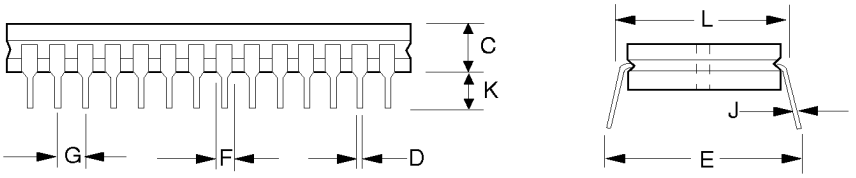
Note: Unless otherwise specified:

1. Dimensions are in inches.

28-Pin Plastic DIP



DIM.	MILLIMETERS MIN.	MILLIMETERS MAX.	INCHES MIN.	INCHES MAX.
A	36.32	37.34	1.430	1.470
B	12.95	13.46	0.510	0.530
C	3.68	4.19	0.145	0.165
D	0.41	0.51	0.016	0.020
E	16.26	17.27	0.640	0.680
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	4.19	4.95	0.165	0.195
L	15.24 BSC		0.600 BSC	
M	0°	10°	0°	10°
REF: PD28S/GP00-D310				



28-Pin Ceramic DIP