# μPD23128A
# 16,384 x 8-BIT MASK-PROGRAMMABLE NMOS ROM

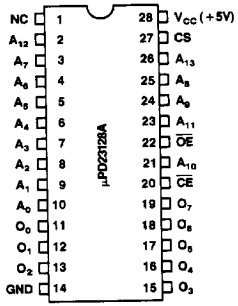
## Description

The μPD23128A is a 131,072-bit edge-enabled Read-only Memory utilizing MOS N-channel silicon gate technology. The device is organized as 16,384 words by 8 bits and operates from a single +5V power supply. All inputs and outputs are fully TTL-compatible. The device has one programmable chip select with three-state outputs that allow memory expansion without the use of external logic. Programming is accomplished during the fabrication process. Pinout is compatible with 27128 EPROMs.

## Features

- ☐ Fast access time: 200ns max
- ☐ All inputs and outputs TTL-compatible
- ☐ Single +5V ± 10% power supply
- ☐ Three-state outputs for direct bus compatibility
- ☐ Edge-enabled operation
- ☐ Mask-programmable chip select for memory expansion
- ☐ Low-power standby mode

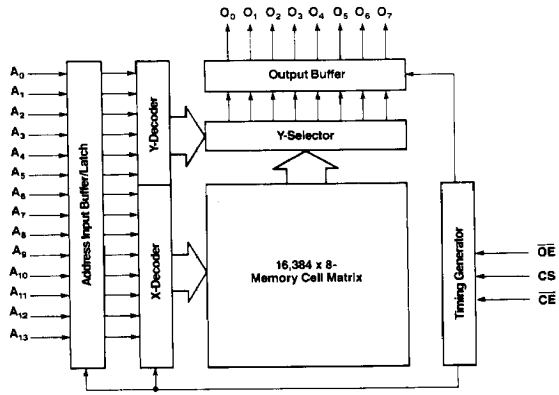
## Pin Configuration




## Pin Identification

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | NC | No Connection. |
| 2-10, 21, 23-26 | $A_0$-$A_{13}$ | Address Inputs. |
| 11-13, 15-19 | $O_0$-$O_7$ | Three-state Data Outputs. |
| 14 | GND | Ground. |
| 20 | $\overline{CE}$ | Chip Enable. |
| 22 | $\overline{OE}$ | Output Enable. |
| 27 | CS | Mask-programmable Chip Select. |
| 28 | $V_{CC}$ | Single +5V Power Supply. |

## Block Diagram




## Absolute Maximum Ratings*

| | |
|---|---|
| Supply Voltage, $V_{CC}$ | −0.5V to +7V |
| Input Voltage, $V_I$ | −0.5V to +7V |
| Output Voltage, $V_O$ | −0.5V to +7V |
| Operating Temperature, $T_{OPR}$ | −10°C to +70°C |
| Storage Temperature, $T_{STG}$ | −65°C to +150°C |

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Capacitance

$T_A$ = 25°C

| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input Capacitance | $C_I$ | | | 10 | pF | f = 1MHz |
| Output Capacitance | $C_O$ | | | 15 | pF | f = 1MHz |

6

## DC Characteristics

**$T_A$ = −10°C to +70°C; $V_{CC}$ = +5V ± 10%**

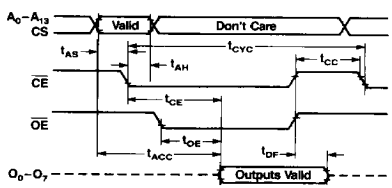
| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Input High Voltage | $V_{IH}$ | +2.0 | | $V_{CC}$+1 | V | |
| Input Low Voltage | $V_{IL}$ | −0.5 | | +0.8 | V | |
| Output High Voltage | $V_{OH}$ | +2.4 | | | V | $I_{OH}$ = −400μA |
| Output Low Voltage | $V_{OL}$ | | | +0.4 | V | $I_{OL}$ = +3.2mA |
| Input Leakage Current High | $I_{LIH}$ | | | +10 | μA | $V_I = V_{CC}$ |
| Input Leakage Current Low | $I_{LIL}$ | | | −10 | μA | $V_I$ = 0V |
| Output Leakage Current High | $I_{LOH}$ | | | +10 | μA | $V_O = V_{CC}$, chip deselected |
| Output Leakage Current Low | $I_{LOL}$ | | | −10 | μA | $V_O$ = 0V, chip deselected |
| Power Supply Current | $I_{CC1}$ | | +25 | +40 | mA | $t_{CYC}$ = 350ns |
| | $I_{CC2}$ | | +7 | +15 | mA | Standby mode |

## AC Characteristics

**$T_A$ = −10°C + 70°C; $V_{CC}$ = +5V ± 10%**

| Parameter | Symbol | Limits Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Cycle Time | $t_{CYC}$ | 300 | | | ns | |
| Address Set-up Time | $t_{AS}$ | 0 | | | ns | |
| Address Hold Time | $t_{AH}$ | 50 | | | ns | Output load = 1 TTL + 100pF |
| Chip Enable Access Time | $t_{CE}$ | | | 200 | ns | Input voltage ($t_R$, $t_F$) = 20ns |
| Output Enable Access Time | $t_{OE}$ | | | 100 | ns | Timing reference levels: Input and output voltages = 0.8V and 2.0V |
| Access Time | $t_{ACC}$ | | | 200 | ns | |
| Output Disable Time | $t_{DF}$ | 0 | | 70 | ns | |
| Chip Enable Off Time | $t_{CC}$ | 50 | | | ns | |

## Timing Waveform




## Definitions

### Cycle Time, $t_{CYC}$

The minimum time between data access cycles as measured from one chip enable pulse to the next.

### Address Set-up Time, $t_{AS}$

The minimum time between application of a valid address to be latched into the device, and the negative transition of the chip enable pulse.

### Address Hold Time, $t_{AH}$

The minimum time that valid address inputs must be held after the latching chip enable pulse reaches a logic zero level.

### Chip Enable Access Time, $t_{CE}$

The minimum time between application of a valid chip enable input and the corresponding valid outputs.

### Output Enable Access Time, $t_{OE}$

The minimum time between application of a valid output enable input and the corresponding valid outputs.

### Access Time, $t_{ACC}$

The minimum time between application of valid inputs and chip selects and the corresponding valid outputs.

### Output Disable Time, $t_{DF}$

The maximum delay between output enable or chip enable becoming false and data outputs going to a high impedance state.

### Chip Enable Off Time, $t_{CC}$

The minimum time that chip enable must be off (at Logic 1) before the next access cycle may be initiated.

## Custom Programming Instructions

### Bit pattern submittal options

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 27128 EPROM
2. Two programmed 2764 EPROMs
3. Four programmed 2732 EPROMs

### Bit pattern verification

For customer verification of the submitted bit pattern, several alternatives are also available. The following are those found to be most expeditious.

| Customer Pattern Submitted Via | Verification Routine |
|---|---|
| 1. One programmed 27128 EPROM | Customer sends NEC one additional erased 27128. NEC programs the spare 27128 with the data from the programmed 27128, and returns it to the customer for verification. |
| 2. Two programmed 2764 EPROMs | Customer sends NEC two additional erased 2764s. NEC programs the spare 2764s with the data from the programmed 2764s and returns them to the customer for verification. |
| 3. Four programmed 2732 EPROMs | Customer sends NEC four additional erased 2732s. NEC programs the spare 2732s with the data from the programmed 2732s and returns them to the customer for verification. |

## Package Outlines

**For information, see Section 9.**

**Plastic, μPD23128AC**