

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

## T6C13B

### COLUMN AND ROW DRIVER FOR A DOT MATRIX LCD

The T6C13B is a 240-channel-output column and row driver for an STN dot matrix LCD.

The T6C13B features a 42-V LCD drive voltage and a 20-MHz maximum operating frequency. The T6C13B is able to drive LCD panels with a duty ratio of up to 1 / 480.

#### Features

- Display duty application : to 1 / 480
- LCD drive signal : 240
- Data transfer : 8-bit bidirectional
- Operating frequency : 27 MHz (V<sub>DD</sub> = 4.5 to 5.5 V)
- LCD drive voltage : 14 to 40 V
- Power supply voltage : 2.7 to 5.5 V
- Operating temperature : -20 to 75°C
- LCD drive output resistance : 800 Ω (max) (20 V, 1 / 13 bias)
- Display-off function : When / DSPOF is L, all LCD drive outputs (O1 to O240) remain at the V<sub>5</sub> level.
- Low power consumption : Cascade connection and auto enable transfer functions are available.

Unit: mm

T6C13B	LEAD PITCH	
	IN	OUT
(UAN, 5DS)	0.50	0.086

Please contact Toshiba or an authorized Toshiba dealer for information on package dimensions.

TCP (Tape Carrier Package)

000707EBE1

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• Polyimide base film is hard and thin. Be careful not to injure yourself on the film or to scratch any other parts with the film. Try to design and manufacture products so that there is no chance of users touching the film after assembly, or if they do, that there is no chance of them injuring themselves. When cutting out the film, try to ensure that the film shavings do not cause accidents. After use, treat the leftover film and reel spacers as industrial waste.

• Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.

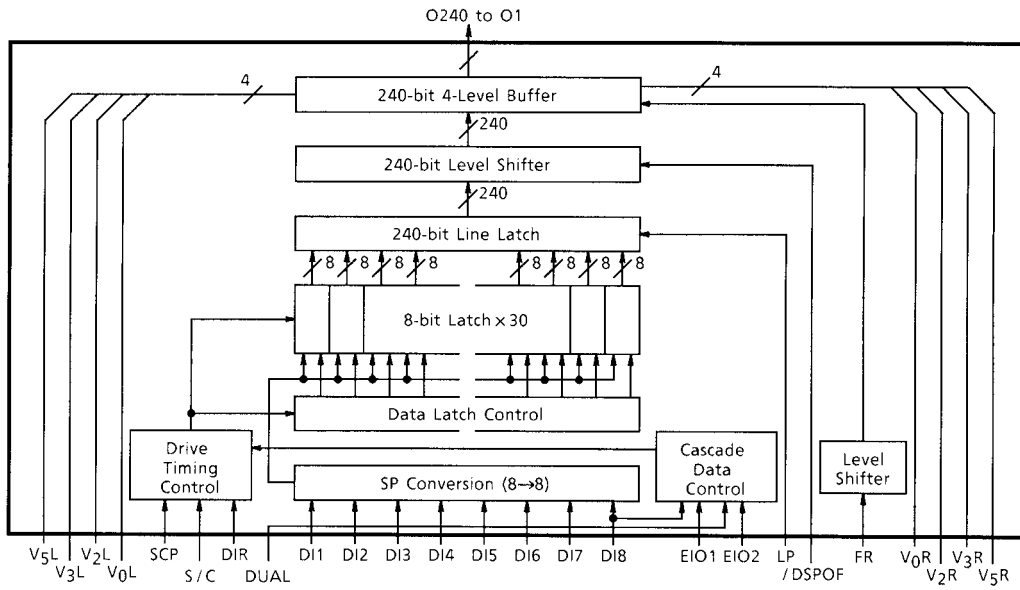
This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.

• The products described in this document are subject to the foreign exchange and foreign trade laws.

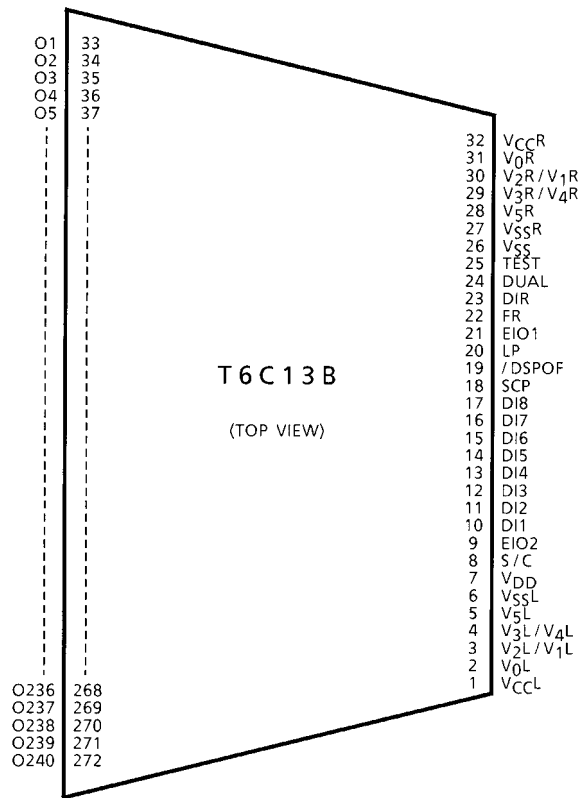
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**Block Diagram**



**Pin Assignment**



Note: The above diagram shows the pin configuration of the LSI chip, not that of the tape carrier package.

## Pin Functions

Pin Name	I / O	Functions	Level
O1 to O240	Output	Output for LCD drive signal	V <sub>0</sub> to V <sub>5</sub>
EIO1, EIO2	I / O	Input / output for enable signal DIR selects In or Out. Connect EIO (IN) of 1st LSI to L. For a cascade connection, connect EIO (OUT) to EIO (IN) of next LSI.	V <sub>DD</sub> to V <sub>SS</sub>
DI1 to DI8	Input	(Column mode) Input for data signal	
		(Row mode) DI1 to DI7 : Fix to H or L DI8 : 121st enable terminal in dual mode.	
DIR	Input	(Direction) Input for data flow direction select	
/ DSPOF	Input	(Display off) / DSPOF = L : Display-off mode, (O1 to O240) remain at the V <sub>5</sub> level. / DSPOF = H : Display-on mode, (O1 to O240) are operational.	
DUAL	Input	(Column mode) Fix to H or L	
		(Row mode) Terminal for dual input mode or single input mode select	
LP	—	(Column mode) Display data is latched on falling edges of LP. When EIO (IN) = L, setting $\overline{\text{SCP}} \cdot \text{LP} = \text{H}$ enables the 1st LSI.	
		(Row mode) Input for shift clock pulse	
FR	Input	(Frame) Input for frame signal	
SCP	Input	(Column mode) Input for shift clock pulse	
		(Row mode) Fix to H or L	
TEST	Input	(Test) Fix to L or open	
S / C	Input	Input for mode select: H = Column mode, L = Row mode	
V <sub>DD</sub>	—	Power supply for internal logic (+5.0 V)	—
V <sub>SS</sub>	—	Power supply for internal logic (0 V)	
V <sub>SS</sub> L-R	—	Power supply for LCD drive circuit	
V <sub>5</sub> L-R	—	Power supply for LCD drive circuit	
V <sub>3/4</sub> L-R	—	Power supply for LCD drive circuit	
V <sub>2/1</sub> L-R	—	Power supply for LCD drive circuit	
V <sub>0</sub> L-R	—	Power supply for LCD drive circuit	
V <sub>CC</sub> L-R	—	Power supply for LCD drive circuit	

## Relation between FR, Data Input and Output Level

F R	Data Input (DI1 to DI8)	/ DSPOF	Output Level (Column Mode)	Output Level (Row Mode)
L	L	H	V <sub>3</sub>	V <sub>4</sub>
L	H	H	V <sub>5</sub>	V <sub>0</sub>
H	L	H	V <sub>2</sub>	V <sub>1</sub>
H	H	H	V <sub>0</sub>	V <sub>5</sub>
—	—	L	V <sub>5</sub>	V <sub>5</sub>

## Data Input Format

### Column mode

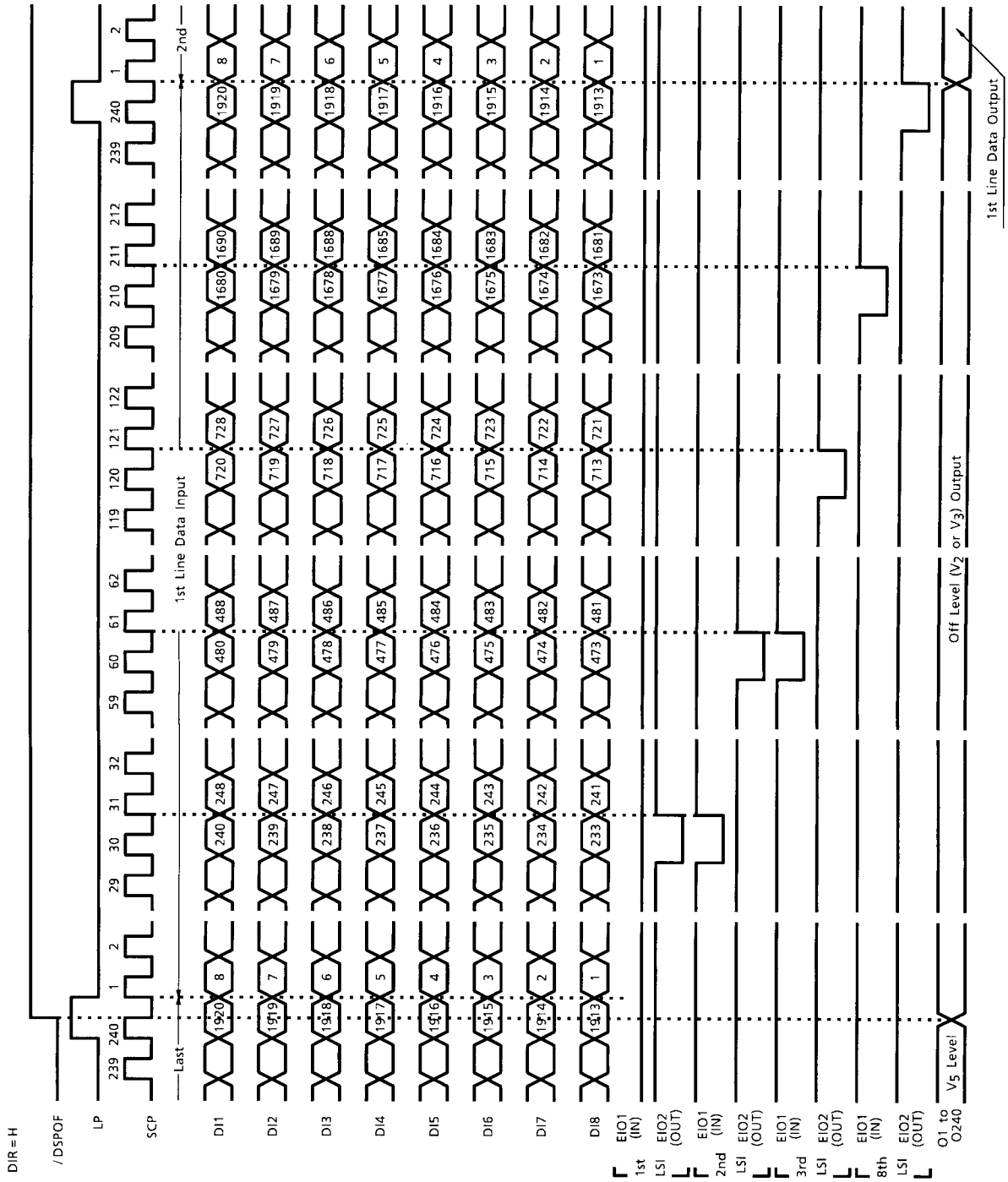
DIR	BIT Mode	Enable Pin		(*1)	Input Data Line and Output Buffers							
		EIO1	EIO2		DI1	DI2	DI3	DI4	DI5	DI6	DI7	DI8
H	8-BIT	IN	OUT	L	O240	O239	O238	O237	O236	O235	O234	O233
				F	O8	O7	O6	O5	O4	O3	O2	O1
L		OUT	IN	L	O1	O2	O3	O4	O5	O6	O7	O8
				F	O233	O234	O235	O236	O237	O238	O239	O240

\*1: L: Last Data      F: First Data

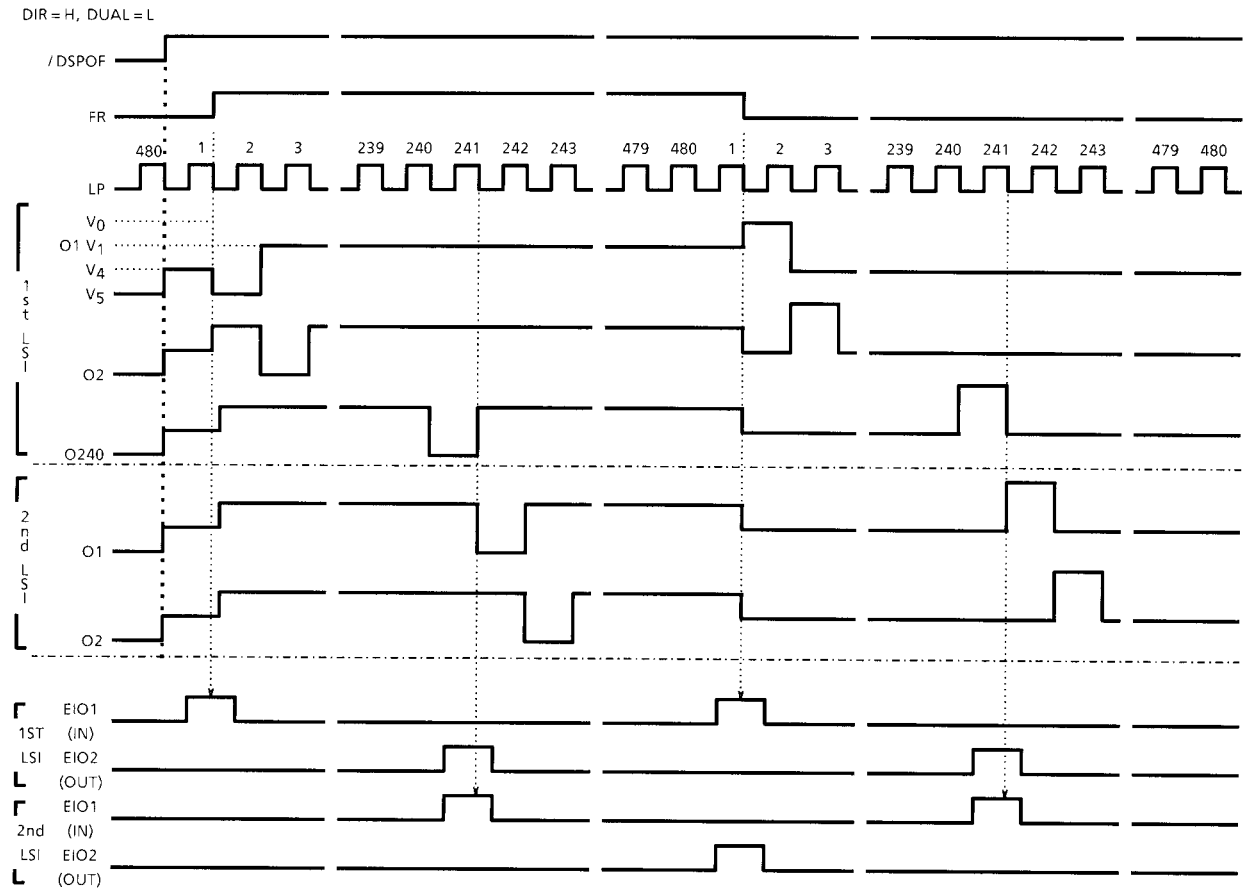
### Row mode

DUAL	DIR	Data Flow	Data Input Terminals		
			EIO1	EIO2	DI8
L	L	O240 → O1	OUT	IN	—
L	H	O1 → O240	IN	OUT	—
H	L	O120 → O1 O240 → O121	OUT	IN	IN
H	H	O1 → O120 O121 → O240	IN	OUT	IN

Timing Diagram (Column Mode)



**Timing Diagram (Row Mode)**



## Absolute Maximum Ratings

(Ensure that the following conditions are maintained,  $V_{CC} \geq V_0 \geq V_{2,1} \geq V_{3,4} \geq V_5 \geq V_{SS}$ )

Item	Symbol	Pin Name	Rating	Unit
Supply Voltage 1	$V_{DD}$	$V_{DD}$	-0.3 to 6.5	V
Supply Voltage 2	$V_{CC}$	$V_{CCL} / R$	-0.3 to 42.0	V
Supply Voltage 3	$V_0, V_2$	$V_{0L} / R, V_{2,1L} / R$	-0.3 to $V_{CC} + 0.3$	V
Supply Voltage 4	$V_3, V_5$	$V_{3,4L} / R, V_{5L} / R$	-0.3 to 42.0	V
Input Voltage	$V_{IN}$	(Note 2)	-0.3 to $V_{DD} + 0.3$	V
Operating Temperature	$T_{opr}$	—	-20 to 75	°C
Storage Temperature	$T_{stg}$	—	-40 to 125	°C

Note 2: SCP, FR, LP, DIR, DUAL, EIO1, EIO2, DI1 to DI8, / DSPOF, TEST, S / C

## Electrical Characteristics

### DC Characteristics

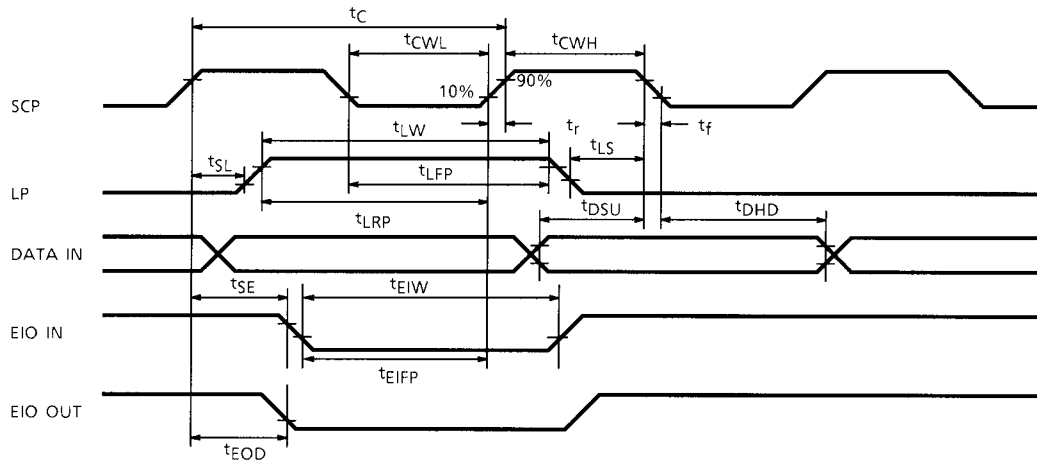
(Unless otherwise noted,  $V_{SS} = 0$  V,  $V_{DD} = 2.7$  to 5.5 V,  $T_a = -20$  to 75°C)

Item	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Pin Name		
Supply Voltage 1	$V_{DD}$	—	—	2.7	5.0	5.5	V	$V_{DD}$		
Supply Voltage 2	$V_{CC}$	—	—	14.0	—	40.0		$V_{CCL} / R$		
Input Voltage	H Level	$V_{IH}$	—	0.8 $V_{DD}$	—	$V_{DD}$		V	SCP, FR, LP, DIR, DUAL EIO1, EIO2, DI1 to DI8, / DSPOF, TEST, S / C	
	L Level	$V_{IL}$	—	0	—	0.2 $V_{DD}$				
Output Voltage	H Level	$V_{OH}$	$I_{OH} = -0.5$ mA	$V_{DD} - 0.5$	—	$V_{DD}$	V			EIO1, EIO2
	L Level	$V_{OL}$	$I_{OL} = 0.5$ mA	0	—	0.5				
Output Resistance	H Level	$R_{OH}$	$V_{OUT} = V_0 - 0.5$ V (Note 3)	—	0.4	0.8	kΩ	O1 to O240		
	M Level	$R_{OM}$	$V_{OUT} = V_2 \pm 0.5$ V (Note 3)	—	0.4	0.8				
		$R_{OM}$	$V_{OUT} = V_3 \pm 0.5$ V (Note 3)	—	0.4	0.8				
	L Level	$R_{OL}$	$V_{OUT} = V_5 + 0.5$ V (Note 3)	—	0.4	0.8				
Current Consumption (Note 4)	$I_{DD}$	—	$V_{DD} = 5.5$ V, $V_{CC} = 42$ V $f_{FR} = 40$ Hz, $f_{scp} = 8.0$ MHz Input Data: every bit inverted $V_{IH} = 5.5$ V, $V_{IL} = 0$ V (Current consumption while the internal data receiver is operating)	—	—	81.5	mA	$V_{DD}$		
	$I_{DD}^{ST/BY}$	—	Current consumption while the internal data receiver is sleeping	—	—	240	μA	$V_{DD}$		

Note 3:  $V_{CC} = 20$  V, 1 / 13 bias



## AC Electrical Characteristics (Column Mode)



### Test Conditions (1) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 2.7\text{ to }4.5\text{ V}$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Clock Cycle	$t_C$	—	76	—	ns
SCP Pulse Width	$t_{CWL}$ , $t_{CWH}$	—	26	—	
Data Set-up Time	$t_{DSU}$	—	26	—	
Data Hold Time	$t_{DHD}$	—	26	—	
SCP Rise / Fall Time	$t_r$ , $t_f$	—	—	(Note 4)	
LP Rise Time	$t_{LRP}$	—	26	—	
LP Fall Time	$t_{LFP}$	—	26	—	
LP Pulse Width	$t_{LW}$	—	26	—	
SCP to LP Delay Time (SCP → LP)	$t_{SL}$	—	26	—	
LP to SCP Delay Time (LP → SCP)	$t_{LS}$	—	26	—	
EIO IN Rise Time	$t_{EIFP}$	—	26	—	
EIO IN Pulse Width	$t_{EIW}$	—	26	—	
SCP to EIO Delay Time (SCP → EIO)	$t_{SE}$	—	0	—	
EIO OUT Delay Time	$t_{EOD}$	(Note 5)	—	50	

Note 4:  $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r, t_f \leq 50\text{ ns}$

Note 5:  $C_L = 10\text{ pF}$

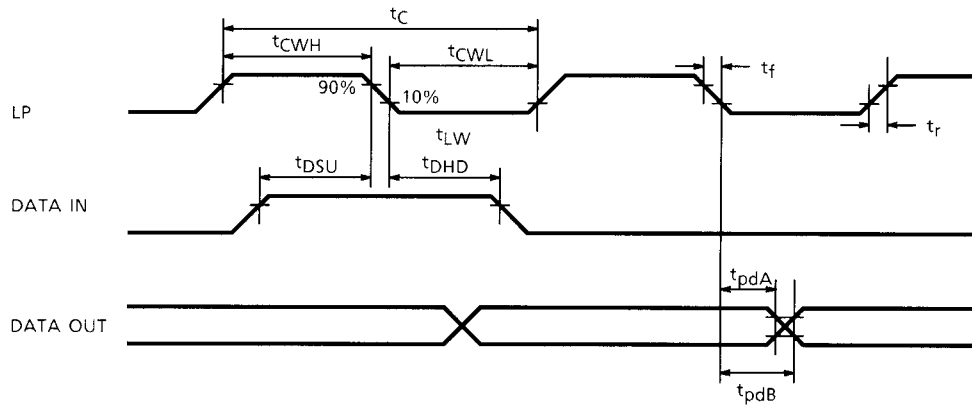
## Test Conditions (2) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 4.5\text{ to }5.5\text{ V}$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Clock Cycle	$t_C$	—	37	—	ns
SCP Pulse Width	$t_{CWH}$ , $t_{CWL}$	—	15	—	
Data Set-up Time	$t_{DSU}$	—	15	—	
Data Hold Time	$t_{DHD}$	—	15	—	
SCP Rise / Fall Time	$t_r$ , $t_f$	—	—	(Note 6)	
LP Rise Time	$t_{LRP}$	—	15	—	
LP Fall Time	$t_{LFP}$	—	15	—	
LP Pulse Width	$t_{LW}$	—	15	—	
SCP to LP Delay Time	$t_{SL}$	—	15	—	
LP to SCP Delay Time	$t_{LS}$	—	15	—	
EIO IN Rise Time	$t_{EIFP}$	—	15	—	
EIO IN Pulse Width	$t_{EIW}$	—	15	—	
SCP to EIO Delay Time	$t_{SE}$	—	0	—	
EIO OUT Delay Time	$t_{EOD}$	(Note 7)	—	25	

Note 6:  $t_r$ ,  $t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r$ ,  $t_f \leq 50\text{ ns}$

Note 7:  $C_L = 10\text{ pF}$

## AC Electrical Characteristics (Row Mode)



### Test Conditions (1) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 2.7\text{ to }4.5\text{ V}$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Clock Cycle	$t_C$	LP	250	—	ns
LP Pulse Width H	$t_{CWH}$	LP	40	—	
LP Pulse Width L	$t_{CWL}$	LP	170	—	
SCP Rise / Fall Time	$t_r, t_f$	LP, FR, EIO1, EIO2, DI8	—	(Note 8)	
Data Set-up Time	$t_{DSU}$	EIO1, EIO2, DI8	100	—	
Data Hold Time	$t_{DHD}$	EIO1, EIO2, DI8	0	—	
EIO OUT Delay Time A (Note 9)	$t_{pdA}$	EIO1, EIO2	40	—	
EIO OUT Delay Time B (Note 9)	$t_{pdB}$	EIO1, EIO2	0	130	

### Test Conditions (2) ( $V_{SS} = 0\text{ V}$ , $V_{DD} = 4.5\text{ to }5.5\text{ V}$ , $V_{CC} = 14\text{ to }42\text{ V}$ , $T_a = -20\text{ to }75^\circ\text{C}$ )

Item	Symbol	Test Condition	Min	Max	Unit
Clock Cycle	$t_C$	LP	150	—	ns
LP Pulse Width H	$t_{CWH}$	LP	20	—	
LP Pulse Width L	$t_{CWL}$	LP	100	—	
SCP Rise / Fall Time	$t_r, t_f$	LP, FR, EIO1, EIO2, DI8	—	(Note 10)	
Data Set-up Time	$t_{DSU}$	EIO1, EIO2, DI8	50	—	
Data Hold Time	$t_{DHD}$	EIO1, EIO2, DI8	0	—	
EIO OUT Delay Time A (Note 11)	$t_{pdA}$	EIO1, EIO2	20	—	
EIO OUT Delay Time B (Note 11)	$t_{pdB}$	EIO1, EIO2	0	100	

Note 8, 10:  $t_r, t_f \leq (t_C - t_{CWH} - t_{CWL}) / 2$  and  $t_r, t_f \leq 50\text{ ns}$

Note 9, 11:  $C_L = 10\text{ pF}$

Note: Insert the bypass capacitor (0.1  $\mu\text{F}$ ) between  $V_{DD}$  and  $V_{SS}$  and between  $V_{CC}$  and  $V_{SS}$  to decrease power supply noise.

Place the bypass capacitor as close to the LSI as possible.