

VastLane HDMI Transmitter PHY

Low-power, dual-mode HDMI™ 1.3 / MHL™ transmitter PHY for high-definition consumer electronics

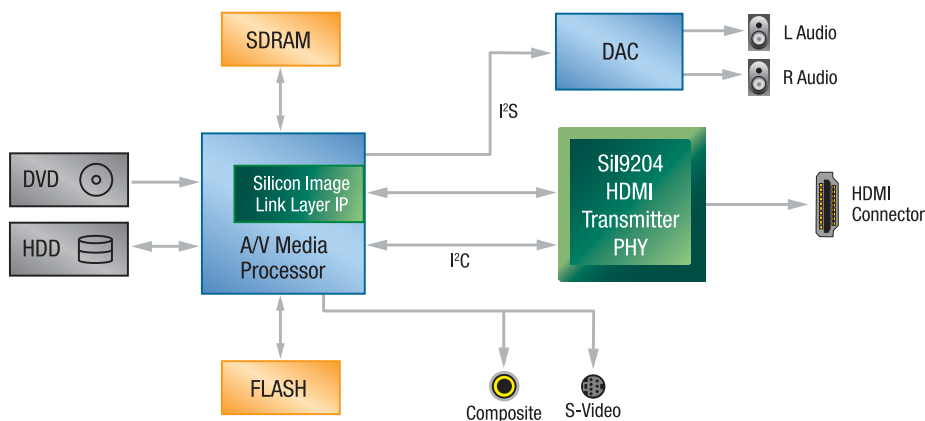
The VastLane™ SiI9204 is a dual-mode HDMI/MHL transmitter PHY designed for home-theater applications, consumer electronics and high-end mobile devices. Together with Silicon Image's digital link layer IP core that is integrated in the device's system-on-a-chip (SoC), the SiI9204 PHY enables SoC suppliers to offer a low-cost yet extremely powerful HDMI solution in a single SoC design. Coupled with a full featured SoC, the SiI9204 can provide support for high-end HDMI 1.3 features such as high bit-rate audio and x.v.Color. With its SiI9002 compatibility mode, the SiI9204 is also attractive for those Silicon Image customers who already combine their SoCs with the SiI9002 PHY.

The SiI9204 PHY simplifies high-speed mixed signal design by resolving many of the design challenges faced by consumer electronics SoC suppliers. The SiI9204 PHY supports a 12-bit dual-edge digital interface to the SoC that reduces SoC I/O requirements. Its integrated Consumer Electronics Control (CEC) significantly reduces the bill-of-materials cost.

The SiI9204 PHY is capable of supporting color depths and resolutions up to 36-bit Deep Color @ 1080p/60.

The SiI9204 transmitter PHY combined with Silicon Image's SoC-integrated link layer IP allows for shorter design cycles, simplified testing and faster compliance versus full transmitter integration. Silicon Image's solution provides benefits of both approaches: lower bill-of-materials cost than discrete transmitter implementations and faster time-to-market and less chip I/O than full transmitter integration into the SoC.

SiI9204 Application Example Diagram: PVR / Blu-ray Disc Player



SiI9204

Applications

- Blu-ray Disc Players and Recorders
- High-Definition Set-Top Boxes
- Personal Video Recorders

Key Features

- Dual-mode HDMI 1.3 and MHL
- Supports Deep Color
- Integrated CEC
- Low Power
- 40-pin 6x6mm QFN package
- SiI9002 compatible



SiI9204 Features

SiI9204 Software & Documentation

Software

- SiI9204 firmware

Documentation

- Datasheet
- Programmer's Reference
- CEC Programming Interface (CPI) Programmer's Reference
- Application Notes

Industry-Standard Compliance

- HDMI 1.3* • DVI 1.0*
- HDCP 1.2* • EIA/CEA-861D*

*With Silicon Image Link Layer IP

Digital Video Output

- Integrated TMDS core:
 - HDMI - 4 differential pairs (1 clock, 3 data)
 - MHL - 2 differential pairs (1 clock, 1 data)
- DTV and PC resolution support:
 - HDMI - up to 1080p/60, UXGA
 - MHL - up to 1080i/60 and 1080p/30, SXGA
- Color depth:
 - HDMI - 24/30/36-bit @1080p/60 (Deep Color)
 - MHL - 24-bit @1080i/60 and 1080p/30

Digital Data Input

- 12-bit dual-edge interface to Silicon Image's digital link layer IP integrated in the SoC
- De-skewing option to adjust data setup and hold time
- Multiplexed control for reduced pin-count
- PLL generated TMDS reference clock to SoC
- SiI9002 compatibility mode

Consumer Electronics Control (CEC)

- Dedicated CEC signal
- Integrated CEC control for universal remote

System Operation

- I²C slave interface for host communication
- Simplified API programming via CEC Programming Interface (CPI)
- Monitor detection through hot plug and receiver detection

Power Management

- Flexible power supply options: 1.8V, 2.5V or 3.3V
- 1.2V core for low-power operation
- Low-power standby mode

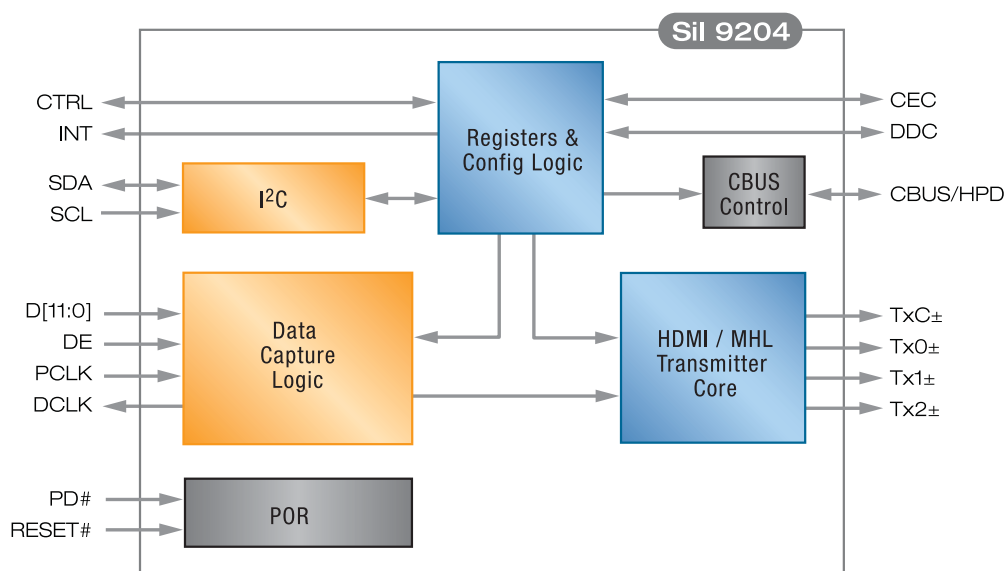
Package

- 40-pin QFN (6mm x 6mm)

Operating Range

- 0C° to +70C° temperature support

SiI9204 Functional Block Diagram



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