PJ4800

30V N-Channel Enhancement Mode MOSFET

FEATURES

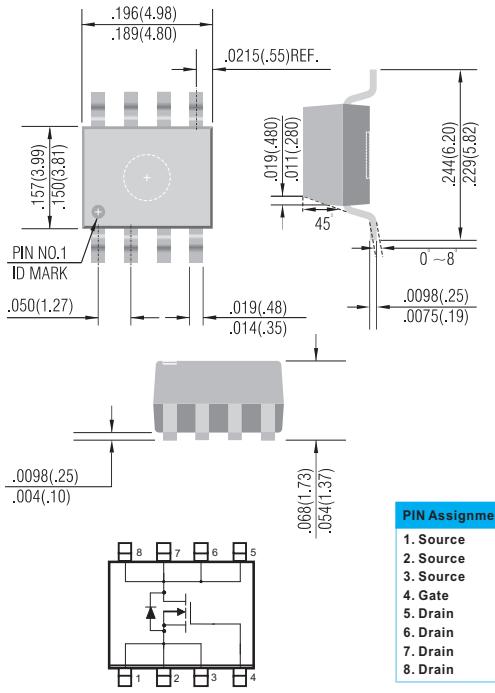
- $R_{DS(ON)}$, V_{GS}@10V,I_{DS}@8A=20mΩ
- $R_{DS(ON)}$, V_{GS}@5.0V,I_{DS}@6A=31mΩ

- Advanced Trench Process Technology
- High Density Cell Design For Ultra Low On-Resistance
- Specially Designed for DC/DC Converters
- Fully Characterized Avalanche Voltage and Current
- Pb free product : 99% Sn above can meet RoHS environment substance directive request

MECHANICALDATA

- Case: SOIC-08 Package
- Terminals : Solderable per MIL-STD-750D,Method 1036.3
- Marking : 4800

SOIC-08 Unit: inch (mm)



Maximum RATINGS and Thermal Characteristics (T_A=25°C unless otherwise noted)

PARAMETER		SYMBOL	VALUE	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continous Drain Current	T_C=25°C	I_D	8	A
Pulsed Drain Current (1)		I_{DM}	32	A
Avalanche Energy L=0.1mH,I_D=8A,V_{DD}=25V		E_{AS}	3.2	mJ
Power Dissipation	T_C=25°C	P_D	3	W
	T_C=75°C		2	
Operating Junction and Stroage Temperature Range		T_J,T_{STG}	-55 to +175	°C
Junction-to-Ambient Thermal Resistance(PCB Mounted)(2)		$R_{\Theta JA}$	50	°C/W

Note: 1. Maximum DC current limited by the package
2. Surface mounted on FR4 board, t ≤ 10 sec

PAN JIT RESERVES THE RIGHT TO IMPROVE PRODUCT DESIGN,FUNCTIONS AND RELIABILITY WITHOUT NOTICE

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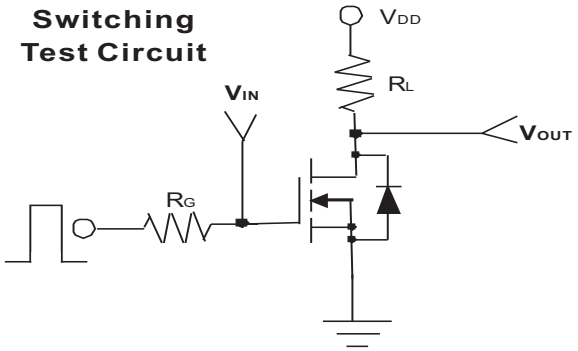
ELECTRICAL CHARACTERISTICS (Tc=25oC,Unless Otherwise Noted)

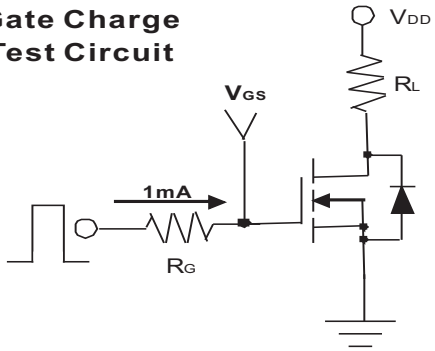
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	30	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250μA	1	-	3	V
Drain-Source On-state Resistance	$R_{DS(ON)}$	V_{GS}=10V,I_D=8A	-	16	20	mΩ
		V_{GS}=5V,I_D=6A	-	23	31	mΩ
Gate-Body Leakage	I_{GSS}	V_{DS}=0V,V_{GS}=±20V	-	-	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V	-	-	1	μA
		V_{DS}=24V,V_{GS}=0V,T_J=125°C	-	-	25	μA
On-State Drain Current	$I_{D(ON)}$	V_{DS}=10V,V_{GS}=10V	8	-	-	A
Forward Transconductance	gfs	V_{DS}=5V,I_D=8A	10	-	-	S
DYNAMIC						
Total Gate Charge	Q_G	V_{DS}=15V,V_{GS}=5V,I_D=8A	-	7.0	-	nC
		V_{DS}=15V,V_{GS}=10V I_D=8A	-	14.2	-	nC
Gate-Source Charge	Q_{GS}		-	1.22	-	nC
Gate-Drain Charge	Q_{GD}		-	3.44	-	nC
Turn-On Delay Time	td(on)	V_{DS}=15V,I_D=1A,V_{GS}=10V R_{GS}=6Ω	-	7.8	-	nS
Rise Time	tr		-	11.6	-	nS
Turn-Off Delay Time	td(off)		-	28.8	-	nS
Fall Time	tf		-	5.6	-	nS
Input Capacitance	C_{ISS}	V_{GS}=0V,V_{DS}=15V f=1MHz	-	520	-	pF
Output Capacitance	C_{OSS}		-	112	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	98	-	pF
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS						
Continuous Current	I_S		-	-	2.3	A
Forward Voltage	V_{SD}	I_F=2.3A,V_{GS}=0V	-	-	1.2	V

NOTE : Plus Test: Pluse Width ≤ 300us, Duty Cycle ≤ 2%.

Switching Test Circuit



Gate Charge Test Circuit



PJ4800

Typical Characteristics Curves (Ta=25℃, unless otherwise noted)

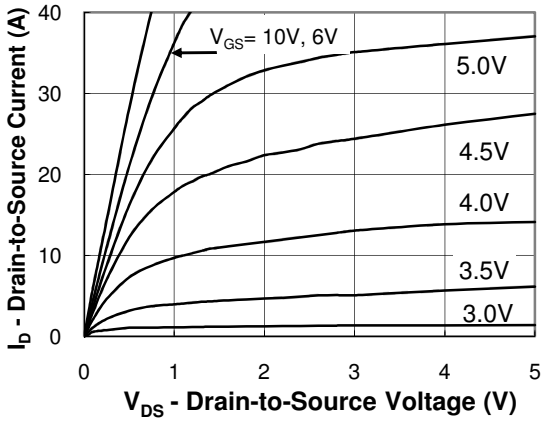


Fig.1 Output Characteristic

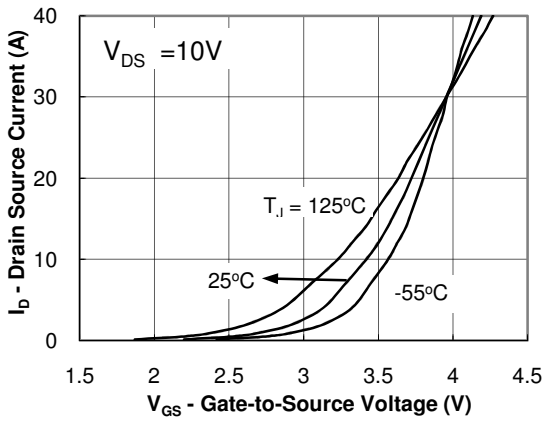


Fig.2 Transfer Characteristic

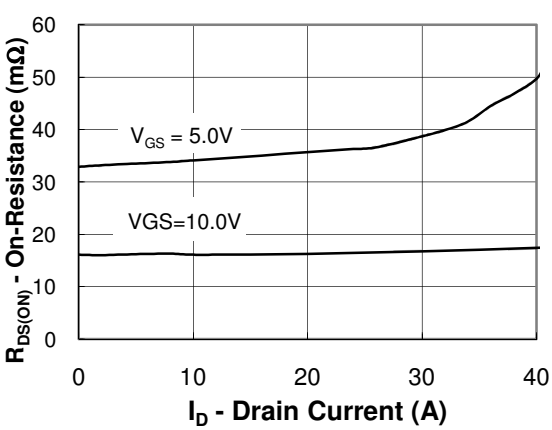


Fig.3 On Resistance vs Drain Current

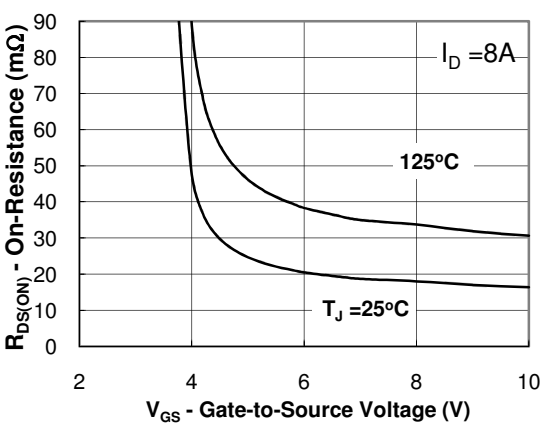


Fig.4 On Resistance vs Gate to Source Voltage

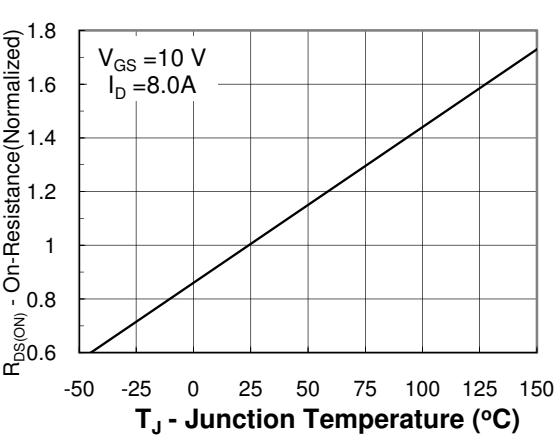


Fig.5 On Resistance vs Junction Temperature

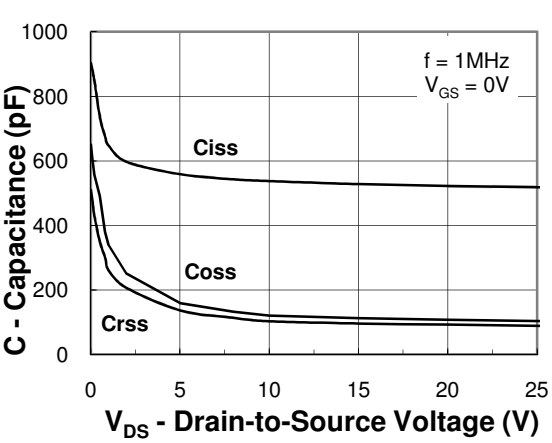


Fig.6 Capacitance

PJ4800

Typical Characteristics Curves (Ta=25℃, unless otherwise noted)

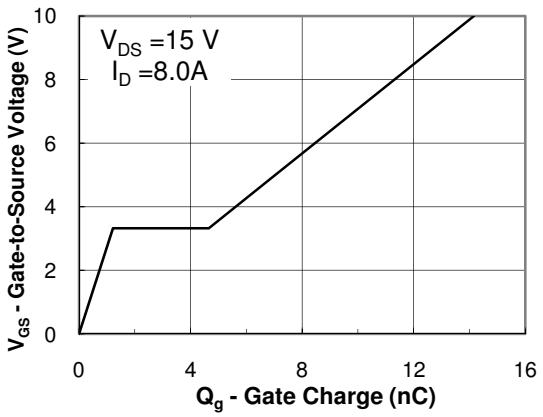


Fig. 7 Gate Charge Waveform

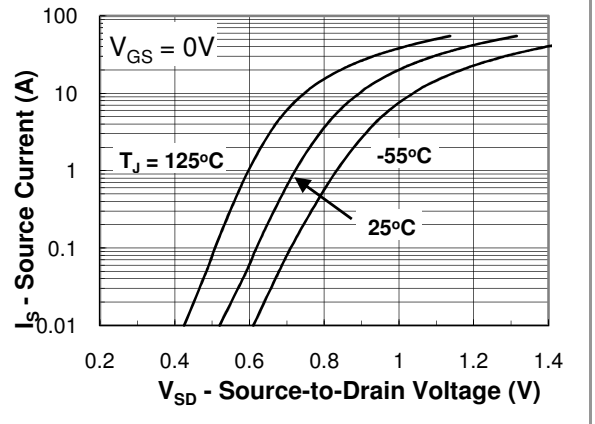


Fig.8 Source-Drain Diode Forward Voltage

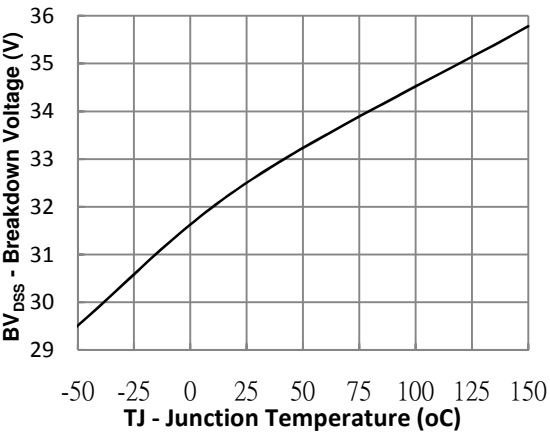


Fig.9 Breakdown Voltage vs Junction Temperature

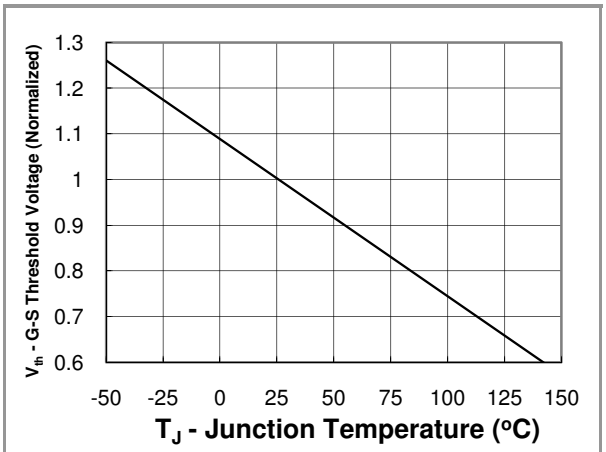
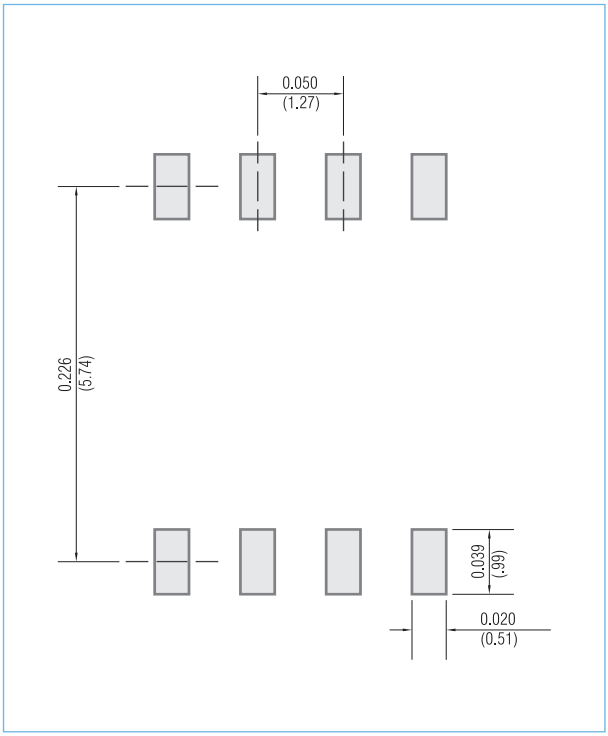


Fig.10 Threshold Voltage vs Junction Temperature

PJ4800

MOUNTING PAD LAYOUT

SOIC-08 Unit: inch (mm)



ORDER INFORMATION

- Packing information

  T/R - 3K per 13" plastic Reel

LEGAL STATEMENT