

M66333FP

FACSIMILE IMAGE DATA PROCESSOR

DESCRIPTION

The M66333 is a facsimile image processing controller that converts analog signals that are photoelectrically converted by an image sensor into bi-level signals.

It has image processing functions such as, peak detection, uniformity correction, γ correction, MTF compensation, detector of background and object level, dither control, separation of image data area, error diffusion, scale down, and area specification.

This controller has a built-in 7bits flash type A-D converter and interface circuits to image sensor, analog signal processing circuit, and CODEC (Coder & Decoder) to simplify control of the readout mechanism.

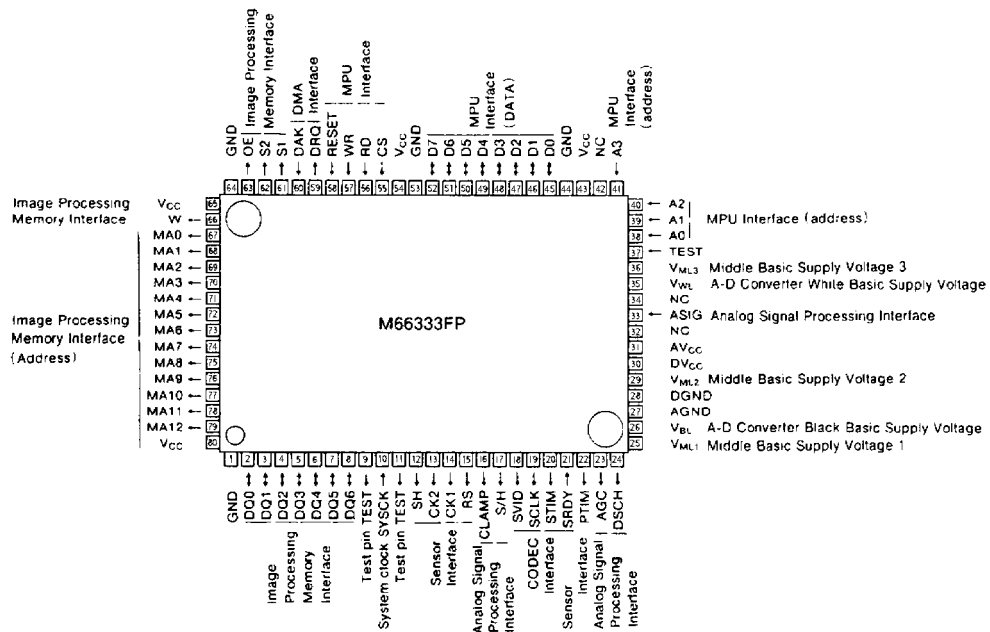
FEATURES

- High Speed Scan..... MAX 2ms/Line, TYP 5ms/Line
- A3 (8pixels/mm) Line Sensor Attachment
- Image sensor (CCD, CIS) control signal generation
 CCD : SH, CK1, CK2, RS
 Contact sensor (CIS) : SH, CK1 (or CK2)
- Analog signal processing circuit control signal generation
 CLAMP, S/H, AGC, DSCH
- Built-in 7bit Flash A-D Converter
- Bi-level data external output interface
 Serial output (→M66330)
 8-bit MPU bus output with external DMA control signal
- Image Data Processing
 Uniformity Correction (All pixel Correction)
 MTF compensation (2 dimension)
 Detector of background and object level (programmable)
 Pseudo half-tone
 - Dither method (32 levels using 4X8 matrix)
 - Error diffusion (6-bit data processing)
 Separation of image data area (2 dimension)
 Scale Down A3→B4, A3→A4, B4→A4
- 5V Single Power Supply

APPLICATION

Facsimile

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N-A

NC : No Connection

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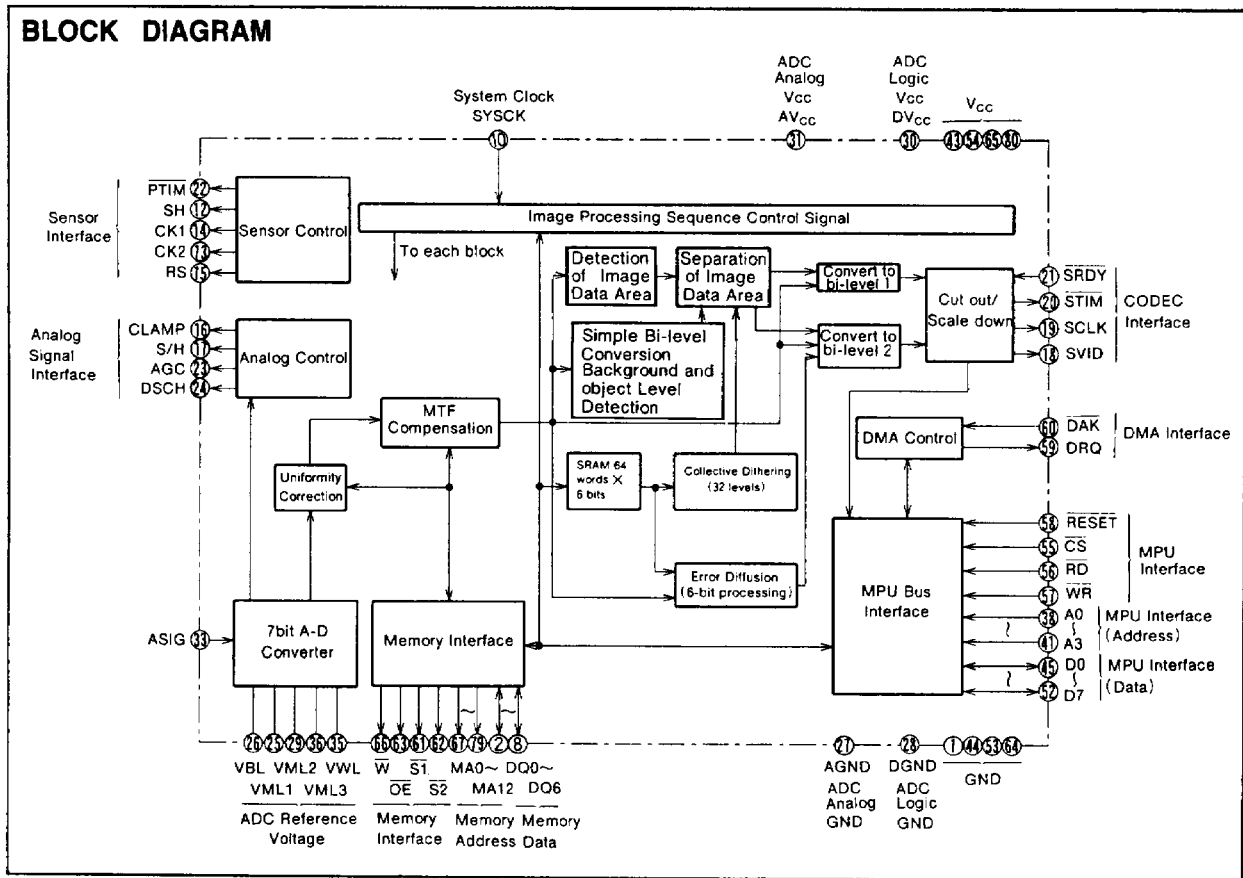


Table 1 Image processing functions

Image Processing Function	Specifications	Remarks
Read Width	• A4, B4, A3	
Resolution	• 8 pixels/mm (primary scanning direction)	
Read speed	• 5ms/line Typ, 2ms/line maximum	• Operated with system clock and PRE_DATA (registers 3, 4)
Uniformity Correction	• White Correction for CCD • White/black Correction for CIS • All pixel correction • Correction range 50%	• External correction memory is used (read/write allowed from MPU)
MTF Compensation	• Laplacian filter circuit before, after, left, and right of target pixel (2 dimension)	• External compensation memory is used
Simple Bi-level Conversion	• Floating threshold method using background and object level detection circuit	
Pseudo half-tone	• Dither method : 32 levels (4X8 matrix)	• Built-in 64 wordsX6 bit SRAM for dither memory (read/write allowed from MPU)
	• Error diffusion : 6-bit data processing (64 levels)	• External error buffer memory is used
Separation of Image Data Area	• Detection by brightness difference of 3X3 pixels in previous, current, and next lines	• Processing memory area is the same as correction memory area
Scale Down	• Selection method • Scale down : A3→B4 set to 13/15, B4→A4 set to 9/11, A3→A4 is set to 12/17	
γ Correction	• Logarithmic correction	• Apply external voltage (resistor connection is also allowed) to A-D converter middle basic supply voltage pins.
Image Sensor Control Signal	• Contact sensor (CIS) and CCD control signal generation	
Analog Signal Processing	• Generate control signals for external CLAMP circuit, sample/hold circuit, and AGC circuit	• Built-in 7-bit flash A-D converter

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PIN DESCRIPTIONS

Block	Pin Names	I/O	Description
Sensor Interface	SH	O	CCD : Shift pulse signal to transmit photo charges from the sensor to the transfer unit. CIS : Start signal for the sensor read circuit.
	CK1	O	CCD : Clock pulse signal for sequentially transmitting the transfer unit signal charge of the sensor. CIS : Clock pulse signal for the sensor read circuit shift register.
	CK2	O	Reverse of CK1.
	RS	O	Pulse to reset the voltage of the CCD sensor floating capacitor to initial status.
	PTIM	O	Read roller pulse motor control signal.
Analog Circuit Interface	CLAMP	O	CLAMP pulse to set the dark level of the sensor to reference voltage of the digital circuit.
	S/H	O	Sample hold signal to smooth out sensor image signal waveform.
	ASIG	I	Analog signal.
	AGC	O	External AGC circuit gain down signal.
	DSCH	O	External AGC circuit gain up signal.
Memory Interface	\overline{W}	O	External RAM write enable signal.
	\overline{OE}	O	External RAM output enable signal.
	$\overline{S1}, \overline{S2}$	O	External RAM, ROM chip select signal.
	MA0~12	O	External RAM, ROM address signals. MA0 is LSB.
	DQ0~DQ6	I/O	External RAM, ROM data bus. DQ0 is LSB and DQ6 is MSB.
CODEC Interface	\overline{SRDY}	I	Data transmission ready signal from CODEC.
	\overline{STIM}	O	Data transmission bound signal for CODEC.
	SCLK	O	Clock signal for transmitting image data to CODEC.
	SVID	O	Serial output of image data to CODEC. "H" : Black, "L" White.
DMA Interface	DRQ	O	DMA request signal to external DMA controller for parallel output of image data through MPU bus.
	DAK	I	DMA acknowledge signal from external DMA controller for the above DRQ signal.
Clock	SYSCK	I	System clock input pin.
MPU Interface	\overline{RESET}	I	System reset signal. Resets counter, register, F/F, latch and sets internal memory in standby mode and halts clock generation circuit.
	\overline{CS}	I	Chip select signal used by MPU to access M66333. Set to "H" in operating mode (AGC, UNIF, SCAN).
	\overline{RD}	I	Control signal used by MPU to read data from M66333.
	\overline{WR}	I	Control signal used by MPU to write data to M66333.
	A0~A3	I	Address signals used to access M66333 internal registers.
	D0~D7	I/O	8-bit bidirectional buffer.

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PIN DESCRIPTIONS (CONTINUED)

Block	Pin Names	I/O	Description
Other	V _{CC}	—	Plus supply voltage.
	AV _{CC}	—	Plus supply voltage for A-D converter analog units.
	DV _{CC}	—	Plus supply voltage for A-D converter logic units.
	GND	—	GND pin.
	AGND	—	Ground for A-D converter analog units.
	DGND	—	Ground for A-D converter digital units.
	V _{WL}	—	A-D converter white basic supply voltage pin.
	V _{BL}	—	A-D converter black basic supply voltage pin.
	V _{ML1}	—	Middle basic supply voltage pin. $V_{ML1} = (V_{WL} - V_{BL}) / 4$.
	V _{ML2}	—	Middle basic supply voltage pin. $V_{ML2} = 2 \cdot (V_{WL} - V_{BL}) / 4$.
	V _{ML3}	—	Middle basic supply voltage pin. $V_{ML3} = 3 \cdot (V_{WL} - V_{BL}) / 4$.
	TEST (IN)	—	Test input pin. Fix to "L".
TEST (OUT)	—	Test output pin. Keep open.	

FUNCTIONAL DESCRIPTION

The following items which are necessary to use the image processing functions of the M66333 are described.

- (1) Operating mode
- (2) Line period and read sequence
- (3) Image processing function
- (4) Sensor unit/analog signal processing unit interface
- (5) CODEC interface
- (6) External memory interface
- (7) Read/write to dither memory and uniformity correction memory
- (8) Image scale down and \overline{PTIM} signal
- (9) Reset
- (10) Image quality control using registers

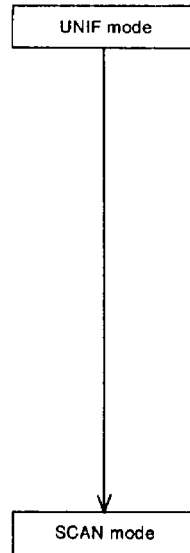
(1) Operating mode

The M66333 performs three basic operations.

- Peak value detection : The peak value of the analog signal output from the recommended analog signal processing circuits shown in Figures 20 to 23 is matched to the white basic supply voltage (V_{WL}) of the M66333 internal A-D converter.
- Uniformity correction data creation : White reference data is created for sensor unit uniformity correction and written to the correction memory.
- Read operation : A document is read and the image is processed to output bi-level data as serial or parallel output.

These three basic operations are performed in the following sequence depending on whether the sensor is CCD or CIS. The sensor is selected with register 0 (SENS).

When the sensor is CCD



Operation is started by setting the UNIF command in register 0 to "H". If the sensor is CCD, peak detection (16 line period) and white uniformity correction data creation (8 line period) are performed consecutively.

To exit this operating mode, wait 30 line periods (at least 24 lines) from the start and set the UNIF command to "L".

The read operation is started by setting the SCAN command in register 0 to "H". Set the SCAN command to "L" to exit this operating mode.

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When the sensor is CIS

(Creation and transmission of uniformity correction data)

AGC mode

Peak detection is performed for 16 line periods when the AGC command in register 0 is set to "H".

To exit this operating mode, wait 20 line periods (at least 16 lines) from the start and set the AGC command to "L".

UNIF mode

This mode is started when the UNIF command in register 0 is set to "H".

When the sensor is CIS, if black correction and white correction are both started with the UNIF command, uniformity correction data creation (8 line period) is started for each correction.

To exit this operating mode, wait 10 line periods (at least 8 lines) from the start and set the UNIF command to "L".

Data transfer

The black and white uniformity correction data created in UNIF mode are transferred to the back-up memory.

(Read operation)

AGC mode

Peak detection is performed for 16 line periods when the AGC command in register 0 is set to "H".

To exit this operating mode, wait 20 line periods (at least 16 lines) from the start and set the AGC command to "L".

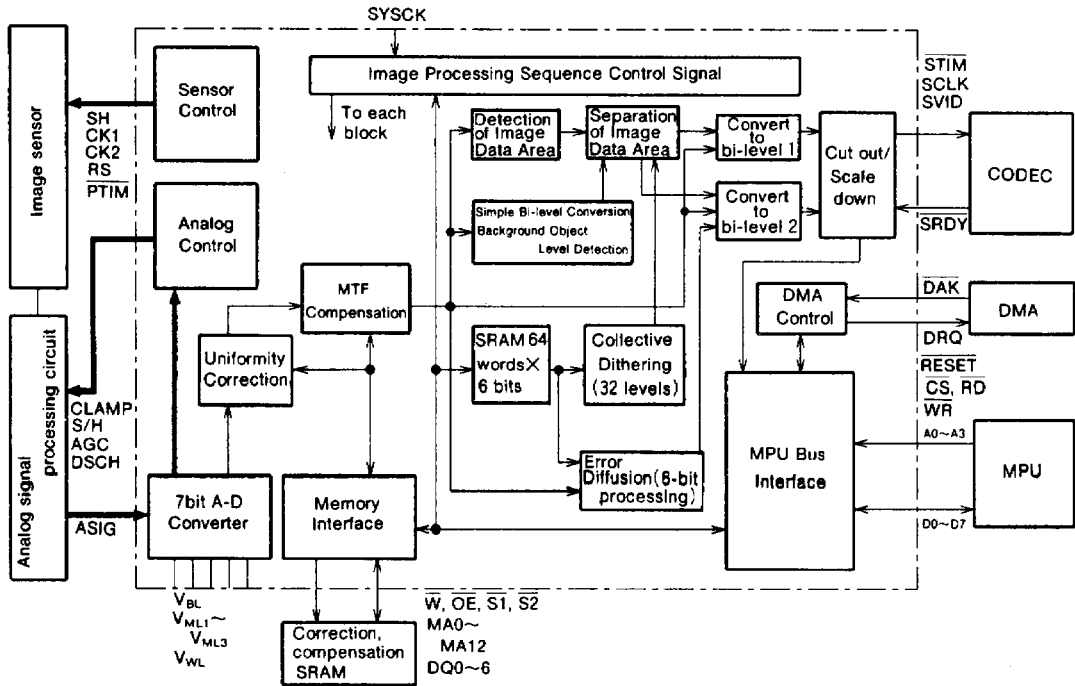
SCAN mode

The read operation is started by setting the SCAN command in register 0 to "H". Set the SCAN command to "L" to exit this operating mode.

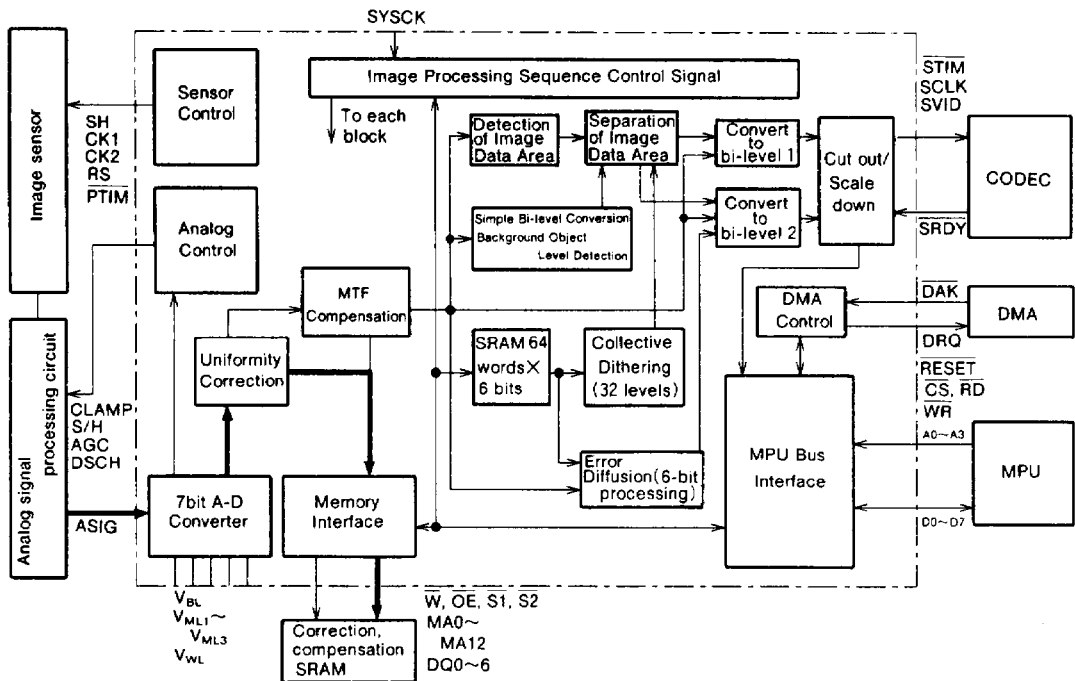
The signal functions and data flow in each mode are shown on pages 4-167 and 4-168. Flowcharts are shown on pages 4-207 to 4-209.

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Operation During Peak Detection

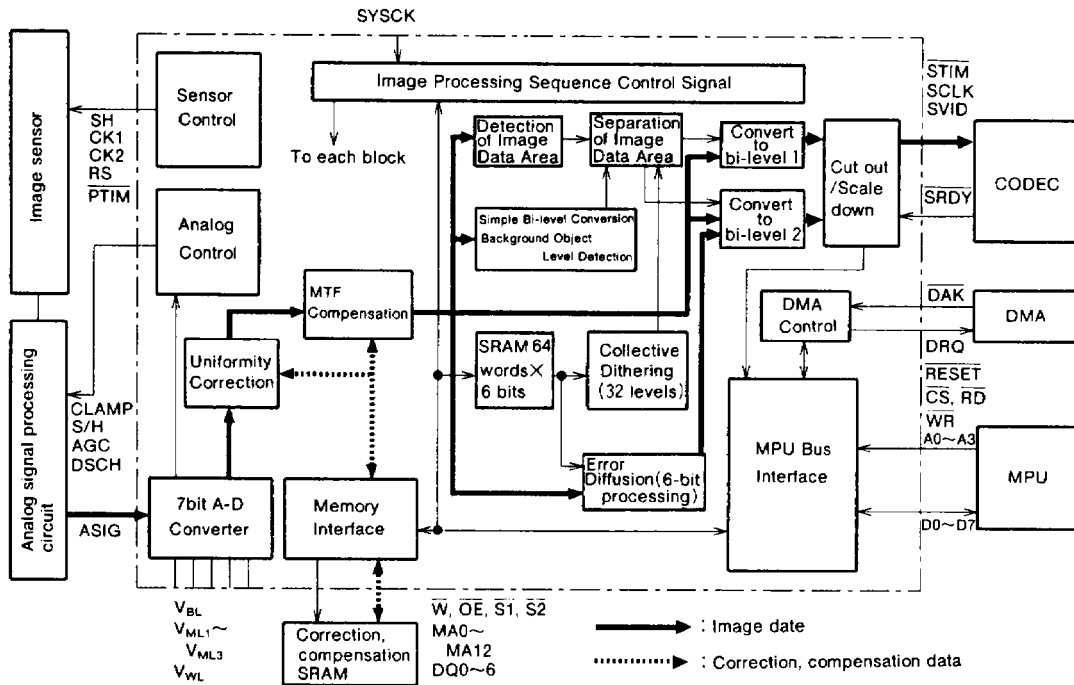


Operation During Peak Detection

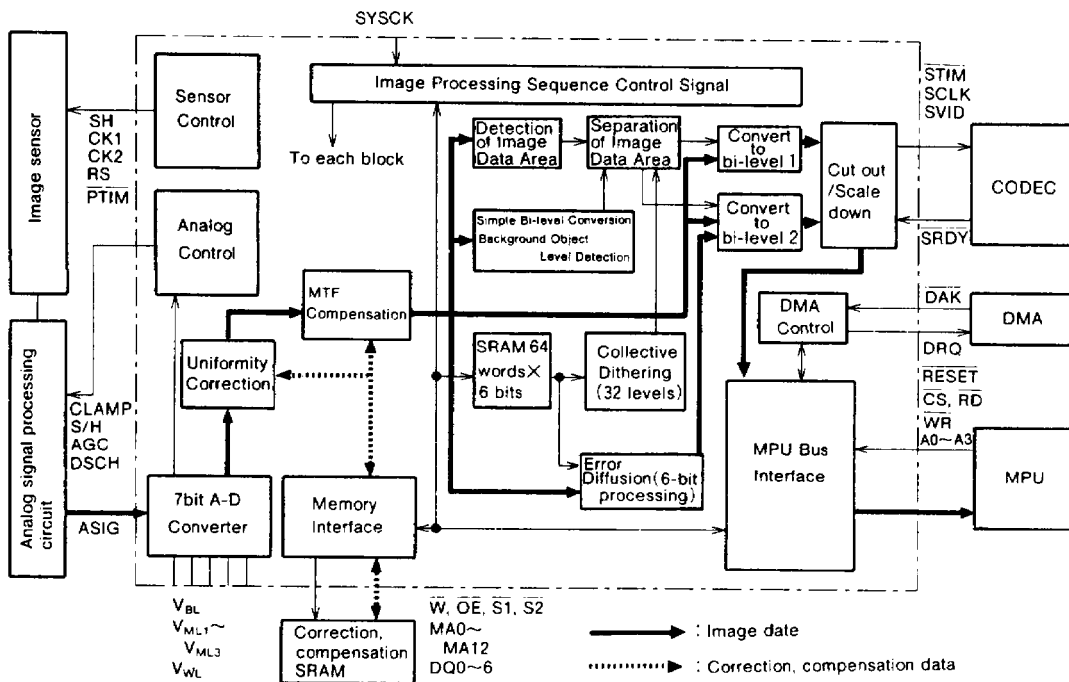


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Data Flow During Read Operation (for serial output)



Data Flow During Read Operation (for parallel output)



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(2) Line period and read sequence

Figure 1 shows the relationship between the M66333 line period and the read sequence.

Figure 2 shows the relationship between the CODEC interface and the read sequence.

- 1 line period (1/ACCK) : Defines the processing time per line for M66333. The line period is determined from the line period counter registers 3 and 4 (PRE_DATA) and pixel transmission clock (ADCK). ADCK is 1/16th of SYSCK.

1 line period (1/ACCK) [NS]

=line period counter X pixel transmission clock period [NS]

=(PRE_DATA+1) X 1/ADCK [NS]

=(PRE_DATA+1) X 16/SYSCK [NS]

The line period counter is counted down with the pixel transmission clock after after loading the PRE_DATA value and generates the following addresses.

- Sensor start pulse (SH) : Image sensor start pulse. The position of the start pulse is determined by the value in register 5 (ST_PL) which is the offset from the uniformity correction range (UNIFG). Set ST_PL to the following values according to the type of image sensor.
 CCD : ST_PL = sensor dummy pixel + 2
 CIS : ST_PL = 2

- Uniformity correction range (UNIFG) : Defines the uniformity correction range. This range corresponds to the sensor width (A3 to A4). Refer to Table 2 for the relationship between sensor width and uniformity correction range.
- AGC range (AGCG) : Defines the peak detection range. This range corresponds to the sensor width (A3 to A4). Auto gain control is performed for the entire width (solid line) of the sensor in AGC mode and for the range inside the sensor width (dotted line) in SCAN mode. Refer to Table 2 for the relationship between sensor width and AGC range.
- Source document read width : Defines the source document read width. If the document width is less than the sensor width, the document should be centered on the sensor because the read range is set from the center of the sensor. Refer to Table 3 for the relationship between sensor width and source document read width.
- Pulse motor control signal (PTIM) : Generates the pulse motor control signals for the read roller.

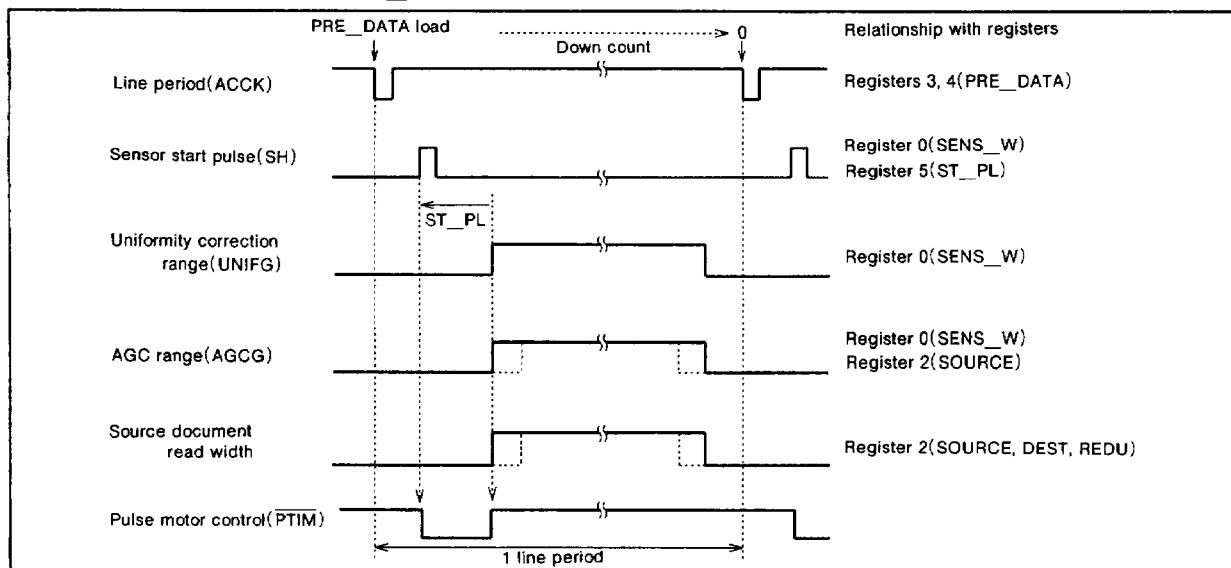


Fig. 1 Line period and read sequence

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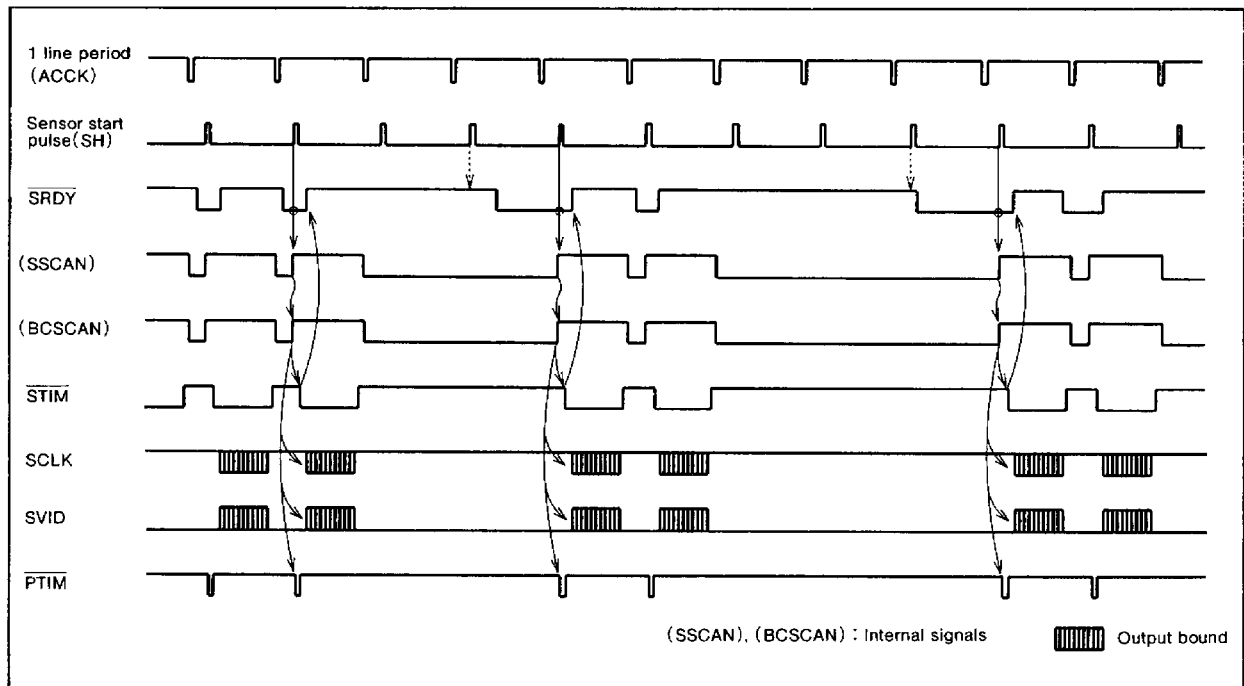


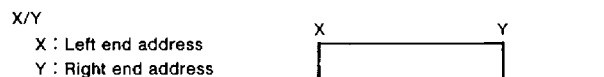
Fig. 2 CODEC Interface and read sequence

Table 2 Sensor width and gate signal range

Gate signal		Sensor width		
		A3	B4	A4
Uniformity correction range (UNIFG)		2487/55	2279/231	2119/391
AGC range (AGCG)	AGC mode	2487/55	2279/231	2119/391
	SCAN mode	2370/162	2194/306	1760/740

Table 3 Source document read width according to sensor width and source document size

Source document size		Sensor width		
		A3	B4	A4
A3		2487/55	—	—
B4		2278/230	2278/230	—
A4		2118/390	2118/390	2118/390



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(3) Image processing function

The M66333 converts image signals from the image sensor to bi-level signals. Bi-level conversion can be either simple bi-level conversion or pseudo half-tone conversion which converts image shades into bi-levels.

The signal output from the image sensor must be corrected and compensated to reduce distortion and degradation before it can be converted to bi-level signals.

Furthermore, separation of image data area must be performed to reduce transmission time and perform optimum bi-level conversion.

The functions necessary for image processing are described below.

- Peak detection
- Uniformity correction
- γ correction
- MTF compensation
- Background and object level detection (simple bi-level conversion)
- Pseudo half-tone Dither method
- Error diffusion
- Separation of image data area
- Image scale down/area specification

● Peak detection

The A-D converter of the M66333 is used with its reference voltages (V_{WL} , V_{BL}) fixed. Normally, V_{WL} is set to V_{CC} and V_{BL} is set to 0V to keep the dynamic range of the A-D converter wide. Peak detection must be performed for analog signals to match them with the full scale value of the A-D converter before they are input to the A-D converter. Figures 19 to 22 show examples of analog signal processing circuits.

Peak detection is performed by reading white data in AGC mode (one of the three M66333 operating modes).

In AGC mode, 8 line period worth of DSCH signal to raise gain and 16 line period worth of AGC signal to lower gain are generated after AGC command start (register 0 : AGC) as shown in Figure 3.

This changes the gain as shown in Figure 4 .

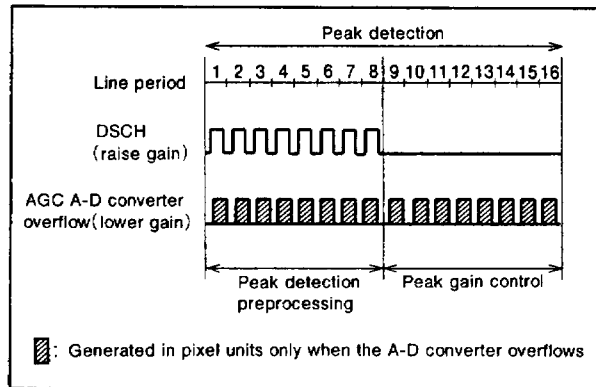


Fig. 3 Peak detection

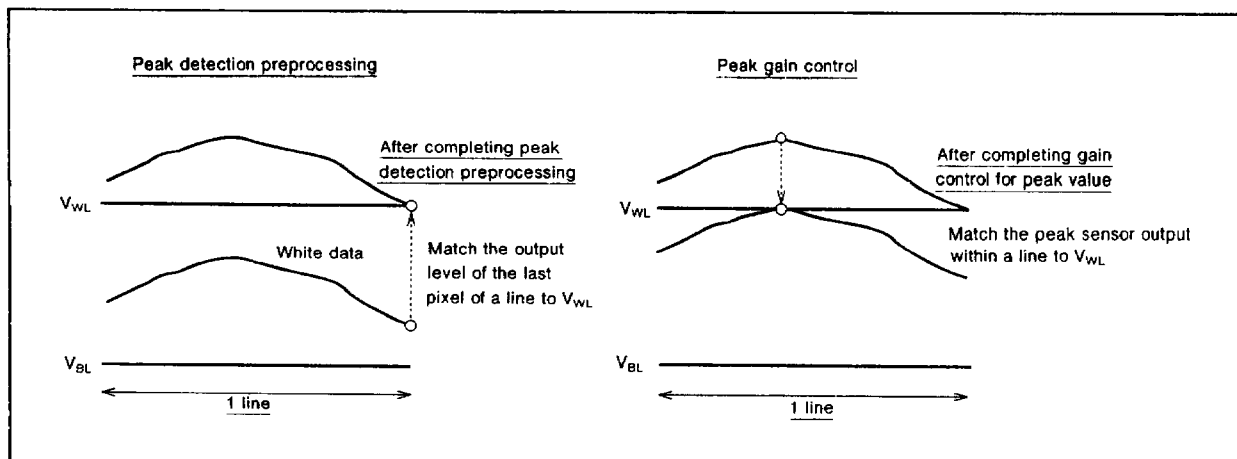


Fig. 4 Change in gain during peak detection

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● Uniformity correction

Uniformity correction corrects the drop in lighting level at both ends of the light source, shading distortion due to drop in lighting level at the rim of the lens, and high frequency distortion caused by the scattering of pixel-unit image sensor characteristic (see Figure 5).

The M66333 creates uniformity correction data in UNIF mode (one of the three operating modes) and writes it to an external correction memory.

In SCAN mode, the correction data is read from the external correction memory to successively correct the input image data in pixel units.

As shown in Table 4, either white correction only, or both white correction and black correction can be selected.

This selection is made with register 0 (SENS, UMODE) and register 1 (UNIFM).

When performing both black correction and white correction, black correction must be performed first.

The M66333 performs entire pixel correction for 50% correction range as shown in Figure 6.

Correction is not possible if the white correction data exceeds the 50% correction range as shown in Figure 6. Therefore, be sure to keep the input signal within the correction range.

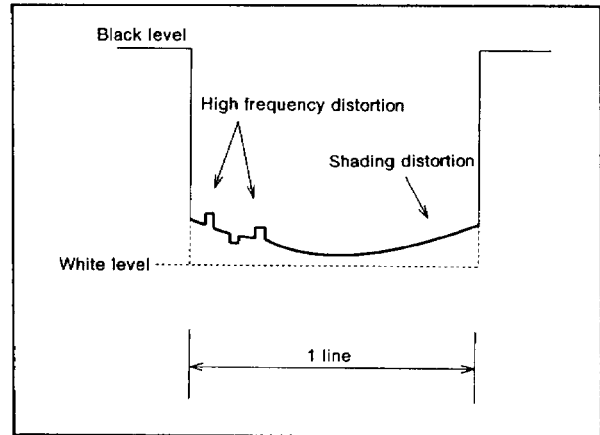


Fig. 5 Image sensor white data output waveform

Table 4 Image sensor uniformity correction

Image Sensor	Correction	Register		
		Sensor Type Register 0 (SENS)	Uniformity Correction Data Creation Register 0 (UMODE)	Correction Mode Selection During SCAN Register 1 (UNIFM)
CCD	White Correction	0	1	—
CIS	White Correction	1	1	0
	Black Correction White Correction	1	Black Correction : 1 White Correction : 0	1

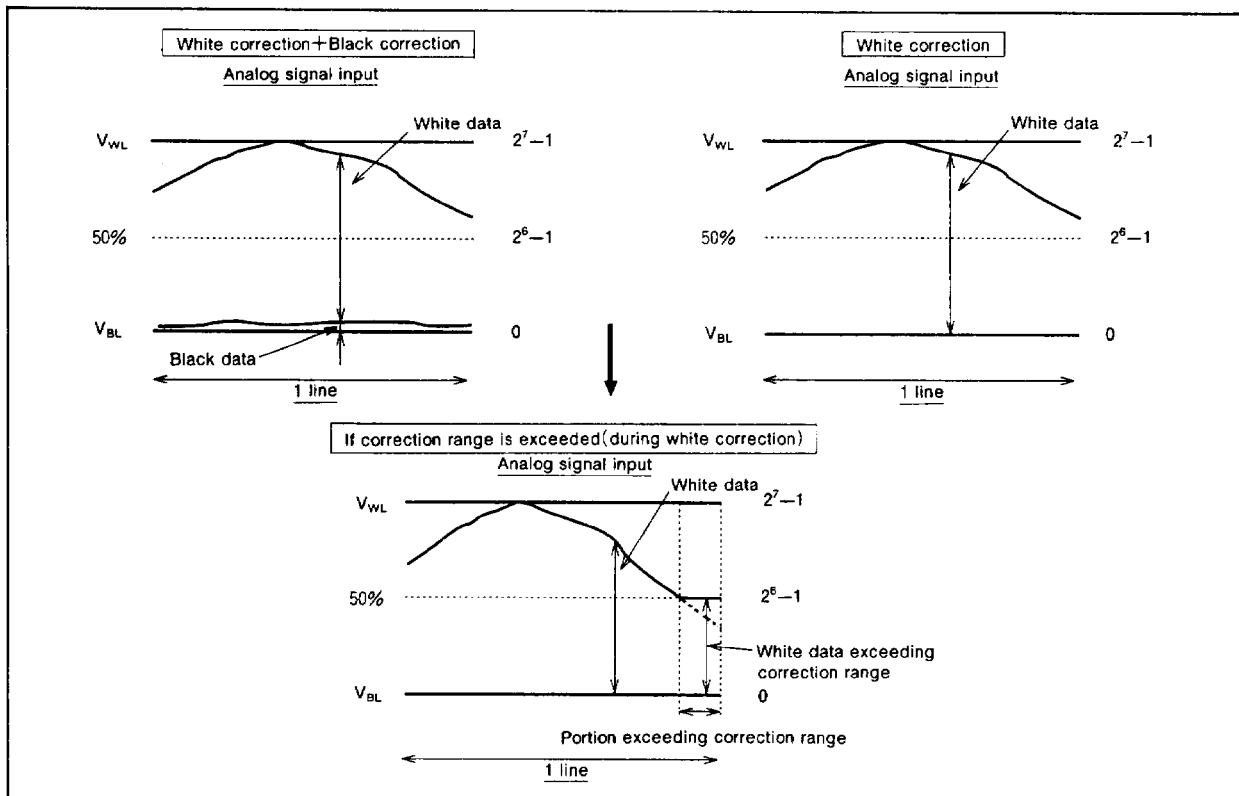


Fig. 6 Uniformity correction

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● γ correction

γ correction is performed to simulate the sensitivity characteristics of the human eye in order to make the image data more similar to natural image.

The M66333 performs γ correction by externally applying voltage to the middle basic supply voltage pins (V_{ML1} , V_{ML2} , V_{ML3}) of the A-D converter.

$\gamma = 0.45$ is said to be the optimum γ correction when using a thermal head printer. Figure 7 shows an example of the characteristic when $\gamma = 0.45$. γ correction approximating $\gamma = 0.45$ can be realized by applying $V_{ML1} = 0.31V$, $V_{ML2} = 1.25V$, and $V_{ML3} = 2.50V$ to the middle basic supply voltage

pins of the A-D converter.

γ correction using the middle basic supply voltage pins is performed during error diffusion. γ correction by dither method should be performed using the value to be written in the dither matrix. Refer to the section on dither method for details.

Figure 24 shows an example of a circuit to apply voltage to the middle basic supply voltage pins. This circuit can be used to choose whether to perform γ correction or not according to the operating mode and to perform repeatable bi-level conversion.

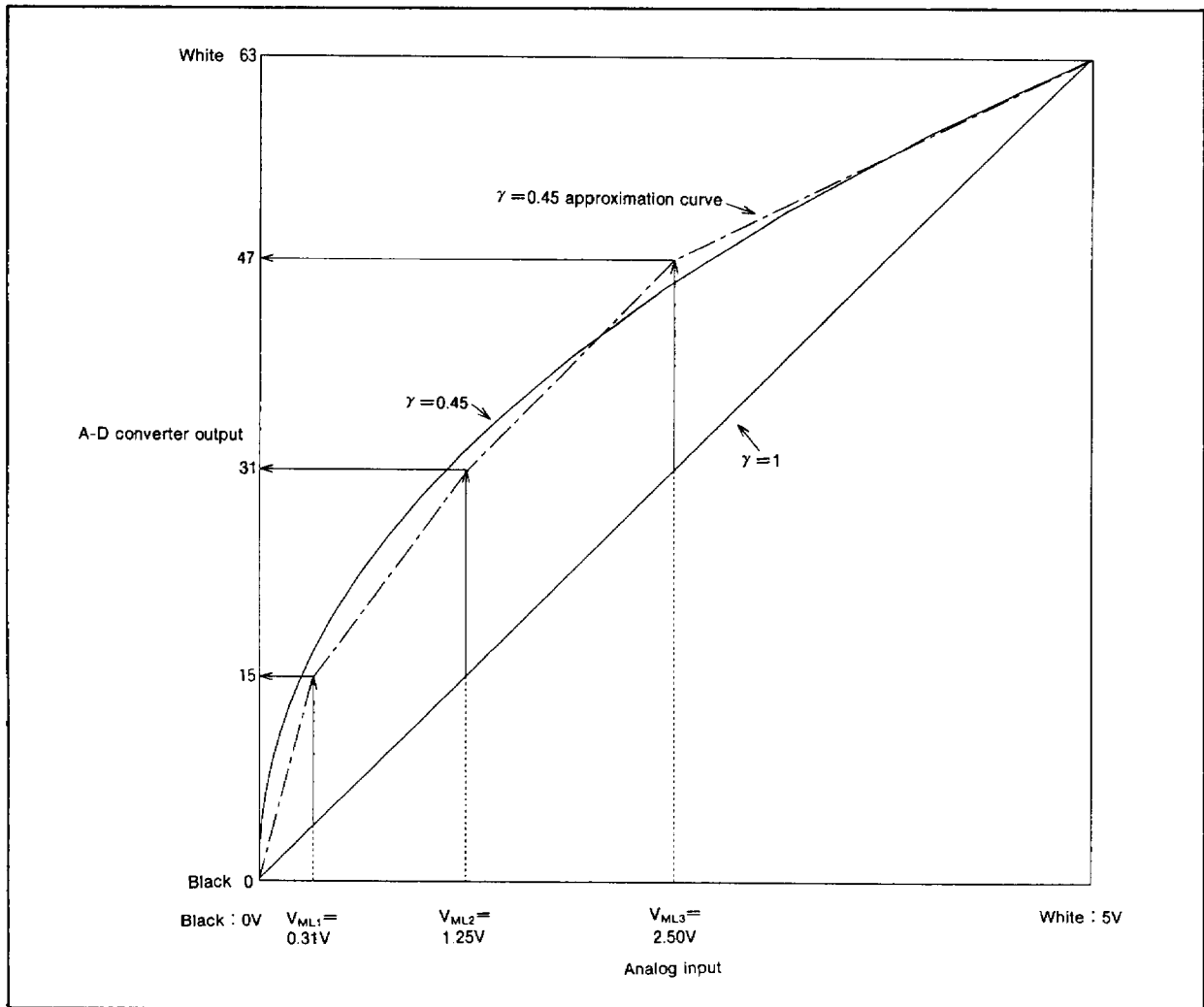


Fig. 7 Example of middle basic supply voltage during γ correction

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● MTF compensation

As shown in Figure 8, characters and photos that have been photoelectrically converted by the sensor unit are characterized by a drop in resolution. The MTF compensa-

tion performed by the M66333 enhances the high-frequency components with a Laplacian filter to maintain the resolution of the image data and creates a perception of increased dynamic range.

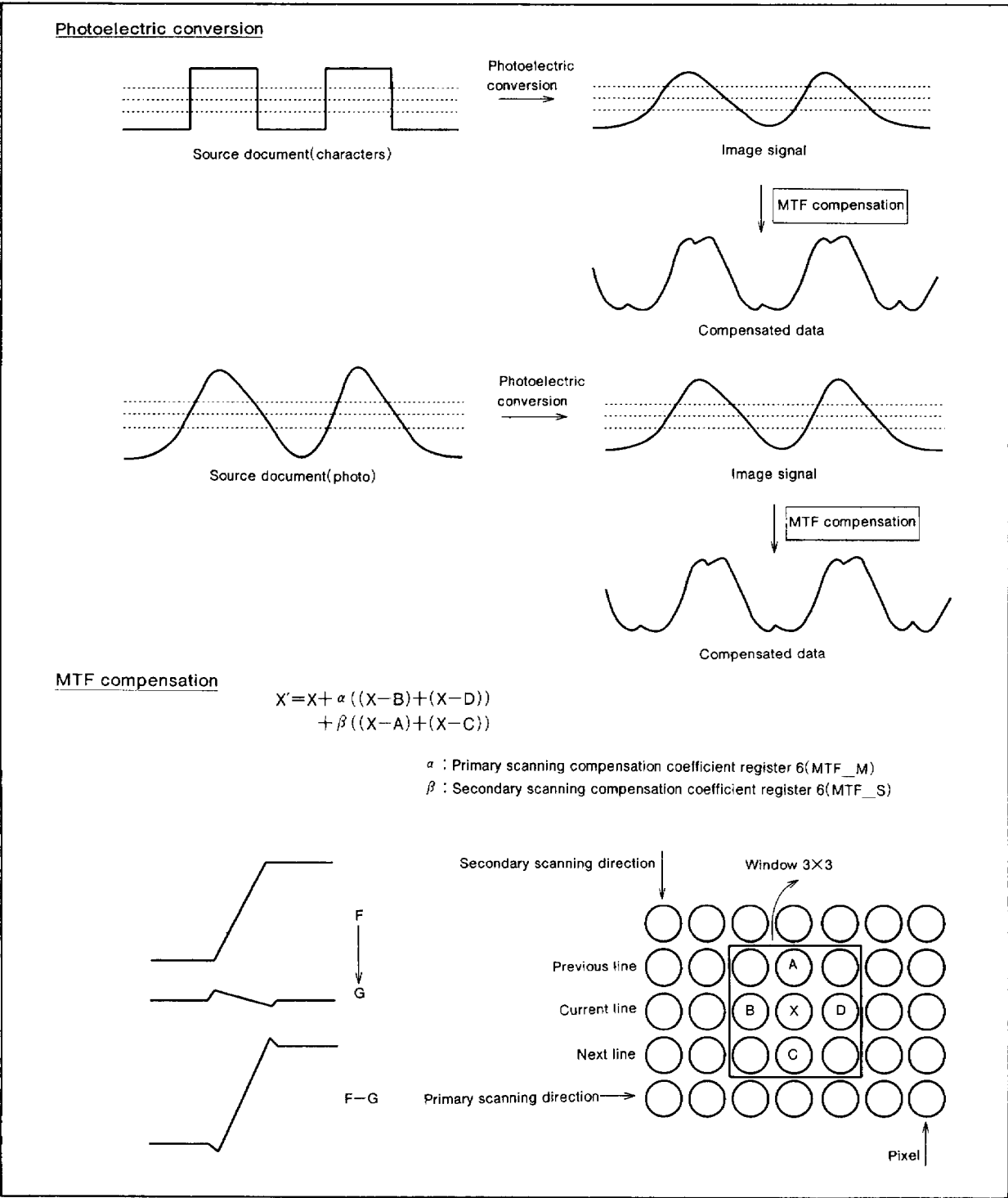


Fig. 8 MTF Compensation

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● Background and object level detection

The M66333 uses the floating threshold method rather than the fixed threshold method. This method successively generates a threshold for optimum simple bi-level conversion of the target pixel.

Therefore, a threshold matching the picture data is generated without modifying the image data.

This value is used as the threshold of the bi-level area when simple bi-level conversion or image separation is selected as bi-level conversion mode.

: register 6 (MODE)

Background level counter

If an image data greater (brighter) than the current counter value is input, this counter is incremented to approach the image data.

If an image data less (darker) than the current counter value is input, this counter is decremented to approach the image data.

The count up/down speed can be set with the following

register.

: register B (MAX_UP, MAX_DOWN)

The lower limit of the background level can be set with the following register.

: register D (LL_MAX)

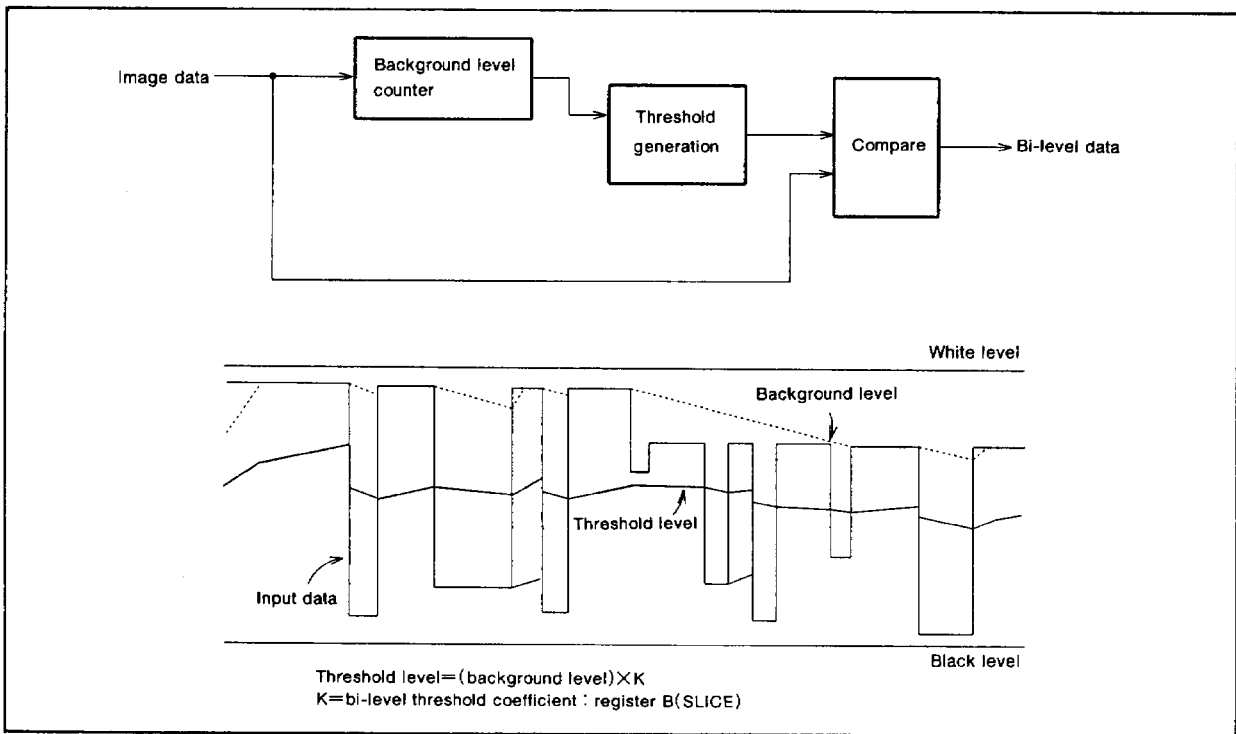


Fig. 9 Background-object level

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● **Dither method**

The M66333 has a built-in 64 words×6 bit SRAM which is used as a collective dithering memory. During initialization, the dither matrix size is set and then the threshold matching the desired dither pattern is written in the dither memory.

- : register 6 (DITH)
- : register E (DITH_D)

Figure 10 shows some examples of dither patterns. Refer to the section on dither memory and uniformity correction memory write/read for details on how to write/read

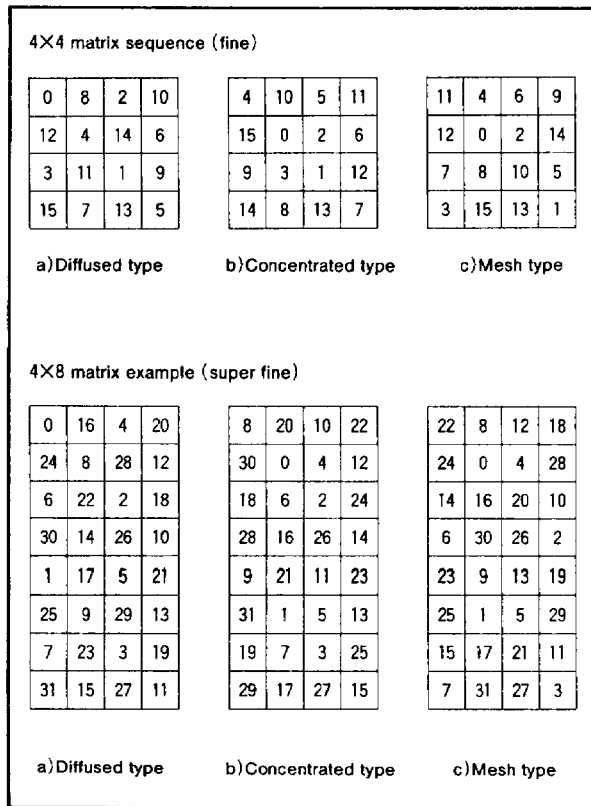


Fig. 10 Collective dithered pattern

If dither method is used to perform pseudo half-tone, γ correction with the middle basic supply voltage pin of the A-D converter is not used. Instead, the γ characteristic is ap-

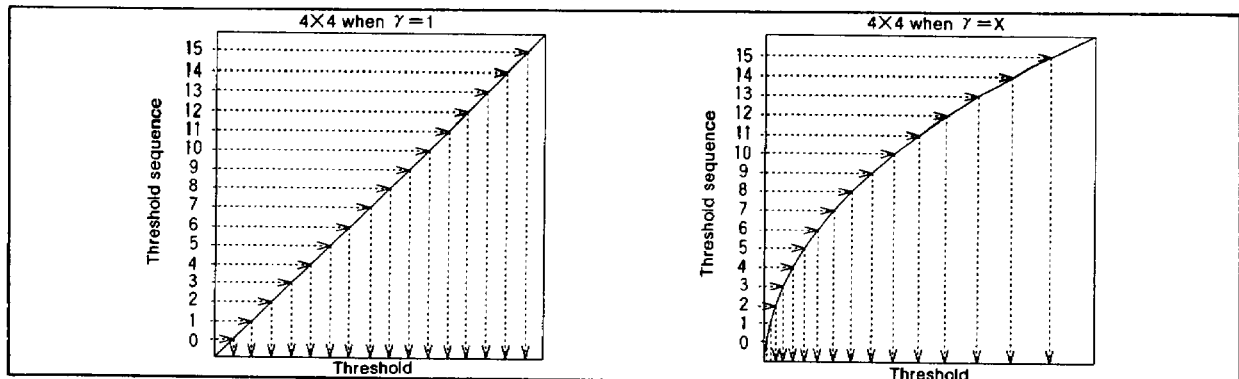


Fig. 12 γ Correction using dither matrix

plied to the dither memory.

This is used when dither method, image data area separation, or error diffusion (see section on error diffusion) is selected for bi-level conversion mode during read. : register 6 (MODE)

The matrix size shown in Table 5 is selected for the dither matrix depending on whether the scanning line density is fine or super fine. If the matrix size 8×8 is selected for super fine, the 4×8 dither pattern shown in Figure 11 is repeated.

Table 5 Scanning line density and dither matrix size

Scanning Line Density	Primary/Secondary Scanning Line (lines/mm)	Level	Matrix Size
Normal	8×3.85	—	—
Fine	8×7.7	16	4×4
Super Fine	8×15.4	32	4×8, 8×8

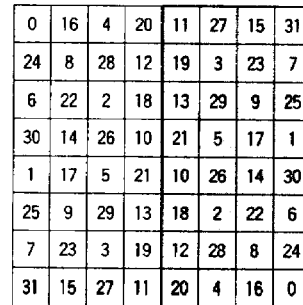


Fig. 11 8×8 Matrix dither pattern example (diffused type)

plied to the threshold value to be written in the dither matrix to perform γ correction. This method is shown in Figure 12.

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● Error diffusion

Error diffusion method, which is a type of conditional identification method, locally diffuses the density error between the source and the result to obtain a close approximation. This produces pictures with balanced gradation and resolution. This is performed by selecting error diffusion during bi-

level conversion mode selection. : register 6 (MODE)

Error diffusion adds dither in addition to image data density error. In this case, the dither matrix data is shared. : register 7 (ERROR)

γ correction must be performed when performing error diffusion.

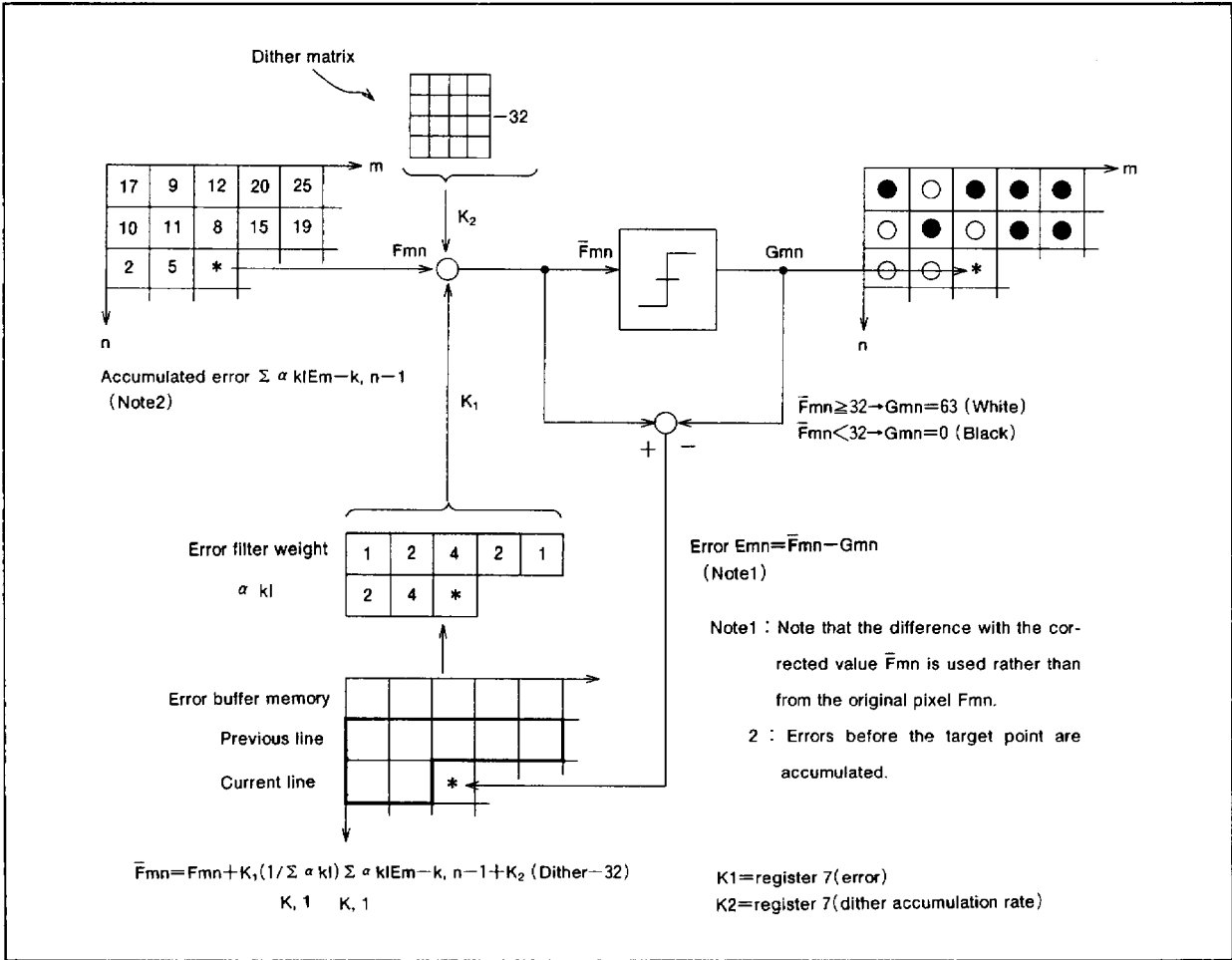


Fig. 13 Error diffusion method

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● Separation of image data area

In order to perform bi-level conversion appropriate for the image, a black and white image is separated into bi-level conversion area and gradation conversion area. Simple bi-

level conversion is applied to the bi-level conversion area and dither method is applied to the gradation area.

: register 2 (MODE)

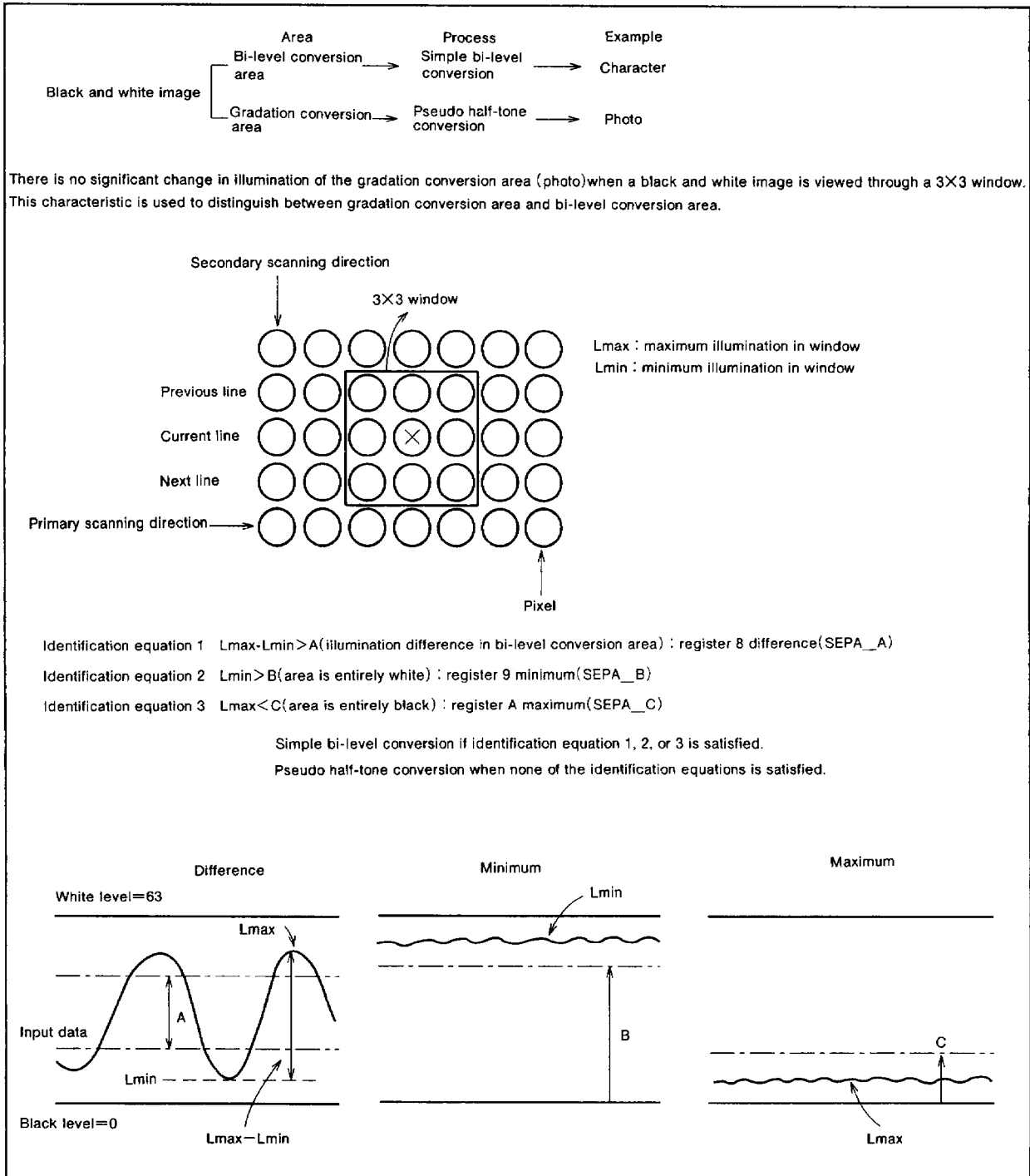


Fig. 14 Separation of image data area

● Image scale down/area specification

Scale down function

The image data input from the analog signal processing circuit can be scaled down (A3 → B4, A3 → A4, B4 → A4) by leaving out pixels in the primary scanning direction for bi-level conversion. : register 2 (SOURCE, DEST, REDU)

Scale down in secondary scanning direction can be performed either by controlling the read roller pulse motor according to the PTIM signal (with scaling) or by leaving it up to the MPU (without scaling) . : register C (REDM)

With scaling in secondary scanning direction : The image data to be left out is read by the M66333, but is not output.

Without scaling in secondary scanning direction : No image data is left out in the secondary scanning direction. Leave the PTIM pin open.

Table 6 Scaling rate

OUT \ IN	A3	B4	A4
B4	13/15	1	—
A4	12/17	9/11	1

Area specification function

When area specification is selected, bi-level conversion is performed only in the specified area from the center of the source document. : register 2 (SOURCE, DEST, REDU)

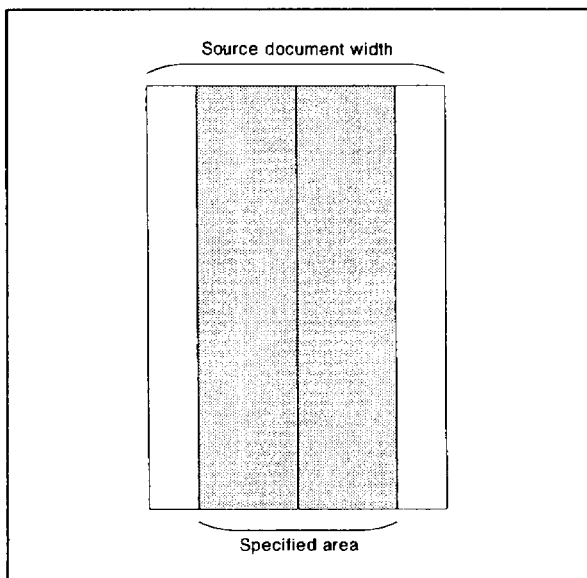
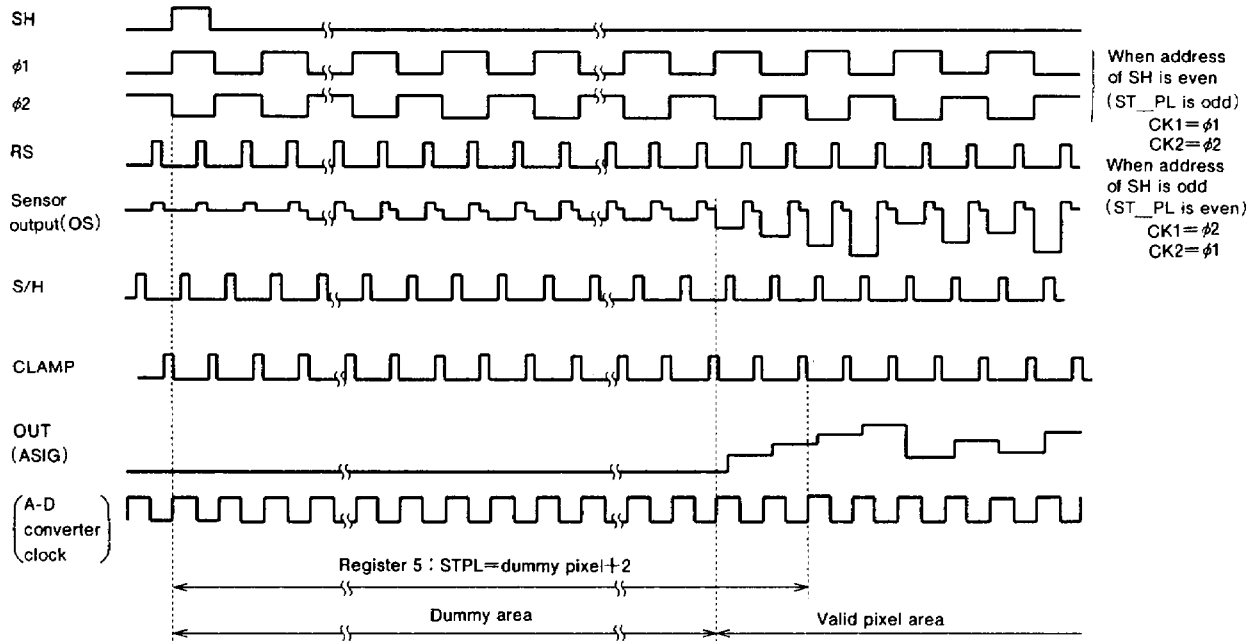


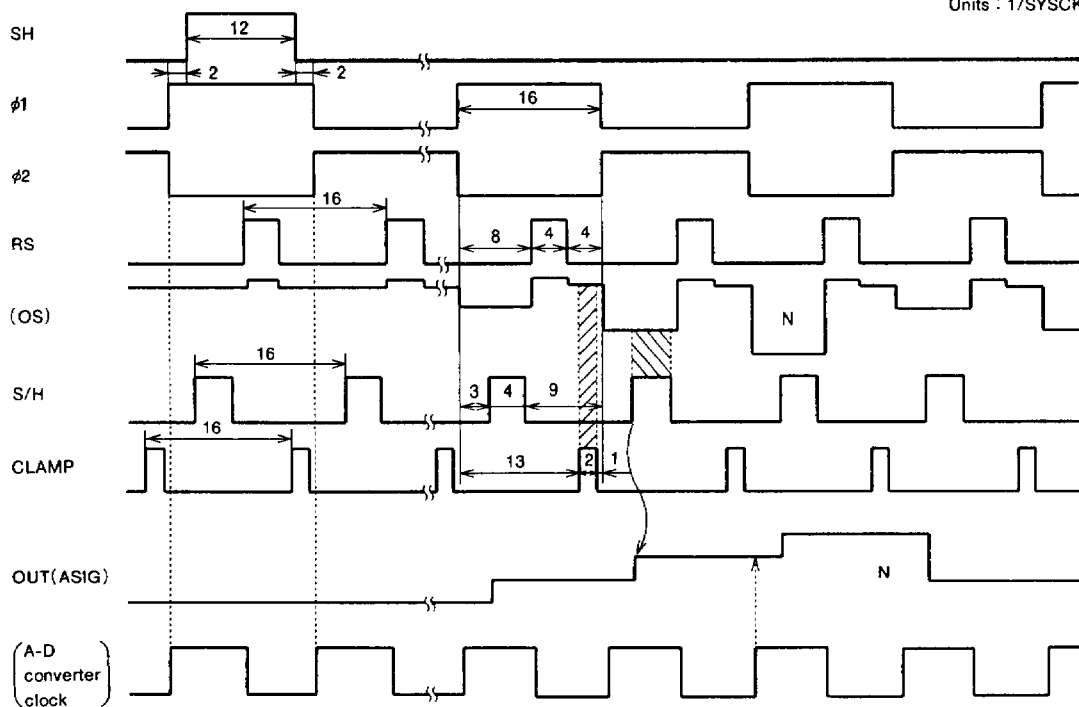
Fig. 15 Cut out function

(4) Sensor unit/analog signal processing unit interface

CCD-bit clamp type

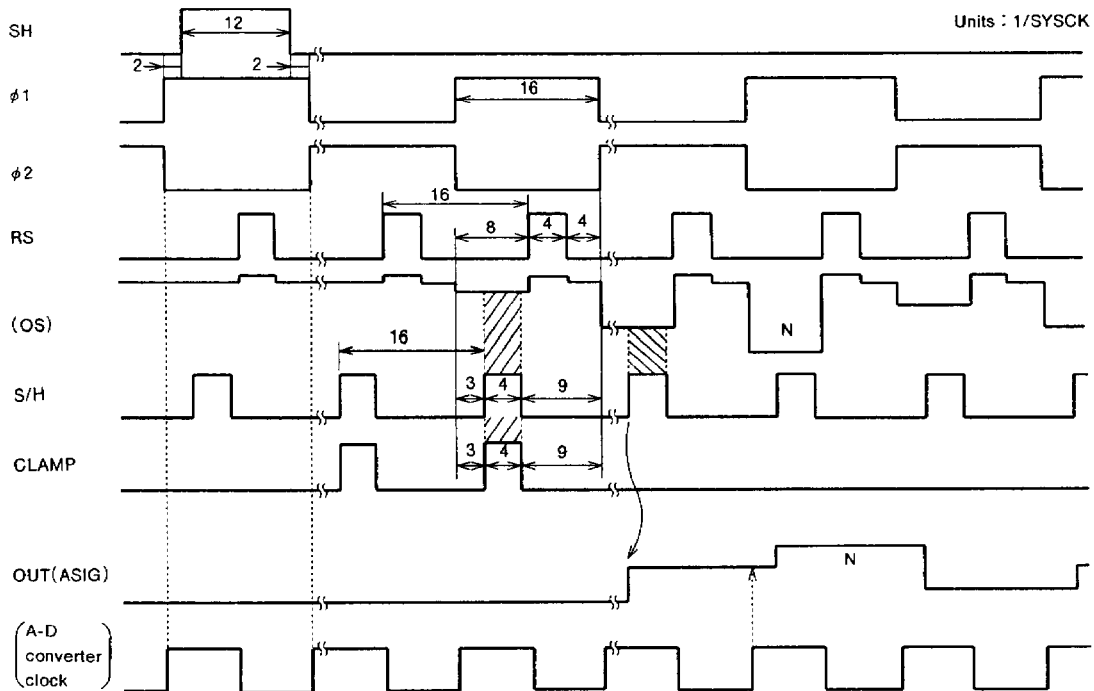
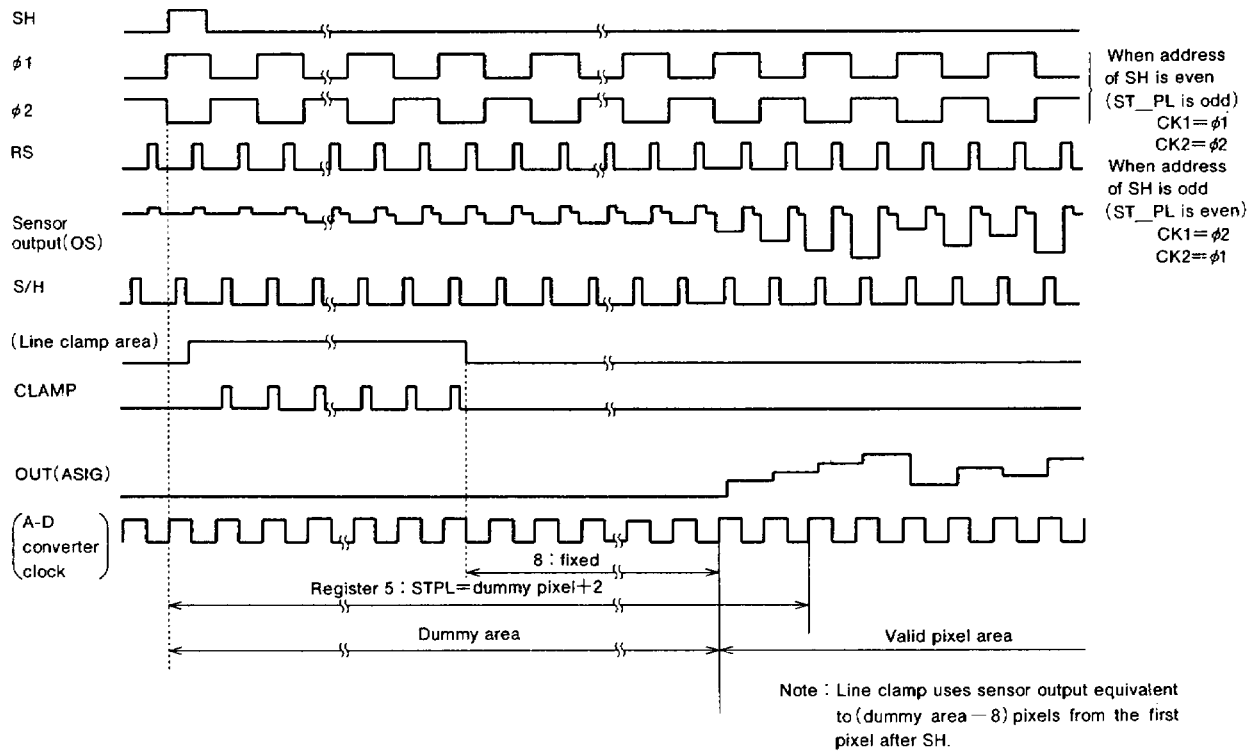


Units : 1/SYSCK



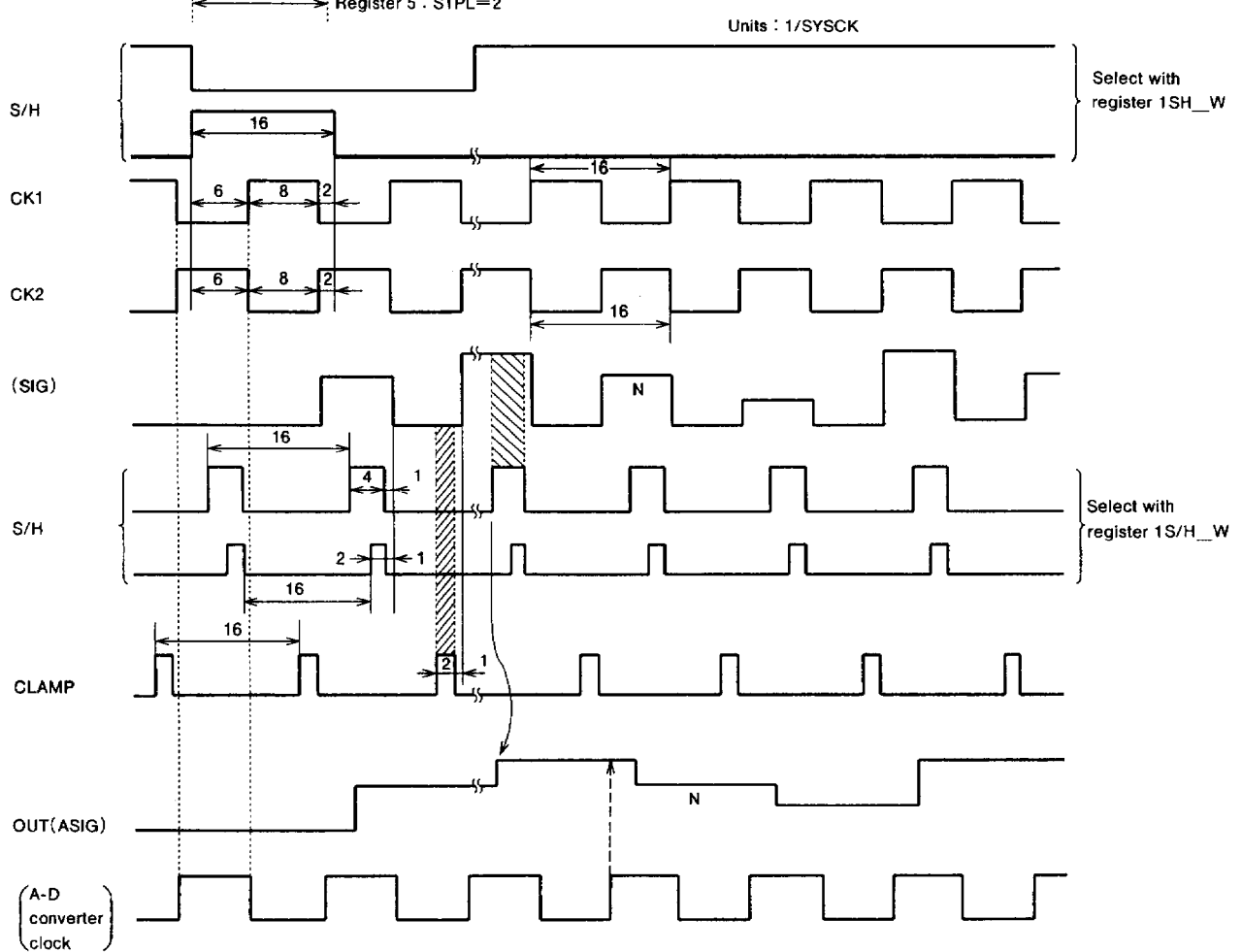
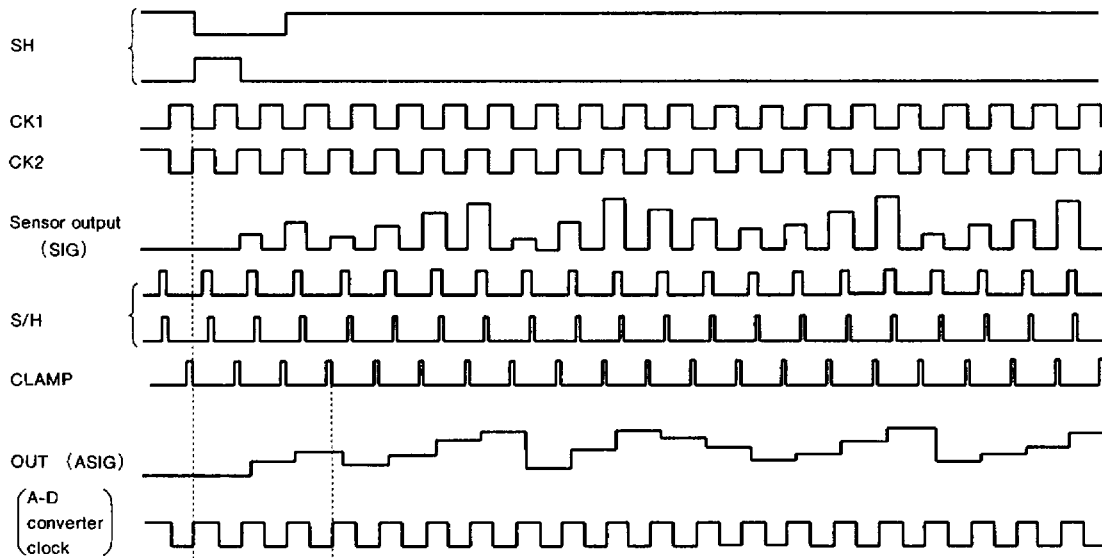
FACSIMILE IMAGE DATA PROCESSOR

CCD-line clamp type



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CIS type



Note : CLAMP

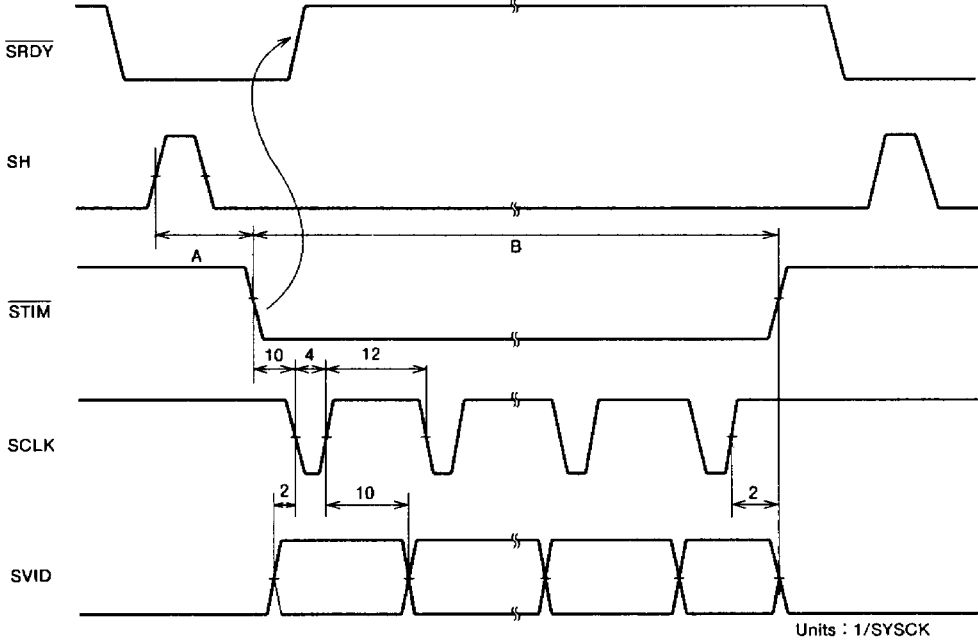
: In case of CIS, check with the sensor manufacturer for the use of CLAMP.

SH and CK1, CK2 : SH can be selected with register 1 and CK can be selected with CK1 and CK2(2 selections each)to provide interface to various types of CIS.

FACSIMILE IMAGE DATA PROCESSOR

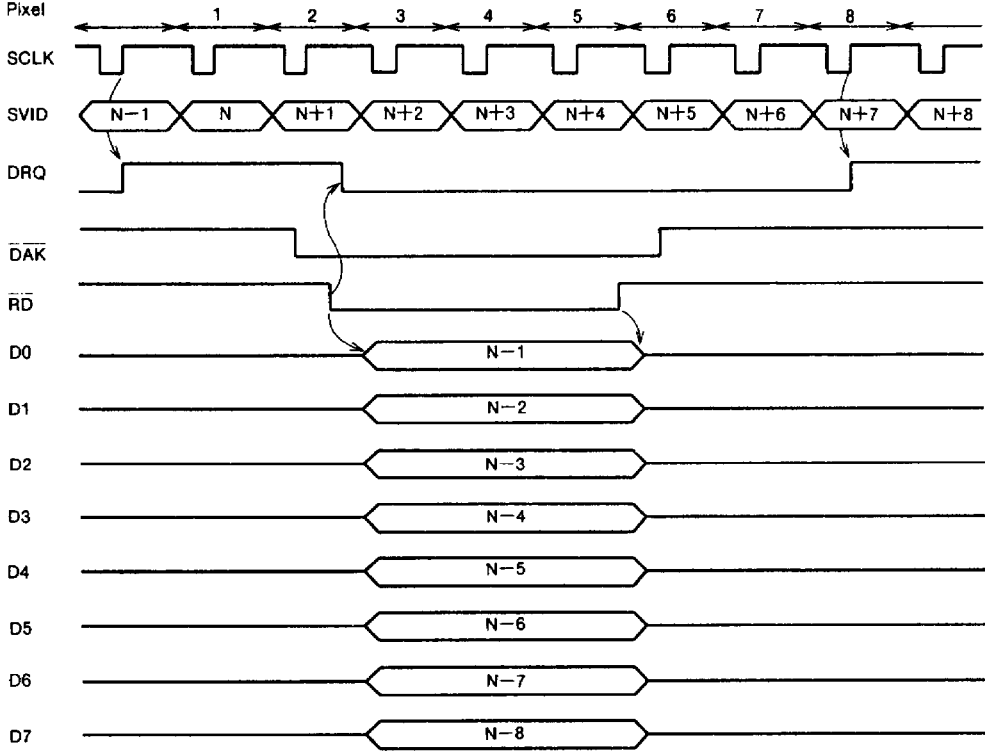
(5) CODEC interface

Serial output



Note : A is determined by register 5(ST_PL) and B is determined by register 2(SOURCE, DEST, REDU).

Parallel output



Note : Handshaking of three lines SRDY, SH, and STIM, which are interface to the CODEC, is the same as serial output.

FACSIMILE IMAGE DATA PROCESSOR

(6) External memory interface

The pixel transmission period during operation is 16/ SYSCK.

In SCAN mode, 4 to 7 cycle write/read is performed to the

external memory during one pixel transmission period in order to read the source document width and perform uniformity correction and error diffusion.

The memory address for each cycle is shown below.

Table 7 Read width in SCAN mode, Memory write/read cycle vs memory address map

Source document read width			Memory R/W cycle	External memory capacity	Chip select	Uniformity correction memory area		MTF compensation memory area (shared with data image area separation memory area)		Error diffusion memory area
						Black correction	White correction	Current line	Previous line	Error buffer
A3	B4	A4				Address	Address	Address	Address	Address
○	○	○	4 cycles	64KS	S2	—	0 _H ~097F _H	0A00 _H ~137F _H	1400 _H ~1D7F _H	—
×	○	○	5 cycles	64KS	S2	0 _H ~07FF _H	0800 _H ~0FFF _H	1000 _H ~17FF _H	1800 _H ~1FFF _H	—
×	○	○		64KS	S1	—	0800 _H ~0FFF _H	1000 _H ~17FF _H	1800 _H ~1FFF _H	0 _H ~07FF _H
○	○	○	6 cycles	64KS	S1	—	0 _H ~097F _H	—	—	—
○	○	○		64KS	S2	—	—	0A00 _H ~137F _H	1400 _H ~1D7F _H	0 _H ~097F _H
○	○	○		256KS	S2	—	0 _H ~097F _H	2A00 _H ~337F _H	3400 _H ~3D7F _H	2000 _H ~297F _H
×	○	○	7 cycles	32KR	S1	0 _H ~07FF _H	0800 _H ~0FFF _H	—	—	—
○	○	○		64KS	S2	—	—	0A00 _H ~11FF _H	1400 _H ~1BFF _H	0 _H ~07FF _H
○	○	○		64KS, R	S1	0A00 _H ~137F _H	0 _H ~097F _H	—	—	—
○	○	○		64KS	S2	—	—	0A00 _H ~137F _H	1400 _H ~1D7F _H	0 _H ~097F _H
○	○	○		256KS	S2	0A00 _H ~137F _H	0 _H ~097F _H	2A00 _H ~337F _H	3400 _H ~3D7F _H	2000 _H ~297F _H

32KR : 32K EPROM
 64KR : 64K EPROM
 64KS : 64K SRAM
 256KS : 256K SRAM

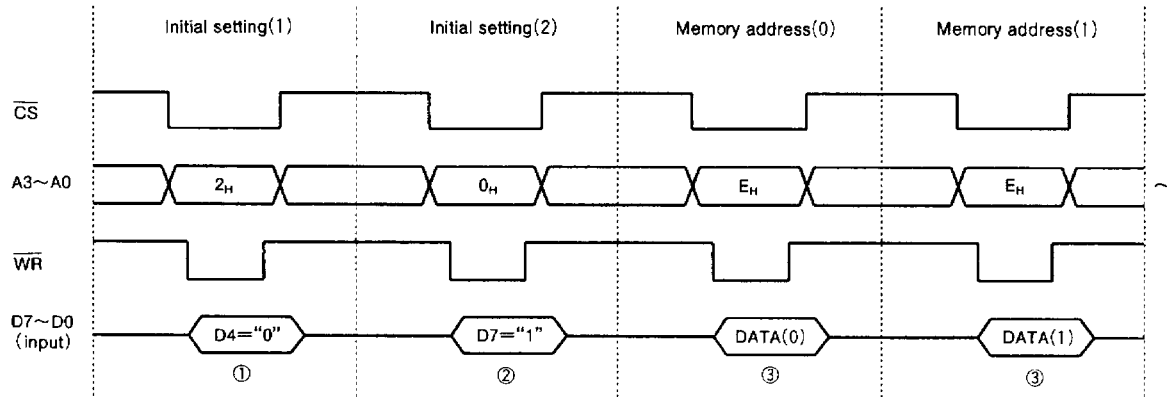
FACSIMILE IMAGE DATA PROCESSOR

(7) Read/write to dither memory, uniformity correction memory

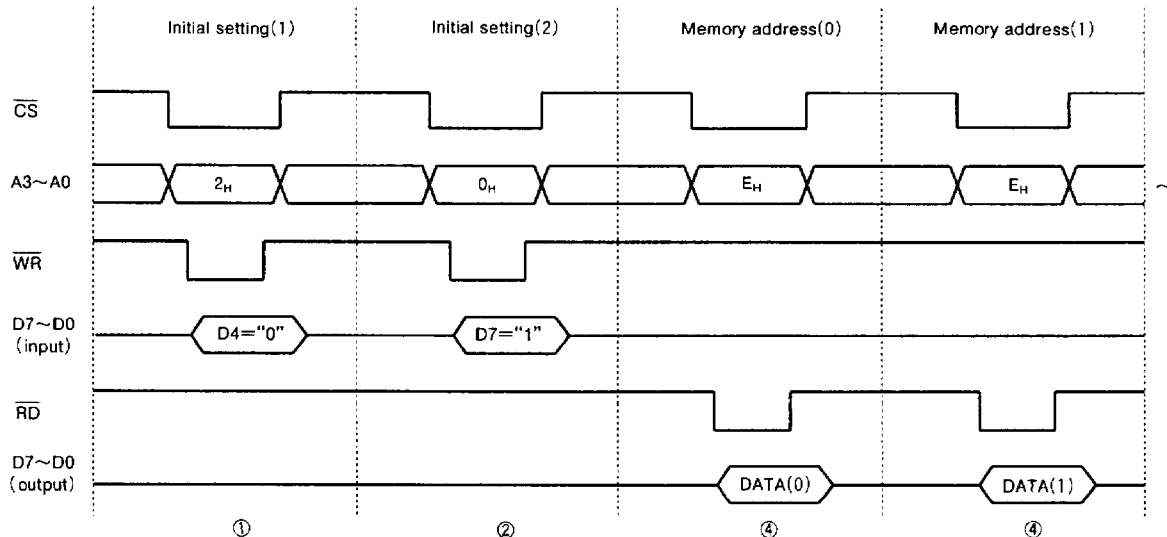
reading dither patterns in the 64 words × 6 bit collective dithering SRAM built in the M66333.

The following figures show the sequence for writing and

Dither memory write (MPU → M66333)



Dither memory read (M66333 → MPU)



- ① Clear D4(PO) in register 2 to "0" in order to set the MPU bus (D7-D0) to dither matrix memory data output mode.
- ② Set D7(RESET) in register 0 to "1" in order to reset the dither memory address counter.
- ③ Select DITH_D with register E and write DATA(0) on the MPU bus (D5-D0). Increment the address counter of the dither memory at the rising edge of WR. (during write)
- ④ Select DITH_D with register E and read DATA(0) in dither memory to the MPU bus (D5-D0). Increment the address counter of the dither memory at the rising edge of RD. (during read)

Dither matrix address

A0	A1	A2	A3
A4	A5	A6	A7
A8	A9	A10	A11
A12	A13	A14	A15

4×4 matrix

A0	A1	A2	A3
A4	A5	A6	A7
A8	A9	A10	A11
A12	A13	A14	A15
A16	A17	A18	A19
A20	A21	A22	A23
A24	A25	A26	A27
A28	A29	A30	A31

4×8 matrix

A0	A1	A2	A3	A4	A5	A6	A7
A8	A9	A10	A11	A12	A13	A14	A15
A16	A17	A18	A19	A20	A21	A22	A23
A24	A25	A26	A27	A28	A29	A30	A31
A32	A33	A34	A35	A36	A37	A38	A39
A40	A41	A42	A43	A44	A45	A46	A47
A48	A49	A50	A51	A52	A53	A54	A55
A56	A57	A58	A59	A60	A61	A62	A63

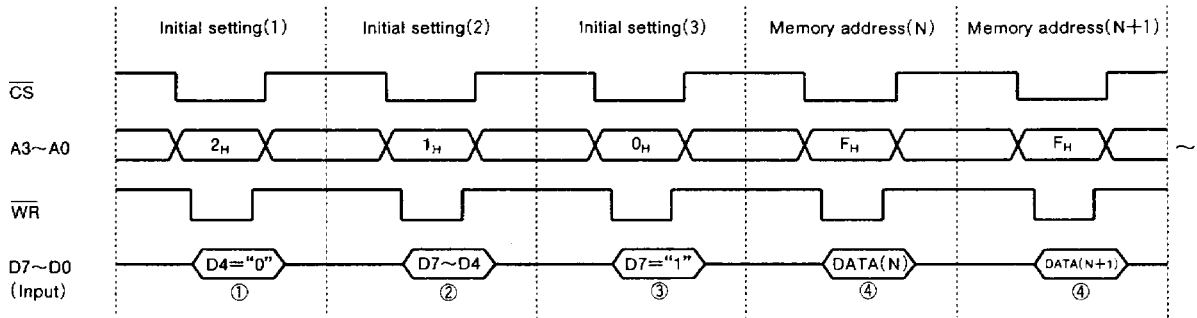
8×8 matrix

FACSIMILE IMAGE DATA PROCESSOR

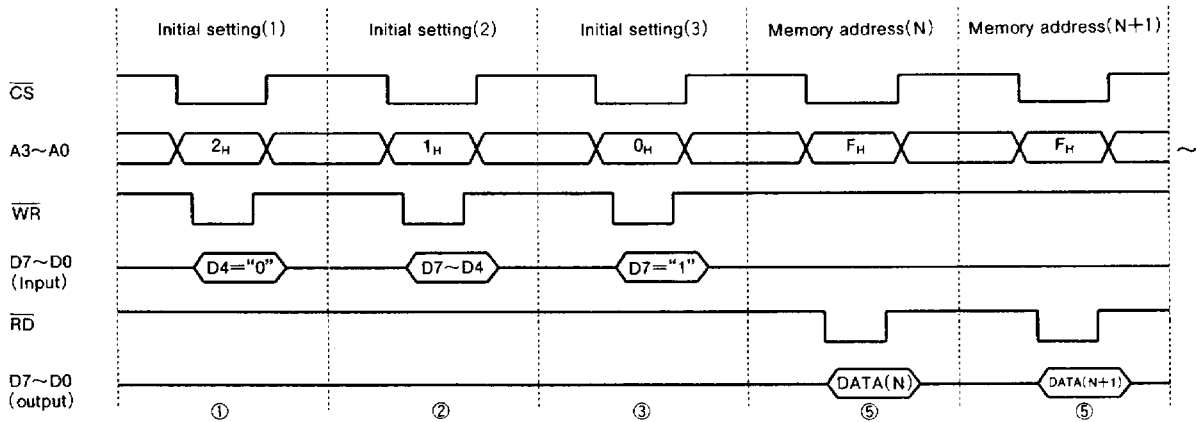
The M66333 can write/read uniformity correction data in the external correction SRAM through the MPU bus. This enables the uniformity correction data to be temporarily

saved in backup memory during power off. The following figures shown the uniformity correction data write/read sequence.

Uniformity correction memory write(MPU→M66333)



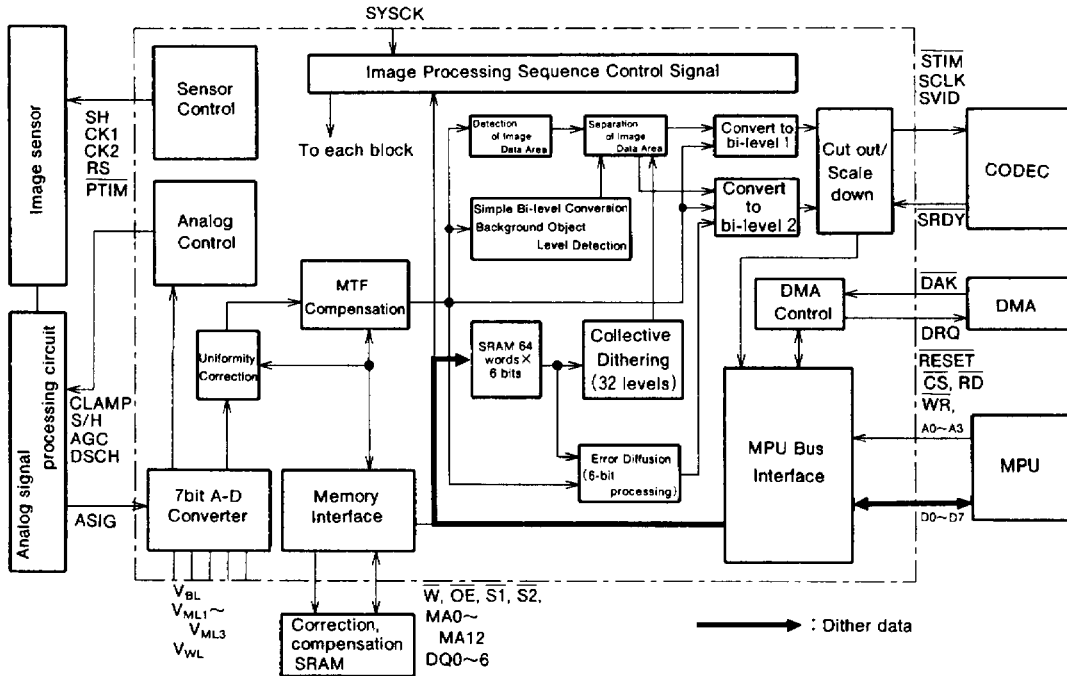
Uniformity correction memory read(M66333→MPU)



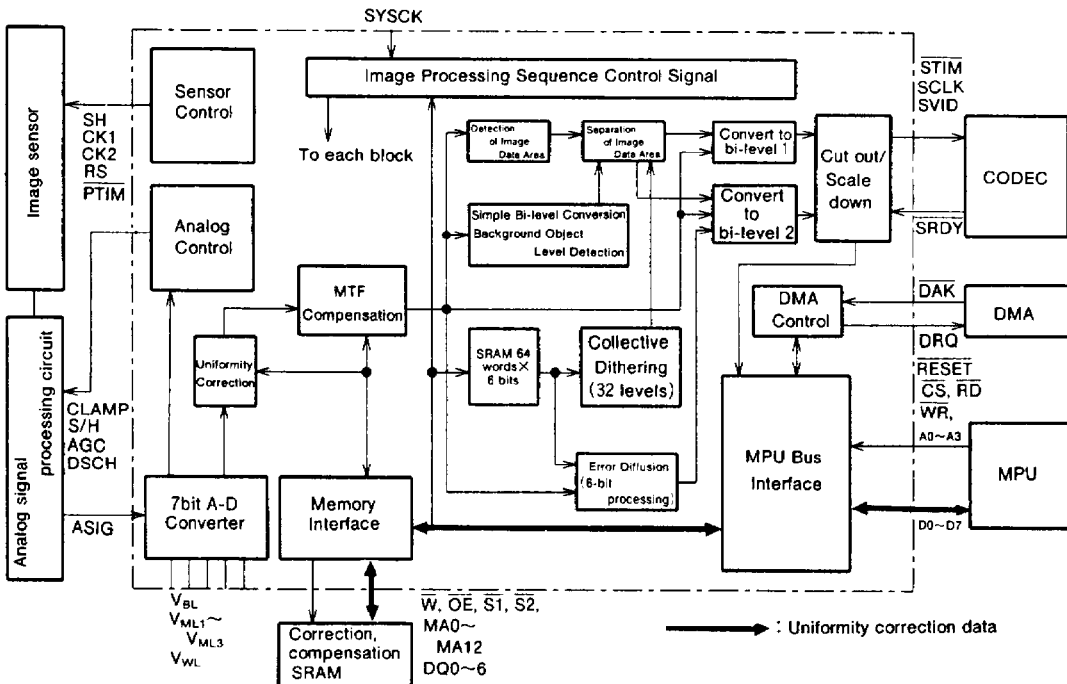
- ① Clear D4 (PO) in register 2 to "0" in order to set the MPU bus (D7-D0) to uniformity correction memory data output mode.
- ② Set D7D6 (M CLK) and D5D4 (MEMO) in register 1.
- ③ Set D7 (RESET) in register 0 to "1" in order to reset the uniformity correction memory address counter.
- ④ Select UNIF__D with register F and write DATA (N) on the MPU bus (D6-D0). Increment the address counter of the uniformity correction memory at the rising edge of WR. (during write)
- ⑤ Select UNIF__D with register F and read DATA (N) in uniformity correction memory to the MPU bus (D6-D0). Increment the address counter of the uniformity correction memory at the rising edge of RD. (during read)

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Dither memory write/read



Uniformity correction memory write/read



FACSIMILE IMAGE DATA PROCESSOR

(8) Image scale down and PTIM signal

Use the PTIM signal as the read roller pulse motor control signal. Figure 16 shows the sequence without scale down

and Figure 17 shows the sequence with scale down (B4→A4, scaling rate : 9/11).

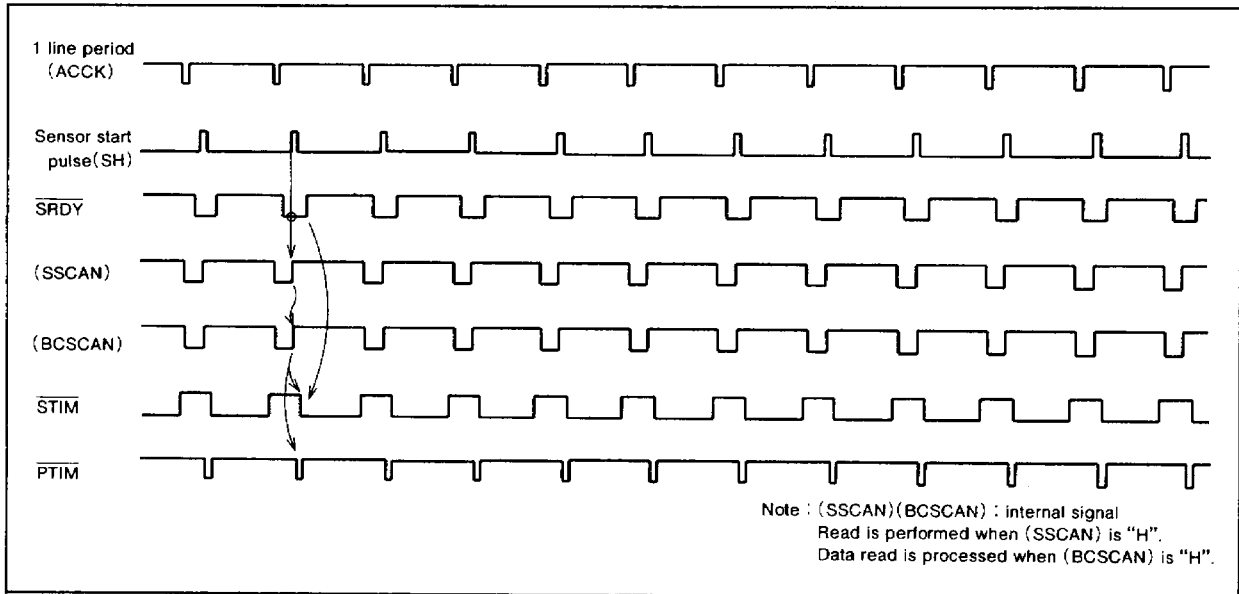


Fig. 16 Without scale down

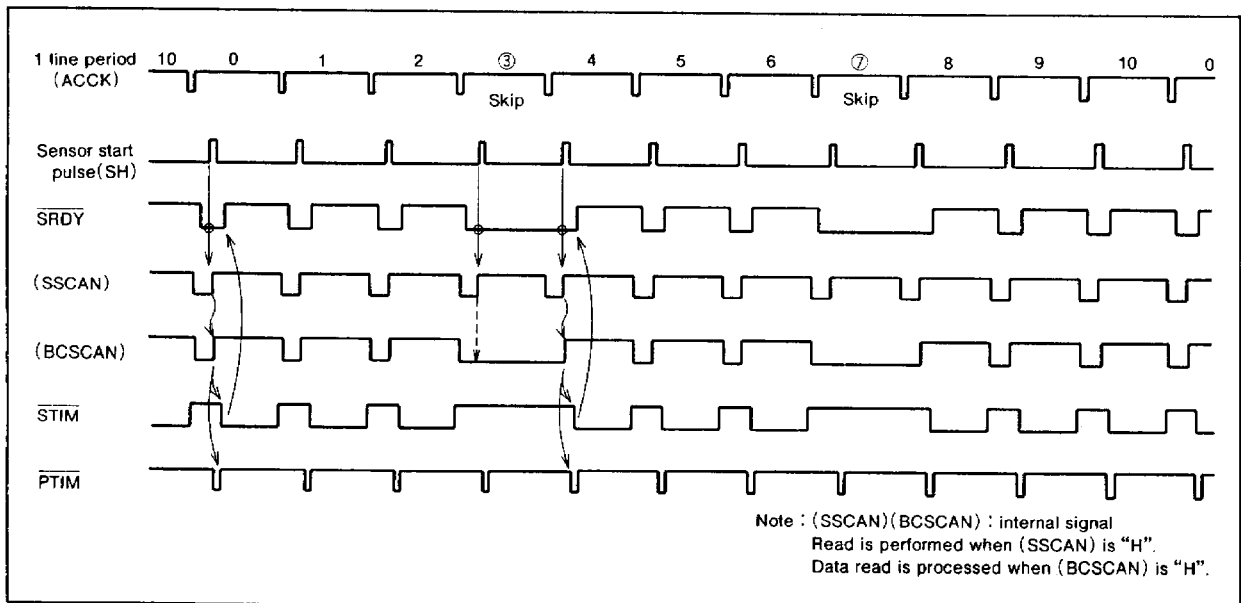


Fig. 17 With B4→A4 reduction

FACSIMILE IMAGE DATA PROCESSOR

(9) Reset

The M66333 has three types of reset. Each reset function is described below.

Hard reset : Initializes the circuit. Hard reset also performs the following soft reset and standby reset.

Soft reset : Used when cancelling a line read operation in the middle during SCAN mode. Read operation is resumed starting from the next line. This is used during write/read of dither memory (register E) and uniformity correction memory (register F) .

Soft reset is used to reset the address counter

before write/read.

Standby : Used as standby mode. The internal clock is stopped by stopping the clock generator which generates the internal clock from the system clock.

Therefore, the internal circuit is stopped and power is saved.

The period counter and register statuses are saved and the internal memory is placed in standby mode.

Table 8 Reset function

Function Reset Types	Initialize Register	Initialize Internal F/F	Reset Period Counter	Reset Memory Interface Address Counter*	Stop Clock Generator Operation	Stop Line Read
Hard Reset RESET	○	○	○	○	○	
Soft Reset Register 0 (RESET)				○		○
Standby Register 2 (STNBY)		○		○	○	

* : Dither memory and uniformity correction memory address counter

(10) Image quality control using registers

- **MTF compensation**

If the sensor has high resolution, MTF compensation need not be performed for half-tone area.

MTF compensation should be performed for bi-level area regardless of the sensor resolution in order to achieve good object reproduction.

- **Simple bi-level conversion, background and object level detection**

Set the background level detection counter and object level detection counter as follows in order to obtain clear output of objects that do not have completely white background and objects that are not entirely black.

$$\leftarrow \text{fast} \\ \text{MAX_UP} > \text{MAX_DOWN} > \text{MIN_UP}$$

The output becomes darker as bi-level conversion threshold coefficient (SLICE) is increased.

Select a large SLICE value for light source document.

- **Pseudo half-tone conversion, dither method**

Select 16 gradation using 4×4 dither matrix for fine mode and 32 gradation using 4×8 dither matrix for super fine mode. Refer to the section on image processing function for details on providing dither pattern threshold.

- **Error diffusion**

γ correction must be performed for error diffusion. This is performed by applying voltage to the middle basic supply voltage pin of the A-D converter as described in the section on image processing function.

If the printer has a thermal head, $\gamma = 0.45$ is said to be the optimum γ characteristic for the human eye.

- **Separation of image data area**

The optimum parameter is selected to perform the best bi-level conversion for each area : simple bi-level conversion for the object and pseudo half-tone conversion for half-tone.

Table 9 shows the recommended values for parameters related to picture quality.

Use these values as reference to determine the optimum parameter.

FACSIMILE IMAGE DATA PROCESSOR

Table 9 Recommended parameter values

Image	Uniformity Correction	MTF Compensation		Background and Object Level					γ Correction	Dither Pattern	ERROR		Separation of Image Data Area*		
		MTF_M	MTF_S	SLICE	MAX UP	MAX DOWN	MIN UP	UL MIN			LL MAX	Error	Dither	SEP A A	SEP A B
Simple Bi-level Conversion	Yes	1/2	5/8	Normal	Normal	Normal	1F _H	20 _H	No	—	—	—	—	—	—
Dithering	Yes	1/4	—	—	—	—	—	—	No	4×4 diffusion (pattern 1)	—	—	—	—	—
Error Diffusion	Yes	NON	5/8	—	—	—	—	—	$\gamma=0.45$ $V_{ML1}=0.31V$ $V_{ML2}=1.25V$ $V_{ML3}=2.50V$	4×4 diffusion (pattern 2)	7/8	1/8	3F _H	3A _H	00 _H
Separation of Image Data Area	Yes	1/4	5/8	Normal	Normal	Normal	1F _H	20 _H	No	4×4 diffusion (pattern 1)	—	—	18 _H	34 _H	00 _H

Dither pattern 1 ($\gamma=0.6$)

0	8	2	10
02	14	04	1C
12	4	14	6
25	07	2F	0D
3	11	1	9
05	20	03	17
15	7	13	5
35	10	2A	09

Dither pattern 2

0	8	2	10
02	22	0A	2A
12	4	14	6
32	12	3A	1A
3	11	1	9
0E	2E	06	26
15	7	13	5
3E	1E	36	16

* : The value in the error diffusion column is the background processing value.

FACSIMILE IMAGE DATA PROCESSOR

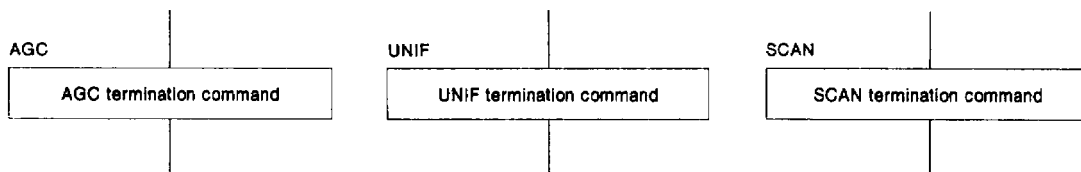
USAGE PRECAUTIONS

● **Operating mode termination command**

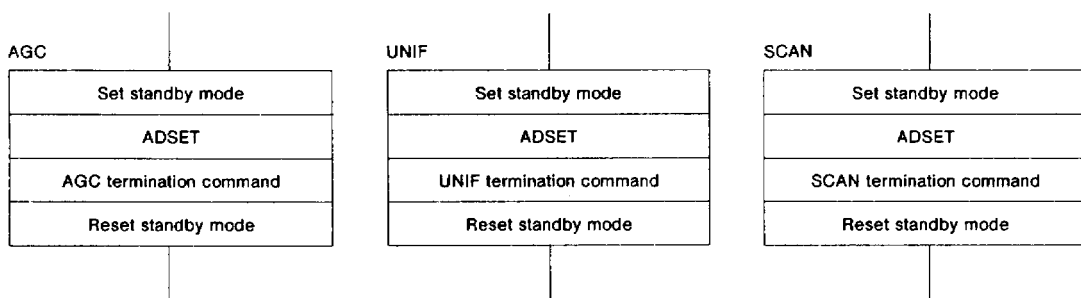
When accessing the M66333 after terminating the AGC, UNIF, or SCAN command, wait at least 1 line period after

terminating the AGC, UNIF, or SCAN command. Furthermore, the ADSET processing described below is required when accessing immediately after terminating the command.

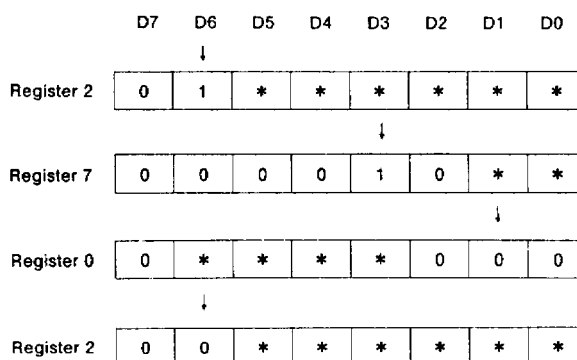
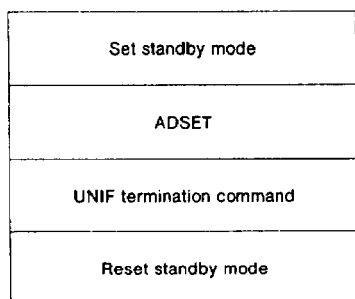
General termination commands



Termination command with ADSET processing



Example of UNIF termination with ADSET processing



* : Set same as operating mode.

FACSIMILE IMAGE DATA PROCESSOR

● **TIME function**

When TIME = "1" is set in register 2, the processing time per line is doubled to 2 line periods. Data is read once every two line periods and processed.

When the read and write motors operate simultaneously during copy operation, this command can be used to reduce the processing speed to 1/2 in order to reduce the power load.

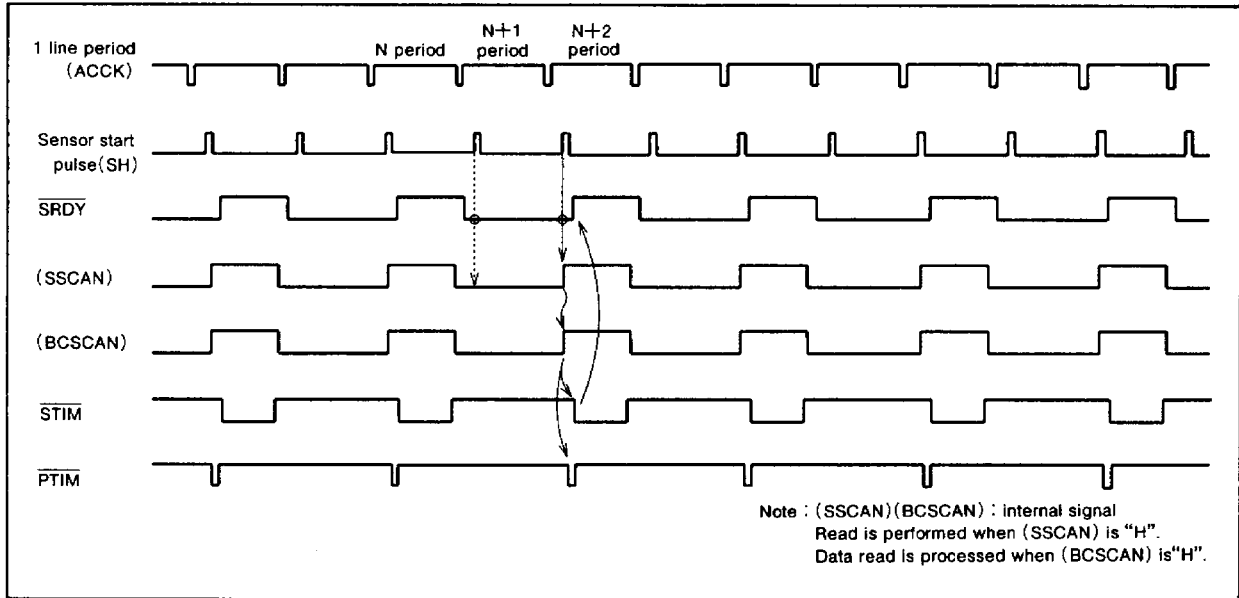


Fig. 18 When processing speed is 1/2

● **Peak detection in SCAN mode**

In SCAN mode, successive peak detection is performed for the image data being read as shown for the AGC range (dotted line) in Figure 1.

This enables better picture reproduction when picture data brighter than the white reference used during peak detection is input in SCAN mode.

This is especially effective for sensor units such as CIS which do not have a built-in white reference.

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Register Structure

Address	R/W	Explanation																																																																																																								
0 _H	W	<table border="1" style="width: 100%; text-align: center;"> <tr> <td>D7</td> <td>D6</td> <td>D5</td> <td>D4</td> <td>D3</td> <td>D2</td> <td>D1</td> <td>D0</td> <td></td> </tr> <tr> <td>RESET</td> <td>SENS</td> <td colspan="2">SENS_W</td> <td>UMODE</td> <td>AGC</td> <td>UNIF</td> <td>SCAN</td> <td>(Default is 00_H)</td> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td>D7</td> <td>RESET</td> <td>System Reset</td> <td rowspan="3">• Reset while write pulse is "L" when D7="1".</td> </tr> <tr> <td>0</td> <td colspan="2">Normal Mode</td> </tr> <tr> <td>1</td> <td colspan="2">Reset Mode</td> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td>D6</td> <td>SENS</td> <td>Sensor Type</td> </tr> <tr> <td>0</td> <td colspan="2">CCD</td> </tr> <tr> <td>1</td> <td colspan="2">CIS</td> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td>D5</td> <td>D4</td> <td>SENS_W</td> <td>Sensor Width</td> </tr> <tr> <td>0</td> <td>0</td> <td colspan="2">A4</td> </tr> <tr> <td>0</td> <td>1</td> <td colspan="2">B4</td> </tr> <tr> <td>1</td> <td>0</td> <td colspan="2">A3</td> </tr> <tr> <td>1</td> <td>1</td> <td colspan="2">—</td> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td>D3</td> <td colspan="2">UMODE</td> <td>Uniformity Correction Mode</td> <td rowspan="3">• For selecting correction mode in UNIF mode. Refer to Table 4.</td> </tr> <tr> <td></td> <td>White & Black Correction</td> <td colspan="2">White Correction only</td> </tr> <tr> <td>0</td> <td colspan="2">White Correction</td> <td>—</td> </tr> <tr> <td>1</td> <td colspan="2">Black Correction</td> <td>White Correction</td> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td>D2</td> <td>AGC</td> <td>Auto Gain Control</td> <td rowspan="3">• Controls AGC mode start/stop.</td> </tr> <tr> <td>0</td> <td colspan="2">Stop</td> </tr> <tr> <td>1</td> <td colspan="2">Start</td> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td>D1</td> <td>UNIF</td> <td>Uniformity Correction</td> <td rowspan="3">• Controls UNIF mode start/stop.</td> </tr> <tr> <td>0</td> <td colspan="2">Stop</td> </tr> <tr> <td>1</td> <td colspan="2">Start</td> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td>D0</td> <td>SCAN</td> <td>Source Scanning</td> <td rowspan="3">• Controls SCAN mode start/stop.</td> </tr> <tr> <td>0</td> <td colspan="2">Stop</td> </tr> <tr> <td>1</td> <td colspan="2">Start</td> </tr> </table>	D7	D6	D5	D4	D3	D2	D1	D0		RESET	SENS	SENS_W		UMODE	AGC	UNIF	SCAN	(Default is 00 _H)	D7	RESET	System Reset	• Reset while write pulse is "L" when D7="1".	0	Normal Mode		1	Reset Mode		D6	SENS	Sensor Type	0	CCD		1	CIS		D5	D4	SENS_W	Sensor Width	0	0	A4		0	1	B4		1	0	A3		1	1	—		D3	UMODE		Uniformity Correction Mode	• For selecting correction mode in UNIF mode. Refer to Table 4.		White & Black Correction	White Correction only		0	White Correction		—	1	Black Correction		White Correction	D2	AGC	Auto Gain Control	• Controls AGC mode start/stop.	0	Stop		1	Start		D1	UNIF	Uniformity Correction	• Controls UNIF mode start/stop.	0	Stop		1	Start		D0	SCAN	Source Scanning	• Controls SCAN mode start/stop.	0	Stop		1	Start	
D7	D6	D5	D4	D3	D2	D1	D0																																																																																																			
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1 _H	W	<table border="1" style="width: 100%; text-align: center;"> <tr> <td>D7</td> <td>D6</td> <td>D5</td> <td>D4</td> <td>D3</td> <td>D2</td> <td>D1</td> <td>D0</td> <td></td> </tr> <tr> <td colspan="2">M_CLK</td> <td colspan="2">MEMO</td> <td>UNIFM</td> <td>S/H_W</td> <td>SH_W</td> <td>CLAMP</td> <td>(Default is 00_H)</td> </tr> </table> <table border="1" style="width: 100%;"> <tr> <td>D7</td> <td>D6</td> <td>M_CLK</td> <td>Memory Read/Write Cycle</td> <td>Correction</td> <td>Compensation</td> <td>Error</td> </tr> <tr> <td>0</td> <td>0</td> <td colspan="2">7 Cycle</td> <td>Black, White</td> <td>Now, Pre, Next</td> <td>R, W</td> </tr> <tr> <td>0</td> <td>1</td> <td colspan="2">4 Cycle</td> <td>White</td> <td>Now, Pre, Next</td> <td>—</td> </tr> <tr> <td>1</td> <td>0</td> <td colspan="2">5 Cycle</td> <td>Black, White</td> <td>Now, Pre, Next</td> <td>—</td> </tr> <tr> <td>1</td> <td>1</td> <td colspan="2">6 Cycle</td> <td>White</td> <td>Now, Pre, Next</td> <td>R, W</td> </tr> </table>	D7	D6	D5	D4	D3	D2	D1	D0		M_CLK		MEMO		UNIFM	S/H_W	SH_W	CLAMP	(Default is 00 _H)	D7	D6	M_CLK	Memory Read/Write Cycle	Correction	Compensation	Error	0	0	7 Cycle		Black, White	Now, Pre, Next	R, W	0	1	4 Cycle		White	Now, Pre, Next	—	1	0	5 Cycle		Black, White	Now, Pre, Next	—	1	1	6 Cycle		White	Now, Pre, Next	R, W																																																			
D7	D6	D5	D4	D3	D2	D1	D0																																																																																																			
M_CLK		MEMO		UNIFM	S/H_W	SH_W	CLAMP	(Default is 00 _H)																																																																																																		
D7	D6	M_CLK	Memory Read/Write Cycle	Correction	Compensation	Error																																																																																																				
0	0	7 Cycle		Black, White	Now, Pre, Next	R, W																																																																																																				
0	1	4 Cycle		White	Now, Pre, Next	—																																																																																																				
1	0	5 Cycle		Black, White	Now, Pre, Next	—																																																																																																				
1	1	6 Cycle		White	Now, Pre, Next	R, W																																																																																																				

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FACSIMILE IMAGE DATA PROCESSOR

Address	R/W	Explanation																												
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			UNIF_D																											

FACSIMILE IMAGE DATA PROCESSOR

ABSOLUTE MAXIMUM RATING ($T_a = -20 \sim 75^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		$-0.3 \sim +7.0$	V
V_I	Input voltage		$-0.3 \sim V_{CC} + 0.3$	V
V_O	Output voltage		$0 \sim V_{CC}$	V
AV_{CC}	Analog supply voltage		$V_{CC} - 0.3 \sim V_{CC} + 0.3$	V
V_{WL}	Reference voltage (White)		$-0.3 \sim AV_{CC} + 0.3$	V
V_{BL}	Reference voltage (Black)		$-0.3 \sim AV_{CC} + 0.3$	V
V_{ML}	Reference voltage (Middle)		$-0.3 \sim AV_{CC} + 0.3$	V
V_{AIN}	Analog Input voltage		$-0.3 \sim AV_{CC} + 0.3$	V
Tstg	Storage temperature range		$-65 \sim 150$	$^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
GND	Ground		0		V
V_I	Input voltage	0		V_{CC}	V
AV_{CC}	Analog supply voltage	4.5	5.0	5.5	V
A_{GND}	Analog ground (Note)		0		V
V_{WL}	Reference voltage (White)		3	AV_{CC}	V
V_{BL}	Reference voltage (Black)	0.0	0.0	1.0	V
V_{AIN}	Analog input voltage	ASIG		V_{BL}	V
T_{opr}	Operating temperature range	-20		75	$^\circ\text{C}$

Note : Please connect AGND with GND.

FACSIMILE IMAGE DATA PROCESSOR

ELECTRICAL CHARACTERISTICS (T_a = -20~75°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V _{IH}	"H" Input voltage	SYSCK, DQ0~DQ6, SRDY, DAK,		2.0			V
V _{IL}	"L" Input voltage	CS, RD, WR, A0~A3, D0~D7				0.8	V
V _{T+}	Positive-going threshold voltage					2.4	V
V _{T-}	Negative-going threshold voltage	RESET		0.6			V
V _H	Hysteresis voltage				0.2		V
V _{OH}	High-level output voltage		I _{OH} = -12mA	V _{CC} - 0.8			V
V _{OL}	Low-level output voltage	D0~D7	I _{OL} = 12mA			0.55	V
V _{OH}	High-level output voltage	SH, CK1, CK2, RS PTIM, CLAMP, S/H, AGC, DSCH	I _{OH} = -4mA	V _{CC} - 0.8			V
V _{OL}	Low-level output voltage	STIM, SCLK, SVID W, OE, S1, S2, DQ0~DQ6 MA0~MA12, DRQ	I _{OL} = 4mA			0.55	V
I _{IH}	High-level input current	SRDY, DAK RESET, CS	V _{CC} = 5.5V V _I = 5.5V			1.0	μA
I _{IL}	Low-level input current	RD, WR, A0~A3	V _{CC} = 5.5V V _I = 0V			-1.0	μA
I _{OZH}	Off-state high-level output current	D0~D7	V _{CC} = 5.5V V _O = 5.5V			5.0	μA
I _{OZL}	Off-state low-level output current	DQ0~DQ6	V _{CC} = 5.5V V _O = 0V			-5.0	μA
I _{AIN}	Analog input current	ASIG				±10	μA
R _L	Reference resistance				1.3		KΩ
S _{INL}	A-D converter Non-linear error (Note 1)		V _{CC} = 5.0V		±0.5	±1.5	LSB
I _{CCS}	Quiescent supply current (Standby) (Note 2)		V _{CC} = 5.5V V _I = V _{CC} , GND		20	40	mA
I _{CCA}	Quiescent supply current (Active state) (Note 2)		V _{CC} = 5.5V V _I = V _{CC} , GND		30	60	mA
I _{CC}	Dynamic supply current	SYSCK = 8MHz	V _{CC} = 5.5V V _I = V _{CC} , GND		45		mA

Note 1 : The A-D converter has a 7-bit resolution.

2 : Current flowing in the reference resistor in the A-D converter is not included.

FACSIMILE IMAGE DATA PROCESSOR

TIMING REQUIREMENT (T_a=-20~75°C, V_{CC}=5V±10%, unless otherwise noted)

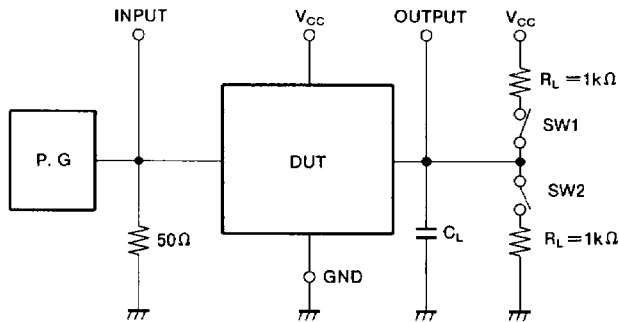
Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
t _{C(SYS)}	System clock	Period		125		ns	
t _{W+(SYS)}		High-level pulse width		62.5		ns	
t _{W-(SYS)}		Low-level pulse width		62.5		ns	
t _{r(SYS)}		Rise time			20	ns	
t _{f(SYS)}		Fall time			20	ns	
t _{W(RD)}	Read pulse	Pulse width		100		ns	
t _{SU(CS-RD)}		Setup time	CS	20		ns	
t _{SU(A-RD)}		Setup time	A0~A3	20		ns	
t _{SU(DAK-RD)}		Setup time	DAK	20		ns	
t _{H(RD-CS)}		Hold time	CS	10		ns	
t _{H(RD-A)}		Hold time	A0~A3	10		ns	
t _{H(RD-DAK)}		Hold time	DAK	10		ns	
t _{W(WR)}		Write pulse	Pulse width		100		ns
t _{SU(CS-WR)}			Setup time	CS	20		ns
t _{SU(A-WR)}	Setup time		A0~A3	20		ns	
t _{SU(D-WR)}	Setup time		D0~D7	50		ns	
t _{H(WR-CS)}	Hold time		CS	20		ns	
t _{H(WR-A)}	Hold time		A0~A3	10		ns	
t _{H(WR-D)}	Hold time		D0~D7	0		ns	
t _{H(STIM-SRDY)}	STIM		Hold time	SRDY	0		ns

FACSIMILE IMAGE DATA PROCESSOR

SWITCHING CHARACTERISTICS ($T_a = -20 \sim 75^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{PZL}(\overline{RD-D})$	Output enable time to low-level and high-level (RD-D)	$C_L = 150\text{pF}$			75	ns
$t_{PZH}(\overline{RD-D})$						
$t_{PLZ}(\overline{RD-D})$	Output disable time from low-level and high-level (RD-D)	$C_L = 150\text{pF}$	10		50	ns
$t_{PHZ}(\overline{RD-D})$						
$t_{PHL}(\overline{RD-DRQ})$	High-level to low-level output propagation time (RD-DRQ)	$C_L = 50\text{pF}$			50	ns

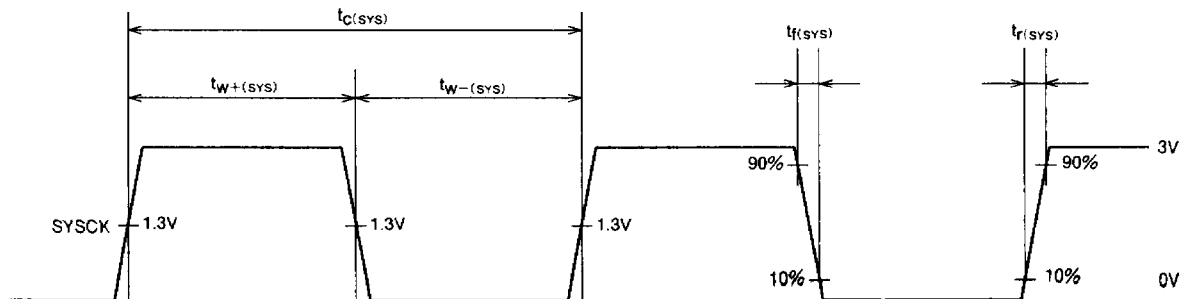
Test Circuit



Parameter	SW1	SW2
t_{PLH} , t_{PHL}	Open	Open
t_{PLZ}	Closed	Open
t_{PHZ}	Open	Closed
t_{PZL}	Closed	Open
t_{PZH}	Open	Closed

- (1) The pulse generator (PG) has the following characteristics (10% ~ 90%) : $t_r = 3\text{ns}$, $t_f = 3\text{ns}$
- (2) The capacitance $C_L = 150\text{pF}$ includes stray wiring capacitance and the probe input capacitance.

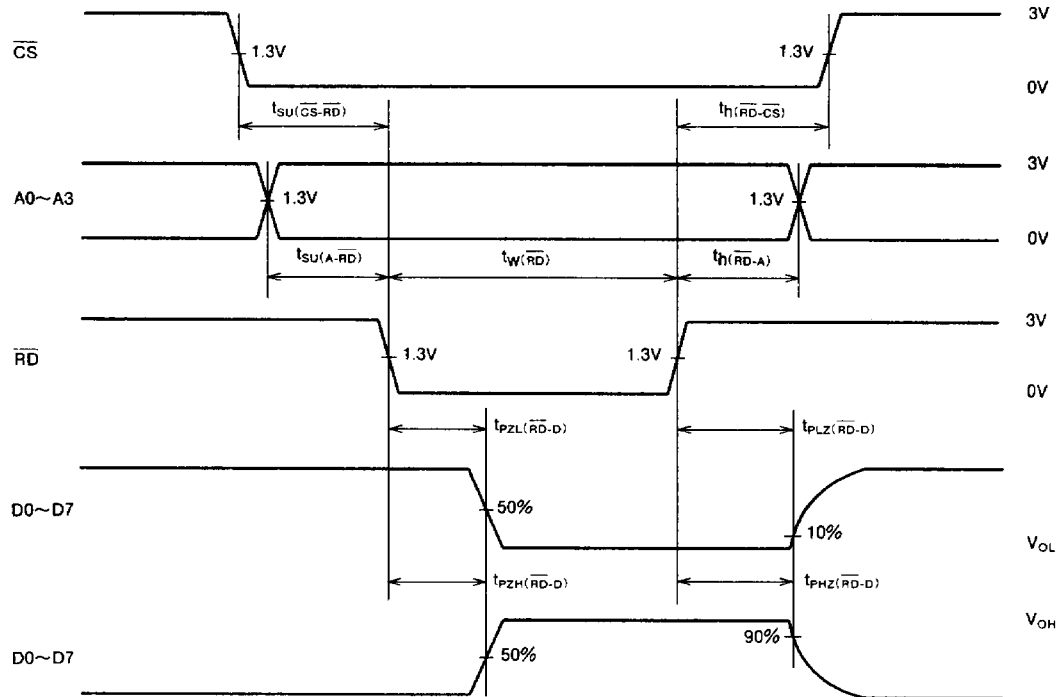
System clock



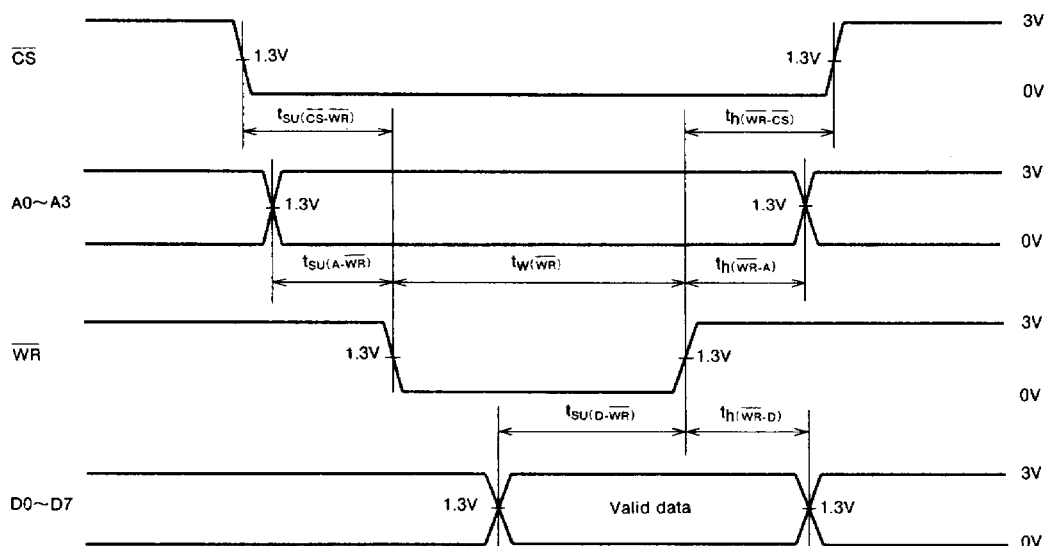
FACSIMILE IMAGE DATA PROCESSOR

MPU Interface

1) Read timing (M66333→MPU)



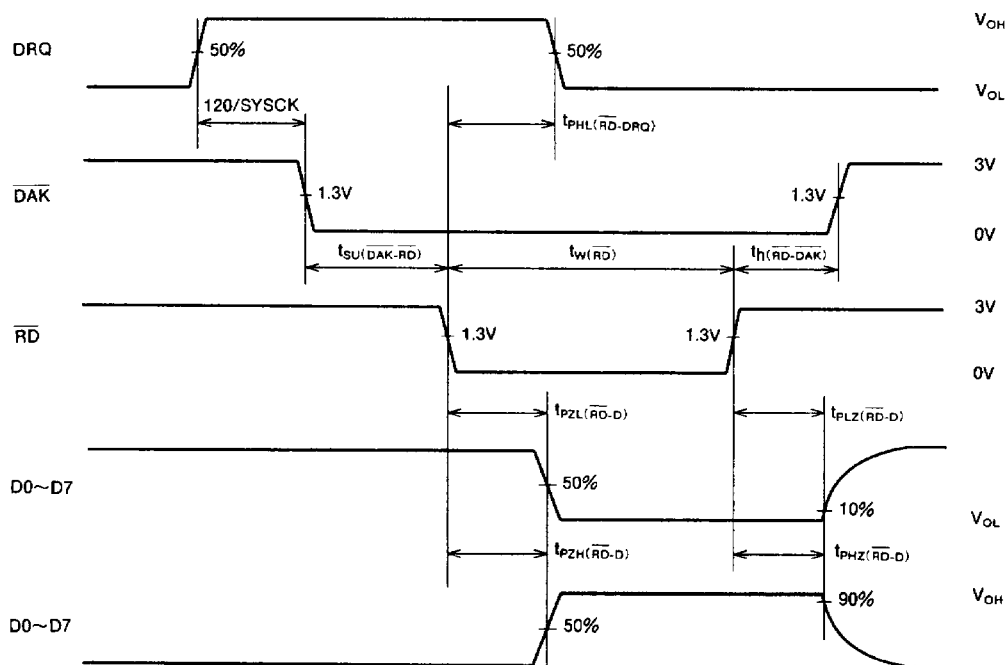
2) Write timing (MPU→M66333)



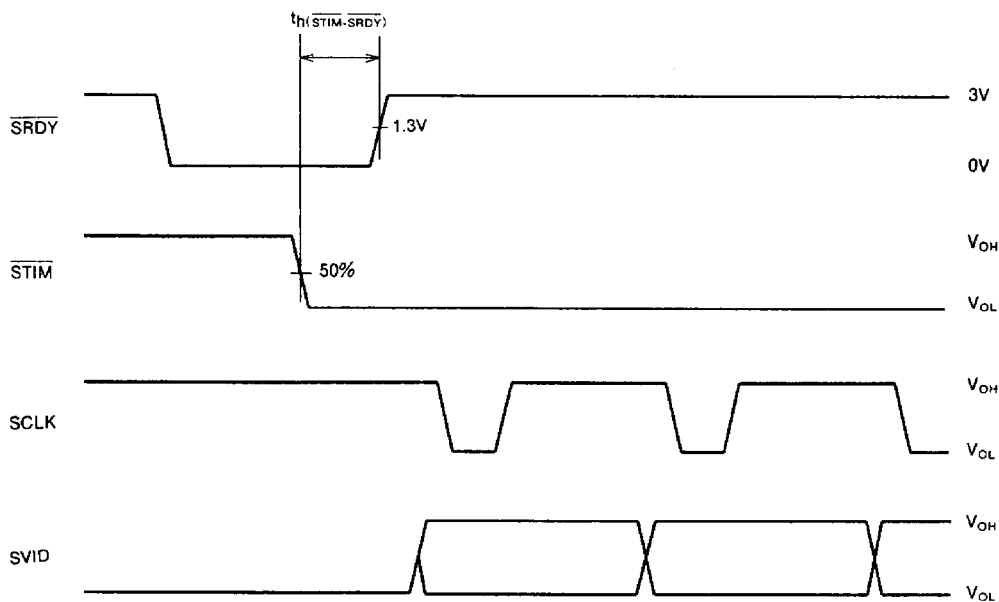
FACSIMILE IMAGE DATA PROCESSOR

DMA timing

Read timing (M66333→System bus)



CODEC Interface



FACSIMILE IMAGE DATA PROCESSOR

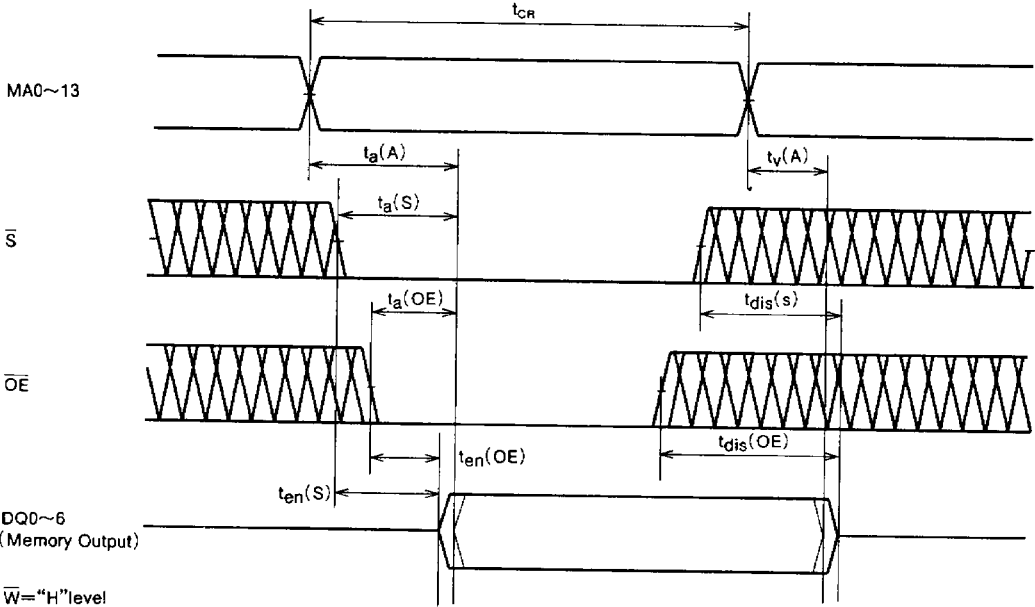
TIMING REQUIREMENT OF EXTERNAL MEMORY

Symbol	Parameter		Test Condition	Limits			Unit
				Min.	Typ.	Max.	
t_{CR}	Read cycle time			100			ns
$t_{a(A)}$	Access time	Address	MA0~13			100	ns
$t_{a(S)}$		Chip select	\bar{S}			100	ns
$t_{a(OE)}$		Output enable	\overline{OE}			50	ns
$t_{dis(S)}$	Disable time	Chip select	\bar{S}			35	ns
$t_{dis(OE)}$		Output enable	\overline{OE}			35	ns
$t_{en(S)}$	Enable time	Chip select	\bar{S}	10			ns
$t_{en(OE)}$		Output enable	\overline{OE}		10		ns
$t_{V(A)}$	Data effective time after Address			10			ns
t_{CW}	Write cycle			100			ns
$t_{W(W)}$	Write pulse			60			ns
$t_{su(A)}$	Setup time	Address	MA0~13	0			ns
$t_{su(S)}$		Chip select	\bar{S}	80			ns
$t_{su(D)}$		Data	DQ0~6	35			ns
$t_{h(D)}$	Data hold time			0			ns
$t_{rec(W)}$	Write recovery time			0			ns
$t_{dis(W)}$	Output disable time after write enable					35	ns
$t_{en(W)}$	Output enable time after write enable			10			ns

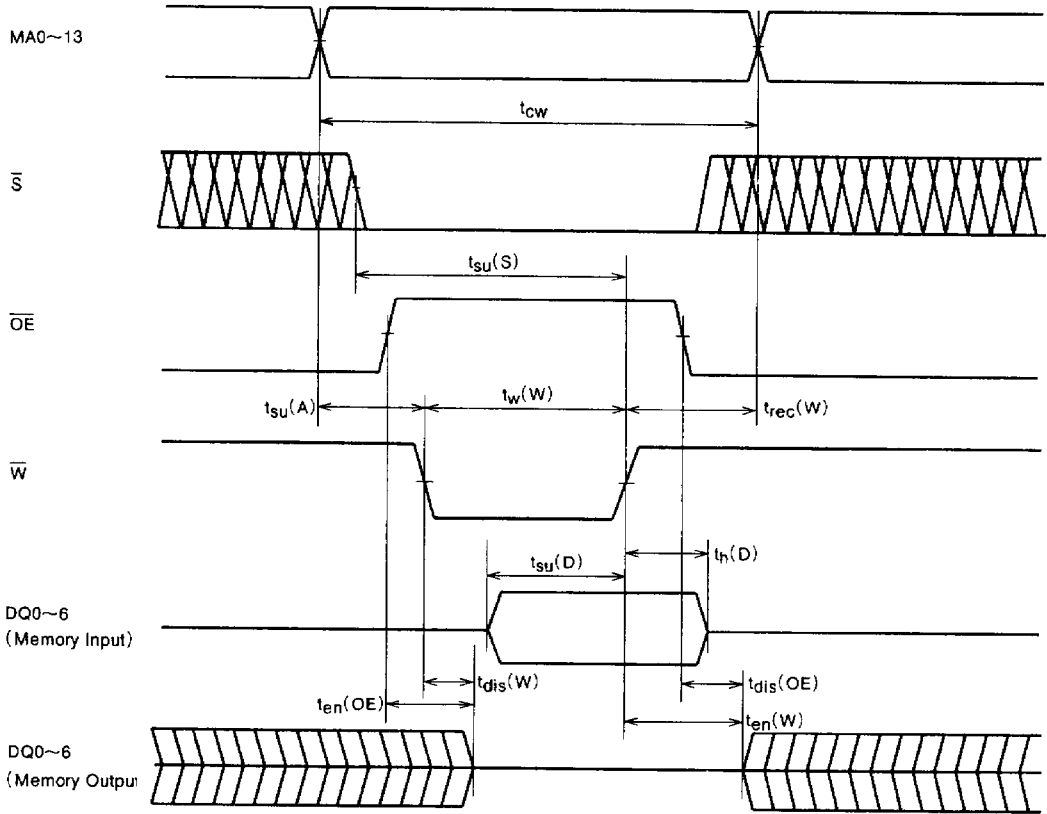
FACSIMILE IMAGE DATA PROCESSOR

Memory Interface

a) Read cycle

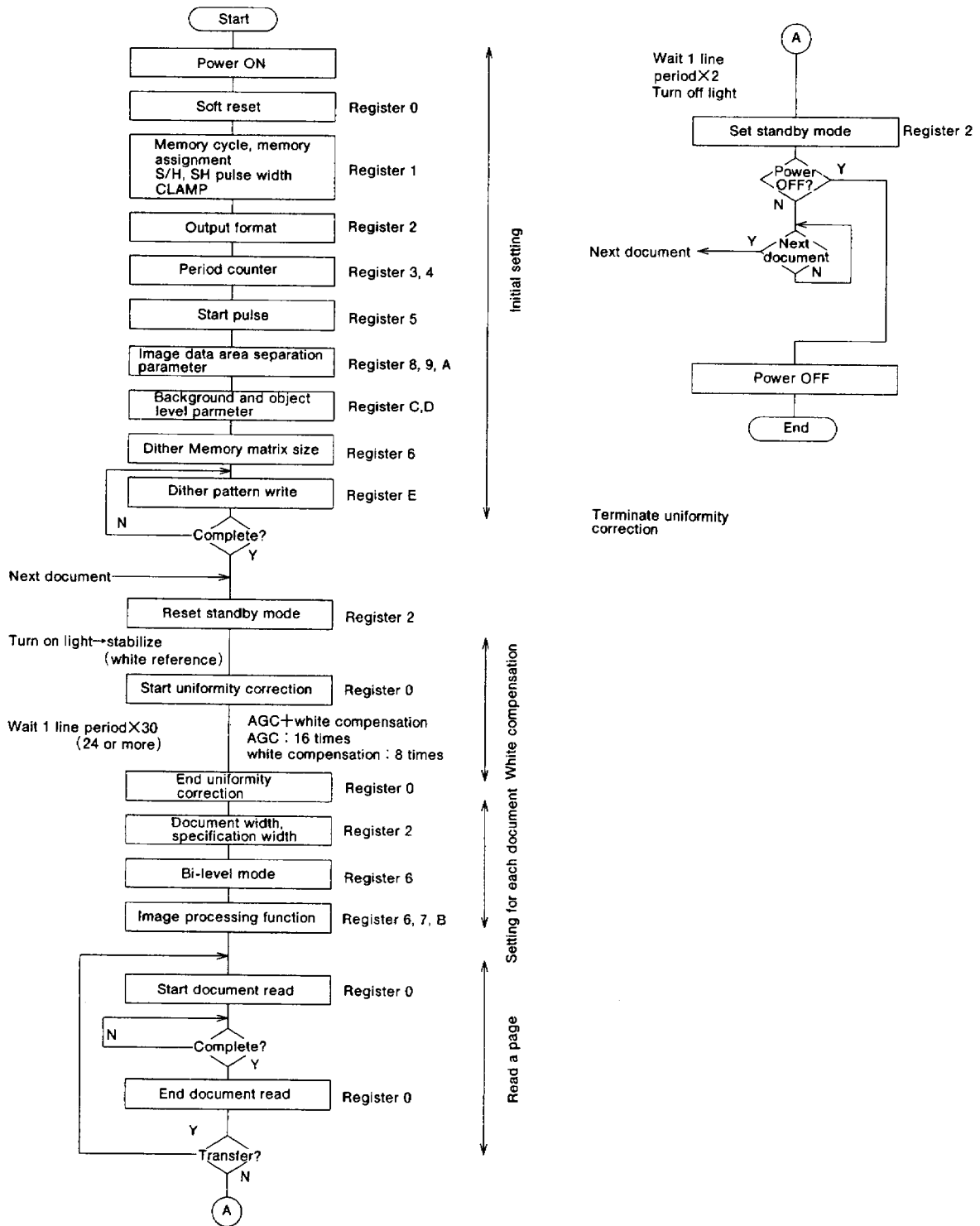


b) Write cycle (Write control Mode)



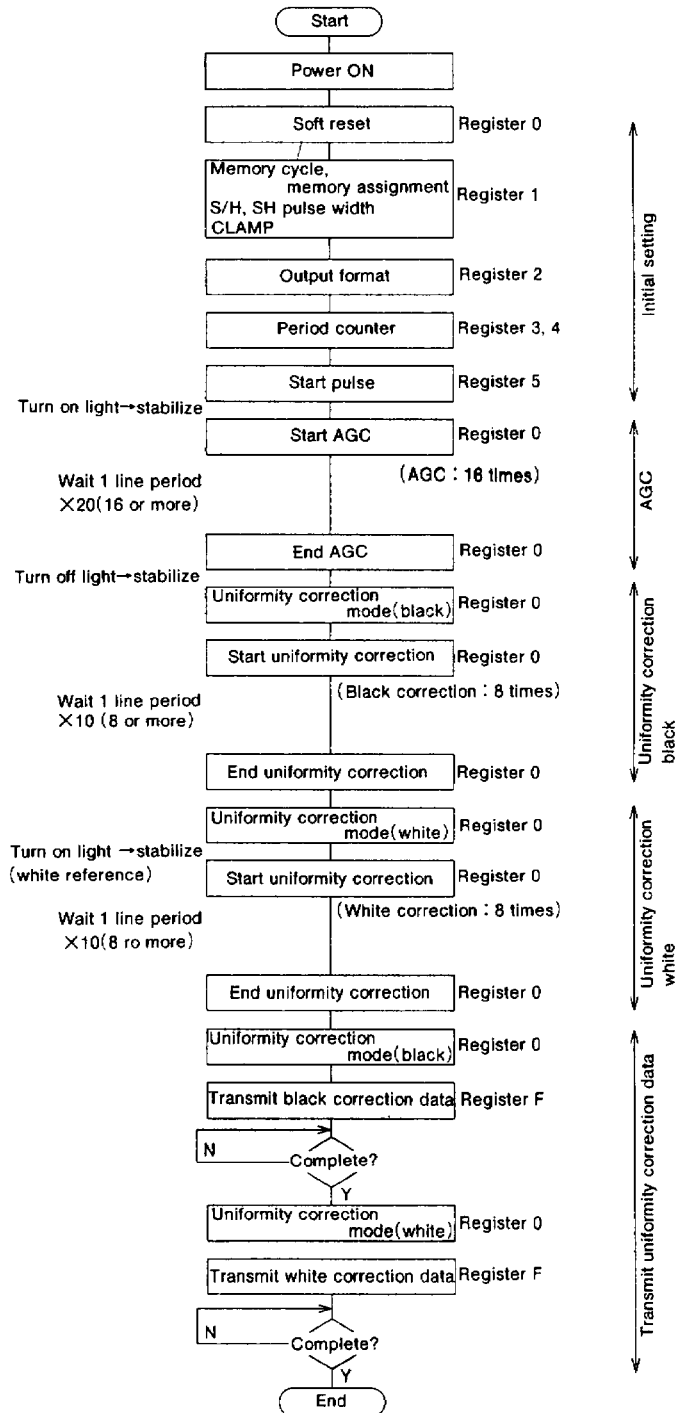
FACSIMILE IMAGE DATA PROCESSOR

Flowchart
Read Operation(Sensor : CCD)



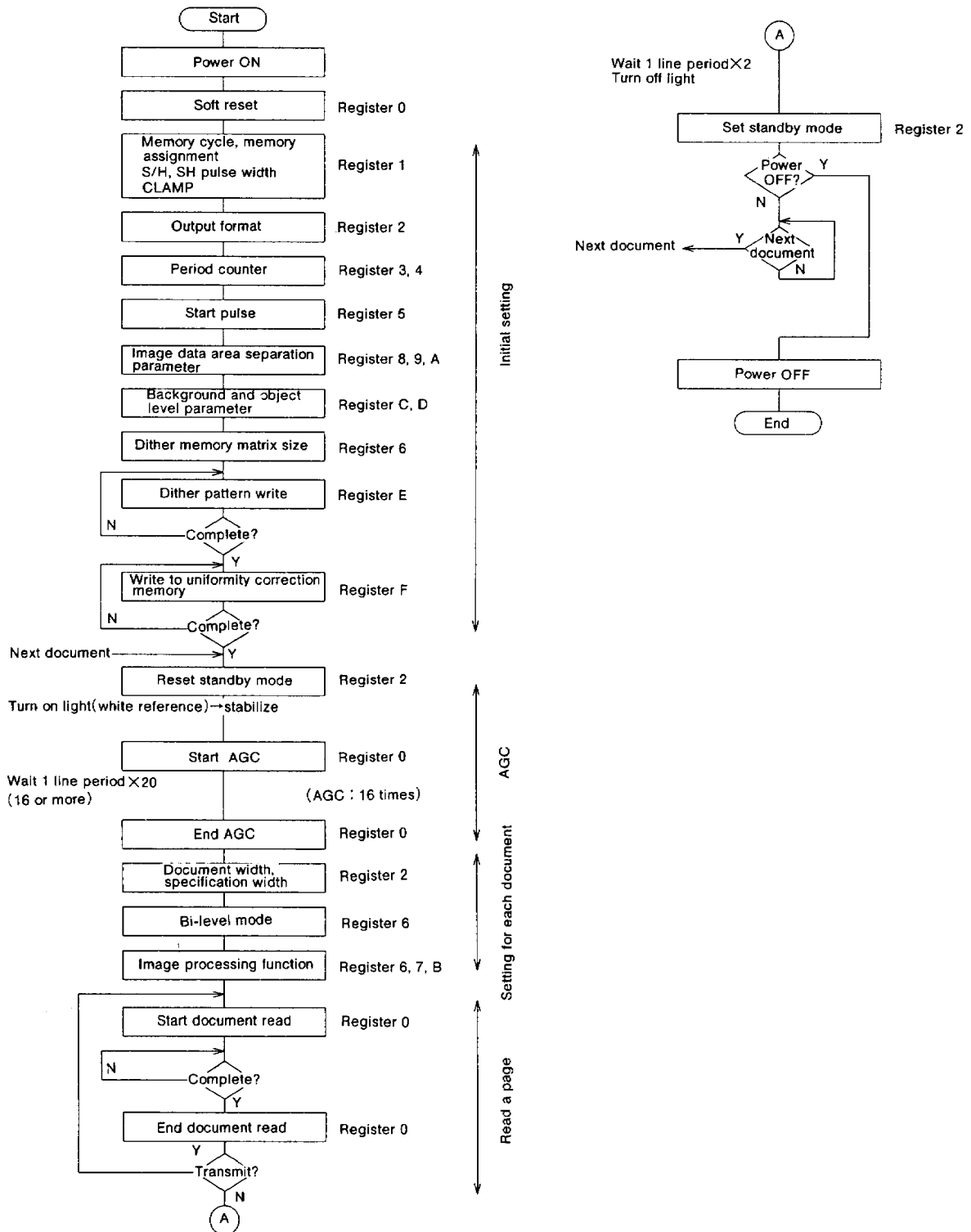
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Uniformity correction data creation, transmission(sensor : CIS)



FACSIMILE IMAGE DATA PROCESSOR

Read operation(sensor : CIS)



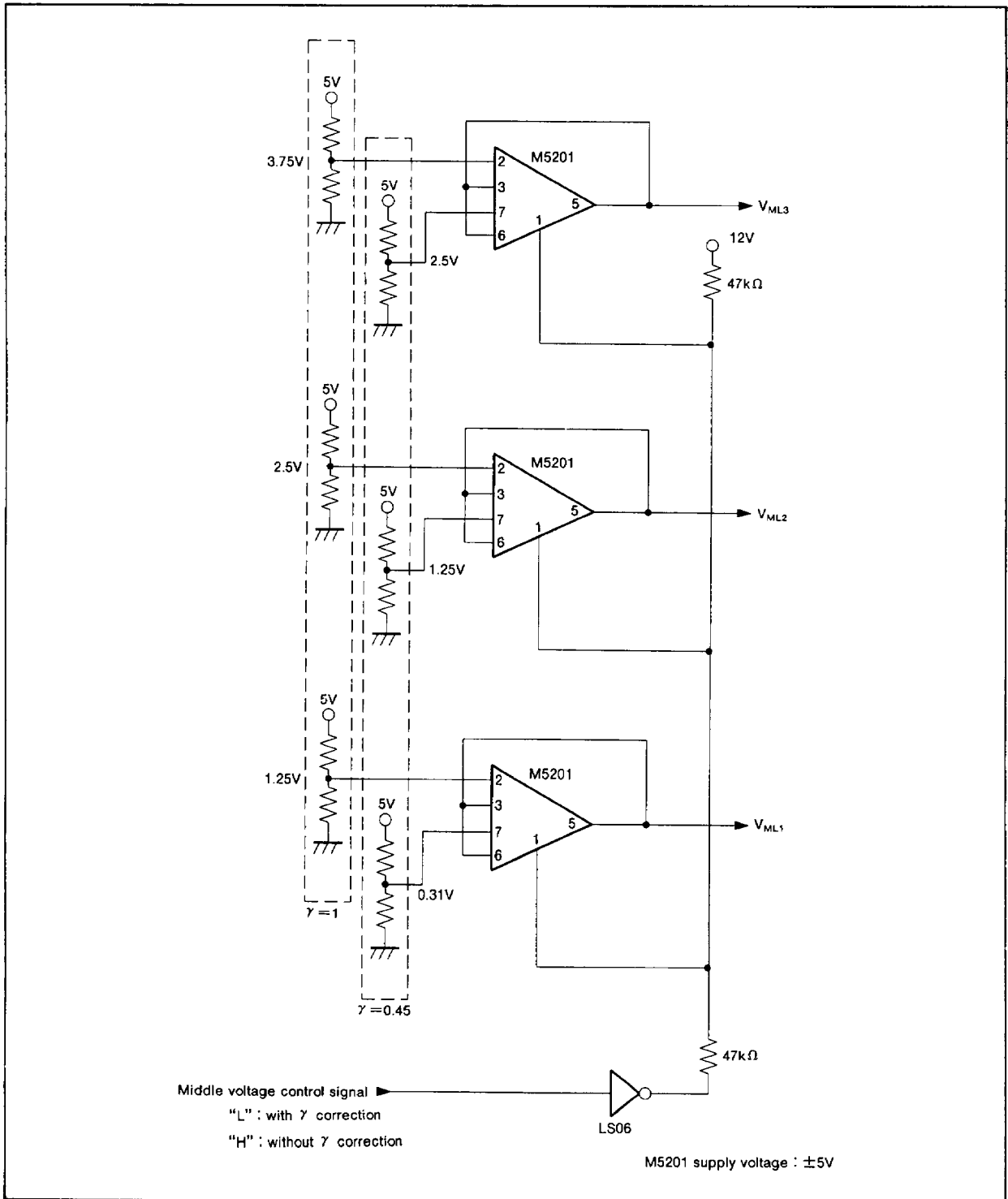


Fig. 19 Middle voltage control circuit example

FACSIMILE IMAGE DATA PROCESSOR

System Formation

