Document Title

64Kx36-Bit Synchronous Burst SRAM

Revision History

Rev. No.	History	Draft Date	Remark
0.0	Initial draft	July. 03. 1998	Preliminary
0.1	Change DC Characteristics. I_{CC} value from 320mA to 250mA at -7. I_{CC} value from 300mA to 230mA at -8. I_{CC} value from 280mA to 200mA at -9. I_{SB} value from 90mA to 70mA at -7. I_{SB} value from 80mA to 60mA at -8. I_{SB} value from 70mA to 50mA at -9. I_{SB1} value from 30mA to 20mA I_{SB2} value from 30mA to 20mA	Sep. 14. 1998	Preliminary
1.0	Final spec release.	Nov. 16. 1998	Fianl
2.0	Add V_{DDQ} Supply voltage(2.5V)	Dec. 02. 1998	Final
3.0	Min t_{OH} Parameter Change : from 2.0ns to 3.0ns Min t_{LZC} Parameter Change : from 0ns to 3ns	Dec. 17. 1998	Final

64Kx36-Bit Synchronous Burst SRAM

FEATURES

- Synchronous Operation.
- On-Chip Address Counter.
- Write Self-Timed Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 3.3V+0.3V/-0.165V Power Supply.
- V_{DDQ} Supply Voltage 3.3V+0.3V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- Asynchronous Output Enable Control.
- $\overline{\text{ADSP}}$, $\overline{\text{ADSC}}$, $\overline{\text{ADV}}$ Burst Control Pins.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention.
- TTL-Level Three-State Output.
- 100-TQFP-1420A

FAST ACCESS TIMES

PARAMETER	Symbol	-75	-80	-90	Unit
Cycle Time	t_{CYC}	8.5	10	12	ns
Clock Access Time	t_{CD}	7.5	8	9	ns
Output Enable Access Time	t_{OE}	3.5	3.5	3.5	ns

GENERAL DESCRIPTION

The K7B203625A is 2,359,296 bits Synchronous Static Random Access Memory designed to support zero wait state performance for advanced Pentium/Power PC based system. And with $\overline{\text{CS}}_1$ high, $\overline{\text{ADSP}}$ is blocked to control signals.

It can be organized as 64K words of 36 bits. And it integrates address and control registers, a 2-bit burst address counter and high output drive circuitry onto a single integrated circuit for reduced components counts implementation of high performance cache RAM applications.

Write cycles are internally self-timed and synchronous.

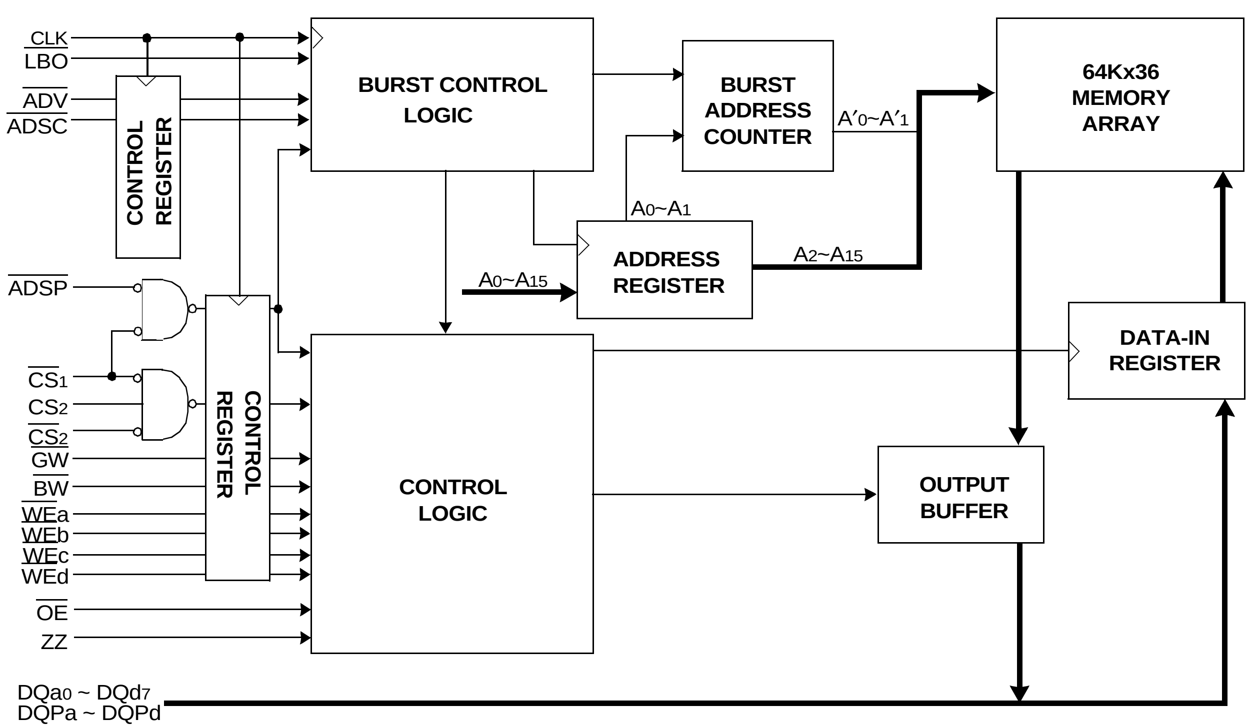
The self-timed write feature eliminates complex off chip write pulse shaping logic, simplifying the cache design and further reducing the component count.

Burst cycle can be initiated with either the address status processor($\overline{\text{ADSP}}$) or address status cache controller($\overline{\text{ADSC}}$) inputs. Subsequent burst addresses are generated internally in the system′s burst sequence and are controlled by the burst address advance($\overline{\text{ADV}}$) input.

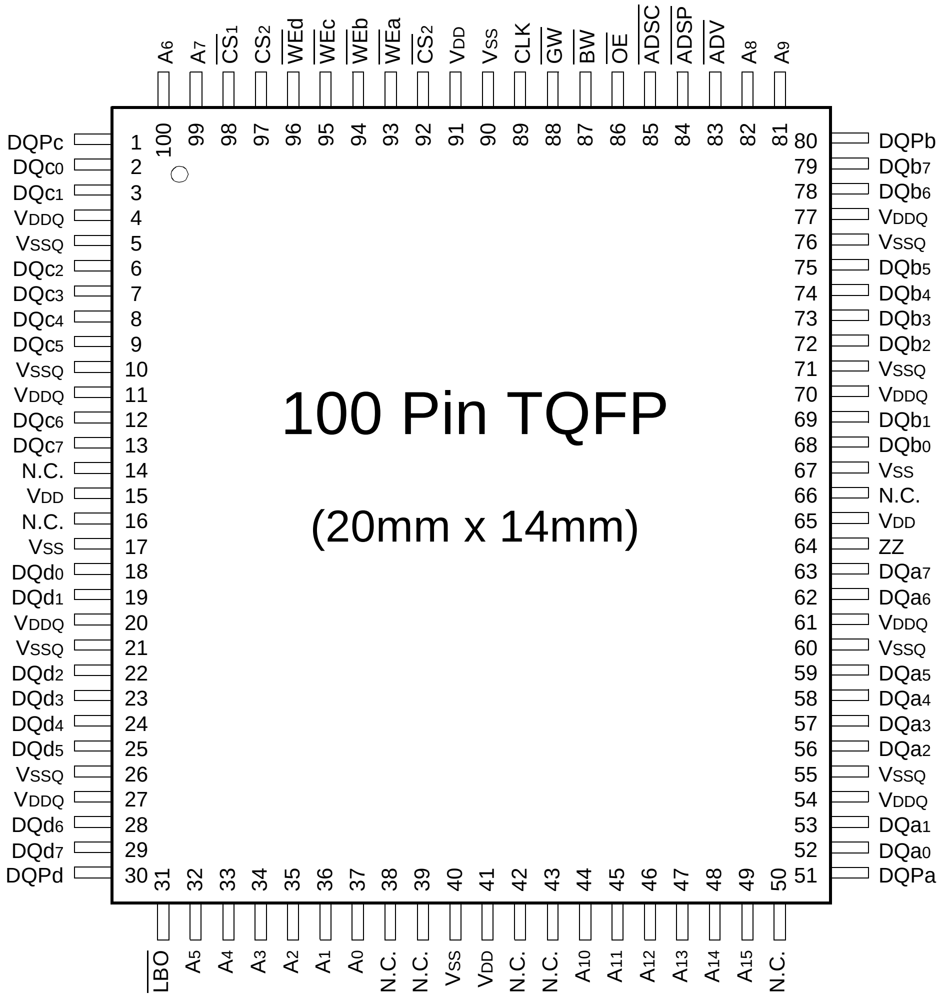
ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

The K7B203625A is implemented with SAMSUNG′s high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A15	Address Inputs	32,33,34,35,36,37,44,45,46,47,48,49,81,82,99,100	VDD VSS N.C.	Power Supply(+3.3V) Ground No Connect	15,41,65,91 17,40,67,90 14,16,38,39,42,43,50,66
ADV	Burst Address Advance	83			
ADSP	Address Status Processor	84	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
ADSC	Address Status Controller	85	DQb0~b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0~c7		2,3,6,7,8,9,12,13
CS1	Chip Select	98	DQd0~d7		18,19,22,23,24,25,28,29
CS2	Chip Select	97	DQPa~Pd		51,80,1,30
CS2	Chip Select	92			
WEx	Byte Write Inputs	93,94,95,96	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
OE	Output Enable	86			
GW	Global Write Enable	88	VSSQ	Output Ground	5,10,21,26,55,60,71,76
BW	Byte Write Enable	87			
ZZ	Power Down Input	64			
LBO	Burst Mode Control	31			

FUNCTION DESCRIPTION

The K7B203625A is a synchronous SRAM designed to support the burst address accessing sequence of the Pentium and Power PC based microprocessor. All inputs (with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, ADSP and ADV and chip select pins.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with ADSP(or ADSC) using the new external address clocked into the on-chip address register when both GW and BW are high or when BW is low and WEa, WEb, WEc, and WEd are high. When ADSP is sampled low, the chip selects are sampled active, and the output buffer is enabled with OE. the data of cell array accessed by the current address are projected to the output pins.

Write cycles are also initiated with ADSP(or ADSC) and are differentiated into two kinds of operations; All byte write operation and individual byte write operation.
All byte write occurs by enabling GW(independent of BW and WEx.), and individual byte write is performed only when GW is high and BW is low. In K7B203625A, a 64Kx36 organization, WEa controls DQa0 ~ DQa7 and DQPa, WEb controls DQb0 ~ DQb7 and DQPb, WEc controls DQc0 ~ DQc7 and DQPc and WEd controls DQd0 ~ DQd7 and DQPd.

CS_1 is used to enable the device and conditions internal use of ADSP and is sampled only when a new external address is loaded.

ADV is ignored at the clock edge when ADSP is asserted, but can be sampled on the subsequent clock edges. The address increases internally for the next access of the burst when ADV is sampled low.

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. And this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. LBO pin must be tied to high or low, and floating state must not be allowed.

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

OPERATION	ZZ	OE	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffersmust be disabled with OE, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADS}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	Operation
H	X	X	X	L	X	X	$\uparrow$	N/A	Not Selected
L	L	X	L	X	X	X	$\uparrow$	N/A	Not Selected
L	X	H	L	X	X	X	$\uparrow$	N/A	Not Selected
L	L	X	X	L	X	X	$\uparrow$	N/A	Not Selected
L	X	H	X	L	X	X	$\uparrow$	N/A	Not Selected
L	H	L	L	X	X	X	$\uparrow$	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	$\uparrow$	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	$\uparrow$	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	$\uparrow$	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	$\uparrow$	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	$\uparrow$	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	$\uparrow$	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	$\uparrow$	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	$\uparrow$	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	$\uparrow$	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	$\uparrow$	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don′t Care".
2. The rising edge of clock is symbolized by $\uparrow$.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
$\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don′t Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK($\uparrow$).

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to V_{SS}	V_{IO}	-0.3 to V_{DDQ} + 0.5	V
Power Dissipation	P_D	1.2	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Notes** : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C≤ T_A≤70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
	V_{DDQ}	3.135	3.3	3.6	V
Ground	V_{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.6	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	5	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

***Note :** Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(T_A=0 to 70°C, V_{DD}=3.3V+0.3V/-0.165V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Input Leakage Current(except ZZ)	I_{IL}	V_{DD}=Max , V_{IN}=V_{SS} to V_{DD}		-2	+2	µA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT}=V_{SS} to V_{DDQ}		-2	+2	µA
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ≤V_{IL}, All Inputs=V_{IL} or V_{IH} Cycle Time ≥ t_{CYC} min	-75	-	250	mA
			-80	-	230	
			-90	-	200	
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA, ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-75	-	70	mA
			-80	-	60	
			-90	-	50	
	I_{SB1}	Device deselected,I_{OUT}=0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	20	mA
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	20	mA
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL} = 1.0mA		-	0.4	V
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH} = -1.0mA		2.0	-	V
Input Low Voltage(3.3V I/O)	V_{IL}			-0.5*	0.8	V
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.5**	V
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.5**	V

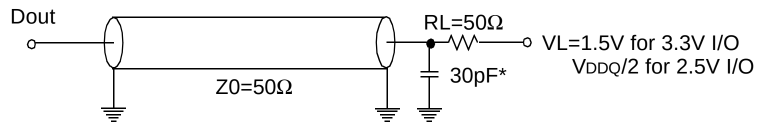
* V_{IL}(Min)=-2.0(Pulse Width ≤ t_{CYC}/2)
** V_{IH}(Max)=4.6(Pulse Width ≤ t_{CYC}/2)
** In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.5V

TEST CONDITIONS

(V_{DD}=3.3V+0.3V/-0.165V,V_{DDQ}=3.3V+0.3/-0.165V or V_{DD}=3.3V+0.3V/-0.165V,V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0 to 70°C)

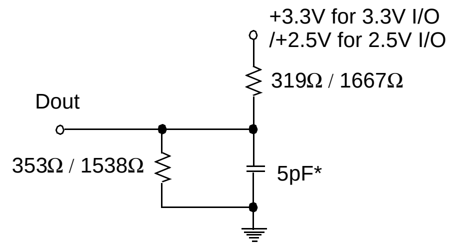
PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	1ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	1ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for t_{LZC}, t_{LZOE}, t_{HZOE} & t_{HZC})



* Including Scope and Jig Capacitance

Fig. 1

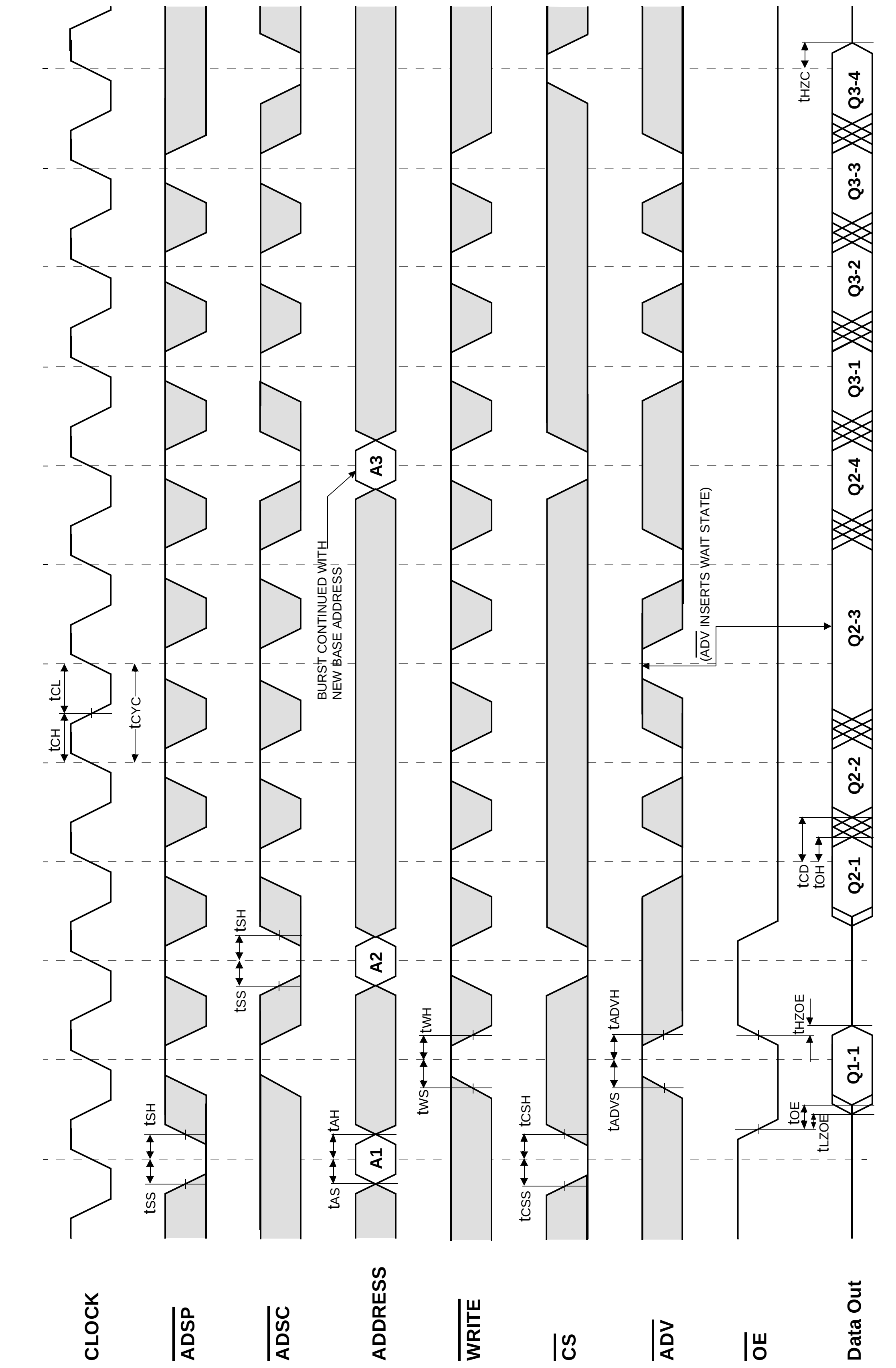
AC TIMING CHARACTERISTICS(T_A=0 to 70°C, V_{DD}=3.3V+0.3V/-0.165V)

PARAMETER	SYMBOL	-75		-80		-90		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CYC}	8.5	-	10	-	12	-	ns
Clock Access Time	t_{CD}	-	7.5	-	8	-	9	ns
Output Enable to Data Valid	t_{OE}	-	3.5	-	3.5	-	3.5	ns
Clock High to Output Low-Z	t_{LZC}	3	-	3	-	3	-	ns
Output Hold from Clock High	t_{OH}	3	-	3	-	3	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	3.5	-	3.5	-	3.5	ns
Clock High to Output High-Z	t_{HZC}	2	3.5	2	3.5	2	3.5	ns
Clock High Pulse Width	t_{CH}	3	-	4	-	4.5	-	ns
Clock Low Pulse Width	t_{CL}	3	-	4	-	4.5	-	ns
Address Setup to Clock High	t_{AS}	2.0	-	2.0	-	2.0	-	ns
Address Status Setup to Clock High	t_{SS}	2.0	-	2.0	-	2.0	-	ns
Data Setup to Clock High	t_{DS}	2.0	-	2.0	-	2.0	-	ns
Write Setup to Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}_x$)	t_{WS}	2.0	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	t_{ADVS}	2.0	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	t_{CSS}	2.0	-	2.0	-	2.0	-	ns
Address Hold from Clock High	t_{AH}	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High($\overline{GW}$, $\overline{BW}$, $\overline{WE}_x$)	t_{WH}	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	2	-	cycle

Notes :
1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and CS is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
2. Both chip selects must be active whenever ADSC or ADSP is sampled low in order for the this device to remain enabled.
3. ADSC or ADSP must not be asserted for at least 2 Clock after leaving ZZ state.
4. At any given voltage and temperature, t_{HZC} is less than t_{LZC}.

SAMSUNG ELECTRONICS

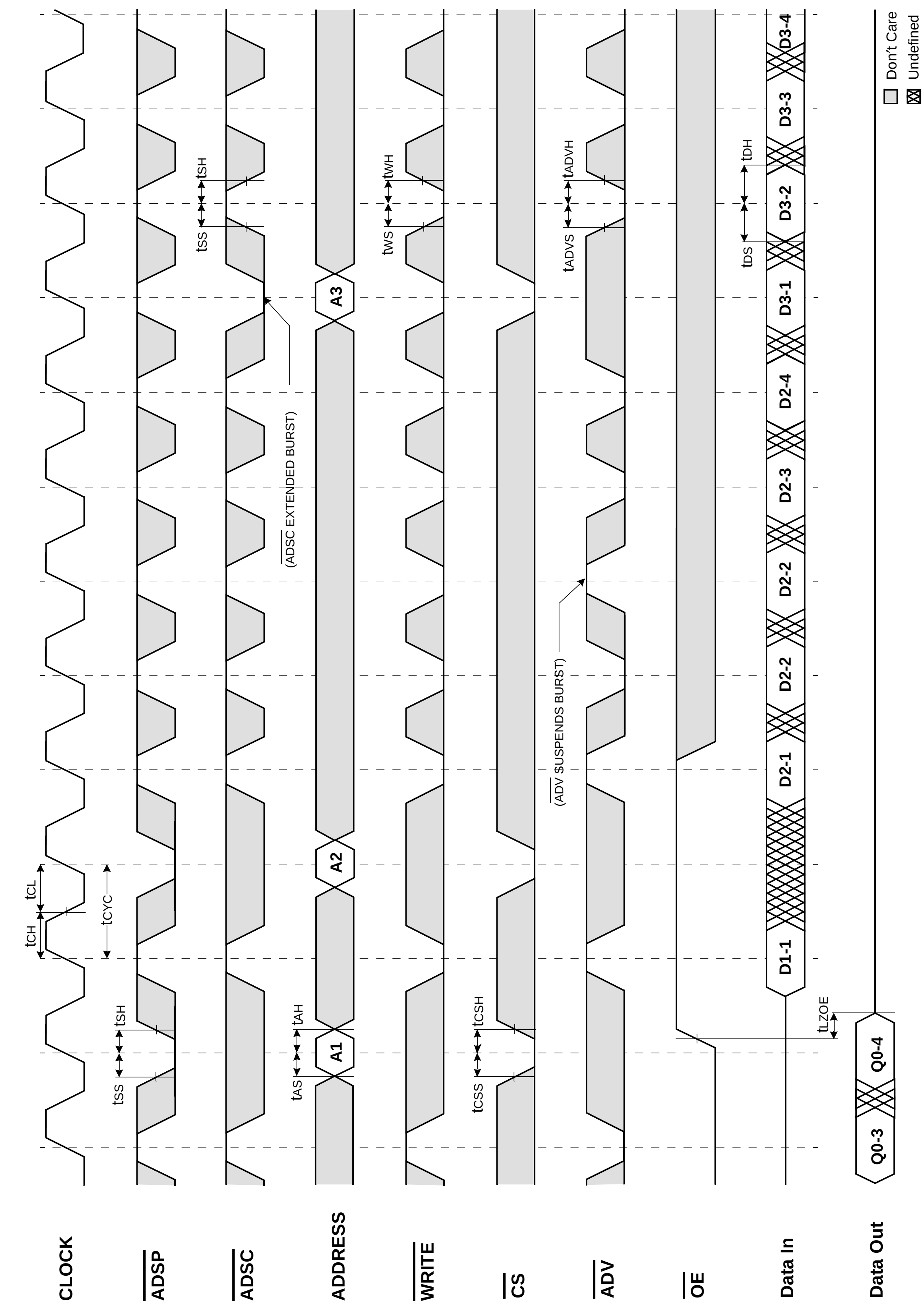
TIMING WAVEFORM OF READ CYCLE



Don't Care
Undefined

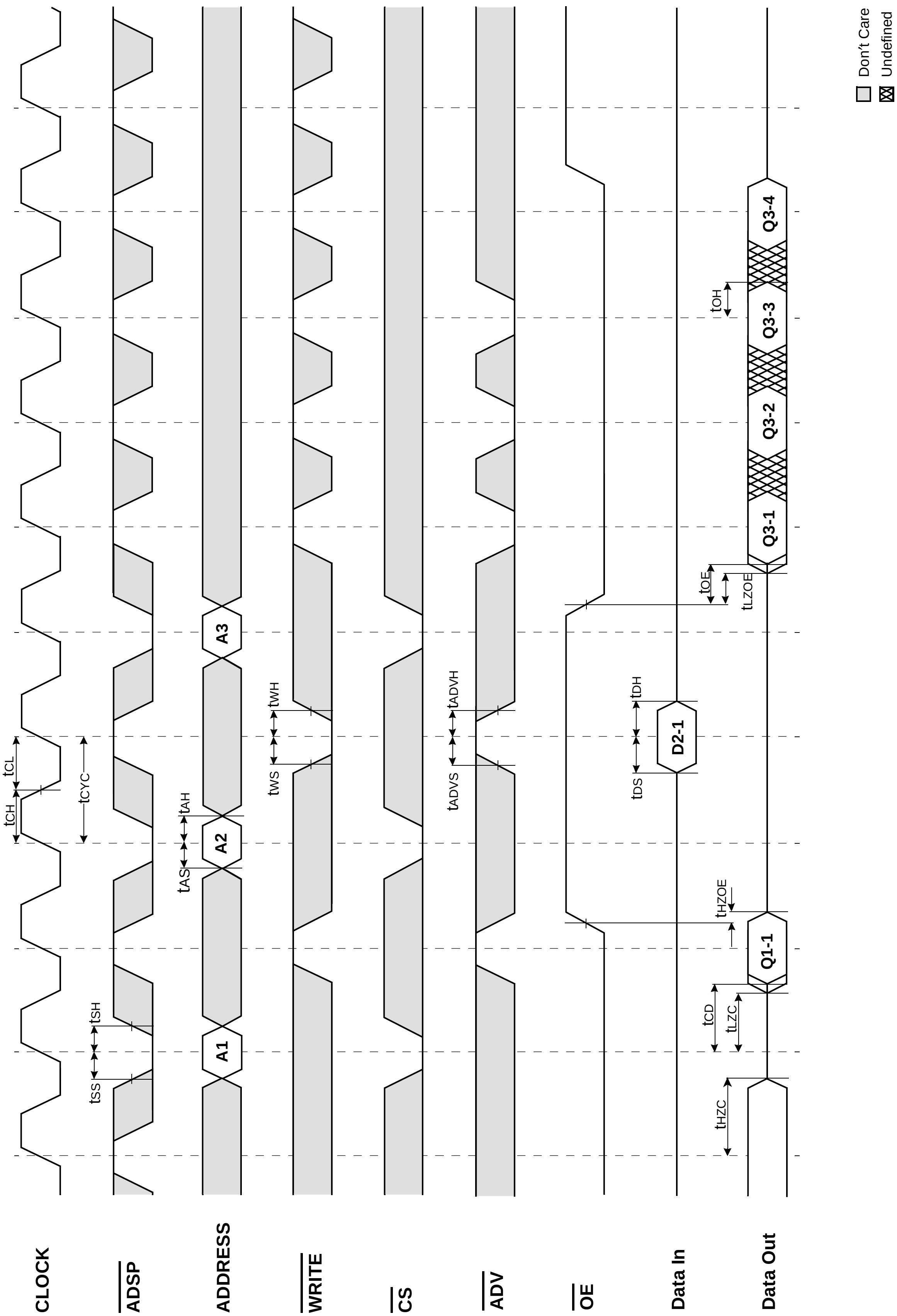
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WEx}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

TIMING WAVEFORM OF WRTE CYCLE

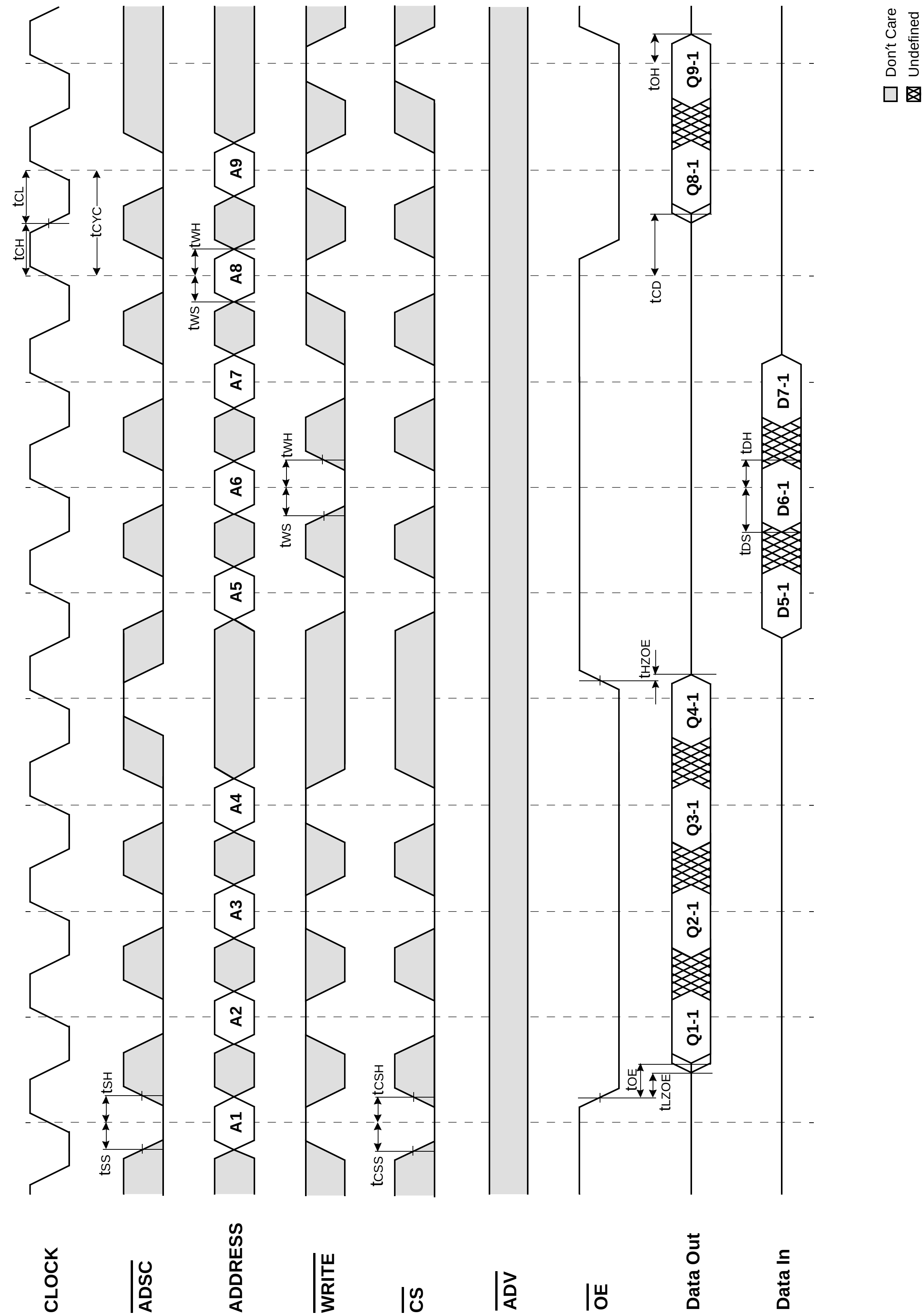


SAMSUNG ELECTRONICS

TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)

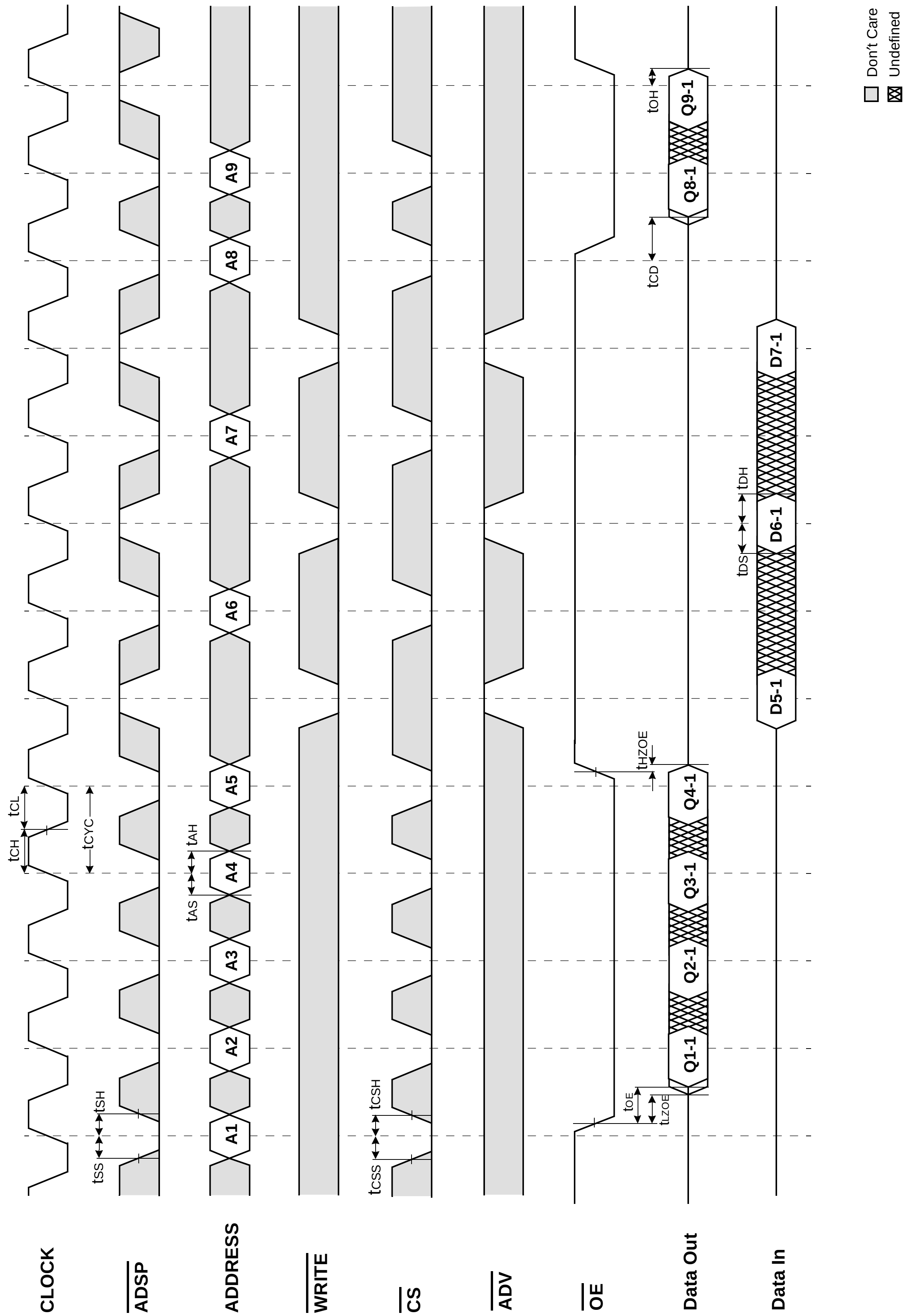


TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSC}$ CONTROLLED, $\overline{ADSP}$=HIGH)



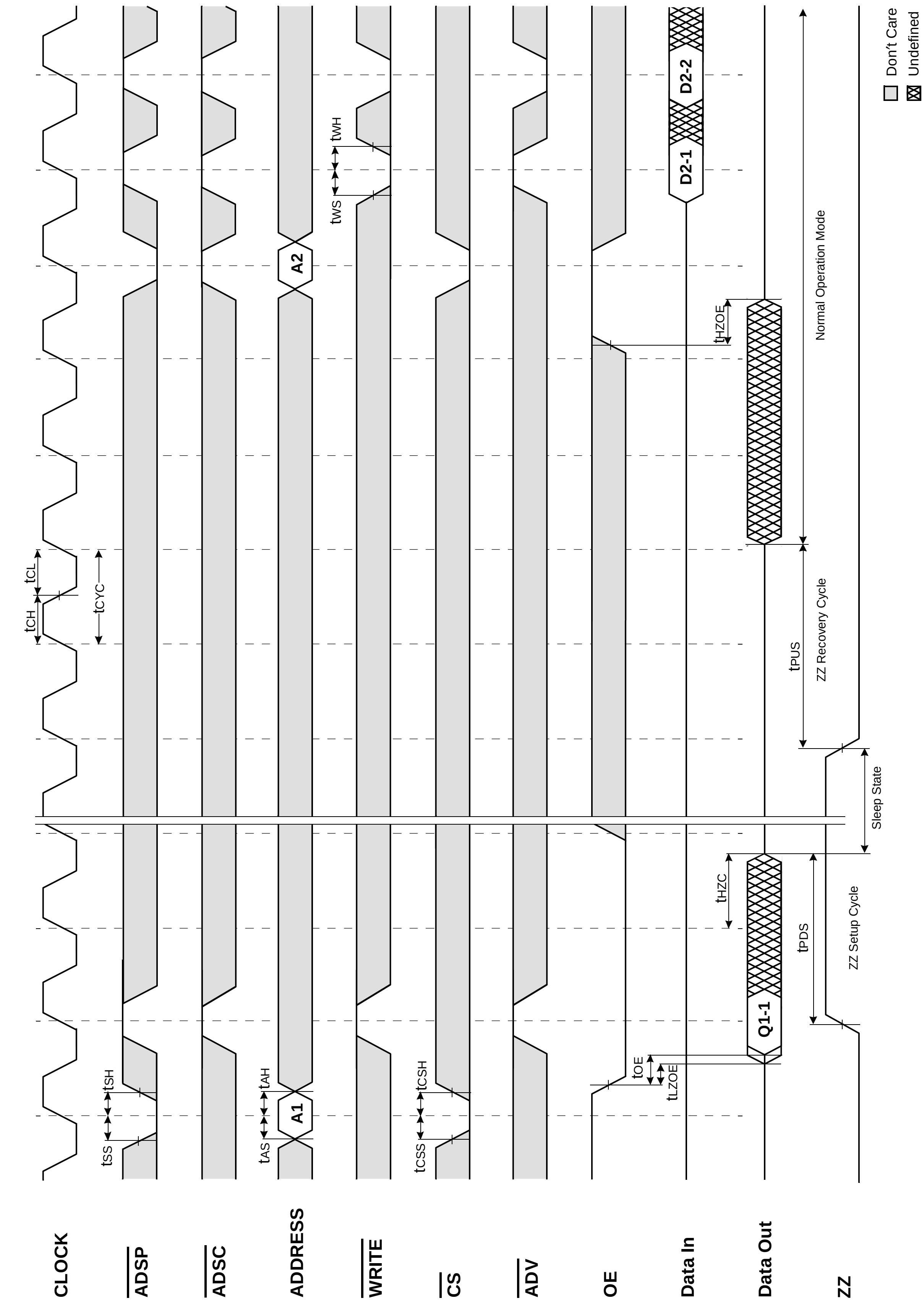
SAMSUNG ELECTRONICS

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE($\overline{ADSP}$ CONTROLLED, $\overline{ADSC}$=HIGH)



SAMSUNG ELECTRONICS

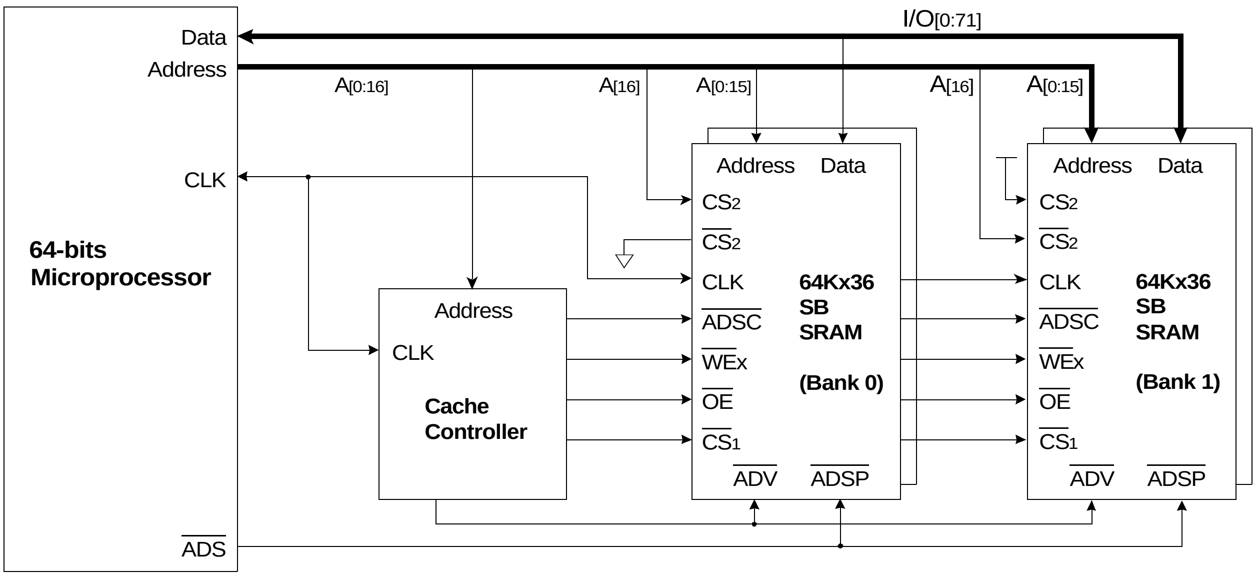
TIMING WAVEFORM OF POWER DOWN CYCLE



APPLICATION INFORMATION

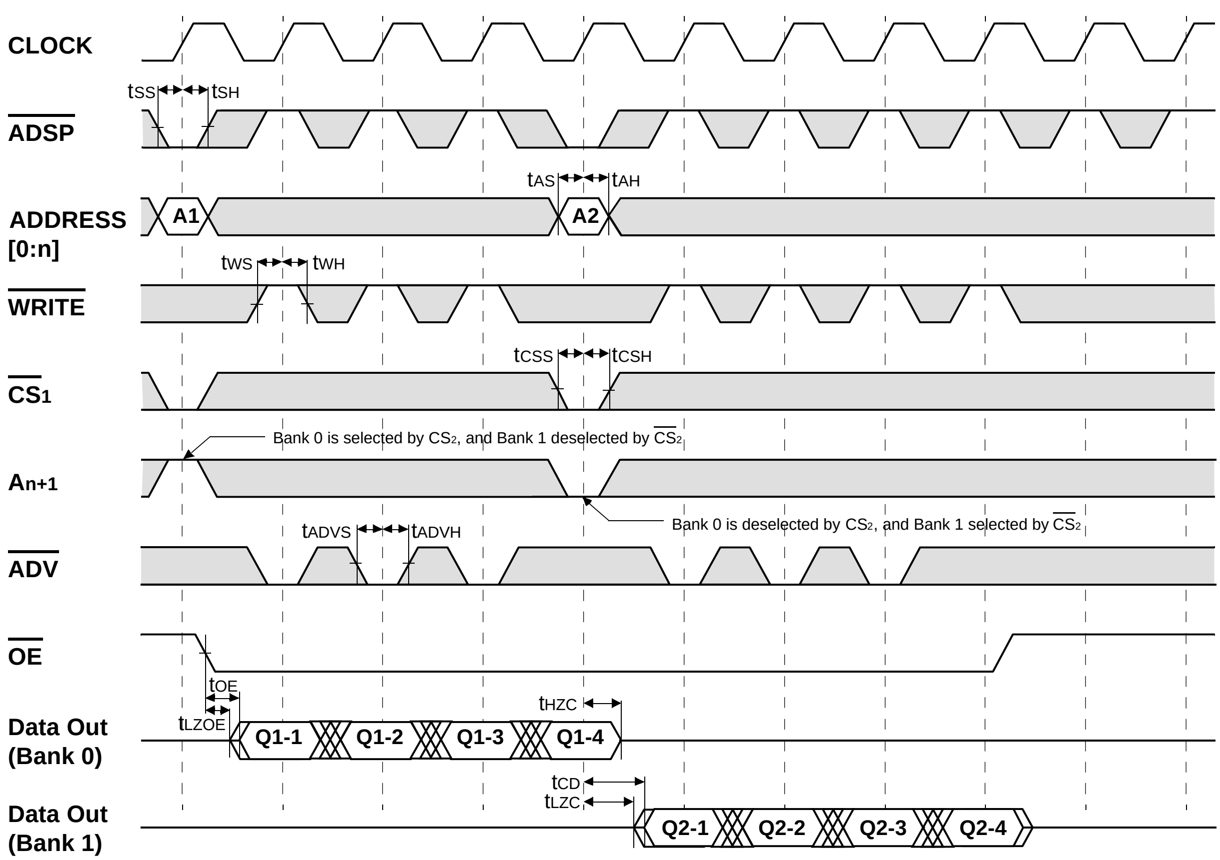
DEPTH EXPANSION

The Samsung 64Kx36 Synchronous Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 64K depth to 128K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HiGH)



*NOTES n = 14 32K depth, 15 64K depth, 16 128K depth

Don't Care Undefined

PACKAGE DIMENSIONS

100-TQFP-1420A

Units:millimeters/inches