Signetics

82S100/82S101

Field Programmable Logic Array

(16 × 48 × 8)

Military
Customer Specific Products

Product Specification

DESCRIPTION

The 82S100 (3-State) and 82S101 (Open-Collector) are bipolar, Fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs ANDed together comprise one P-term. All 48 P-terms are selectively ORed to each output. The user must then only select which P-term will activate an output by disconnecting terms which do not affect the output. In addition, each output can be fused as active-HIGH (H) or active-LOW (L).

The 82S100 and 82S101 are fully TTL compatible, and include chip enable control for expansion of input variables and output inhibit. They feature either Open-Collector or 3-State outputs for ease of expansion of product terms and application in bus-organized systems.

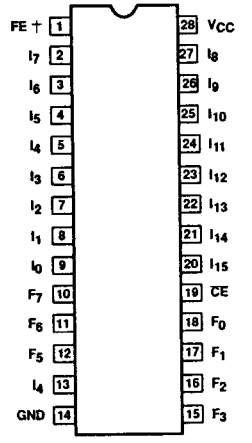
FEATURES

- Field-programmable (Ni-Cr link)
- Input variables: 16
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 80ns max
- Power dissipation: 600mW typ
- Input loading: -150μA max
- Chip enable input
- Output option:
  - 82S100: 3-State
  - 82S101: Open-Collector
- Output disable function;
  - 3-State: HI-Z
  - Open-Collector: HI
- Separate I/O architecture

APPLICATION

- CRT display systems
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Data security encoders
- Fault detectors
- Frequency synthesizers
- 16-bit to 8-bit bus interface
- Random logic replacement

PIN CONFIGURATION



NOTE:
† = Open or grounded during normal operation

For LLCC Pin Assignments, see JEDEC Std. No. 21

LOGIC FUNCTION

TYPICAL PRODUCT TERM:
$Pn = A \bullet \overline{B} \bullet C \bullet D$

TYPICAL LOGIC FUNCTION:
AT OUTPUT POLARITY = H
$Z = P0 + P1 + P2 \ldots$

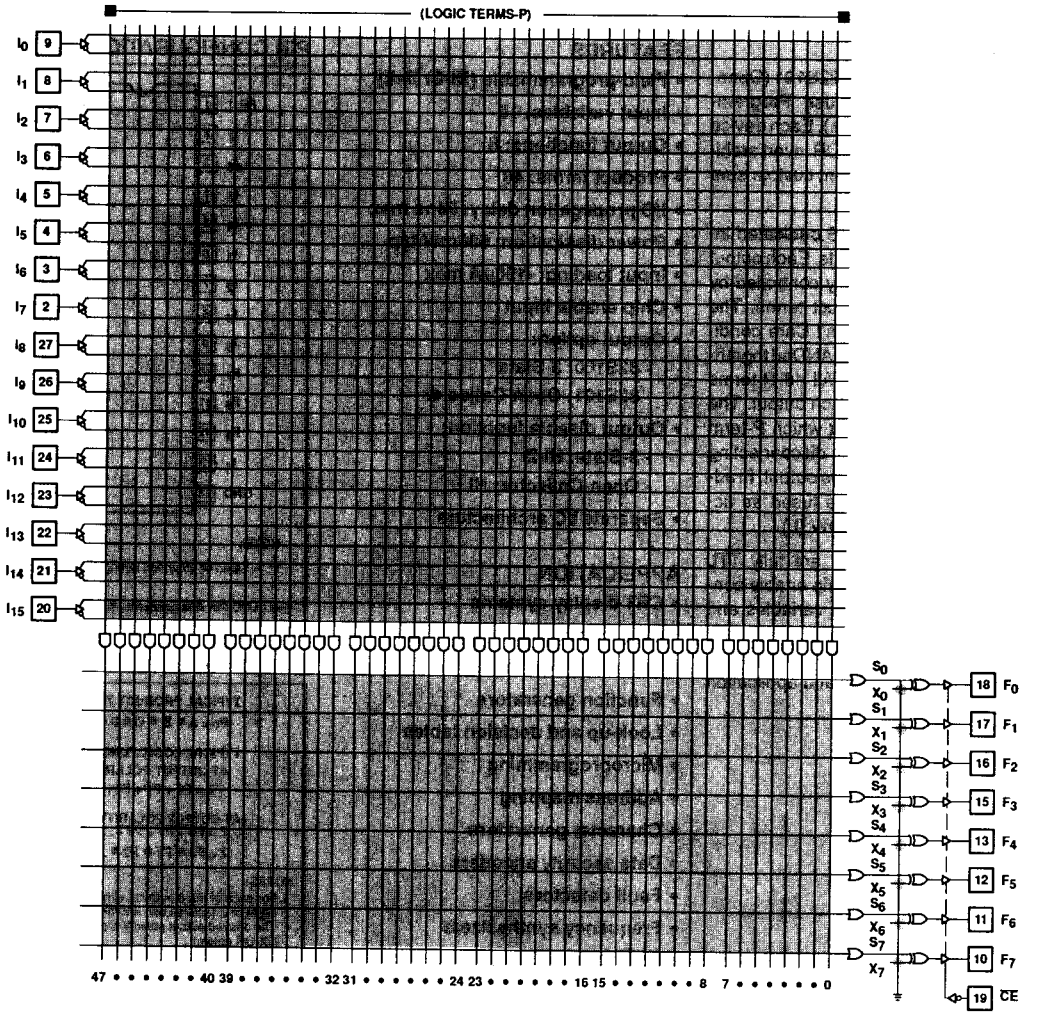
AT OUTPUT POLARITY = L
$\overline{Z} = P0 + P1 + P2 + \ldots$
$Z = \overline{P0} \bullet \overline{P1} \bullet \overline{P2} \bullet \ldots$

NOTES:
1. For each of the 8 outputs, either function Z (active-High) or $\overline{Z}$ (active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. Z, A, B, C etc. are user defined connections to fixed inputs (I) and output pins (O).

ORDERING INFORMATION

DESCRIPTION	3-STATE	OPEN-COLLECTOR
28-pin Ceramic DIP 600mil-wide	82S100/BXA	82S101/BXA
28-pin Ceramic Flat Pack	82S100/BYA	82S101/BYA
28-pin Ceramic LLCC	82S100/B3A	82S101/B3A

FPLA LOGIC DIAGRAM



NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. ▒ Programmable connection.

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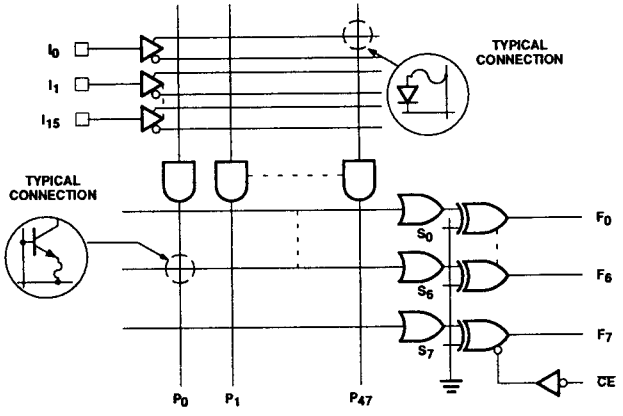
FUNCTIONAL DIAGRAM



Fusible Ni-Cr link are initially intack at all array cross-points.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Power supply voltage	+7	V_{DC}
V_I	Input voltage	+10.0	V_{DC}
V_O	Output voltage	+5.5	V_{DC}
I_I	Input currents	-30 to +30	mA
I_O	Output currents	+100	mA
T_A	Operating Temperature range	-55 to +125	°C
T_{STG}	Storage Temperature range	-65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS[3]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input Voltage						
V_{IH}	High	V_{CC} = 5.5V	2.0			V
V_{IL}	Low	V_{CC} = 4.5V			0.8	V
V_{IK}	Clamp[4]	V_{CC} = 4.5V, I_I = -18mA		-0.8	-1.2	V
Output Voltage						
V_{OH}	High (82S100)[5, 10]	V_{CC} = 4.5V I_{OH} = -2mA	2.4			V
V_{OL}	Low[6]	I_{OL} = 9.6mA		0.35	0.5	V
Input Current						
I_{IH}	High	V_{CC} = 5.5V V_I = 5.5V		<1	50	µA
I_{IL}	Low	V_I = 0.45V		-10	-150	µA
Output Current						
$I_{O(OFF)}$	Hi-Z State	$\overline{CE}$ = HIGH, V_{CC} = Max V_O = 5.5V		1	60	µA
	(82S100)	V_O = 0.45V		-1	-60	µA
I_{OS}	Short circuit (82S100)[4, 7, 10]	$\overline{CE}$ = LOW, V_O = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = 5.5V		120	180	mA
Capacitance[9]						
C_{IN}	Input	$\overline{CE}$ = HIGH V_{CC} = 5.0V V_I = 2.0V		8	13	pF
C_{OUT}	Output	V_O = 2.0V		17	22	pF

AC ELECTRICAL CHARACTERISTICS $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Propagation Delay							
T_{PD}	Input[11]	Output	Input		35	80	ns
T_{CE}	Chip enable	Output	Chip enable		15	40	
Disable Time							
T_{CD}	Chip disable	Output	Chip enable		15	40	ns

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one pin at a time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied through a resistor to V_{CC}.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input at a logic high, 1_1-1_{15} = GND.
9. Guaranteed, but not tested.
10. On unprogrammed device apply 10V - 1_1-I_{15}.
11. Not testable on unprogrammed device.

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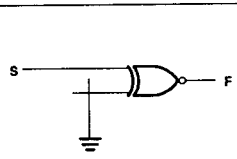
LOGIC PROGRAMMING

The FPLA can be programmed by means of Logic programming equipment.

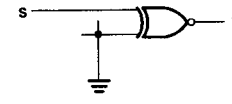
With Logic programming, the AND/OR/EX–OR gate input connections necessary to implement the desired logic function are coded directly from logic equations using the Program Table.

In this Table, the logic state or action of variables I, P and F, associated with each Sum Term S_n, is assigned a symbol which results in the proper fusing pattern of corresponding link pairs, defined as follows:

OUTPUT POLARITY – (F)

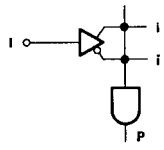


ACTIVE LEVEL	CODE
LOW	L

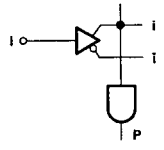


ACTIVE LEVEL	CODE
HIGH[12]	H

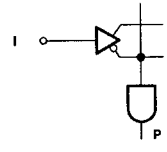
"AND" ARRAY – (I)



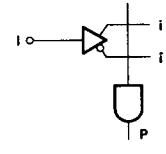
STATE	CODE
INACTIVE[12, 13]	O



STATE	CODE
I	H

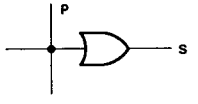


STATE	CODE
I	L

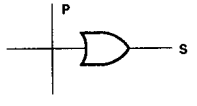


STATE	CODE
DON'T CARE	–

"OR" ARRAY – (F)



P_n STATUS	CODE
ACTIVE[12]	A



P_n STATUS	CODE
INACTIVE	•

NOTES:

12. This is the initial unprogrammed state of all links.
13. Any gate P_n will be unconditionally inhibited if any one of its (I) link pairs is left intact.

TIMING DEFINITIONS

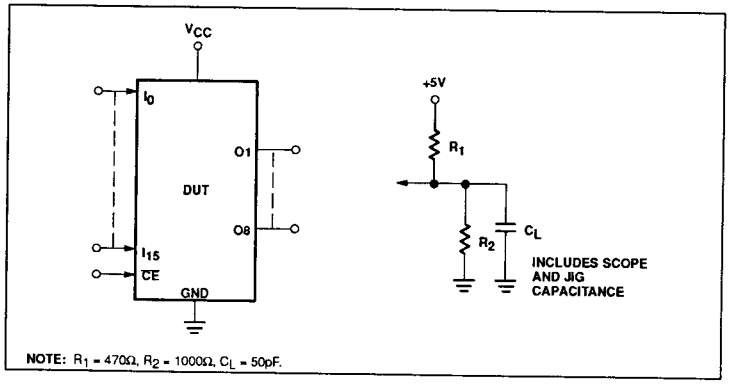
SYMBOL	PARAMETER
t_{CE}	Delay between beginning of Chip Enable Low (with input valid) and when Data Output becomes valid.
T_{CD}	Delay between when Chip Enable becomes High and Data Output is in Off-state (Hi-Z or High).
T_{PD}	Delay between beginning of valid input (with Chip Enable Low) and when Data Output becomes valid.

VIRGIN STATE

The 82S100/101 virgin devices are factory shipped in an unprogrammed state, characterized by:

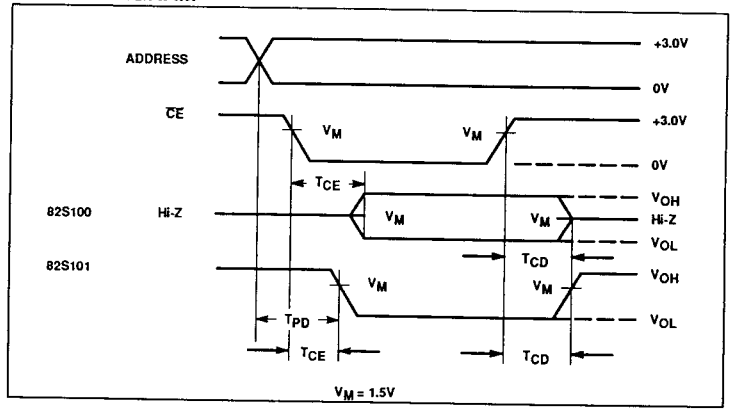
1. All internal Ni-Cr links are intact.
2. Each product term (P-term) contains both True and Complement values of every input variable I (P-terms always logically "false").
3. The "OR" Matrix contains all 48 P-terms.
4. The polarity of each output is set to active-High (Fp function).
5. All outputs are at a Low logic level.

TEST LOAD CIRCUITS

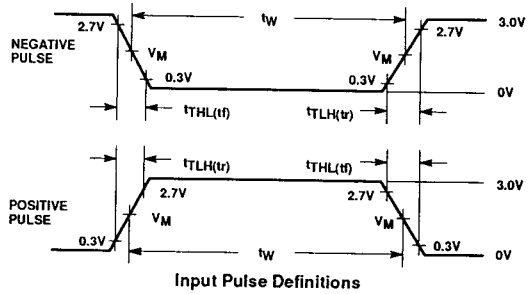


NOTE: R_1 = 470Ω, R_2 = 1000Ω, C_L = 50pF.

TIMING DIAGRAM



VOLTAGE WAVEFORM



Input Pulse Definitions

INPUT PULSE CHARACTERISTICS				
V_M	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
1.5V	1MHz	500ns	≤5ns	≤5ns

Signetics

Packaging Information

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Military Products

SIGNETICS STANDARD PACKAGE DESCRIPTIONS

All Military package case outlines and physical dimensions conform with the current revision MIL-M-38510, Appendix C, except for package types which are not included in that specification.

The physical dimensions for standard package types which are not included in Appendix C are included herein in Appendix C format. Case outline letters are assigned to these packages according to JEDEC Publication 101 as follows:

- U: Leadless chip carriers
- X: Dual-in-line packages
- Y: Flat packages
- Z: All other configurations

A case outline suffix number is assigned herein for identification purposes only, and is not marked on the product.

Signetics Military products are offered in a wide range of package configurations to optimally fit our customer needs.

- Dual-in-line Packages; Frit glass sealed CERDIP (F package family) with 8-40 leads, and side-brazed ceramic (I package family) with 48-64 leads.
- Flat Packages; Frit glass sealed alumina CERPAC (W package family) with 14-28 leads, and brazed leaded ceramic (Q package family) with 52 leads.
- Ceramic Chip Carriers; triple laminated, metal-lidded LCC (G package family) with 20-68 terminals.
- Pin Grid Array; metal-lidded ceramic pin grid (P package family) with 68-100 leads.
- Shown in Table 1 are the case outline letters assigned according to Appendix C of MIL-M-38510 and JEDEC publication 101. Unless otherwise noted, all package types are Configuration 1 and all lead finishes are hot solder dip Finish "A".

Table 1.

Package Description	Type Designation	Case Outline	Theta-JC °C/Watt[4]
8DIP3	D-4	P	28
14DIP3	D-1	C	28
16DIP3	D-2	E	28
18DIP3	D-6	V	28
20DIP3	D-8	R	28
22DIP4	D-7	W	28
24DIP3	D-9	L	28
24DIP4	D-11	X[2]	28
24DIP6	D-3	J	28
28DIP6	D-10	X[2]	28
40DIP6	D-5	Q	28
48DIP6	D-14[1]	X[2]	28
50DIP9	D-12[1]	X[2]	28
64DIP9	D-13[1]	X[2]	28
14FLAT	F-2	D	22
16FLAT	F-5	F	22
18FLAT	F-10	Y[2]	22
20FLAT	F-9	S	22
24FLAT	F-6	K	22
28FLAT	F-11	Y[2]	22
52FLAT	Y-1[1]	Y[2]	22
18LLCC	C-9	U[2]	20
20LLCC	C-2[3]	2	20
28LLCC	C-4[3]	3	20
32LLCC	C-12	U[2]	20
44LLCC	C-5	U[2]	20
68LLCC	C-7	U[2]	20
68PGA	P-AB	Z[2]	20
84PGA	P-AB	Z[2]	20

NOTES:
1. Configuration 2.
2. Per JEDEC publication 101.
3. Dimension A (LLCC thickness) is 75mils maximum.
4. See RADC test report RADC-TR-86-97 for thermal resistance confidence and derating.

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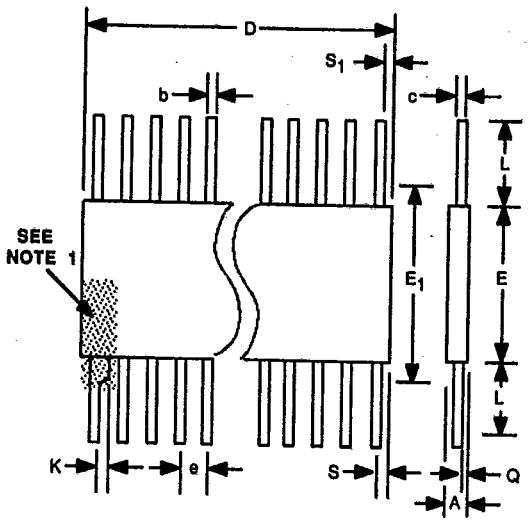
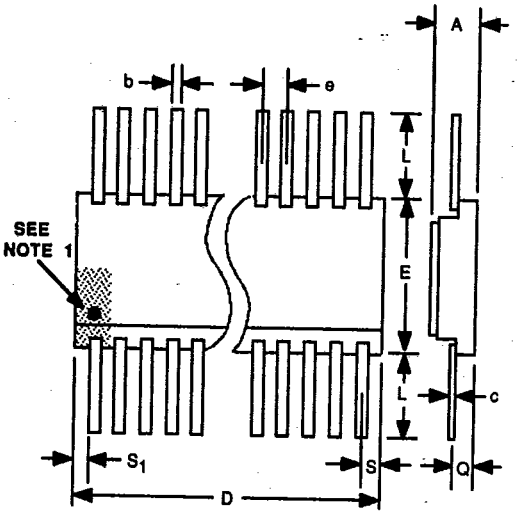
Packaging Information

CASE OUTLINES Y (FLAT PACKAGES)



Configuration 1



Configuration 2

NOTES:

1. A lead tab (enlargement) or index dot is located within the shaded area shown at Pin 1. Other pin numbers proceed sequentially from Pin 1 counterclockwise (as viewed from the top of the device).
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The reference pin spacing is 0.050 between centerlines. Each pin centerline is located within ± 0.005 of its logitudinal position relative to the first and last pin numbers.
4. This dimension is measured at the point of exit of the lead body.
5. This dimension applied to all four corner pins.
6. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

OUTLINE	Y1		NOTES
CONFIGURATION	2		
NO. LEADS	52		
SIG. PKG.	QP		
SYMBOL	INCHES		
	Min	Max	
A	0.045	0.100	
b	0.015	0.026	6
c	0.008	0.015	6
D	- -	1.330	2
E	0.620	0.660	
e	0.050 BSC		3
L	0.250	0.370	
Q	0.054	0.0666	4
S	-	0.045	5
S1	0.005	-	5

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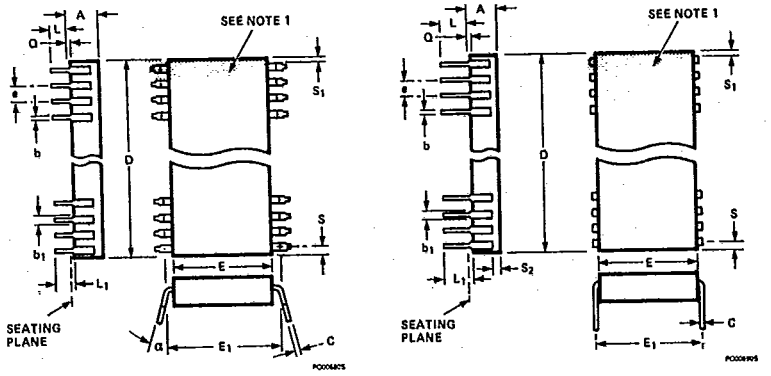
Packaging Information

CASE OUTLINES X (DUAL IN-LINE PACKAGES)



Configuration 1 Configuration 2

1. An index notch is located within the shaded area shown. Pin 1 is adjacent to the notch to the immediate left (as viewed from the top of the device) and other pin numbers proceed sequentially from Pin 1 counterclockwise.
2. The minimum limit for Dimension b1 is 0.023 inches for all four corner pins.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. This dimension is measured at the centerline of the leads for Configuration 2.
5. The reference pin spacing is 0.100 between centerlines. Each pin centerline is located within ±0.010 of its longitudinal position relative to the first and last pin numbers.
6. This dimension is measured from the seating plane to the base plane.
7. This dimension applies to all four corner pins.
8. Lead dimensions include 0.003 inch allowance for hot solder dip lead finish.

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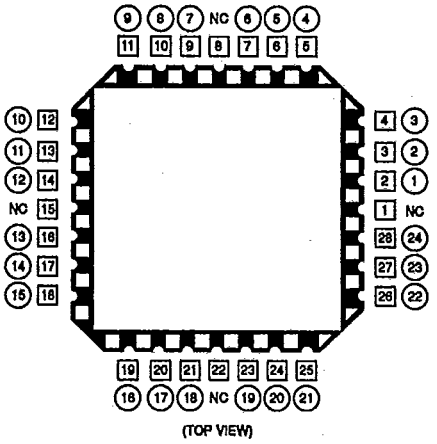
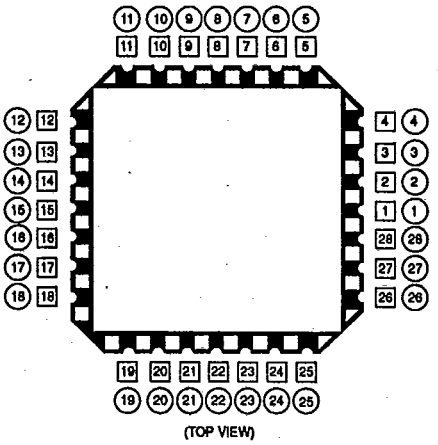
Packaging Information

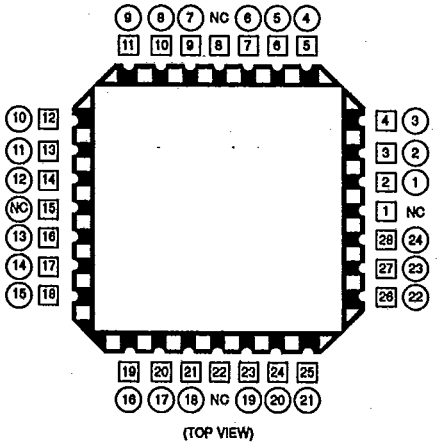
LEADLESS CHIP CARRIER (LLCC) PINOUTS



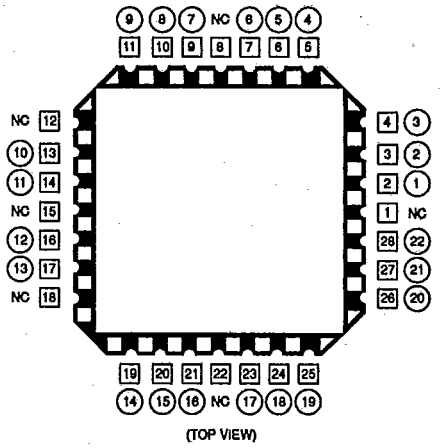
24–Lead Logic Pinout for 28 Terminal Chip Carrier



26–Lead Pinout for 28 Terminal Chip Carrier for all Device Types



24–Lead Memory Pinout for 28 Terminal Chip Carrier



22–Lead Memory Pinout for 28 Terminal Chip Carrier

□ = Chip Carrier Terminal Number
○ = Dual In-Line Lead Number
NC = No Connect