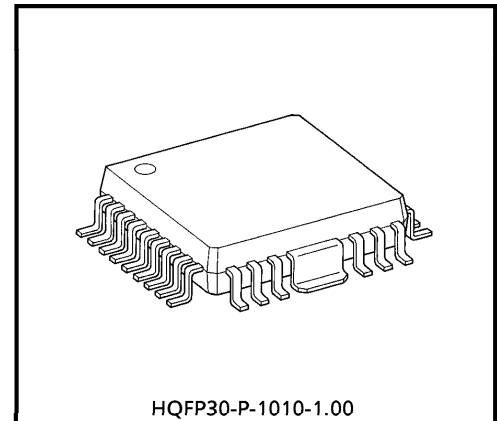


TENTATIVE TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

**TA1248F****I/Q DEMODULATION IC FOR DIGITAL SATELLITE RECEIVER****FEATURES**

- Supply voltage : 5V
- Second IF AGC amp
- dB-linear signal level amp
- Sync, quasi-sync detect PLL
- 90° phase shifter
- Baseband output amp
- HQFP30-P-1010 ideal for surface mounting



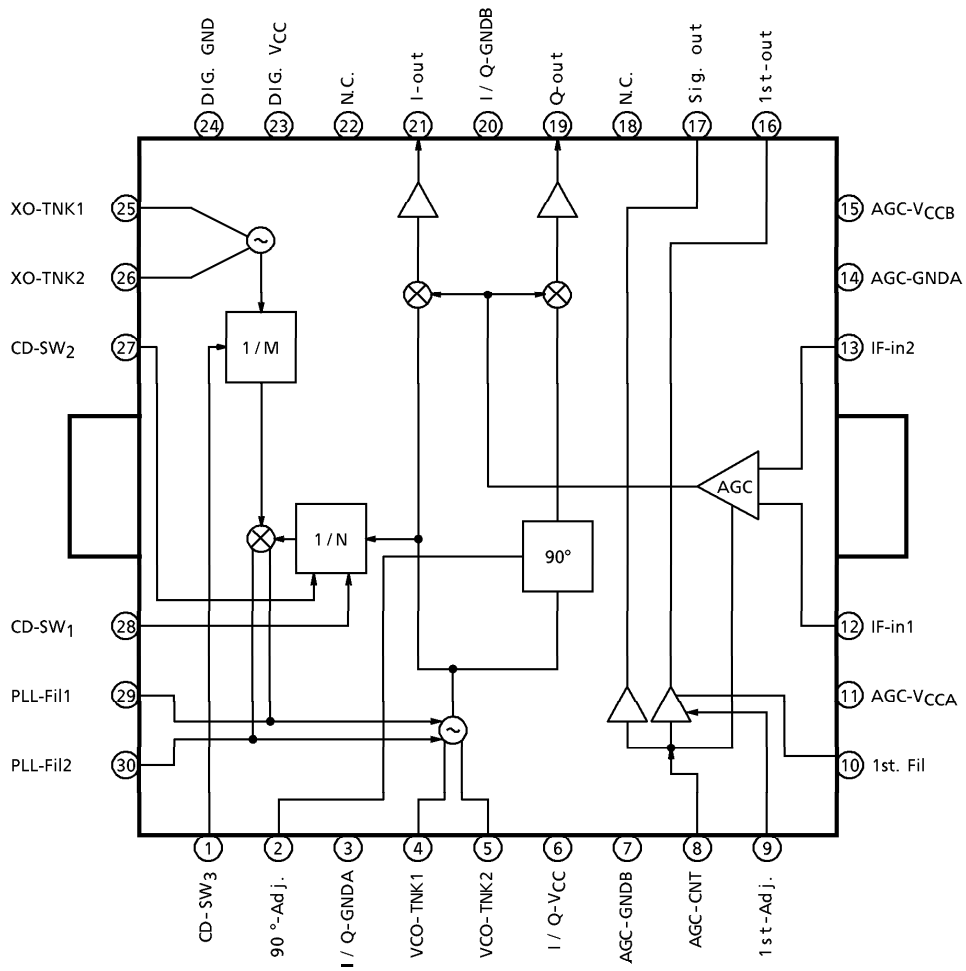
Weight : 0.61g (Typ.)

(Note) : These devices are easy to be damaged by high static voltage or electric fields.  
In regards to this, please handle with care.

000707EBA1

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BLOCK DIAGRAM



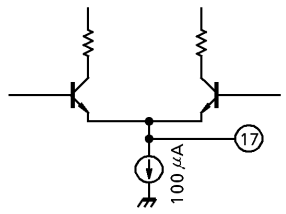
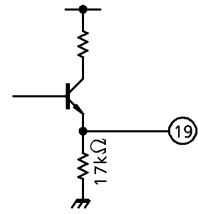
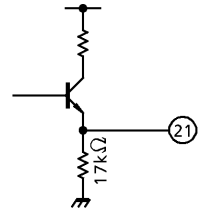
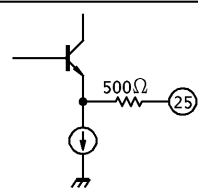
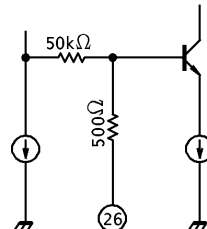
(Note 1) M : XO divider ratio (1/1, 1/2)

(Note 2) N : VCO divider ratio (1/32, 1/64, 1/128, 1/256)

**TERMINAL FUNCTIONS**

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT						
1	XO divider ratio switch	Switches XO divider ratio. <table border="1" style="display: inline-table; margin-right: 20px;"> <tr> <th>SW-3</th> <th>DIVIDER RATIO</th> </tr> <tr> <td>0</td> <td>1/1</td> </tr> <tr> <td>1</td> <td>1/2</td> </tr> </table> (Note) 0 : GND 1 : VCC or open	SW-3	DIVIDER RATIO	0	1/1	1	1/2	
SW-3	DIVIDER RATIO								
0	1/1								
1	1/2								
2	90° phase shifter adjust pin	Fine-adjusts phase difference between I and Q outputs. IC internal bias is $\frac{1}{2}V_{CC}$ .							
3	I/Q GND-A	I/Q block GND pin A	—						
4 5	VCO tank	VCO which uses internal impedance of diode corresponding to control voltage from PLL block. To compensate for internal temperature drift, use a capacitor with UJ characteristic for external tank circuit.							
6	I/Q VCC	I/Q block power supply pin	—						
7	AGC GND-B	AGC block GND pin B	—						
8	AGC control pin	Gain changes according to applied voltage.							

PIN No.	PIN NAME	FUNCTIONS	INTERFACE CIRCUIT
9	First AGC delay point adjust pin	Because control signal is generated to previous stage second converter block of AGC circuit at excess input to IC, sets input level threshold.	
10	First AGC filter	Outputs the result of comparing AGC voltage with first AGC delay point voltage. The comparator is configured with an active load type high gain amp. The active low pass filter is constructed by the capacitance connected to this pin.	
11	AGC V <sub>CC</sub> -A	AGC block power supply pin A	—
12 13	IF input pins	IF input pins. For unbalanced input, ground one of these pins via a capacitor.	
14	AGC GND-A	AGC block GND pin A	—
15	AGC V <sub>CC</sub> -B	AGC block power supply pin B	—
16	First AGC output pin	Outputs control voltage via an emitter follower.	

PIN No.	PIN NAME	FUNCTIONS	INTERFACE CIRCUIT
17	Signal level output pin	Outputs AGC voltage after conversion.	
18	N. C.	Leave this pin open.	—
19	Q signal output	Q signal output pin	
20	I/Q GND-B	I/Q block GND pin B	—
21	I signal output	I signal output pin	
22	N. C.	Leave this pin open.	—
23	90° phase shifter V <sub>CC</sub>	Power supply of 90° phase shifter block	—
24	90° phase shifter GND	GND pin of 90° phase shifter block	—
25	Crystal oscillator	Crystal oscillator used as reference for PLL operation. For external input, input from pin 26.	
26			

PIN No.	PIN NAME	FUNCTIONS	INTERFACE CIRCUIT														
27	VCO divider ratio switch 2	VCO divider switch pin															
28	VCO divider ratio switch 1	<table border="1"> <thead> <tr> <th>SW-1</th> <th>SW-2</th> <th>DIVIDER RATIO</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1/32</td> </tr> <tr> <td>0</td> <td>1</td> <td>1/64</td> </tr> <tr> <td>1</td> <td>0</td> <td>1/128</td> </tr> <tr> <td>1</td> <td>1</td> <td>1/256</td> </tr> </tbody> </table> <p>(Note) 0 : GND 1 : VCC or open</p>		SW-1	SW-2	DIVIDER RATIO	0	0	1/32	0	1	1/64	1	0	1/128	1	1
SW-1	SW-2	DIVIDER RATIO															
0	0	1/32															
0	1	1/64															
1	0	1/128															
1	1	1/256															
29 30	Loop filter	Low-pass filter for PLL block connecting pin															

**MAXIMUM RATINGS (Ta = 25°C)**

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V <sub>CC</sub> MAX	6.0	V
Power Dissipation	P <sub>D</sub> MAX	1080	mW
Operating Temperature	T <sub>opr</sub>	-20~75	°C
Storage Temperature	T <sub>stg</sub>	-55~150	°C

(Note) When using the device at above Ta = 25°C, decrease the power dissipation by 8.7mW for each increase of 1°C.

**RECOMMENDED OPERATING CONDITION**

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
6	I/Q V <sub>CC</sub>	4.5	5.0	5.5	V
11	AGC V <sub>CCA</sub>	4.5	5.0	5.5	V
15	AGC V <sub>CCB</sub>	4.5	5.0	5.5	V
23	DIG. V <sub>CC</sub>	4.5	5.0	5.5	V

**ELECTRICAL CHARACTERISTICS**

DC CHARACTERISTICS (Unless otherwise specified,  $V_{CC} = 5.0V$ ,  $T_a = 25^\circ C$ )

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Supply And Current		$I_{CC}$	1	—	85	108	145	mA
Terminal Voltage	Pin 2	$V_2$	1	—	2.3	2.5	2.7	V
	Pin 4	$V_4$		(Note)	4.6	4.75	4.9	
	Pin 5	$V_5$		(Note)	4.6	4.75	4.9	
	Pin 8	$V_8$		—	2.3	2.5	2.7	
	Pin 9	$V_9$		—	2.3	2.5	2.7	
	Pin 10	$V_{10}$		—	4.4	4.65	4.9	
	Pin 12	$V_{12}$		—	1.5	1.8	2.1	
	Pin 13	$V_{13}$		—	1.5	1.8	2.1	
	Pin 16	$V_{16}$		—	3.8	4	4.2	
	Pin 17	$V_{17}$		—	1.3	1.65	2.0	
	Pin 19	$V_{19}$		—	1.2	1.7	2.2	
	Pin 21	$V_{21}$		—	1.2	1.7	2.2	
	Pin 25	$V_{25}$		—	2.4	2.7	3	
	Pin 26	$V_{26}$		—	1.9	2.1	2.3	
	Pin 29	$V_{29}$		—	2.0	2.3	2.6	
Pin 30	$V_{30}$	—	2.0	2.3	2.6			

(Note) When testing pins 4 and 5, connect pins 4 and 5, and pins 29 and 30.

AC CHARACTERISTICS (Unless otherwise specified,  $V_{CC} = 5.0V$ ,  $T_a = 25^\circ C$ )

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IF Input Frequency Range	$f_{in}$	2	—	350	—	650	MHz
IF Input Level Range	$v_{in}$	—	For IF balanced input	-56	—	-21	dBmW
Gain Control Voltage (Max.)	$V_{cmax}$	2	(Note 1)	1.8	—	—	V
Gain Control Voltage (Min.)	$V_{cmin}$	2	(Note 2)	—	—	3.3	V
Gain Control Sensitivity	S gain	2	(Note 3)	—	—	65	dB/V
First AGC Delay Point	1st 25	2	(Note 4)	—	2.8	—	V
First AGC Maximum Delay Point	1st max	2	(Note 5)	—	3.2	—	V
First AGC Minimum Delay Point	1st min	2	(Note 6)	—	1.9	—	V
First AGC Delay Point Stability	1st A	2	(Note 7)	—	—	100	mV
First AGC Control Sensitivity	S 1st	2	(Note 8)	—	—	200	V/V
First AGC Maximum Output Voltage	1st $V_{max}$	2	(Note 9)	3.5	4	—	V
First AGC Minimum Output Voltage	1st $V_{min}$	2	(Note 10)	—	0.2	0.5	V
Signal Level Sensitivity	S sig	2	(Note 11)	—	1.67	—	V/V
Signal Level Maximum Output Voltage	SigV max	2	(Note 12)	3.5	—	—	V
Signal Level Minimum Output Voltage	SigV min	2	(Note 13)	—	—	1	V
Signal Level Output Stability	SigV A	2	(Note 14)	—	—	100	mV
VCO Lock Range	$f_L$	2	(Note 15)	$\pm 1.5$	—	—	MHz
VCO Capture Range	$f_C$	2	(Note 16)	$\pm 3.5$	—	—	MHz
Side band Rejection Level	$f_S / I$	2	(Note 17)	—	—	-40	dBc
Phase Noise ( $\Delta f = 100Hz$ ) ( $\Delta f = 1kHz$ ) ( $\Delta f = 10kHz$ ) ( $\Delta f = 100kHz$ ) ( $\Delta f = 1MHz$ )	PN100	2	(Note 18)	—	—	-60	dBc/Hz
	PN1k			—	—	-70	dBc/Hz
	PN10k			—	—	-80	dBc/Hz
	PN100k			—	—	-90	dBc/Hz
	PN1M			—	—	-100	dBc/Hz
I/Q Gain Balance	B gain	2	(Note 19)	—	—	$\pm 1$	dB
I/Q Phase Balance	B deg	2	(Note 20)	—	—	$\pm 2$	°
Output Response	$f_{resp.}$	2	(Note 21)	—	—	$\pm 1$	dB
Output $L_O$ Leakage	L $L_O$	2	(Note 22)	—	—	-50	dBc
Tertiary Mutual Modulation Distortion	IM3	2	(Note 23)	—	—	-30	dBc



## TEST CONDITIONS

- (Note 1) Gain control voltage (Max.)
- (1) Input  $f = 404.78\text{MHz}$ ,  $-50\text{dBmW}$  CW in pin 12.
  - (2) Monitor pin 19 using an oscilloscope.
  - (3) Supply DC voltage to pin 8 so that the output amplitude becomes  $1V_{p-p}$ .
  - (4) Measure the DC voltage at (3) above.
- (Note 2) Gain control voltage (Min.)
- (1) Input  $f = 404.78\text{MHz}$ ,  $-20\text{dBmW}$  CW in pin 12.
  - (2) Monitor pin 19 using an oscilloscope.
  - (3) Supply DC voltage to pin 8 so that the output amplitude becomes  $1V_{p-p}$ .
  - (4) Measure the DC voltage at (3) above.
- (Note 3) Gain control sensitivity
- (1) Input  $f = 404.78\text{MHz}$ ,  $-20\text{dBmW}$  CW in pin 12.
  - (2) Monitor pin 19 using an oscilloscope.
  - (3) Supply DC voltage to pin 8 so that the output amplitude becomes  $1V_{p-p}$ .
  - (4) Measure the DC voltage at (3) above.
  - (5) Input  $f = 404.78\text{MHz}$ ,  $-30\text{dBmW}$  CW in pin 12.
  - (6) Monitor pin 19 using an oscilloscope.
  - (7) Supply DC voltage to pin 8 so that the output amplitude becomes  $1V_{p-p}$ .
  - (8) Measure the DC voltage at (3) above.
  - (9) Calculate the sensitivity.  $10 / [\text{Measured value at (4) above} - \text{measured value at (8) above}]$
- (Note 4) First AGC delay point
- (1) Supply 2.5V DC to pin 9.
  - (2) Monitor pin 16 using a voltmeter.
  - (3) Supply between 1.8 and 3.3V DC to pin 8.
  - (4) Measure the pin 8 voltage when the pin 16 voltage drops to 3.5V or below.
- (Note 5) First AGC maximum delay point
- (1) Supply 2.0V DC to pin 9.
  - (2) Monitor pin 16 using a voltmeter.
  - (3) Supply between 1.8 and 3.3V DC to pin 8.
  - (4) Measure the pin 8 voltage when the pin 16 voltage drops to 3.5V or below.
- (Note 6) First AGC minimum delay point
- (1) Supply 3.7V DC to pin 9.
  - (2) Monitor pin 16 using a voltmeter.
  - (3) Supply between 1.8 and 3.3V DC to pin 8.
  - (4) Measure the pin 8 voltage when the pin 16 voltage drops to 3.5V or below.

- (Note 7) First AGC delay point stability
- (1) Supply 2.5V DC to pin 9.
  - (2) Monitor pin 16 using a voltmeter.
  - (3) Supply 2.5V DC to pin 8.
  - (4) Measure the pin 16 voltage.
  - (5) At  $-25^{\circ}\text{C}$  or  $+75^{\circ}\text{C}$  and  $V_{CC}=4.5\text{V}$  or  $5.5\text{V}$ , repeat from (1) to (4) above.
  - (6) Calculate the output stability. [Measured maximum value at (5) above – measured minimum value at (5) above]
- (Note 8) First AGC control sensitivity
- (1) Supply 2.5V DC to pin 9.
  - (2) Monitor pin 16 using a voltmeter.
  - (3) Supply 1.8 to 3.3V DC to pin 8.
  - (4) Measure the pin 8 and 16 voltages when the pin 16 voltage drops to 3.5V or below.
  - (5) Measure the pin 8 and 16 voltages when the pin 16 voltage drops to 1.0V or below.
  - (6) Calculate the output stability.  $-\text{[Pin 16 at (4) above} - \text{pin 16 at (5) above]} / \text{[Pin 8 at (4) above} - \text{pin 8 at (5) above]}$
- (Note 9) First AGC maximum output voltage
- (1) Supply 2.5V DC to pin 9.
  - (2) Monitor pin 16 using a voltmeter.
  - (3) Supply 1.8V DC to pin 8.
  - (4) Measure the pin 16 voltage.
- (Note 10) First AGC minimum output voltage
- (1) Supply 2.5V DC to pin 9.
  - (2) Monitor pin 16 using a voltmeter.
  - (3) Supply 3.3V DC to pin 8.
  - (4) Measure the pin 16 voltage.
- (Note 11) Signal level sensitivity
- (1) Supply 2.5V DC to pin 9.
  - (2) Monitor pin 17 using a voltmeter.
  - (3) Supply 2.2V DC to pin 8.
  - (4) Measure the pin 17 voltage.
  - (5) Supply 2.6V DC to pin 8.
  - (6) Measure the pin 17 voltage.
  - (7) Calculate the sensitivity.  $\text{[Measured value at (6) above} - \text{measured value at (4) above]} / 0.4$

- (Note 12) Signal level maximum output voltage  
(1) Supply 2.5V DC to pin 9.  
(2) Monitor pin 17 using a voltmeter.  
(3) Supply 3.3V DC to pin 8.  
(4) Measure the pin 17 voltage.
- (Note 13) Signal level minimum output voltage  
(1) Supply 2.5V DC to pin 9.  
(2) Monitor pin 17 using a voltmeter.  
(3) Supply 1.8V DC to pin 8.  
(4) Measure the pin 17 voltage.
- (Note 14) Signal level output stability  
(1) Supply 2.5V DC to pin 9.  
(2) Monitor pin 17 using a voltmeter.  
(3) Supply 2.5V DC to pin 8.  
(4) Measure the pin 17 voltage.  
(5) At  $-25^{\circ}\text{C}$  or  $+75^{\circ}\text{C}$  and  $V_{CC}=4.5\text{V}$  or  $5.5\text{V}$ , repeat from (1) to (4) above.  
(6) Calculate the output stability. [Measured maximum value at (5) above – measured minimum value at (5) above]
- (Note 15) VCO lock range  
(1) All of SW-1, SW-2 and SW-3 connect to GND.  
(2) After connecting pins 29 and 30, adjust VCO L so that the desired oscillation frequency,  $f$ , is obtained.  
(3) After disconnecting the crystal oscillator between pins 25 and 26, input frequency :  $f/32$ , amplitude :  $1V_{p-p}$  sine wave signal  $f_{ref}$  to pin 26.  
(4) Change the  $f_{ref}$  frequency in plus and minus directions and observe frequencies  $[\pm\Delta f_{rck}]$  at the upper and lower limits where PLL lock is off.  
(4) VCO lock range :  $32 \times (\pm\Delta f_{rck})$
- (Note 16) VCO capture range  
(1) All of SW-1, SW-2 and SW-3 connect to GND.  
(2) After connecting pins 29 and 30, adjust VCO L so that the desired oscillation frequency,  $f$ , is obtained.  
(3) After disconnecting the crystal oscillator between pins 25 and 26, input frequency :  $f/32$ , amplitude :  $1V_{p-p}$  sine wave signal  $f_{ref}$  to pin 26.  
(4) Change, in the plus and minus directions, from a frequency sufficiently large compared with  $[f_{ref} \pm \Delta f_{rck}]$  (PLL lock is off) to  $f_{ref}$ , the frequency of the signal input to pin 26. Observe frequencies  $[\pm\Delta f_{pU}]$  at the upper and lower limits where PLL is locked.  
(5) VCO capture range :  $32 \times (\pm\Delta f_{pU})$

## (Note 17) Side band rejection level

- (1) All of SW-1, SW-2 and SW-3 connect to GND.
- (2) Provide, with monitor coil (L), the VCO tank which is connected to pins 4 and 5.
- (3) After connecting pins 29 and 30, adjust VCO L so that the desired oscillation frequency,  $f$ , is obtained.
- (4) Observe oscillation strength  $P_{VCO}$  of the VCO spectrum using a spectrum analyzer.
- (5) Observe spectrum  $P_{Sp}$  located at the frequency obtained by integer – multiplying the PLL compare reference frequency (12.587MHz).
- (6) Calculate  $(P_{VCO} - P_{Sp})$ .

## (Note 18) Phase noise

- (1) All of SW-1, SW-2 and SW-3 connect to GND.
- (2) Provide, with monitor coil (L), the VCO tank which is connected to pins 4 and 5.
- (3) After connecting pins 29 and 30, adjust VCO L so that the desired oscillation frequency,  $f$ , is obtained.
- (4) Observe oscillation strength  $P_{VCO}$  of the VCO oscillator spectrum using a spectrum analyzer.
- (5) Observe spectrum  $P_{noise}$  at a frequency which is  $\Delta f$  away from the oscillation frequency.
- (6) Calculate  $(P_{VCO} = P_{noise}) / \Delta f$ .

## (Note 19) I/Q gain balance

- (1) Input  $f = 417.78\text{MHz}$ ,  $-20\text{dBmW}$  CW to pin 12.
- (2) Monitor pin 19 using an oscilloscope.
- (3) Supply DC voltage to pin 8 so that the pin 19 output amplitude becomes  $1V_{p-p}$ .
- (4) Measure the amplitude ratio of pin 21 and pin 19.
- (5) Set the input level to  $-50\text{dBmW}$  and repeat (2) to (4) above.

## (Note 20) I/Q phase balance

- (1) Input  $f = 417.78\text{MHz}$ ,  $-20\text{dBmW}$  CW to pin 12.
- (2) Monitor pin 19 using an oscilloscope.
- (3) Supply DC voltage to pin 8 so that the pin 19 output amplitude becomes  $1V_{p-p}$ .
- (4) Measure the phase difference of pin 21 and pin 19.
- (5) Set the input level to  $-50\text{dBmW}$  and repeat (2) to (4) above.

## (Note 21) Output response

- (1) Input  $f = 382.78\text{MHz}$ ,  $-20\text{dBmW}$  CW to pin 12.
- (2) Monitor pin 19 using an oscilloscope.
- (3) Supply DC voltage to pin 8 so that the pin 19 output amplitude becomes  $1V_{p-p}$ .
- (4) While varying the input frequency from 382.78 to 422.78MHz, observe the output amplitude of pin 19.
- (5) Calculate the gain deviation.  $20\log [\text{Measured value at (4) above} / 1.0]$

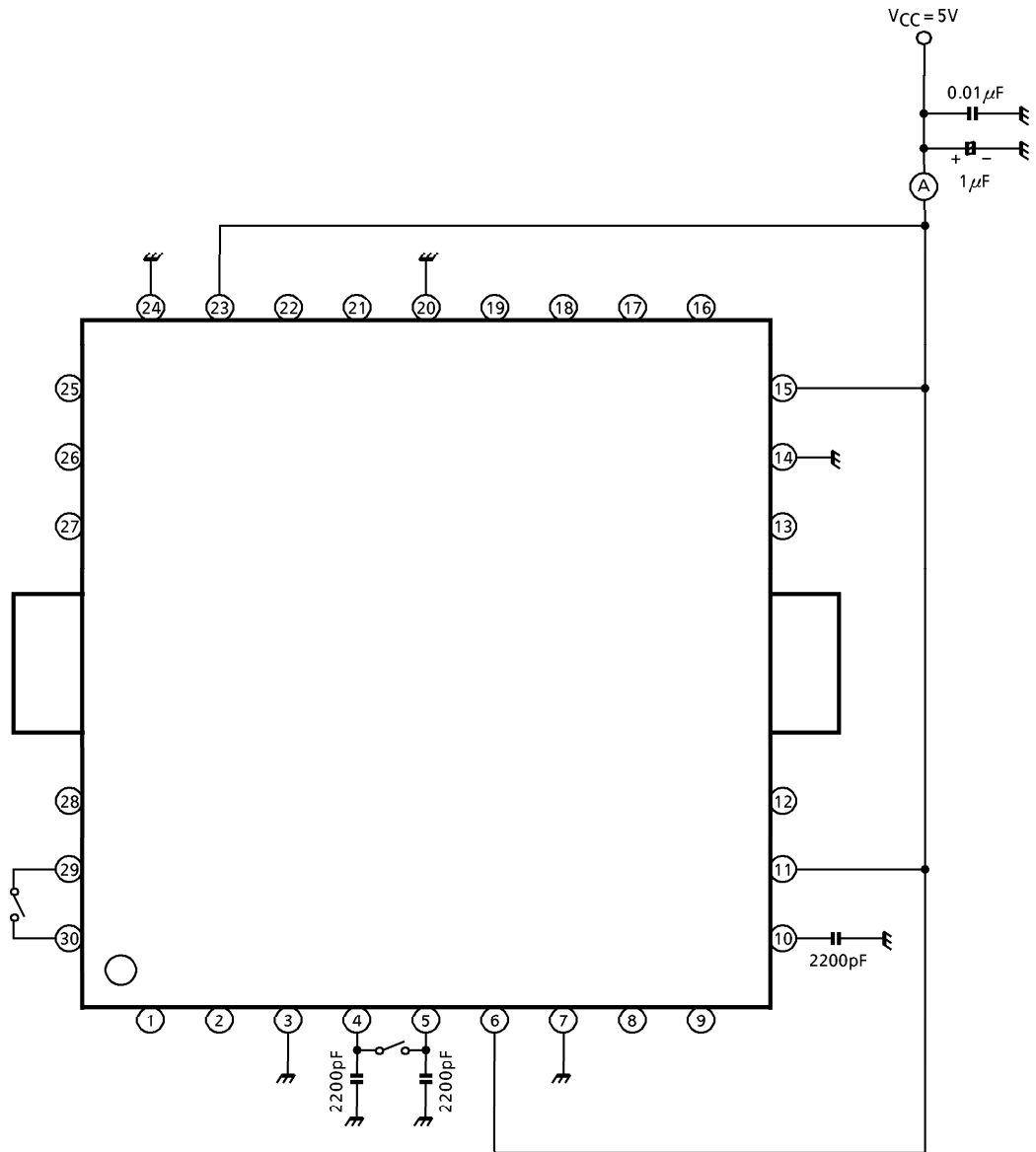
(Note 22) Output  $L_o$  leakage

- (1) Input  $f = 382.78\text{MHz}$ ,  $-54\text{dBmW}$  CW to pin 12.
- (2) Monitor pin 19 using an oscilloscope.
- (3) Supply DC voltage to pin 8 so that the pin 19 output amplitude becomes  $1V_{p-p}$ .
- (4) Measure the pin 19 level using a spectrum analyzer.
- (5) Measure the  $L_o$  signal (402.78MHz) level using the spectrum analyzer.
- (6) Calculate the relative value against the pin 19 level.  $[\text{Measured value at (4) above} - \text{measured value at (5) above}]$

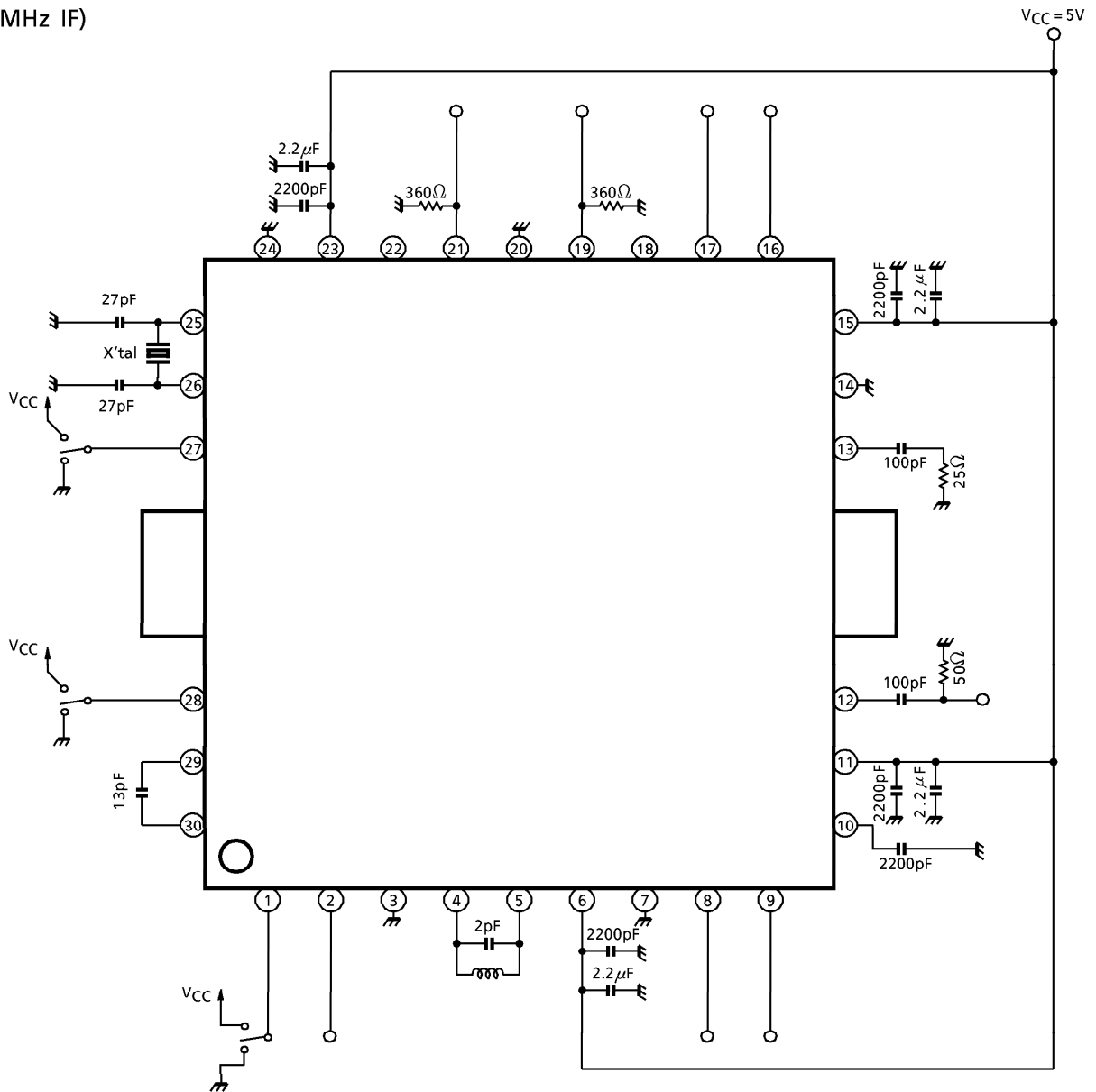
## (Note 23) Tertiary mutual modulation distortion

- (1) Input the following two CW signals to pin 12.  
 $f_1 = 404.78\text{MHz}$ ,  $-20\text{dBmW}$   
 $f_2 = 405.28\text{MHz}$ ,  $-20\text{dBmW}$
- (2) Monitor pin 19 using an oscilloscope.
- (3) Supply DC voltage to pin 8 so that the pin 19 output amplitude becomes  $1V_{p-p}$ .
- (4) Measure the pin 19 level using a spectrum analyzer.
- (5) Measure the IM3 (spurious) level using the spectrum analyzer.
- (6) Calculate the IM3 relative value.  $[\text{Measured value at (5) above} - \text{measured value at (4) above}]$

TEST CIRCUIT 1  
DC CHARACTERISTICS



**TEST CIRCUIT 2**  
**AC CHARACTERISTICS**  
 (402.78MHz IF)



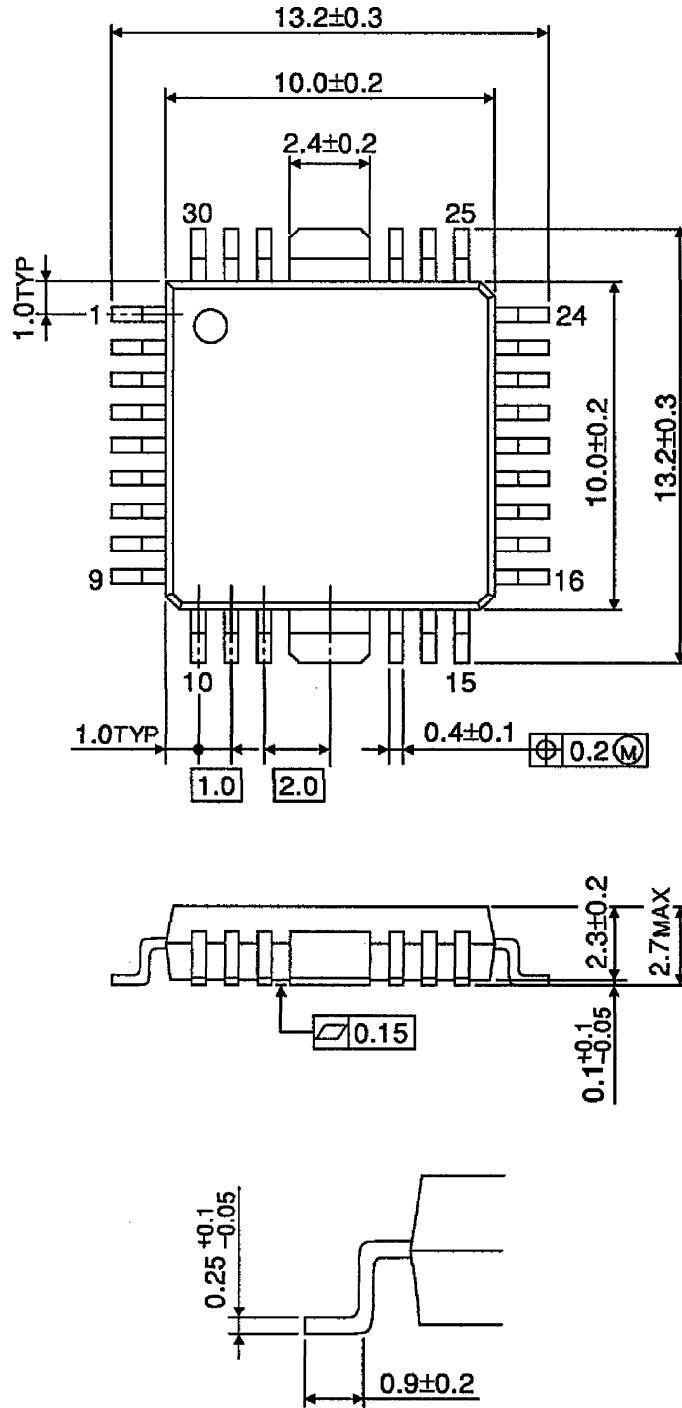
**Crystal oscillator specifications**

FREQUENCY [MHz]	FREQUENCY DEVIATION [ppm]	LOAD CAPACITANCE [pF]	EQUIVALENT SERIES RESISTANCE [Ω]	PARALLEL CAPACITANCE [pF]	TEMPERATURE
12,586875	± 30	10.0 ± 0.5	below 40	2.6 ± 0.5	- 25 ~ + 80°C

(\*) Resonance condition : parallel

**PACKAGE DIMENSIONS**  
 HQFP30-P-1010-1.00

Unit : mm



Weight : 0.61g (Typ.)