DATA SHEET

SAA7724H
Car radio digital signal processor

Preliminary specification

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Philips
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PHILIPS

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1 FEATURES

- AM and FM digitize at IF
- AM and FM narrow-band/IF AGC
- AM and FM IF filtering
- AM and FM adjustable channel detection/variable IF
- IF filter for WX
- AM and FM demodulation
- AM and FM stereo decoding
- AM and FM stereo pilot detection
- FM pilot notch
- AM pilot filter
- FM stereo blend, high blend, high cut, soft muting and de-emphasis
- AM stereo blend, LP filter, high cut and soft muting
- AM and FM noise blanker
- AM and FM gain adjust and calibration (audio)
- FM multipath detection
- FM multipath correction
- Diversity switching
- Radio Data System (RDS) and Radio Broadcast Data System (RBDS) demodulation and decoding
- Tape head calibration, equalization, Dolby B and AMS (from analog tape input)
- CD gain adjust, calibration and compression (from analog or digital SPDIF/I^2S-bus input)
- Parametric equalization
- Volume control
- Bass control
- Treble control
- Balance/fade control
- DC blocking filter
- Dual source select
- Dual playback
- Channel delays
- Analog summer for four channels (through inputs MONO1 and MONO2)
- Audio limiting.

1.1 Sample rates

The SAA7724H runs at a master clock of 43.2 MHz. Audio processing runs at a sample rate of

$$1 \times f_s = 42.1875 \text{ kHz} = \frac{43.2 \text{ MHZ}}{1024}$$

2 GENERAL INFORMATION

2.1 DSP radio system

The Digital Signal Processing (DSP) radio system (see Fig.1) consists of:

- Analog tuner (also called RF/IF)
- SAA7724H
- Audio power amplifier
- Microcontroller
- IF co-processor
- Audio co-processor.

The microcontroller interfaces to the RF/IF and SAA7724H via an I^{2}C-bus. Analog tape and CD inputs are input from other parts of the radio. The IF co-processor and audio co-processor interfaces to the SAA7724H via an I^{2}S-bus.

2.2 SAA7724H

The SAA7724H digitizes up to two IF signals and performs DSP to generate left front, right front, left rear, and right rear audio and RDS/RBDS data output. The SAA7724H also samples analog baseband tape, FM MPX, AUX inputs, analog and digital CD, performs signal processing on these sampled waveforms and multiplexes the proper signal to the output. A microcontroller interface allows the SAA7724H to be controlled and monitored.

The SAA7724H is composed of hardwired and programmable DSP circuitry, with programmable parameters, such as injection frequencies, filter coefficients and control parameters. Some functions or groups of functions are implemented with programmable sequence processors.

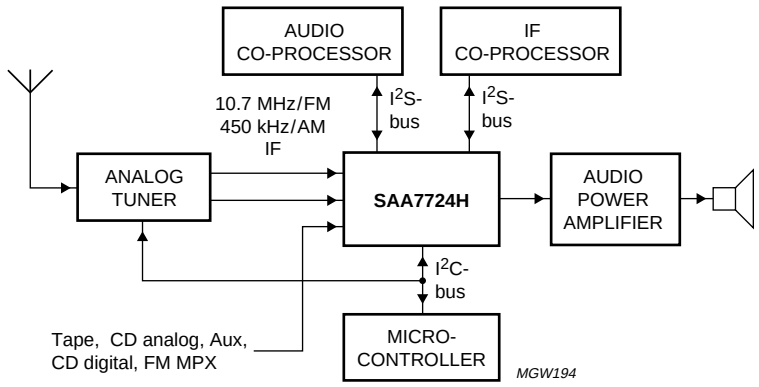


Fig.1 System overview.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA7724H	QFP100	plastic quad flat package; 100 leads (lead length 1.95 mm); body $14 \times 20 \times 2.8$ mm	SOT317-3

4 BLOCK DIAGRAM

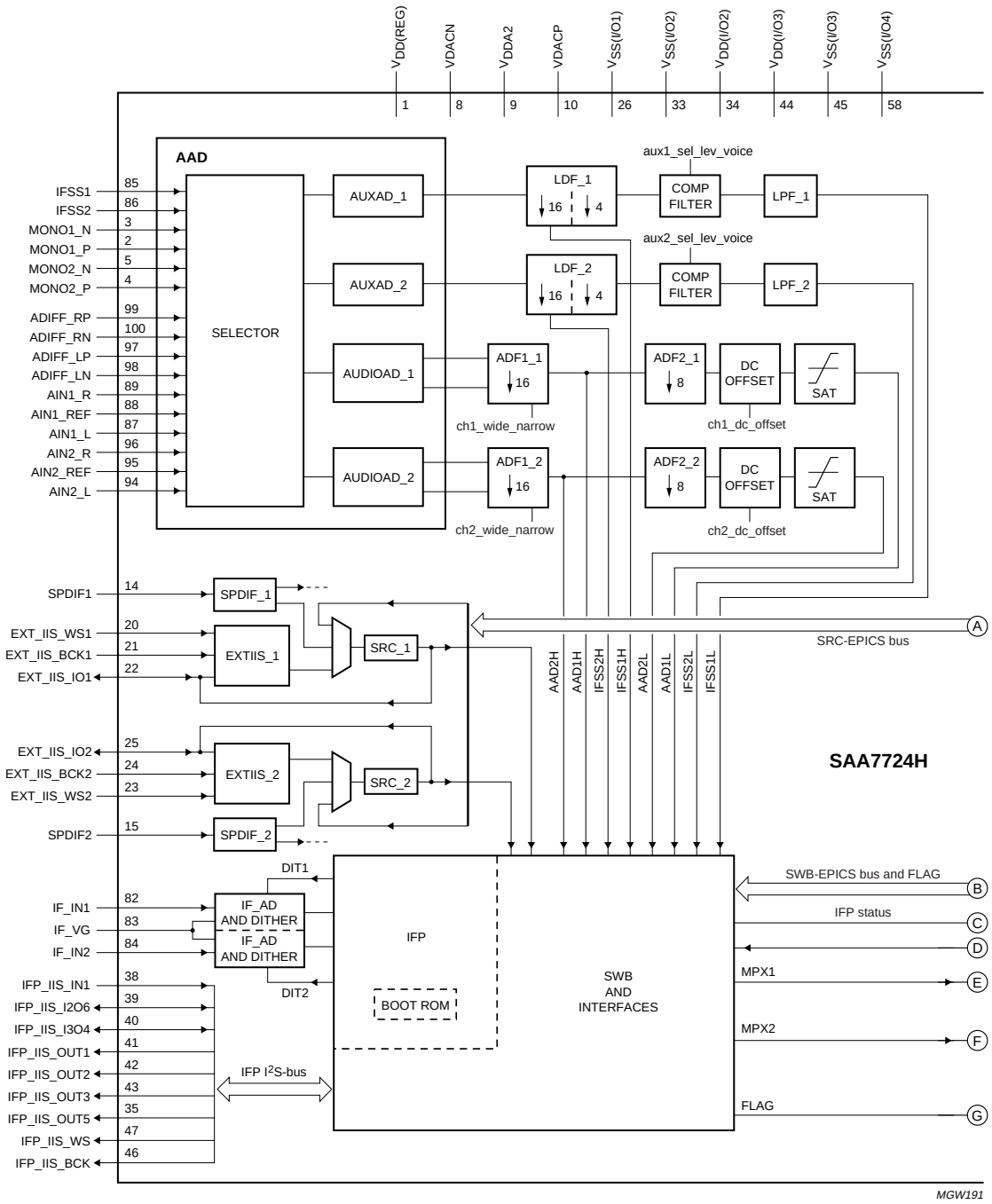


Fig.2 Block diagram (continued in Fig.3).

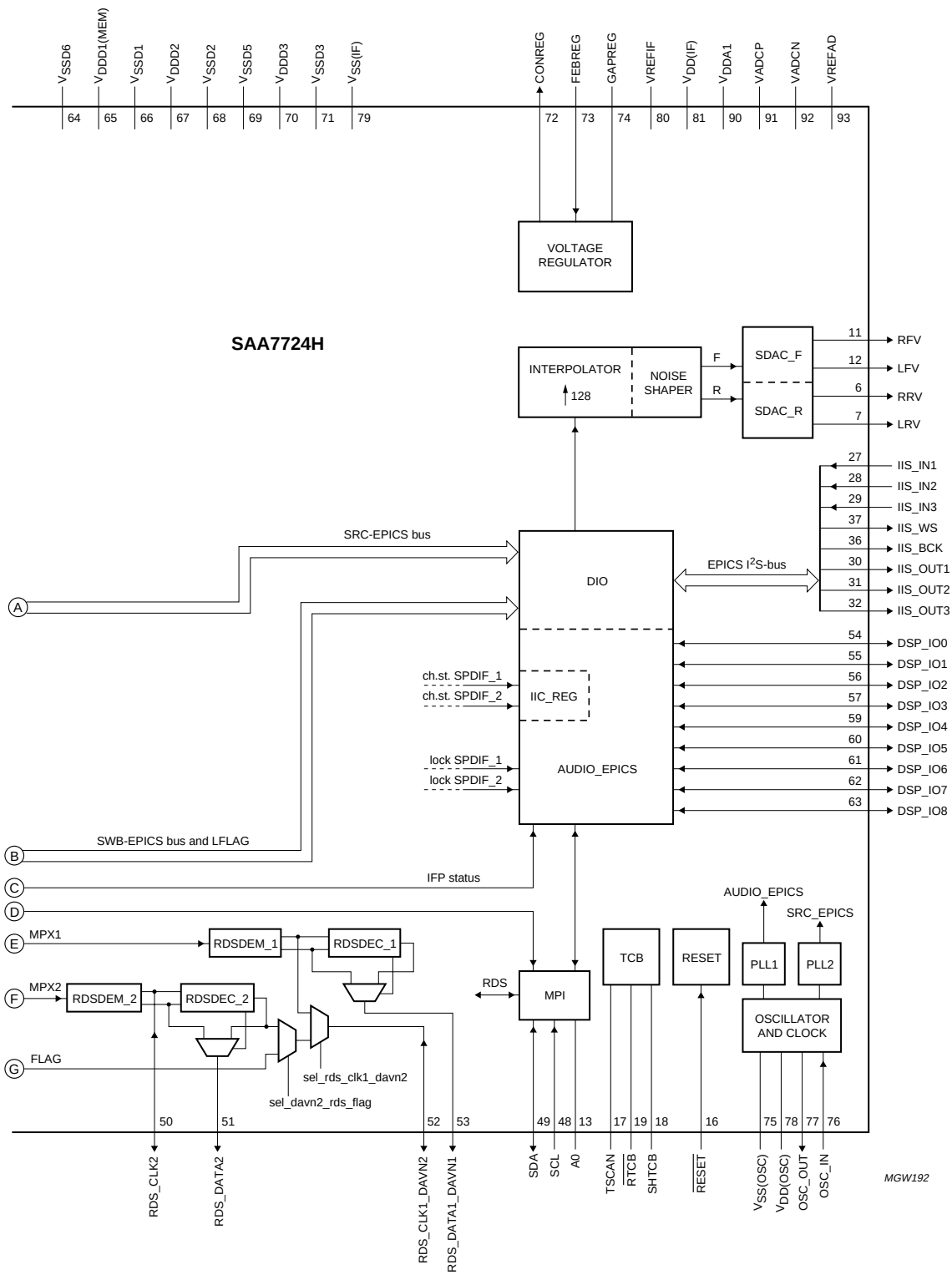


Fig.3 Block diagram (continued from Fig.2)

5 PINNING

Table 1 Functional pin description

SYMBOL	PIN	DESCRIPTION
$V_{DD(REG)}$	1	supply voltage for 2.5 V regulator circuit and bias for ADCs (3.3 V)
MONO1_P	2	differential positive analog input to AUX_AD2, AUDIOAD_1 and AUDIOAD_2
MONO1_N	3	differential negative analog input to AUX_AD2, AUDIOAD_1 and AUDIOAD_2
MONO2_P	4	differential positive analog input to AUX_AD2, AUDIOAD_1 and AUDIOAD_2
MONO2_N	5	differential negative analog input to AUX_AD2, AUDIOAD_1 and AUDIOAD_2
RRV	6	analog audio voltage output for the right-rear speaker
LRV	7	analog audio voltage output for the left-rear speaker
VDACN	8	negative reference voltage for the SDAC
V_{DDA2}	9	analog supply voltage for the SDAC (2.5 V)
VDACP	10	positive reference voltage for the SDAC
RFV	11	analog audio voltage output for the right-front speaker
LFV	12	analog audio voltage output for the left-front speaker
A0	13	slave subaddress for I^2C-bus selection
SPDIF1	14	SPDIF input channel 1 from digital media source
SPDIF2	15	SPDIF input channel 2 from digital media source
$\overline{RESET}$	16	reset input (active LOW)
TSCAN	17	scan control
SHTCB	18	shift clock test control block
$\overline{RTCB}$	19	asynchronous reset test control block (active LOW)
EXT_IIS_WS1	20	word select input from digital media source 1 (I^2S-bus)
EXT_IIS_BCK1	21	bit clock input from digital media source 1 (I^2S-bus)
EXT_IIS_IO1	22	data input/output digital media source 1 (I^2S-bus)
EXT_IIS_WS2	23	word select input from digital media source 2 (I^2S-bus)
EXT_IIS_BCK2	24	bit clock input from digital media source 2 (I^2S-bus)
EXT_IIS_IO2	25	data input/output digital media source 2 (I^2S-bus)
$V_{SS(I/O1)}$	26	ground supply 1 for external digital ports
IIS_IN1	27	data channel input 1 (front channels) from external DSP IC (I^2S-bus)
IIS_IN2	28	data channel input 2 (rear channels) from external DSP IC (I^2S-bus)
IIS_IN3	29	data channel input 3 from external DSP IC (I^2S-bus)
IIS_OUT1	30	data channel output 1 for external DSP IC activated by en_host_io (I^2S-bus)
IIS_OUT2	31	data channel output 2 to external DSP IC activated by en_host_io (I^2S-bus)
IIS_OUT3	32	data channel output 3 to external DSP IC activated by en_host_io (I^2S-bus)
$V_{SS(I/O2)}$	33	ground supply 2 for external digital ports
$V_{DD(I/O2)}$	34	supply voltage 2 for external digital ports (3.3 V)
IFP_IIS_OUT5	35	IFP data channel output 5 to external DSP IC activated by ifp_iis_en; can also be used as $256 \times f_s$ clock output enabled by en_256FS (I^2S-bus)
IIS_BCK	36	clock output for external DSP IC enabled by en_host_io (I^2S-bus)
IIS_WS	37	word select output for external DSP IC enabled by en_host_io (I^2S-bus)
IFP_IIS_IN1	38	IFP data channel input 1 from external DSP IC (I^2S-bus)

SYMBOL	PIN	DESCRIPTION
IFP_IIS_I2O6	39	IFP data channel input 2 from external DSP IC or output data channel 6 to external DSP IC selected by ifp_iis_io_mode (I^2S-bus)
IFP_IIS_I3O4	40	IFP data channel input 3 from external DSP IC or output data channel 4 to external DSP IC selected by ifp_iis_io_mode (I^2S-bus)
IFP_IIS_OUT1	41	IFP data channel output 1 to external DSP IC activated by ifp_iis_en (I^2S-bus)
IFP_IIS_OUT2	42	IFP data channel output 2 to external DSP IC activated by ifp_iis_en (I^2S-bus)
IFP_IIS_OUT3	43	IFP data channel output 3 to external DSP IC activated by ifp_iis_en (I^2S-bus)
$V_{DD(I/O3)}$	44	supply voltage 3 for external digital ports (3.3 V)
$V_{SS(I/O3)}$	45	ground supply 3 for external digital ports
IFP_IIS_BCK	46	IFP output clock for external DSP IC enabled by ifp_iis_en (I^2S-bus)
IFP_IIS_WS	47	IFP word select output for external DSP IC enabled by ifp_iis_en (I^2S-bus)
SCL	48	serial clock input (I^2C-bus)
SDA	49	serial data input/output (I^2C-bus)
RDS_CLK2	50	RDS2 bit clock input/output; default input enabled by rds2_clkin
RDS_DATA2	51	RDS2 data output of RDS2 demodulator
RDS_CLK1_DAVN2	52	DAVN2 or RDS1 bit clock input/output; default input enabled by rds1_clkin
RDS_DATA1_DAVN1	53	RDS1 data output of RDS1 demodulator or RDS1 decoder DAVN1
DSP_IO0	54	general purpose input/output for EPICS (F0 of status register)
DSP_IO1	55	general purpose input/output for EPICS (F1 of status register)
DSP_IO2	56	general purpose input/output for EPICS (F2 of status register)
DSP_IO3	57	general purpose input/output for EPICS (F3 of status register)
$V_{SS(I/O4)}$	58	ground supply 4 for external digital ports
DSP_IO4	59	general purpose input/output for EPICS (F4 of status register)
DSP_IO5	60	general purpose input/output for EPICS (F5 of status register)
DSP_IO6	61	general purpose input/output for EPICS (F6 of status register)
DSP_IO7	62	general purpose input/output for EPICS (F7 of status register)
DSP_IO8	63	general purpose input/output for EPICS (F8 of status register)
V_{SSD6}	64	ground supply for digital circuitry
$V_{DDD1(MEM)}$	65	digital supply voltage 1 for memories (2.5 V)
V_{SSD1}	66	digital ground supply 1
V_{DDD2}	67	digital supply voltage 2 (2.5 V)
V_{SSD2}	68	digital ground supply 2
V_{SSD5}	69	digital ground supply 5
V_{DDD3}	70	digital supply voltage 3 (2.5 V)
V_{SSD3}	71	digital ground supply 3
CONREG	72	2.5 V regulator control output
FEBREG	73	2.5 V regulator feedback input
GAPREG	74	band gap reference decoupling pin for voltage regulator
$V_{SS(OSC)}$	75	ground supply for crystal oscillator circuitry
OSC_IN	76	crystal oscillator input: local crystal oscillator sense for gain control or forced input in slave mode

SYMBOL	PIN	DESCRIPTION
OSC_OUT	77	crystal oscillator output: drive output to crystal
$V_{DD(OSC)}$	78	positive supply voltage for crystal oscillator circuitry
$V_{SS(IF)}$	79	IF_AD ground supply
VREFIF	80	IF_AD reference voltage output
$V_{DD(IF)}$	81	IF_AD 2.5 V supply voltage
IF_IN1	82	analog input to IF_AD1 from tuner IF output
IF_VG	83	IF_AD virtual ground
IF_IN2	84	analog input to IF_AD2 from tuner IF output
IFSS1	85	analog IFSS1 input to AUXAD_1
IFSS2	86	analog IFSS2 input to AUXAD_2
AIN1_L	87	analog input 1 to AAD for left input buffer signal
AIN1_REF	88	common reference voltage input for AIN1 input buffer
AIN1_R	89	analog input 1 to AAD for right input buffer signal
V_{DDA1}	90	analog supply voltage 1 for AUXAD and AAD analog circuitry (2.5 V)
VADCP	91	positive reference voltage input for AAD
VADCN	92	ground reference voltage input for AAD
VREFAD	93	common mode reference voltage output for AAD, AUXAD and buffers
AIN2_L	94	analog input 2 to AAD for left input buffer signal
AIN2_REF	95	common reference voltage input for AIN2 input buffer
AIN2_R	96	analog input 2 to AAD for right input buffer signal
ADIFF_LP	97	analog input to AAD for left positive differential signal
ADIFF_LN	98	analog input to AAD for left negative differential signal
ADIFF_RP	99	analog input to AAD for right positive differential signal
ADIFF_RN	100	analog input to AAD for right negative differential signal

Table 2 Application requirements and padcell type per pin

SYMBOL	PIN	DIGITAL I/O LEVELS	APPLICATION DIGITAL FUNCTION	PIN STATE AFTER RESET	HYSTERESIS REQUIRED	INTERNAL PULL-DOWN	CELL NAME[1]
$V_{DD(REG)}$	1	–	–	–	–	–	vddco
MONO1_P	2	–	–	–	–	–	apio
MONO1_N	3	–	–	–	–	–	apio
MONO2_P	4	–	–	–	–	–	apio
MONO2_N	5	–	–	–	–	–	apio
RRV	6	–	–	–	–	–	apio
LRV	7	–	–	–	–	–	apio
VDACN	8	–	–	–	–	–	vssco
V_{DDA2}	9	–	–	–	–	–	vddco
VDACP	10	–	–	–	–	–	vddco
RFV	11	–	–	–	–	–	apio
LFV	12	–	–	–	–	–	apio
A0	13	0 to 5 V DC tolerant	input	–	yes	pull-down	ipthdt5v
SPDIF1	14	–	–	–	–	–	apio
SPDIF2	15	–	–	–	–	–	apio
$\overline{\text{RESET}}$	16	0 to 5 V DC tolerant	input	input	yes	pull-down	ipthdt5v
TSCAN	17	0 to 5 V DC tolerant	input	input	yes	pull-down	ipthdt5v
SHTCB	18	0 to 5 V DC tolerant	input	input	yes	pull-down	ipthdt5v
$\overline{\text{RTCB}}$	19	0 to 5 V DC tolerant	input	input	yes	pull-down	ipthdt5v
EXT_IIS_WS1	20	0 to 5 V DC tolerant	input	input	yes	pull-down	ipthdt5v
EXT_IIS_BCK1	21	0 to 5 V DC tolerant	input	input	yes	pull-down	ipthdt5v
EXT_IIS_IO1	22	0 to 5 V DC tolerant	bi-directional	input	yes	pull-down	bpts10tht5v
EXT_IIS_WS2	23	0 to 5 V DC tolerant	input	input	yes	pull-down	ipthdt5v
EXT_IIS_BCK2	24	0 to 5 V DC tolerant	input	input	yes	pull-down	ipthdt5v
EXT_IIS_IO2	25	0 to 5 V DC tolerant	bi-directional	input	yes	pull-down	bpts10tht5v
$V_{SS(I/O1)}$	26	–	–	–	–	–	vsse3v3
IIS_IN1	27	0 to 3.3 V DC	input	input	yes	pull-down	bpt4mthd
IIS_IN2	28	0 to 3.3 V DC	input	input	yes	pull-down	bpt4mthd
IIS_IN3	29	0 to 3.3 V DC	input	input	yes	pull-down	bpt4mthd

SYMBOL	PIN	DIGITAL I/O LEVELS	APPLICATION DIGITAL FUNCTION	PIN STATE AFTER RESET	HYSTERESIS REQUIRED	INTERNAL PULL-DOWN	CELL NAME[1]
IIS_OUT1	30	0 to 3.3 V DC	output	output and LOW level	–	–	ops10c
IIS_OUT2	31	0 to 3.3 V DC	output	output and LOW level	–	–	ops10c
IIS_OUT3	32	0 to 3.3 V DC	output	output and LOW level	–	–	ops10c
$V_{SS(I/O2)}$	33	–	–	–	–	–	vsse3v3
$V_{DD(I/O2)}$	34	–	–	–	–	–	vdde3v3
IFP_IIS_OUT5	35	0 to 3.3 V DC	output	output and LOW level	–	–	ops10c
IIS_BCK	36	0 to 3.3 V DC	output	3-state	–	–	ot4mc
IIS_WS	37	0 to 3.3 V DC	output	3-state	–	–	ots10c
IFP_IIS_IN1	38	0 to 3.3 V DC	input	input	yes	pull-down	ipthd
IFP_IIS_I2O6	39	0 to 3.3 V DC	bi-directional	input	yes	pull-down	bpts10thd
IFP_IIS_I3O4	40	0 to 3.3 V DC	bi-directional	input	yes	pull-down	bpts10thd
IFP_IIS_OUT1	41	0 to 3.3 V DC	output	output and LOW level	–	–	ops10c
IFP_IIS_OUT2	42	0 to 3.3 V DC	output	output and LOW level	–	–	ops10c
IFP_IIS_OUT3	43	0 to 3.3 V DC	output	output and LOW level	–	–	ops10c
$V_{DD(I/O3)}$	44	–	–	–	–	–	vdde3v3
$V_{SS(I/O3)}$	45	–	–	–	–	–	vsse3v3
IFP_IIS_BCK	46	0 to 3.3 V DC	output	3-state	–	–	ot4mc
IFP_IIS_WS	47	0 to 3.3 V DC	output	3-state	–	–	ots10c
SCL	48	0 to 5 V DC tolerant	input	input	yes	–	iptht5v
SDA	49	0 to 5 V DC tolerant	bi-directional	input	–	–	iic400kt5v
RDS_CLK2	50	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
RDS_DATA2	51	0 to 5 V DC tolerant	output	output mode (level depends on RDS data)	–	–	bptons10tht5v
RDS_CLK1_DAVN2	52	0 to 5 V DC tolerant	bi-directional	input	yes		bptons10tht5v
RDS_DATA1_DAVN1	53	0 to 5 V DC tolerant	output	output mode (level depends on RDS data)	–	–	bptons10tht5v
DSP_IO0	54	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
DSP_IO1	55	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
DSP_IO2	56	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v

SYMBOL	PIN	DIGITAL I/O LEVELS	APPLICATION DIGITAL FUNCTION	PIN STATE AFTER RESET	HYSTERESIS REQUIRED	INTERNAL PULL-DOWN	CELL NAME[1]
DSP_IO3	57	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
$V_{SS(I/O4)}$	58	–	–	–	–	–	vsse3v3
DSP_IO4	59	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
DSP_IO5	60	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
DSP_IO6	61	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
DSP_IO7	62	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
DSP_IO8	63	0 to 5 V DC tolerant	bi-directional	input	yes	–	bptons10tht5v
V_{SSD6}	64	–	–	–	–	–	vssis
$V_{DDD1(MEM)}$	65	–	–	–	–	–	vddco
V_{SSD1}	66	–	–	–	–	–	vssis
V_{DDD2}	67	–	–	–	–	–	vddi
V_{SSD2}	68	–	–	–	–	–	vssis
V_{SSD5}	69	–	–	–	–	–	vssis
V_{DDD3}	70	–	–	–	–	–	vddi
V_{SSD3}	71	–	–	–	–	–	vssis
CONREG	72	–	–	–	–	–	apio
FEBREG	73	–	–	–	–	–	apio
GAPREG	74	–	–	–	–	–	apio
$V_{SS(OSC)}$	75	–	–	–	–	–	vssco
OSC_IN	76	–	–	–	–	–	apio
OSC_OUT	77	–	–	–	–	–	apio
$V_{DD(OSC)}$	78	–	–	–	–	–	vddco
$V_{SS(IF)}$	79	–	–	–	–	–	vssco
VREFIF	80	–	–	–	–	–	apio
$V_{DD(IF)}$	81	–	–	–	–	–	vddco
IF_IN1	82	–	–	–	–	–	aprf
IF_VG	83	–	–	–	–	–	apio
IF_IN2	84	–	–	–	–	–	aprf
IFSS1	85	–	–	–	–	–	apio
IFSS2	86	–	–	–	–	–	apio

SYMBOL	PIN	DIGITAL I/O LEVELS	APPLICATION DIGITAL FUNCTION	PIN STATE AFTER RESET	HYSTERESIS REQUIRED	INTERNAL PULL-DOWN	CELL NAME[1]
AIN1_L	87	–	–	–	–	–	apio
AIN1_REF	88	–	–	–	–	–	apio
AIN1_R	89	–	–	–	–	–	apio
V_{DDA1}	90	–	–	–	–	–	vddco
VADCP	91	–	–	–	–	–	apio
VADCN	92	–	–	–	–	–	apio
VREFAD	93	–	–	–	–	–	apio
AIN2_L	94	–	–	–	–	–	apio
AIN2_REF	95	–	–	–	–	–	apio
AIN2_R	96	–	–	–	–	–	apio
ADIFF_LP	97	–	–	–	–	–	apio
ADIFF_LN	98	–	–	–	–	–	apio
ADIFF_RP	99	–	–	–	–	–	apio
ADIFF_RN	100	–	–	–	–	–	apio

Note

1. See Table 3.

Table 3 Used padcells and functional specification; notes 1 and 2

PADCELL NAME	LIBRARY NAME	FUNCTIONAL SPECIFICATION
Inputs		
ipthd	iolib_nlm	input pad; hysteresis; pull-down; TTL levels
ipthtt5v	iolib_nlm_danger	input pad; hysteresis; TTL levels; 5 V tolerant
ipthdt5v	iolib_nlm_danger	input pad; hysteresis; pull-down; TTL levels; 5 V tolerant
Outputs		
ot4mc	iolib_nlm	output; 3-state; 4 mA
ops10c	iolib_nlm	output plain; 10 ns slew rate
ots10c	iolib_nlm	output; 3-state; 10 ns slew rate
I/Os		
iic400kt5v	iolib_nlm_danger	input/output; 400 kHz I^2C-bus special cell; 5 V tolerant
bpt4mthd	iolib_nlm	input/output; 4 mA; hysteresis; pull-down; TTL input levels
bpts10thd	iolib_nlm	input/output; 10 ns slew rate; hysteresis; pull-down; TTL input levels
bpts10tht5v	iolib_nlm_danger	input/output; 10 ns slew rate; hysteresis; TTL input levels; 5 V tolerant
bptons10tht5v	iolib_nlm_danger	input/output; open-drain N-channel; 10 ns slew rate; hysteresis; TTL input levels; 5 V tolerant
Special		
apio	iolib_nlm	analog pad input or output
aprf	iolib_nlm	analog high frequency pad input or output
Supply		
vddco	iolib_nlm	V_{DD} core only supply; not connected to internal supply ring
vssco	iolib_nlm	V_{SS} core only supply; not connected to internal supply ring
vddi	iolib_nlm	V_{DD} core supply; connected to internal supply ring
vssis	iolib_nlm	V_{SS} core supply; connected to internal supply ring and substrate
vdde3v3	iolib_nlm	V_{DD} supply peripheral only
vsse3v3	iolib_nlm	V_{SS} supply peripheral only

Notes

1. All pull-down inputs or disabled I/Os with pull-down, may be left open-circuit. Internally the logic level is guaranteed LOW, but the pull-down doesn't behave as a normal resistor seen at the pin itself.
2. 5 V tolerant means that the input or 3-stated/disabled output is functioning correctly and will not be damaged when applying externally 5 V, and can thus be used in a normal application. The tolerances of the 5 V are given in the limiting values; see Chapter 7.

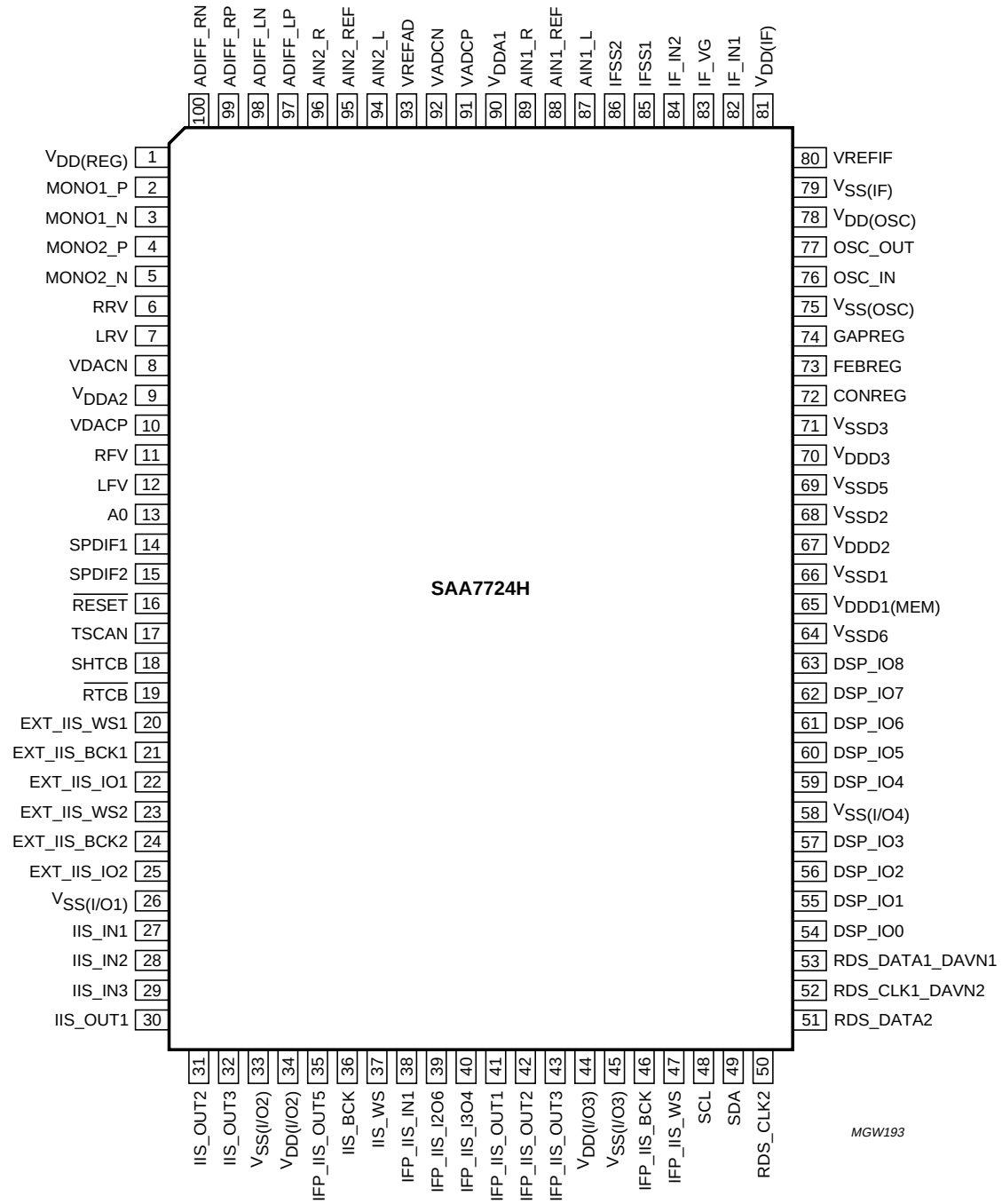


Fig.4 Pin configuration.

6 FUNCTIONAL DESCRIPTION

6.1 Voltage regulator

A voltage regulator (see Fig.5) controls all 2.5 V supplies of the chip (see Fig.6). The input supply voltage is 3.3 V. An external PMOS power transistor (e.g. BSH207) is used to handle power. The regulated 2.5 V supply is derived from a band gap voltage, which is AC-decoupled by an external capacitor.

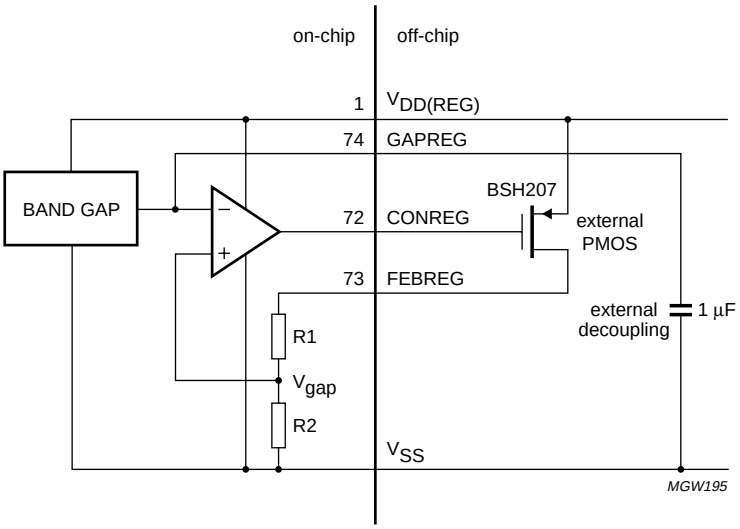


Fig.5 Voltage regulator schematic diagram.

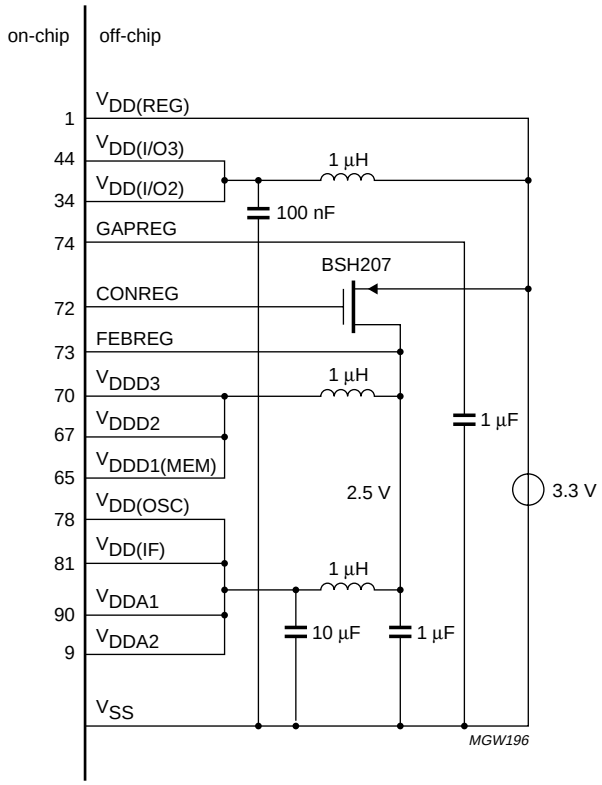


Fig.6 Voltage regulator connection diagram.

6.2 Audio analog front-end

The analog front-end consists of two identical 3rd-order sigma delta stereo ADCs (ADC1 and ADC2) with several input control blocks for handling common mode signals and acting as input selector (see Fig.7).

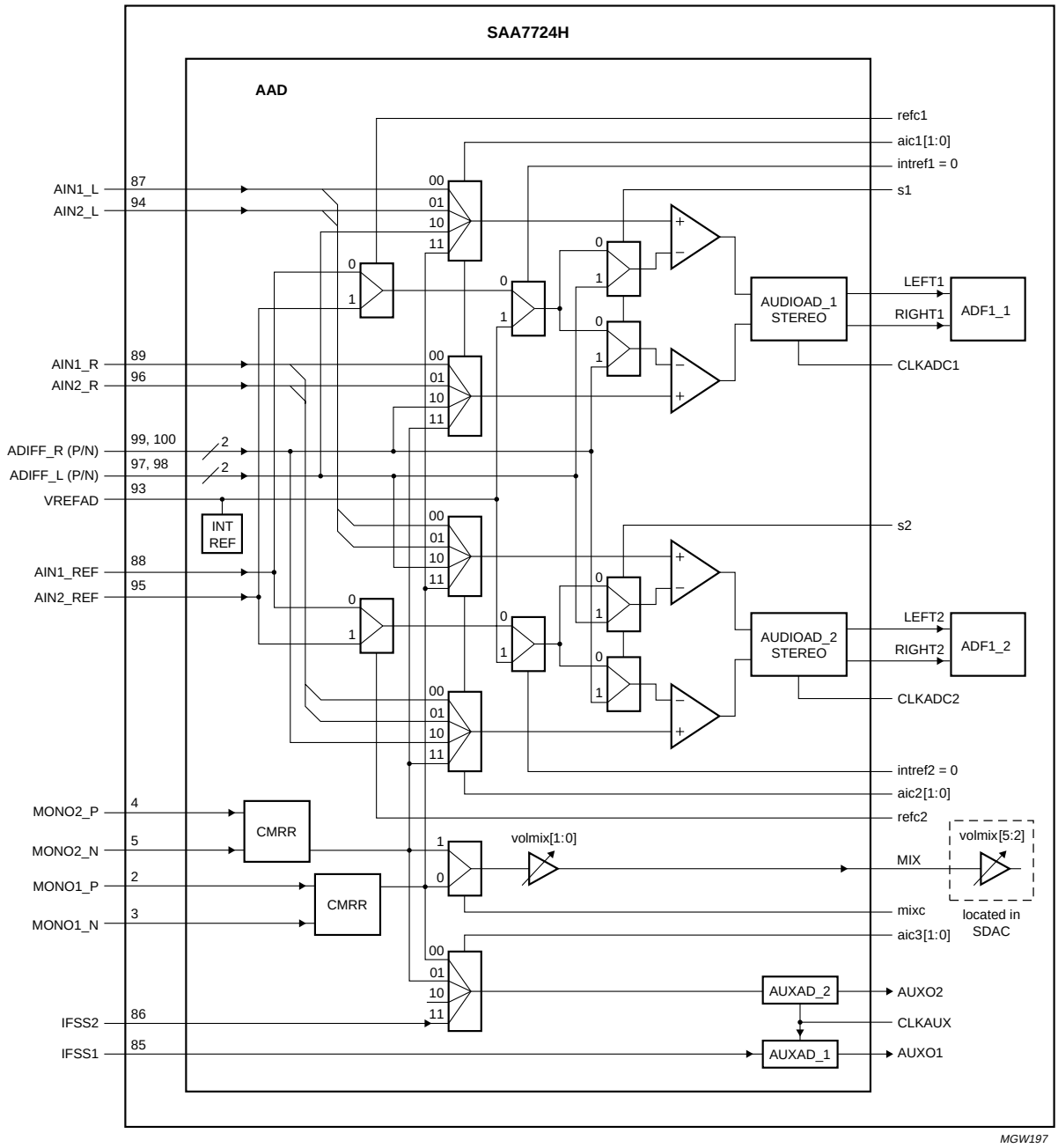


Fig.7 Analog front-end switch diagram.

The inputs ADIFF, AIN1, AIN2, MONO1 and MONO2 can be selected with the audio input controls (aic1 and aic2). The ground reference (REF1 and REF2) can be selected (refc1 and refc2) to enable the handling of common mode signals for AIN1 and AIN2. The switches s1 and s2 are needed for handling fully differential inputs at the ADIFF pins.

The MONO1 and MONO2 inputs have their own CMRR input stage and can be redirected to ADC1 and/or ADC2 via the audio input control (aic1 and aic2). In this event, the ground reference should be switched to internal (intref = 1). It is also possible to pass MONO1/MONO2 to the AUXAD (controlled by aic3) or directly mix the same MONO input with four DAC output channels, incorporating volume control.

6.2.1 SELECTOR DIAGRAM

Three bits are available to make it possible to redirect the inputs with their corresponding reference to the required AUDIOAD (see Tables 4 and 5). The input control for the AUXAD_2 is given in Table 6. The input selection of the mixer is given in Table 7.

Table 4 Reference connection for AUDIOAD_1 and AUDIOAD_2

I²C-BUS BIT			REFERENCE CONNECTION FOR AUDIOAD_1 and AUDIOAD_2
refc1, refc2	intref1, intref2	s1, s2	
0	0	0	REF1
1	0	0	REF2
–	1	0	VREFAD
–	–	1	differential

Table 5 Input connection for AUDIOAD_1 and AUDIOAD_2

I²C-BUS BIT		PREFERRED REFERENCE	INPUT CONNECTION FOR AUDIOAD_1 and AUDIOAD_2
aic1[1], aic2[1]	aic1[0], aic2[0]		
0	0	REF1	AIN1
0	1	REF2	AIN2
1	0	differential	ADIFF
1	1	VREFAD	MONO1 and MONO2

Table 6 Input connection for AUXAD_2

I²C-BUS BIT		INPUT CONNECTION FOR AUXAD_2
aic3[1]	aic3[0]	
0	0	MONO1
0	1	MONO2
1	0	not connected
1	1	IFSS2

Table 7 Input connection for the MIXER

I²C-BUS BIT	INPUT CONNECTION FOR THE MIXER
mixc	
0	MONO1
1	MONO2

6.2.2 Realization of the common mode input with AIN

A high CMRR can be created by the use of REF1 and REF2. These pins can be connected to the positive input of the second operational amplifier in the signal path with bits intref1, intref2, refc1 and refc2 (see Fig.8). The signal (of which a high CMRR is required) has a signal and a common signal as input. The common signal is connected to pin REF1 and/or REF2 and can be selected with bits refc1 and/or refc2.

The actual input can be selected with the audio input control (bits aic1[1:0] and aic2[1:0]). In Fig.8 the AIN1 input is selected. In this situation both signal lines going to the ADC will contain the common mode signal. The ADC itself will suppress this common mode signal with a high rejection ratio.

The input pins AIN1_L and AIN1_R are connected directly to the source. The 1 MΩ resistor provides the DC biasing of OA3 and OA4. The impedance level, in combination with the parasitic capacitance at input pin AIN_L or AIN_R, greatly determines the achievable common rejection ratio.

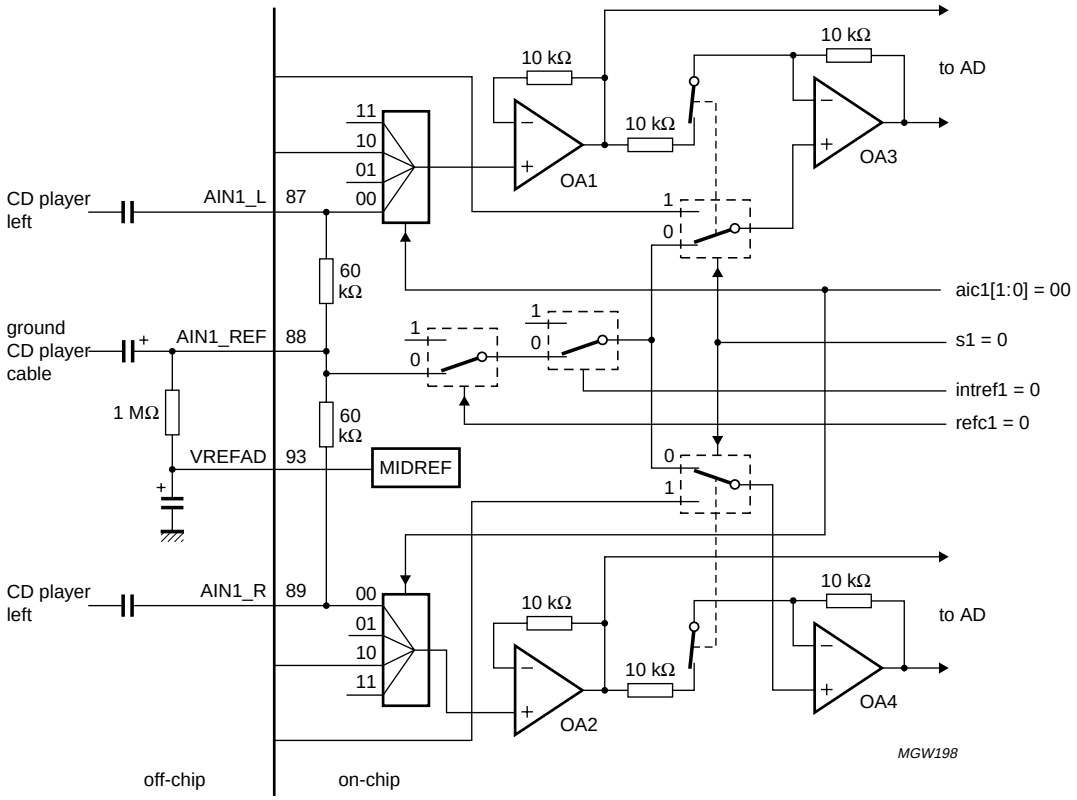


Fig.8 Example of the use of common mode analog input AIN1.

6.2.3 REALIZATION OF THE DIFFERENTIAL ADIFF INPUT

The ADIFF input is fully differential. The signal that is connected to this input should be a symmetrical signal.

Besides bits aic1[1:0] and aic2[1:0], to select the ADIFF_L and ADIFF_R input, the switches s1 and s2 are needed to put the ADIFF_L and ADIFF_R inputs in true differential mode (see Fig.9).

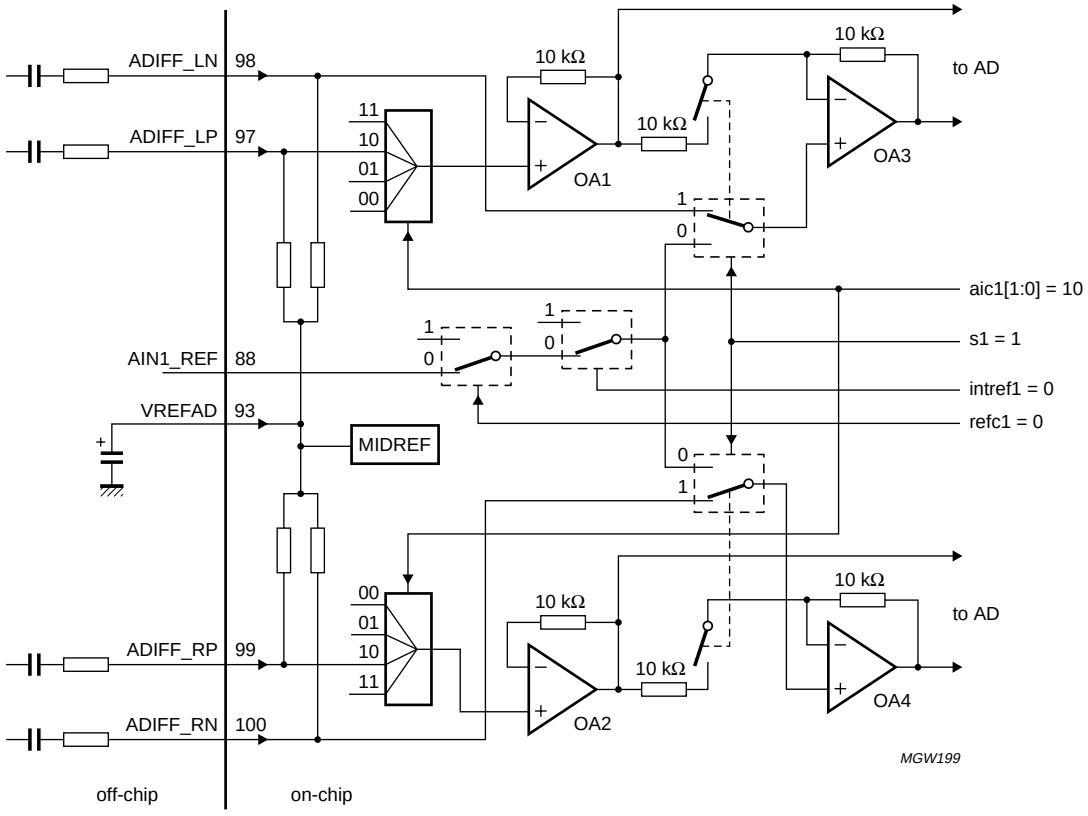


Fig.9 Example of the use of differential analog input ADIFF_L and ADIFF_R.

6.2.4 REALIZATION OF THE AUXILIARY INPUT WITH VOLUME CONTROL

A common mode input with volume control for mixing with four DAC outputs is provided (see Fig.10). The inputs consist of pins MONO1_P and MONO2_P, both accompanied with their ground signals (pins MONO1_N and MONO2_N). After selection of MONO1 or MONO2, with bit mixc, the volume can be changed from 0 to –22.5 dB in 1.5 dB steps. The attenuated signal can be added to the left and/or right front and/or left and/or right rear DAC channels. When the mix signal is added to the output, the gain of the output is automatically adjusted to prevent clipping at high input levels.

The inverse output signal of both CMRR circuits can also be switched to the AUDIOAD_1 and/or AUDIOAD_2 and/or AUXAD_2.

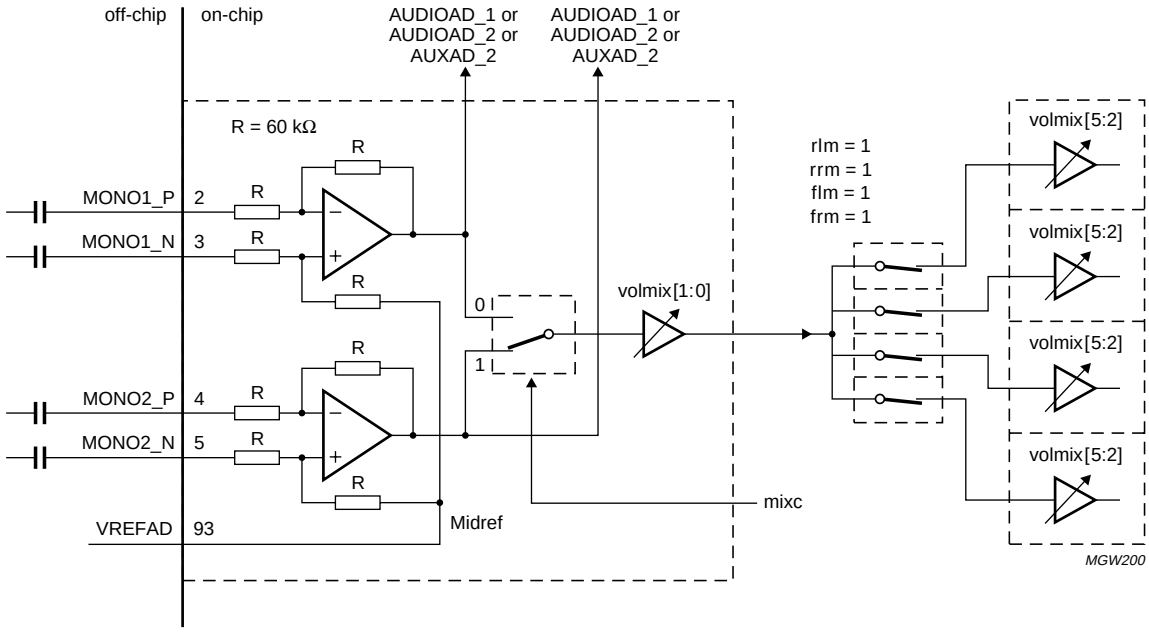


Fig.10 MONO input circuit.

Table 8 Mix volume control

I²C-BUS BIT volmix[5:0] (hex)	OUTPUT MIX GAIN (dB)
3F	0
3B	–1.5
37	–3.0
33	–4.5
2F	–6.0
2B	–7.5
27	–9.0
23	–10.5
1F	–12.0
1B	–13.5
17	–15.0
13	–16.5
0F	–18.0
0E	–19.5
0D	–21.0
0C	–22.5
00	MUTE

The bits volmix[5:2] are binary weighted organized and used for setting the mixer gain from 0 to –18 dB. The selection bits are connected to the mixer in the QSDAC.

The bits volmix[1:0] are also binary weighted organized and connected to the analog front-end.

The MIX signal can be added to all outputs independant of each other.

Table 9 Mix output control; note 1

I²C-BUS BIT		DAC OUTPUT			
BIT	**VALUE**	**FL**	**FR**	**RL**	**RR**
flm	0	off	X	X	X
	1	on	X	X	X
frm	0	X	off	X	X
	1	X	on	X	X
rlm	0	X	X	off	X
	1	X	X	on	X
rrm	0	X	X	X	off
	1	X	X	X	on

Note

1. X = not controlled by this bit.

6.2.5 Supplies and references

6.2.5.1 Reference pins VADCN and VADCP

These pins are used as a negative and positive reference for the AUDIOAD_1 and AUDIOAD_2 and the level ADC. These references needs to be “clean”.

6.2.5.2 Reference pin VREFAD

The midref voltage of the ADCs is filtered via this pin. This midref voltage is used for half supply reference of the ADCs. External capacitors (connected to groundplane) prevent crosstalk between the switched capacitor DACs of the internal ADCs and buffers and improves the power supply rejection ratio of all components (see Fig.11).

$$V_{VREFAD} = \frac{V_{VADCP} - V_{VADCN}}{2}$$

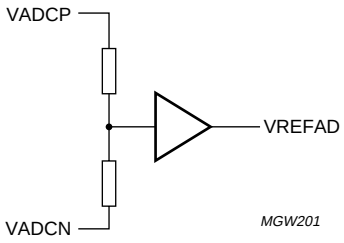


Fig.11 VREFAD reference circuit.

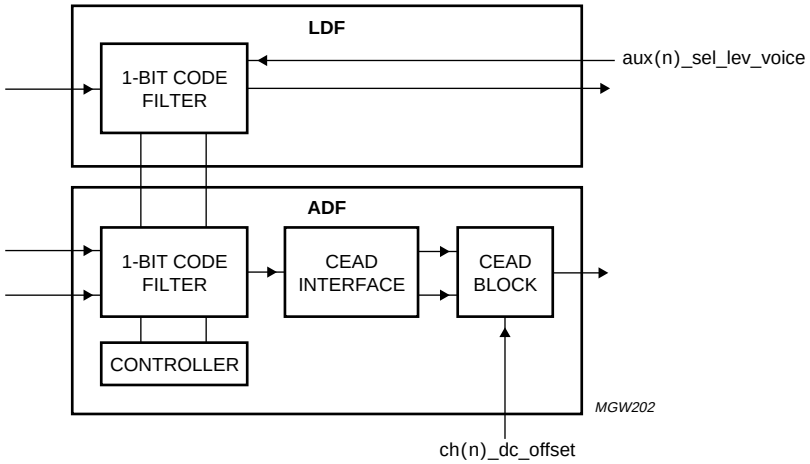
6.2.5.3 Analog supply inputs

The analog input circuit has separate power supply (V_{DDA1}) connections to allow maximum filtering. The input stage of every operational amplifier within the analog front-end is supplied by a 3.3 V supply voltage so as to enable a rail-to-rail input signal.

6.3 AD decimation paths (DAD)

The AD decimation paths for both the level and audio are achieved in the DAD block; (see Fig.12). There are two DAD blocks implemented for the SAA7724H.

The DAD block consists of a Level Decimation Filter (LDF) which handles the AUX decimation and an Audio Decimation Filter (ADF) which handles the AUDIO decimation.



(n) is 1 or 2.

Fig.12 DAD block diagram.

6.3.1 LDF AND AUX DECIMATION PATH

The input signal has a sample frequency of $128 \times f_s$ and comes from a 1st-order ADC. The first part of the decimation is done using a CIC filter. For the AUX decimating filter a 2nd-order CIC filter is implemented.

A branch is also available from this filter for a signal having a sample frequency of $8 \times f_s$. This signal also passes a built-in high-pass filter section to make it adequate for level IAC detection purposes. With a sampling frequency of 8×42.1875 kHz the –3 dB point of this filter is at approximately 60 kHz.

The CIC filter decimates the sample frequency by 64. The new output sample rate is $2 \times f_s$. The $\frac{\sin x}{x}$ roll-off of the CIC filter needs to be compensated for, therefore, a roll-off compensation filter is utilized.

The last stage of the AUX decimation filter is the realization of the appropriate bandwidth characteristic. The bits aux1_sel_lev_voice and aux2_sel_lev_voice selects between the level characteristic and the audio characteristic for voice input.

The transfer characteristics, level and audio, of the AUX decimation filter are illustrated in Fig.13. It should be noted that the figure corresponds with a 38 kHz sample rate. For the SAA7724H a 42.1875 kHz sample rate is used, the horizontal values need to be scaled with a factor of $\frac{42.1875}{38}$

Remark: The absolute gain or attenuation of the graphs in Fig.13 has no meaning. The relative levels however have. When bit aux1_sel_lev_voice or aux2_sel_lev_voice is logic 1, the coefficient for audio processing is active. When bit aux1_sel_lev_voice or aux2_sel_lev_voice is logic 0, the coefficient for level processing is selected.

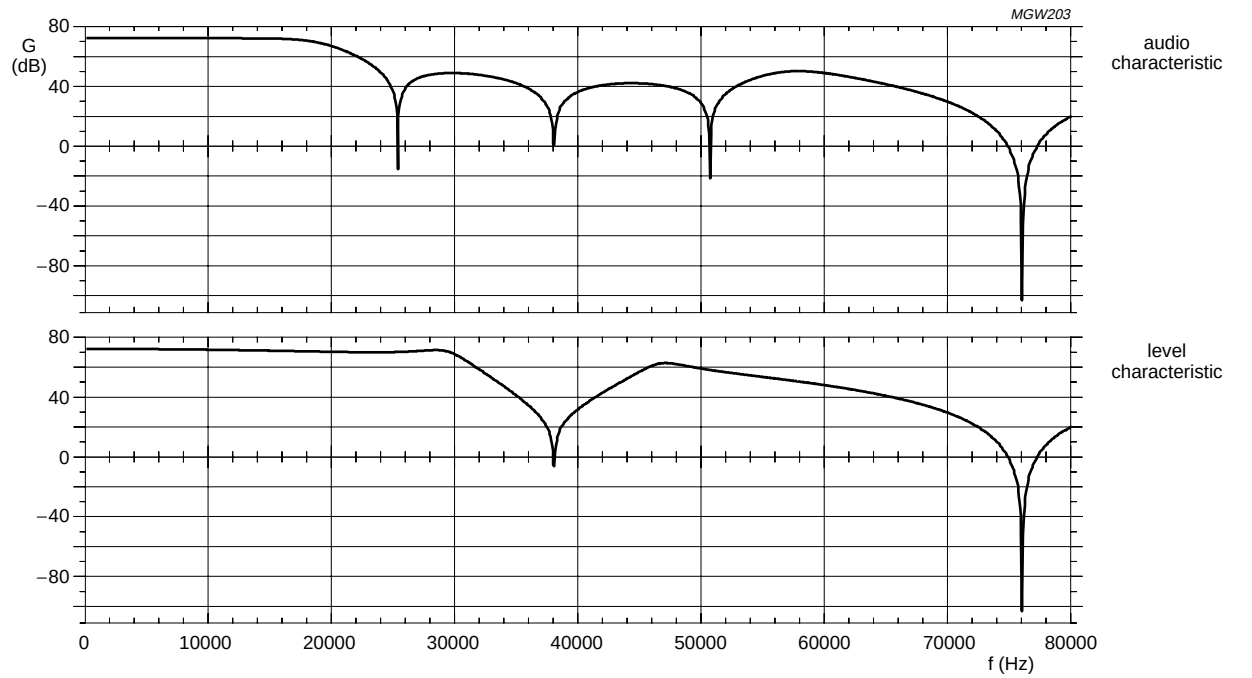


Fig.13 AUX decimation path transfer characteristics.

6.3.2 ADF AND AUDIO DECIMATION PATH

The input signal has a sample frequency of $128 \times f_s$ and comes from a third order sigma delta ADC. The first step in the decimation process is done by the 1-bit code (CIC) filter. This CIC filter decimates the input sample rate by a factor of 16, which results in a sample rate of $8 \times f_s$.

After the 1-bit code filter, sample rehashing is necessary prior to entering the CEAD block. The CEAD block decimates the audio samples further by a factor of 8, resulting in a sample rate of $1 \times f_s$. The overall gain in the pass-band of the decimation filter, including the CIC filter and CEAD block becomes 4.85 dB. A nominal input level of −7.36 dB coming from the ADC will result in a −2.5 dB level after decimation.

The DC filter in the CEAD block is controlled by I²C-bus bit ch1_dc_offset or ch2_dc_offset; see Table 27. There is no power-on reset circuitry implemented. This means that after power-up, all filters will go through a fast transient phase before they reach their steady state behaviour.

6.4 Digital audio input/output

This section describes the external I²S-bus input/output ports, the EPICS host I²S-bus port and the SPDIF inputs.

6.4.1 GENERAL

There are two external I²S-bus input/output ports available on the circuit, and three host I²S-bus ports. The I²S-bus inputs and host I²S-bus outputs are capable of handling Philips I²S-bus, and LSB-justified formats of 16, 18, 20 and 24-bit word sizes. The external I²S-bus output ports only support Philips I²S-bus. For the general waveforms of the five possible formats see Fig.14. More general information on the Philips I²S-bus format is given in Chapter 12.

Note: When the applied word length is smaller than 24 bits, the LSB bits will get (internally) a zero value. When the applied word length exceeds 24 bits, the LSBs are skipped.

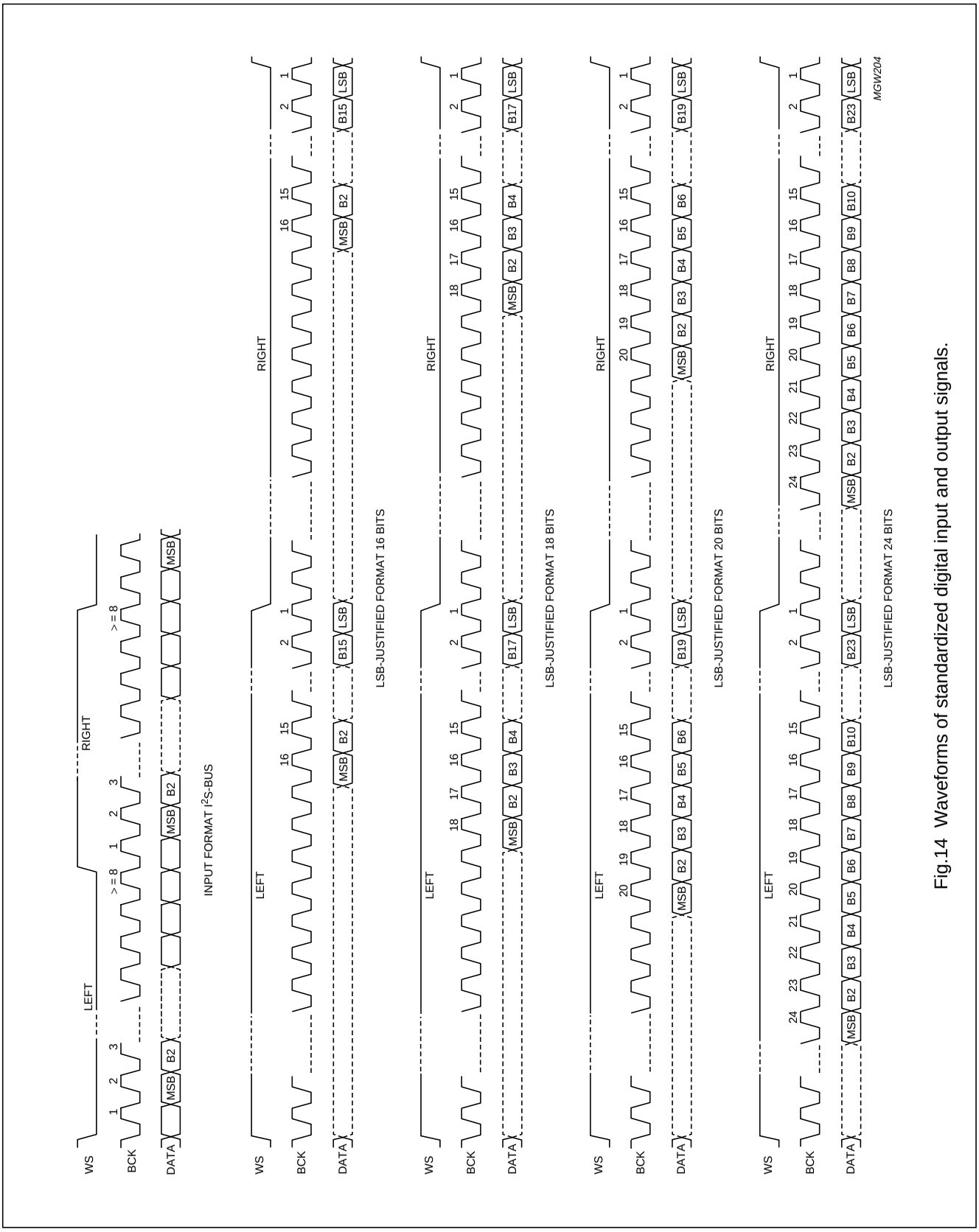


Fig.14 Waveforms of standardized digital input and output signals.

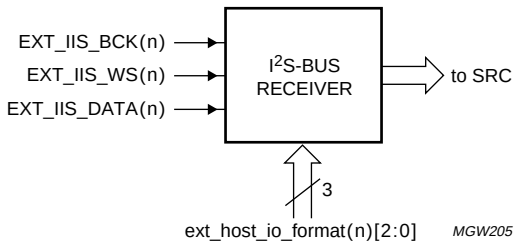
6.4.2 External I²S-bus input/output ports

An I²S-bus interface is provided for communication with external digital sources. It is a serial 3-line bus, having one line for data, one line for clock and one line for the word select. For external digital sources the circuit acts as a slave, so the external source is master and supplies the Bit Clock (BCK) and Word Select (WS).

Figure 15 shows the external I²S-bus receiver and controls.

Table 10 defines the possible modes that must be set for the I²S-bus inputs.

An extra function that is provided is that the EXT_IIS ports can also be set, as an output, from the Sample Rate Converters (SRC). In this event only the Philips I²S-bus format is supported.



(n) is 1 or 2.

Fig.15 External I²S-bus input and controls.

Table 10 External I²S-bus input formats

ext_host_io_format1 [2:0] ext_host_io_format2 [2:0]			FORMAT
0	X(1)	X(1)	Philips I²S-bus
1	0	0	LSB -justified 16 bits
1	0	1	LSB-justified 18 bits
1	1	0	LSB-justified 20 bits
1	1	1	LSB-justified 24 bits

Note

1. X = don't care.

6.4.2.1 SRC audio signal flows

Figure 16 shows the audio signal flow possibilities for the sample rate converters SRC1 and SRC2. The inputs to the SRCs can be either an external source, or an internal signal from the AUDIO_EPICS.

The outputs from the SRCs can either work as a slave output from an externally connected bus to an external I²S-bus Port 1 or 2, or it can convert the internal SAA7724H sample rate directly to the AUDIO_EPICS and the switchboard in the IFP. If conversion to an external sample rate is selected, the audio signals to the IFPs switchboard and the AUDIO_EPICS are muted, while their sample rates are maintained at the internal SAA7724H sample rate.

All I/O possibilities of the SRCs can be set by eight independent I²C-bus bits. Some selections are conflicting or make no sense. In order to keep as much flexibility as possible there is no detection of conflicting settings, however the circuitry is guaranteed not to cause a hang-up situation.

All audio paths to and from the SRCs are 24 bits wide. Inside the switchboard from the IFP, the audio is always truncated to 16 bits.

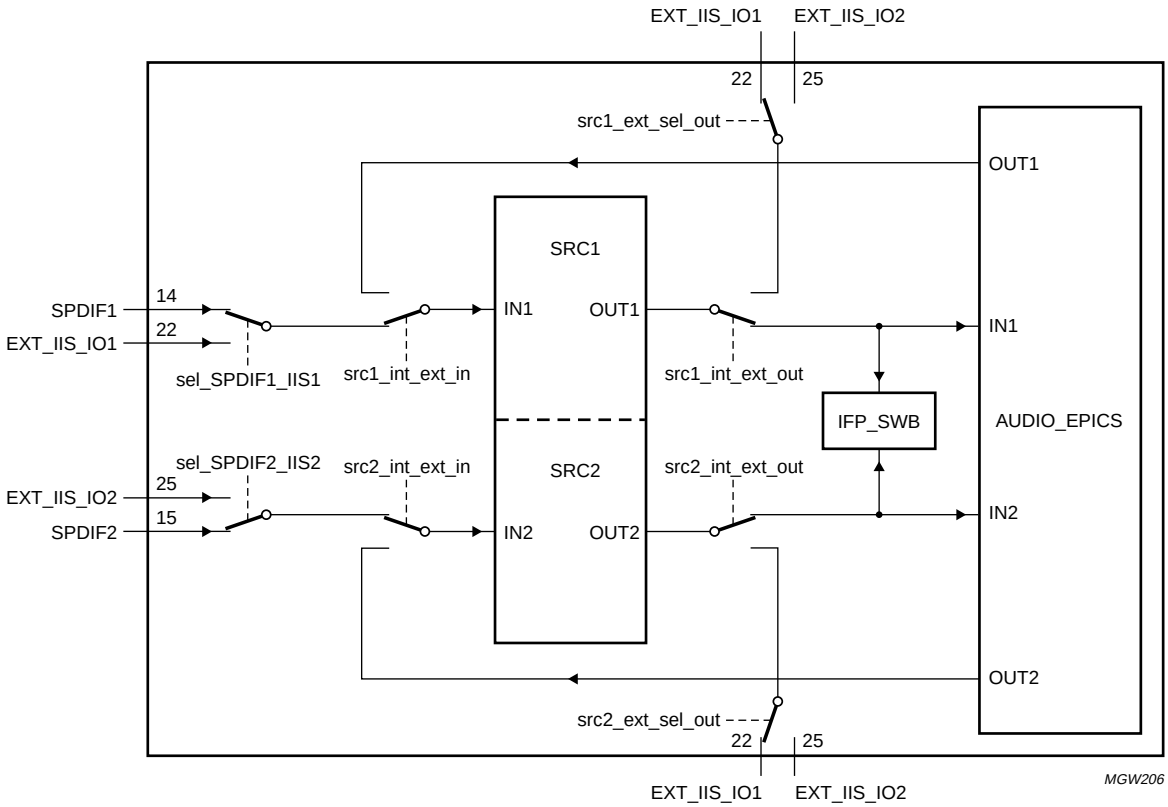


Fig.16 SRC audio signal flows.

6.4.2.2 Sampling frequency range limitations

The external I²S-bus inputs are guaranteed for a continuous 8 kHz to 48 kHz sampling frequency range.

6.4.2.3 BCK and WS limitations

The rate at which the I²S-bus receivers decode data available to the system, depends on the WS frequency. For normal application only $1 \times f_s$ is used. The WS duty cycle does not need to be 50 % for any of the applied formats.

The BCK is limited to a maximum frequency of $256 \times f_s$.

The lower limit is defined by the number of bits that are required to be sent. For LSB-justified formats the number of BCKs must be at least the number of bits that is selected per channel.

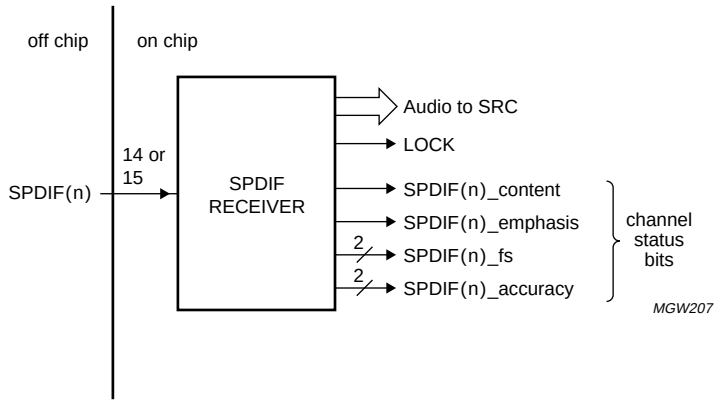
6.4.3 External SPDIF input

A signal can be applied to one or both of the SPDIF inputs that conforms to the IEC 60958 specification.

The SPDIF receivers support SPDIF audio data up to 24 bits. Some channel status bits are also decoded and made available to the system.

There is no support for user data decoding, nor availability of the validity bit.

Figure 17 shows the SPDIF receiver and its outputs. The exact meaning of the output bits is given in Table 30. The SPDIF inputs do not have any specific control signals.



(n) is 1 or 2.

Fig.17 SPDIF receiver and its outputs.

6.4.3.1 SPDIF input application diagram

Figure 18 shows the general set-up for an SPDIF input for consumer applications.

Figure 19 shows an example of how to prevent crosstalk from two adjacent SPDIF inputs, due to the parasitic capacitance from lead finger and bond wires. Therefore extra capacitors are added near the pins.

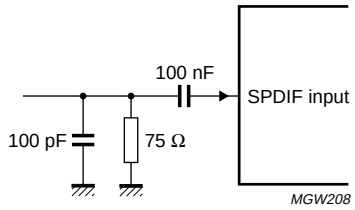


Fig.18 General SPDIF input application.

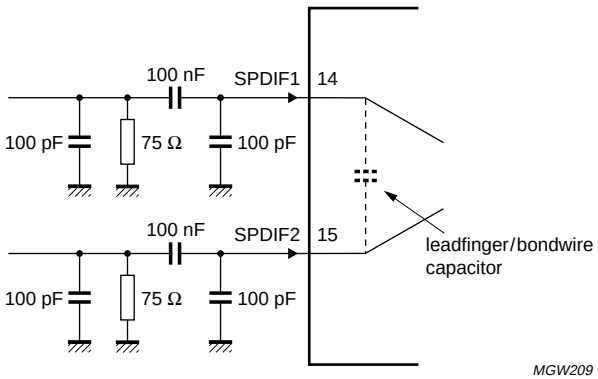


Fig.19 Example of crosstalk prevention for SPDIF inputs.

6.4.3.2 Sampling frequency range limitations

The external SPDIF input sample rates are 32, 44.1 and 48 kHz.

The accuracies of the supported standardized sampling frequencies at the SPDIF inputs meets the requirements of Level II accuracy as specified in IEC 60958, being 0.1 %.

6.4.3.3 Channel status bits

The channel status bits given in Table 11 are available from the SPDIF receiver. The information is taken from the left audio channel.

The channel status bits are available in the I²C-bus map, where the exact meaning of the bits can also be found; see Table 30.

Table 11 SPDIF channel status bits

CHANNEL STATUS BIT NUMBER	CONSUMER FORMAT MEANING
1	data/audio mode
3	pre-emphasis
25 and 24	sampling frequency
29 and 28	clock accuracy

6.4.3.4 Lock indicator

The SPDIF receiver has a LOCK pin. The polarity is described in the I²C-bus map. When the system is not in lock, the audio data will be muted (being zero data values). In the event that the SPDIF signal is missing or very distorted, the timing information to the SRC from the SPDIF receiver will not be good or may even disappear. This will cause the SRC to get unlocked.

Locking will occur within 5 ms after reset, or 5 ms after the availability of a proper SPDIF signal at the input.

The lock indicator is available at one of the EPICS status flags, and thus also readable via the I²C-bus. The exact location is given in Table 25.

6.4.4 EPICS HOST I²S-BUS PORT

Because this is a master I/O port the EPICS host I²S-bus generates its own WS and BCK. There is one WS and BCK for all three output and input data paths. The definition of how the WS and BCK are generated can be found in Chapter 11. Figure 20 shows the EPICS host I²S-bus I/O and controls.

The EPICS host I²S-bus has its own setting for selecting the formats; see Table 12. The setting of the EPICS rate should be taken into account, for setting the desired host I²S-bus format. The LSB-justified formats 18, 20 and 24 bits are not available when the EPICS is running at a rate other than $1 \times f_s$.

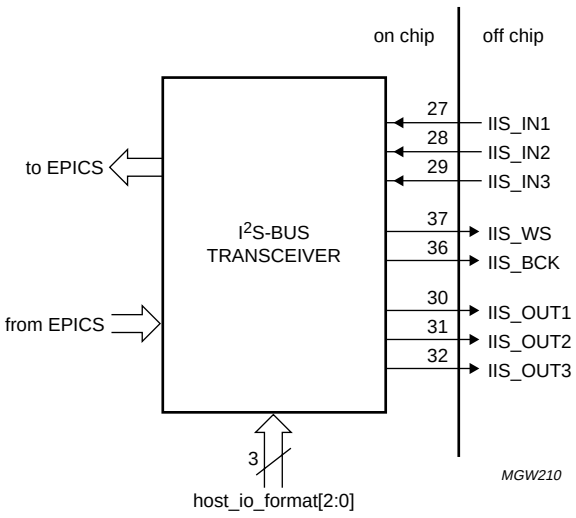


Fig.20 EPICS host I²S-bus with controls.

Table 12 External EPICS host I²S-bus formats

host_io_format2	host_io_format1	host_io_format0	FORMAT
0	X(1)	X(1)	Philips I²S-bus
1	0	0	LSB-justified 16 bits
1	0	1	LSB-justified 18 bits; note 2
1	1	0	LSB-justified 20 bits; note 2
1	1	1	LSB-justified 24 bits; note 2

Notes

1. X = don't care.
2. Not supported for EPICS rates other than $1 \times f_s$.

6.5 Sample rate converter

There are two Sample Rate Converters (SRCs) available in the SAA7724H. The input of each SRC can be an external source or internal audio from the AUDIO_EPICS. The outputs are fed to the IFPs switchboard and the AUDIO_EPICS or to an external I²S-bus port; see Section 6.4.2.1.

Both SRCs meet the requirements given in Table 13.

Table 13 SRC specification

SRC CHARACTERISTIC	SPECIFICATION
Input sample rate	continuously 8 kHz to 48 kHz; absolute accuracy 0.1 %
Output sample rate	continuously 8 kHz to 48 kHz
THD + N	≥ 96 dB at 1 kHz
Overall gain	0 dB
Maximum ripple amplitude (0 to 0.45 f_s)	0.1 dB
Stop band suppression (0.55 f_s to 1 f_s)	≥ 98 dB
Output word width	24 bits
Lock time	≤ 45 ms
Audio during unlocked state	muted (zero data)

6.6 IF_AD

The IF_AD performs the analog-to-digital conversion of the FM/AM-IF signal. It generates 10-bit data. For dual radio two IF_AD convertors are incorporated (see Fig.21).

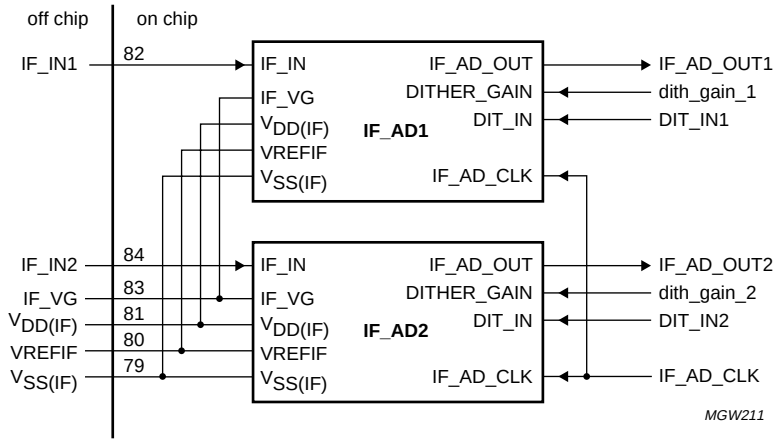


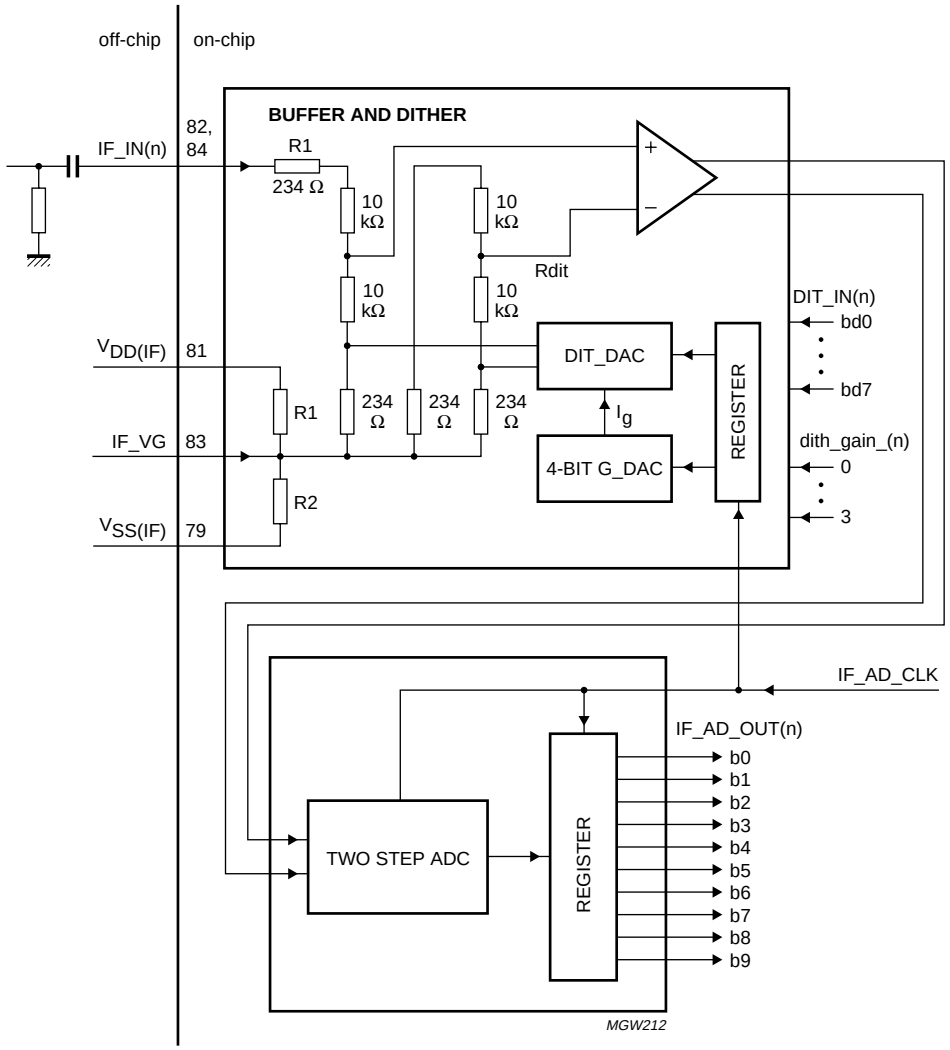
Fig.21 IF_AD dual block diagram.

6.6.1 IF_AD SINGLE BLOCK DIAGRAM

The IF_AD block diagram shows the analog part. It consists of a buffer and dither block and a two-step ADC.

6.6.2 IF_AD DETAILED FUNCTIONAL DESCRIPTION

The IF_AD consists of several blocks. These blocks are the ADC itself preceded by a buffer and dither differential summing point. The dither is made with a dither DAC (DIT_DAC) combined with gain variation in G_DAC. The interface to the IFP is fed via the registers shown in Fig.22.



(n) is 1 or 2.

Fig.22 IF_AD single block diagram; analog part.

6.6.2.1 ADC

The ADC is based on the two-step principle.

6.6.2.2 Buffer

The buffer is configured as a single-ended to differential convertor.

6.6.2.3 Dithering

Dither can be applied via the dither DACs DIT_DAC and G_DAC. The input voltage range and the dither level are both proportional to the supply voltage.

DIT_DAC is driven by the IFP. The source is an 8-bit word having 9 values representing –4 (00000000) to +4 (11111111). The total number of 1s in the 8-bit input word represent the code that the DIT_DAC is using. The maximum negative output voltage is represented by all 0s on the 8-bit word, and the maximum positive output voltage is represented by all 1s on the 8-bit word. A nominal value of 0 V, which is half way between the maximum positive output voltage and the maximum negative output voltage at the output of the DIT_DAC, is represented by setting any four of the eight bits to logic 1 and the other four bits to logic 0.

To adjust the G_DAC dither to the required level, the multiplying current of the DIT_DAC can be changed with a binary weighted current DAC. The reference current is derived from an internal reference source which is proportional to $V_{DD(IF)}$. As a reference point for the equivalent input dither level, at nominal supply voltage, the following equation is used:

$V_{ditppeq} = 3.7 \times$ ditgain (mV).

6.7 AUDIO_EPICS specific information

This chapter contains specific additional information, over the EPICS7A programmers guide, specifically for the SAA7724H.

The I^2C-bus registers, some of which are mapped onto XMEM address space, are shown in Chapter 11.5, Tables 21 to 23.

6.7.1 AUDIO_EPICS START-UP

The AUDIO_EPICS will start running the code after the reset procedure has been completed. This code will start running from address 0 by default, if not reprogrammed by the user before releasing the pc_reset bit.

6.7.2 AUDIO_EPICS MEMORY OVERVIEW

The memory sizes for the AUDIO_EPICS are given in Table 14.

Table 14 AUDIO_EPICS memory list

MEMORY TYPE	PRODUCT VERSION
DSP program memory	ROM: 5120 words
DSP X memory	RAM: 3584 words
DSP Y memory	RAM: 1024 words

6.8 SDAC output path

There are two SDACs implemented in the SAA7724H, one for the front channels (SDAC_F) and one for the rear channels (SDAC_R).

The total digital-to-analog conversion path, consists of the following components (see Fig.23):

1. An upsample filter
2. A 3rd-order noise shaper
3. A compensation and dynamic element matching (CoDEM) scrambler
4. The multibit SDAC with current compensation.

All circuitry including the analog part use a $128 \times f_s$ clock.

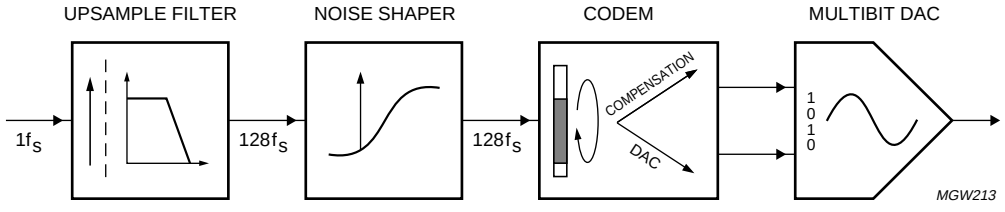


Fig.23 SDAC path diagram.

6.8.1 DAC UPSAMPLING FILTER

The upsampling filter interpolates a 24-bit stereo signal from $1 \times f_s$ to $8 \times f_s$ by cascading two half-band FIR filters. Interpolating to $128 \times f_s$ is done by a sample-and-hold filter.

6.8.2 DAC NOISE SHAPER

A 3rd-order noise shaper is used to quantize the 24-bit input signal that is fed from the upsampling filter into a 5-bit output signal. The generated quantization noise is shaped outside the audio band.

6.8.3 DAC CODEM SCRAMBLER

The CoDEM scrambler has three different functions. Firstly it converts the 5-bit signal from the noise shaper into a thermometer code. Secondly, after conversion, the thermometer code is scrambled by means of a Dynamic Element Matching (DEM) algorithm. Thirdly, by using this code, matching errors in the analog part of the SDAC have less influence on the performance. The CoDEM also generates a compensation vector for the compensation part of the DAC.

6.8.4 MULTI-BIT SDAC

The SDAC is a multi-bit DAC based upon 31 switched resistors. The 31 resistors form a network which can create 32 DC output levels. The exact analog output level is the sum of the DC level and the superimposed bitstream signal. In the application a simple low-pass filter (one capacitor) must be used at the outputs of the SDAC.

The overall DAC filters spectral plot is illustrated in Fig.24.

As an example a left filtered output is selected, which also has a 3.3 nF output filtering capacitor connected.

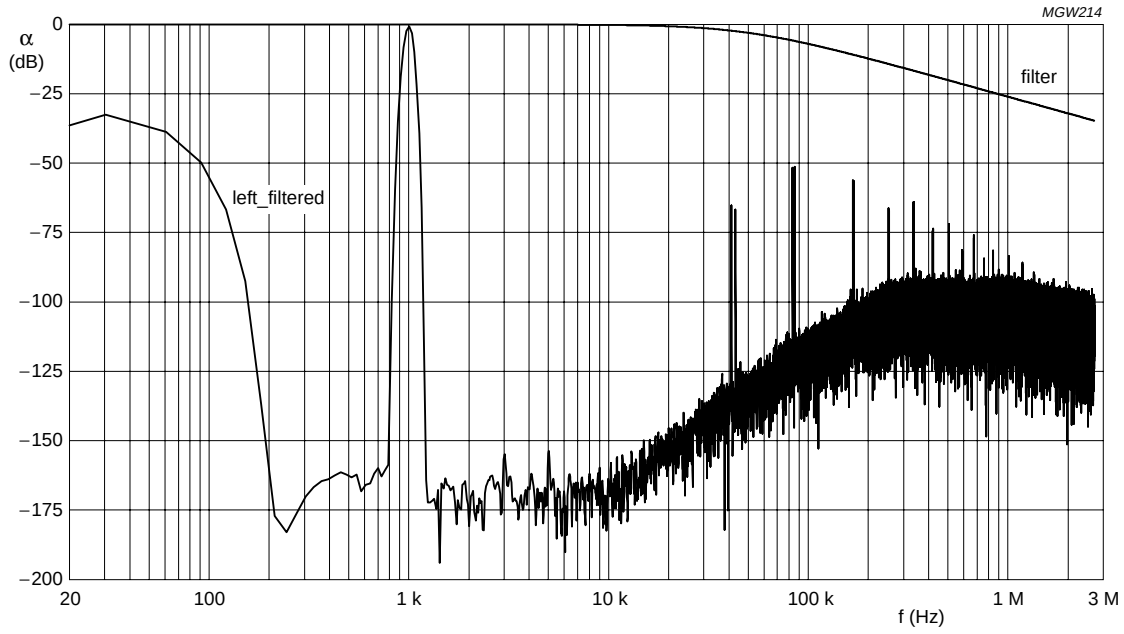


Fig.24 DAC filters spectral diagram.

6.8.5 ANALOG SUMMER FUNCTION

The SDAC is featured with the analog summing of signals from the ADCs; for details of this function see Chapter 6.2.

6.8.6 SDAC APPLICATION DIAGRAM

An example of the circuitry surrounding the DAC outputs is illustrated in Fig.25.

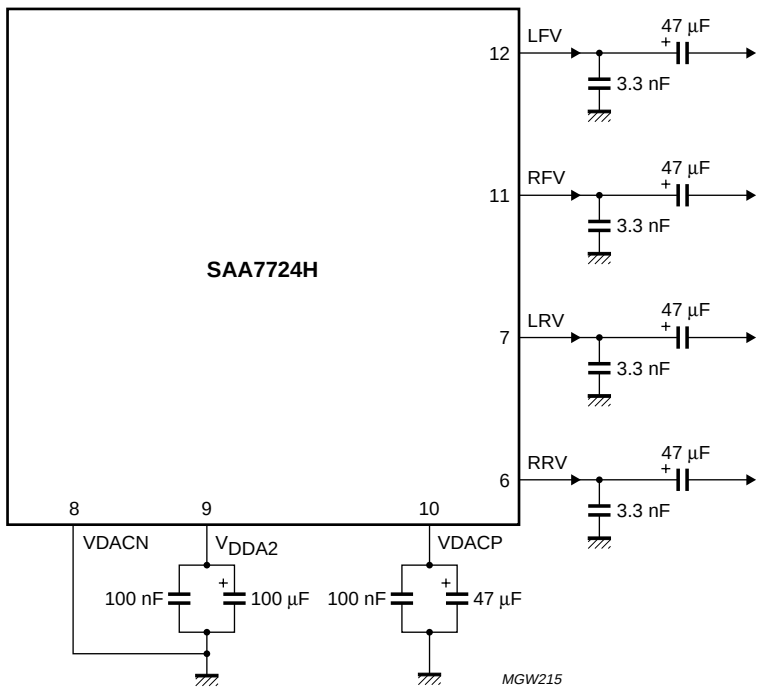


Fig.25 DAC outputs application diagram.

6.9 Reset block functional overview

The reset block uses the asynchronous reset signal from pin $\overline{\text{RESET}}$ to generate synchronous reset signals. The generated reset signals are described in the following sections.

6.9.1 ASYNCHRONOUS RESET

The asynchronous reset signal from pin $\overline{\text{RESET}}$ asynchronously disables the SDA pin (set HIGH) whenever the reset signal is active.

Furthermore, all 3-state and bidirectional outputs are kept 3-state asynchronously as long as pin $\overline{\text{RESET}}$ is kept LOW, and the internal reset sequence is still ongoing. It requires approximately 1100 OSCIN_CLK cycles to complete the reset sequence after the $\overline{\text{RESET}}$ pin has gone HIGH. After reset the state of the SAA7724H will be as specified in Table 2.

6.10 Clock circuit and oscillator

6.10.1 CIRCUIT DESCRIPTION

The chip has an on-board crystal clock oscillator with amplitude control based on a Pierce oscillator; see Fig.26. The oscillator is implemented as an inverter with capacitive coupling at the input. When the transconductance of this inverter is sufficiently high, the feedback loop becomes unstable and the circuit starts to oscillate.

This oscillation grows until its amplitude has reached a specific value which is detected by the AGC. In this way, clipping of the output voltage against the supply voltages is prevented. The AGC also ensures that the transconductance builds up very rapidly after power-on and stays sufficiently high during oscillation.

The sinusoidal output is converted into a CMOS compatible clock by the comparator.

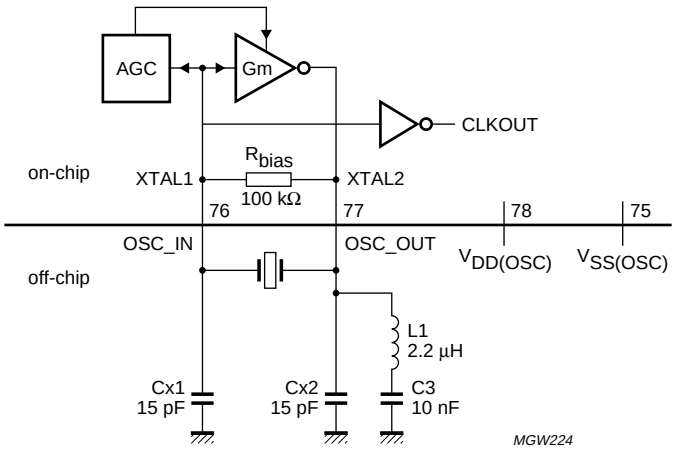


Fig.26 Schematic diagram of the crystal oscillator circuit.

6.10.2 External clock input mode

It is possible to use the oscillator as a clock input. In external clock input mode, an external clock signal is input on pin OSC_IN and this clock signal is transferred to the output via an extra output inverter stage. In this mode, the quartz crystal, L1, Cx2 and C3 may be removed, but this is not obligatory.

6.10.3 Crystal oscillator supply

The power supply connections to the oscillator are separated from the other supply lines to minimize feedback from on-chip ground bounce to the oscillator circuit. Noise on the power supply affects the AGC operation therefore the power supply should be decoupled. The $V_{SS(OSC)}$ pin is used as ground supply and the $V_{DD(OSC)}$ as the positive supply.

6.10.4 Application guidelines

For correct operation of the oscillator, two load capacitors (Cx1 and Cx2) need to be added externally to the chip. This configuration is adequate for the required crystal frequency of 43.2 MHz.

The external components shown in Fig.26 are specified in Table 15. The use of other values may prevent the oscillator from start-up.

A quartz crystal oscillator is used to generate the clock signal CLKOUT. In the case of an overtone oscillator, the ground harmonic is filtered out by L1 and Cx2.

A quartz crystal should be used with a series resonance resistance of less than 80 Ω and a capacitance of less than 7 pF. The crystal should be manufactured for a load capacitance of 10 pF. The value of C3 is not critical as long as it is not much lower than 10 nF (10 % is accurate enough). There is no theoretical upper limit.

Table 15 External components specification for the crystal oscillator

COMPONENT	MIN.	TYP.	MAX.	UNIT
Cx1	13.5	15.0	16.5	pF
Cx2	13.5	15.0	16.5	pF
C3	9	10	–	nF
L1	1.98	2.2	2.42	µH

6.11 PLL circuits

In the SAA7724H two PLL circuits (PLL1 and PLL2) are available that deliver the clocks for the AUDIO_EPICS and the SRC_EPICS block.

6.12 RDS

In the SAA7724H there are two RDS demodulation and decoder systems available. The description applies to each of the RDS blocks.

6.12.1 General description

The RDS function recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting. The operational functions of the demodulator and decoder are in accordance with EBU specification EN 50067.

The RDS function processes the RDS signal, that is frequency multiplexed in the stereo-multiplex signal, to recover the information transmitted over the RDS data channel. This processing consists of band-pass filtering, RDS demodulation and RDS/RBDS decoding.

The stereo-multiplex signal is input from the IFP. Under control of I^{2}C-bus bit rds_clkin, an internal buffer can be used to read out the raw RDS stream in bursts of 16 bits. With the I^{2}C-bus bit rds_clkout the RDS clock can be enabled or switched off. The RDS band signal level can be read from a memory location in the SRC_EPICS, which needs to be defined.

The RDS band-pass filter discards the audio content from the input signal and reduces the bandwidth.

The RDS band signal level detector removes a possible Autofahrer Rundfunk Information (ARI) signal from the RDS band-pass filter output and measures the level of the remaining signal.

The RDS demodulator regenerates the raw RDS bitstream (bit rate = 1187.5 Hz) from the modulated RDS signal in two steps. The first step is the demodulation of the double sideband suppressed carrier signal around 57 kHz into a baseband signal, by carrier extraction and down-mixing. The second step is the Binary Phase Shift Key (BPSK) demodulation of the biphase coded baseband signal, by clock extraction and correlation.

The RDS/RBDS decoder provides block synchronization, error detection, error correction, complex flywheel function and programmable block data output. Newly processed RDS/RBDS block information is signalled to the main microcontroller as ‘new data available’ using the DAVN output. The block data itself and the corresponding status information can be read out via an I^{2}C-bus request.

The RDS/RBDS decoder contains the following major functions needed for RDS/RBDS data processing:

- RDS and RBDS block detection
- Error detection and correction
- Fast block synchronization
- Synchronization control (flywheel)
- Mode control for RDS/RBDS processing
- Different RDS/RBDS block information output modes (e.g. A/C’ block output mode).

External decoding of the raw RDS bitstream, would require a microcontroller interrupt every 842 μs. The double 16-bit RDS buffer allows the RDS data to be monitored at a 16 times lower rate, i.e. every 13.5 ms.

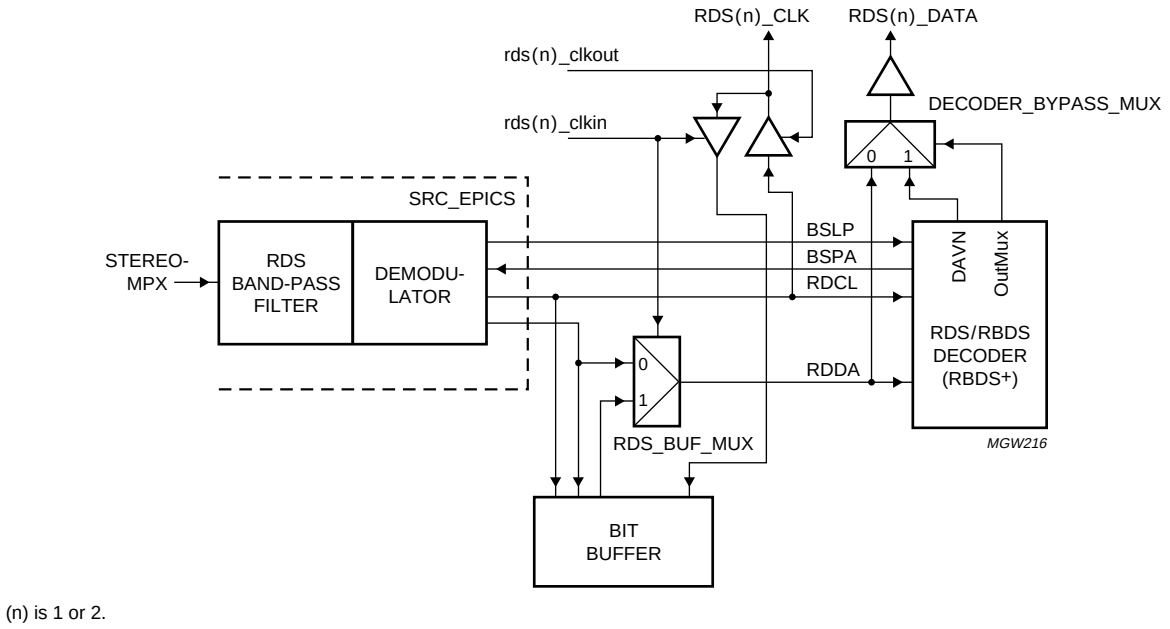


Fig.27 RDS/RBDS functional block diagram.

6.12.2 RDS I/O MODES

Apart from control inputs and data outputs via the I^{2}C-bus, the following inputs and outputs are related to the RDS function.

Unbuffered raw RDS output mode (rds1_clkin = 0, rds2_clkin = 0, rds1_clkout = 1, rds2_clkout = 1 and DAVD mode: dac0 = 1 and dac1 = 1):

- RDS_CLK: clock of the raw RDS bitstream, extracted from the biphase coded baseband signal by the RDS demodulator. A clock period of 1.1875 kHz and 50 % duty cycle. The positive edge can be used to sample the RDS_DATA output.
- RDS_DATA: raw RDS bitstream, generated by the demodulator detection of a positive going edge on the RDCL input signal. The data output changes every 100 μs (this equals $\frac{1}{8}$ of the RDS_BCK period) after the falling edge of RDS_BCK. This allows for external receivers of the RDS data to clock the data on the RDS_BCK signal as well as on its inverse.

Buffered raw RDS output mode (rds1_clkin = 1, rds2_clkin = 1, rds1_clkout = 0, rds2_clkout = 0 and DAVD mode: dac0 = 1 and dac1 = 1):

- RDS_CLK: burst clock generated by the microcontroller. Bursts of 17 clock cycles are expected. The average time between bursts is 13.5 ms.
- RDS_DATA: bursts of 16 raw RDS bits are output under control of the burst clock input. After a data burst, this output is HIGH. It is pulled LOW when 16 new bits are made available and a new clock burst is expected. The microcontroller has to monitor this line at least every 13.4 ms.

DAVA, DAVB and DAVC modes (rds1_clkin = 0, rds2_clkin = 0, rds1_clkout = 0 and rds2_clkout = 0):

- DAVN: data available signal for synchronization of data request between main controller and decoder; see Section 6.12.5.11.

rds1_clkin = 1, rds2_clkin = 1, rds1_clkout = 1 and rds2_clkout = 1 is a not allowed mode.

As shown in Fig.27, the same output is used for RDS_DATA and DAVN, depending on the selected mode.

6.12.3 RDS DEMODULATOR

Phase jumps of the extracted RDS clock are detected and accumulated. If the accumulated phase shift exceeds a certain threshold, the RDS/RBDS decoder is informed by the bit slip (BSLP) signal. If the RDS/RBDS decoder

detects a bit slip, the RDS demodulator is informed by the bit slip acknowledge (BSPA) signal. This causes the accumulation of RDS clock phase shifts to be cleared.

6.12.4 RDS BIT BUFFER

The repetition frequency of RDS data is 1187.5 Hz. This results in an interrupt on the microcontroller every 842 µs. The double 16-bit buffer enables this timing requirement to be relaxed.

The two 16-bit buffers are alternately filled. If a buffer is not read out by the time the other buffer is filled, it will be overwritten and the old data will be lost.

When a 16-bit buffer is being filled, the RDS bit buffer keeps the data line HIGH.

If a 16-bit buffer is full, the data line is pulled down. The microcontroller has to monitor the data line at least every 13.5 ms. The data line remains LOW until the microcontroller pulls the clock line LOW. This initiates the reading of the buffer and the first bit is output on the data line. The RDS bit buffer outputs a bit on the data line after every falling clock edge. The data is valid when the clock is HIGH. After 16 falling and 16 rising edges, the whole buffer is read out and the bits are stored by the microcontroller. After a 17th falling clock edge, the data line is set HIGH until the other 16-bit buffer is full. The microcontroller stops communication by pulling the clock line HIGH again.

6.12.5 RDS/RBDS DECODER

The RDS/RBDS decoder handles the complete data processing and decoding of the continuously received serial RDS/RBDS demodulator output data stream (RDDA and RDCL).

Different data processing modes are software controllable by the external main controller via an I^{2}C-bus request. All control signals are direct inputs to the decoder and are also available via the I^{2}C-bus.

Processed RDS/RBDS data blocks with corresponding decoder status information are available via the I^{2}C-bus. The output signals of the decoder are direct outputs and available via the I^{2}C-bus.

The RDS/RBDS decoder contains the following functions:

- RBDS processing mode
- RDS/RBDS block detection
- Error detection and correction
- Synchronization
- Flywheel for synchronization hold
- Bit slip correction
- Data processing control
- Restart of synchronization mode
- Error correction control mode for synchronization
- Data available control modes
- Data output of RDS/RBDS information.

The functions which are realized in the decoder are described in detail in the following Sections.

6.12.5.1 RBDS processing mode

The decoder is suitable for receivers intended for the European (RDS) and the USA (RBDS) standard. If the RBDS mode is selected (RBDS = 1) via the I^{2}C-bus, the block detection and the error detection and correction are adjusted to RBDS data processing; i.e. E blocks are also treated as valid blocks. If RBDS is reset to zero then RDS mode is selected.

6.12.5.2 RDS/RBDS block detection

The RDS/RBDS block detection is always active.

For a received sequence of 26 data bits, a valid block and corresponding offset are identified using syndrome calculation.

During a synchronization search, the syndrome is calculated with every newly received data bit (bit-by-bit) for a received 26-bit sequence. If the decoder is synchronized, syndrome calculation is activated only after 26 data bits for each new block are received.

During RBDS reception, including the RDS block sequences with (A, B, C/C' and D) offset, block sequences of 4 blocks with offset E may also be received. If the decoder detects an 'E-block', this block is marked in the block identification number (BlNr[2:0]) and is available via an I^{2}C-bus request. In RBDS processing mode the block is signalled as valid 'E-block' and in RDS processing mode, where only RDS blocks are expected, it is signalled as invalid 'E-block'.

This information can be used by the main controller to detect 'E-block' sequences and identify RDS or RBDS transmitter stations.

6.12.5.3 Error detection and correction

The RDS/RBDS error detection and correction recognizes and corrects transmission errors within a received block via parity-check in consideration of the offset word of the expected block. Burst errors, with a maximum length of 5 bits, are corrected using this method; see Table 16.

After synchronization has been detected the error correction is always active, depending on the pre-selected 'error correction mode for synchronization' (mode SYNCA to SYNCD), but cannot be carried out in every reception situation.

During a synchronization search, the error correction is disabled for detection of the first block and is enabled for processing of the second block, depending on the pre-selected error correction mode for synchronization.

The processed block of data and the status of error correction are available for data request, via the I^2C-bus, for the last two blocks.

Table 16 RDS processed error correction

EXB1	EXB0	DESCRIPTION
0	0	no errors detected
0	1	burst error of maximum 2 bits corrected
1	0	burst error of maximum 5 bits corrected
1	1	uncorrectable block

Processed blocks are characterized as uncorrectable under the following conditions:

- During a synchronization search; if the burst error (for the second block) is higher than allowed by the pre-selected correction mode SYNCA to SYNCD
- After synchronization has been detected; if the burst error exceeds the correctable maximum 5-bit burst error or if errors are detected but error correction is not possible.

6.12.5.4 Synchronization

The decoder is synchronized if two valid blocks in a valid sequence are detected by the block detector; see Figs 8 and 9 for synchronization strategy overview.

The search for the first block is done by a bit-by-bit syndrome calculation, starting after the first 26 bits have been received. This bit-by-bit syndrome calculation is carried out until the first valid, and error free, block has been received. The next block is then calculated and syndrome calculation is done after the next 26 bits have been received. The block-span in which the second valid and expected block can be received is selectable via the previous setting of the maximum bad blocks gain (RDS2_MBBG[4:0] or RDS1_MBBG[4:0]). If the second received block is an invalid block, then the bad_blocks_counter is incremented and the next new block is calculated. If the bad_blocks_counter value reaches the pre-selected max_bad_blocks_gain, then the bit-by-bit search for the first block is restarted.

If the RDS mode is selected then the next block is always calculated from the sequence A-B-C or C'-D, because E blocks are not allowed.

If the RBDS mode is selected additional E blocks are allowed. However, while the synchronization search is active the block sequence E-E is always invalid (no synchronization will be found with E-E blocks in a row). If the first correctly detected block is block E, then the next expected block is block A; in this case no further expected blocks will be calculated. The decoder waits for an A block until the bad_blocks_counter value reaches the pre-selected max_bad_blocks_gain or a valid A block is received.

If the first correct detected block is block D (in RBDS mode) then the next expected block will be block A. If the next expected block is block A (in RBDS mode) then a valid uncorrected block E is always allowed to be synchronized. If both blocks A and E fail, the next expected block calculated is block B and so on.

For the second block, error correction may also be enabled, depending on the pre-selected correction mode SYNCA to SYNCD. Only valid and/or correctable second blocks are accepted for synchronization.

If the pre-selected max_bad_blocks_gain value is set to zero, then (in this case only) the two-path synchronization search function is active independent of the selected RDS or RBDS mode. That is, if the first block was detected as a valid block, then Path 1 is open and the next expected block is calculated and stored.

With each new received bit (bit-by-bit) syndrome calculation is started again until a second valid block is detected or 26 bits are received.

If a second valid block was detected before 26 bits were received, then Path 2 is open, the block position (bit counter) is stored and the next expected block for Path 2 is calculated.

If 26 bits have been received (after the first block Path 1) and the syndrome calculation gives the valid expected block for Path 1, then synchronization is detected and Path 2 is ignored.

If 26 bits have been received (after the first block Path 1) and the syndrome calculation gives no validity or it is not the expected block for Path 1, then Path 1 is set to Path 2 values (if Path 2 is active):
bit_count_path1 ≤ bit_count_path2 and expected_block_path1 ≤ expected_block_path2. Path 2 is

then cleared and ready for new input, but only after reception of the next few bits (until 26) may synchronization be detected.

Thus using this Path 2 implementation a much faster synchronization is given in cases of wrong block interpretation of the first detected block.

If synchronization is detected, the synchronization status flag (SYNC) is set and available via an I^{2}C-bus request. The synchronization is held until the bad_blocks_counter value reaches the pre-selected max_bad_blocks_lose value (used for synchronization hold) or an external restart of synchronization is performed (NWSY = 1 or Power-on reset).

6.12.5.5 Flywheel for synchronization hold

An internal flywheel is implemented to enable a fast detection of loss of synchronization. Therefore one counter (bad_blocks_counter) checks the number of uncorrectable blocks and a second counter (good_blocks_counter) checks the number of error free or correctable blocks. Error blocks increment the bad_blocks_counter value and valid blocks increment the good_blocks_counter value. If the counter value of the good_blocks_counter reaches the pre-selected max_good_blocks_lose value (MGBL[5:0]) then the good_blocks_counter and bad_blocks_counters are reset to zero. However, if the bad_blocks_counter value reaches the pre-selected max_bad_blocks_lose value (MBBL[5:0]) then a new synchronization search (bit-by-bit) is started (SYNC = 0) and both counters are reset to zero.

The flywheel function is only activated if the decoder is synchronized. The synchronization is held until the bad_blocks_counter value reaches the pre-selected max_bad_blocks_lose value (loss of synchronization) or an external forced start of a new synchronization search (NWSY = 1) is performed. The maximum values for the flywheel counters are both adjustable via the I^{2}C-bus in a range of 0 to 63.

6.12.5.6 Bit slip correction

During poor reception situations phase shifts of one bit to the left or right (±1-bit slip) between the RDS/RBDS clock and data may occur, depending on the lock conditions of the demodulators clock regeneration.

If the decoder is synchronized and detects a bit slip (BSLP = 1), the synchronization is corrected by +1, 0 or −1 bit via block detection on the respectively shifted expected new block.

6.12.5.7 Data processing control

The decoder provides different operating modes selectable by the NWSY, SYM0, SYM1, DAC0 and DAC1 inputs via the external I^{2}C-bus. The data processing control performs the pre-selected operating modes and controls the requested output of the RDS/RBDS information.

6.12.5.8 Restart of synchronization mode

The ‘restart synchronization’ (NWSY) control mode immediately terminates the actual synchronization and restarts a new synchronization search procedure (NWSY = 1). The NWSY flag is automatically reset after the restart of synchronization by the decoder [NeW SYnchronization Restart (NWSYRe pulse)].

This mode is required for a fast new synchronization on the RDS/RBDS data from a new transmitter station if the tuning frequency is changed by the radio set.

Restart of a synchronization search is automatically carried out if the internal flywheel signals a loss of synchronization.

6.12.5.9 Error correction control mode for synchronization

For error correction and identification of valid blocks during a synchronization search and synchronization hold, four different modes can be selected by control mode inputs SYM1 and SYM0:

1. Mode SYNCA (SYM1 = 0 and SYM0 = 0): no error correction; the blocks that are detected as correctable are treated as invalid blocks, the internal bad_blocks_counter value is still incremented even if correctable errors are detected. If synchronized, only error free blocks increment the good_blocks_counter value. All blocks except error free blocks increment the bad_blocks_counter value.
2. Mode SYNCB (SYM1 = 0 and SYM0 = 1): error correction of burst error maximum 2 bits; the blocks that are corrected are treated as valid blocks, all other errors detected are treated as invalid blocks. If synchronized, error free and correctable maximum 2-bit errors increment the good_blocks_counter value.
3. Mode SYNCC (SYM1 = 1 and SYM0 = 0): error correction of burst error maximum 5 bits; the blocks that are corrected are treated as valid blocks, all other errors detected are treated as invalid blocks. If synchronized, error free and correctable maximum 5-bit errors increment the good_blocks_counter value.

4. Mode SYNCD (SYM1 = 1 and SYM0 = 1): no error correction; the blocks that are detected as correctable are treated as invalid blocks, if in synchronization search mode. The internal bad_blocks_counter value is always incremented even if correctable errors are detected. If synchronized, error free blocks and correctable maximum 5-bit errors increment the good_blocks_counter value. Only uncorrectable blocks increment the bad_blocks_counter value.

6.12.5.10 Data available control modes

The decoder provides three different RDS/RBDS data output processing modes plus one decoder bypass mode which are selectable via the 'data available' control mode inputs DAC1 and DAC0.

- Mode DAVA (DAC1 = 0 and DAC0 = 0): standard output mode; if the decoder is synchronized and a new block is received (every 26 bits), the actual RDS/RBDS information of the last two blocks is available with every new received block (approximately every 21.9 ms).
- Mode DAVB (DAC1 = 0 and DAC0 = 1): fast PI search mode; during synchronization search and if a new A or C' block is received, the actual RDS/RBDS information of this or the last two A or C' blocks respectively is available with every new received A or C' block. If the decoder is synchronized, the 'standard output mode' is active.
- Mode DAVC (DAC1 = 1 and DAC0 = 0): reduced data request output mode; if the decoder is synchronized and two new blocks are received (every 52 bits), the actual RDS/RBDS information of the last two blocks is available with every two new received blocks (approximately every 43.8 ms).
- Mode DAVD (DAC1 = 1 and DAC0 = 1): decoder bypassed mode; if this mode is selected then the OutMux output of the decoder is reset to LOW (OutMux = 0). The MADRE internal row buffer output is then active and the decoder is bypassed.

The decoder provides data output of the block identification of the last and previously processed blocks, the RDS/RBDS information words and error detection/correction status of the last two blocks together with general decoder status information.

In addition the decoder output is controlled indirectly by the data request from the external main controller. The decoder receives a 'data overflow' (DOFL) signal controlled by the I^{2}C-bus register interface.

This DOFL signal has to be set HIGH (DOFL = 1) if the decoder is synchronized and a new RDS/RBDS block is received before the previously processed block was completely transmitted via the I^{2}C-bus. After detection of data overflow the interface registers are not updated (no DecWrE) until reset of the data overflow flag (DOFL = 0) by reading via the I^{2}C-bus or if NWSY = 1 which results in the start of a new synchronization search (SYNC = 0).

6.12.5.11 Data output of RDS/RBDS information

The decoded RDS/RBDS block information and the current decoder status is available via the I^{2}C-bus. For synchronization of data request between the main controller and decoder the additional data available output (DAVN) is used. For timing information see Section 10.1.

If the decoder has processed new information for the main controller the data available signal (DAVN) is activated (LOW) under the following conditions:

- During a synchronization search in DAVB mode if a valid A or C' block has been detected. This mode can be used for fast search tuning (detection and comparison of the PI code contained in the A and C' blocks).
- During a synchronization search in any DAV mode (except DAVD mode), if two blocks in the correct sequence have been detected (synchronization criterion fulfilled)
- If the decoder is synchronized and, in mode DAVA and DAVB, a new block has been processed; this mode is the standard data output mode
- If the decoder is synchronized and, in DAVC mode, two new blocks have been processed
- If the decoder is synchronized and, in any DAV mode (except DAVD mode), loss of synchronization is detected (flywheel loss of synchronization, resulting in a restart of the synchronization search)
- In any DAV mode (except DAVD mode), if a reset caused by power-on or a voltage drop is detected (PresN = 0).

Remark: If the decoder is synchronized, the DAVN signal is always activated after 21.9 ms in DAVA or DAVB mode and after 43.8 ms in DAVC mode independent of valid or invalid blocks being received.

The processed RDS/RBDS data is available for an I^{2}C-bus request for at least 20 ms after the DAVN signal was activated. The DAVN signal is always automatically deactivated (HIGH) after ~10 ms or almost after the main controller has read the RDS/RBDS status byte via the I^{2}C-bus (see DAVN timing).

The decoder ignores new processed RDS/RBDS blocks if the DAVN signal is active or if data overflow occurs (DOFL = 1).

Tables 17 and 18 show the block identification number and processed error status outputs of the decoder and how to interpret the output data.

Table 17 RDS block identification number

BLNR2	BLNR1	BLNR0	BLOCK IDENTIFICATION
0	0	0	block A
0	0	1	block B
0	1	0	block C
0	1	1	block D
1	0	0	block C’
1	0	1	block E (RBDS mode)
1	1	0	invalid block E (RDS mode)
1	1	1	invalid block

Table 18 RDS processed error correction

EXB1	EXB0	DESCRIPTION
0	0	no errors detected
0	1	burst error of maximum 2 bits corrected
1	0	burst error of maximum 5 bits corrected
1	1	uncorrectable block

6.12.5.12 Power-on reset

Reset of the chip will cause a number of I^2C-bus registers to be set to specific default values; see Chapter 11.5.

If the decoder detects the reset, the status bit ‘reset detected’ (RSTD) is set and available via an I^2C-bus request. The RSTD flag is deactivated after the decoder status register is read by the I^2C-bus.

7 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); note 1

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	supply voltage on pin V_{DDD}		–0.5	+2.5	+3.3	V
$V_{DD(I/O)}$	supply voltage on pin $V_{DD(I/O)}$		–0.5	+3.3	+4.2	V
$V_{DD(REG)}$	supply voltage on pin $V_{DD(REG)}$		–0.5	+3.3	+4.2	V
V_{DDA}	supply voltage on pin V_{DDA}		–0.5	+2.5	+3.3	V
I_{DDD}	supply current pin V_{DDD}	f_c = 43.2 MHz; V_{DDD} = 2.5 V	–	–	750	mA
I_{SSD}	supply current pin V_{SSD}	f_c = 43.2 MHz; V_{DDD} = 2.5 V	–	–	750	mA
$I_{DD(I/O)}$	supply current pin $V_{DD(I/O)}$	f_c = 43.2 MHz; V_{DDD} = 3.3 V	–	–	750	mA
$I_{SS(I/O)}$	supply current pin $V_{SS(I/O)}$	f_c = 43.2 MHz; V_{DDD} = 3.3 V	–	–	750	mA
I_{IK}	DC input clamp diode current	V_{IL} < –0.5 V or V_{IH} > $V_{DD(I/O)}$ + 0.5 V; note 2	–	–	10	mA
$V_{lim(5V)}$	5 V tolerant pins voltage limits	5 V tolerant outputs: disabled mode	–0.5	–	+5.8	V
T_{amb}	ambient temperature		–40	–	+85	°C
T_{stg}	storage temperature		–55	–	+150	°C
V_{esd}	electrostatic discharge voltage	HBM: 100 pF; 1500 Ω	2000	–	–	V
		MM: 200 pF; 2.5 μH; 15 Ω	200	–	–	V
$I_{lu(prot)}$	latch-up protection current	GQS (SNW-FQ-611 part E)	100	–	–	mA

Notes

1. Stresses greater than those listed above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those listed in the following recommended operating and characteristics section is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
2. Not applicable for 5 V tolerant pins.

8 THERMAL RESISTANCE

SYMBOL	PARAMETER	CONDITION	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	45	K/W

9 DC CHARACTERISTICS

Positive current flows into the device; 3.13 V ≤ $V_{DD(I/O)}$, $V_{DD(REG)}$ ≤ 3.47 V; 2.38 V ≤ V_{DDA}, V_{DDD}, $V_{DD(OSC)}$, $V_{DD(IF)}$ ≤ 2.62 V; T_{amb} = –40 °C to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital parameters						
V_{DDD}	supply voltage on pin V_{DDD}		2.38	2.5	2.62	V
$V_{DD(OSC)}$	supply voltage on pin $V_{DD(OSC)}$		2.38	2.5	2.62	V
$V_{DD(I/O)}$	supply voltage on pin $V_{DD(I/O)}$		3.13	3.3	3.47	V
$V_{DD(REG)}$	supply voltage on pin $V_{DD(REG)}$		3.13	3.3	3.47	V
$I_{DD(tot)}$	total supply current	f_{osc_in} = 43.2 MHz				
		pins V_{DDD}	–	215	260	mA
		pins $V_{DD(I/O)}$	–	5	10	mA
		pins V_{DDA1}, V_{DDA2}, $V_{DD(IF)}$, $V_{DD(OSC)}$	–	180	216	mA
V_{IH}	HIGH-level input voltage	$V_{DD(I/O)}$ = 3.3 V; inputs TTL; excluding 5 V tolerant pins	1.7	–	3.3	V
		$V_{DD(I/O)}$ = 3.3 V; 5 V tolerant inputs TTL; including SDA pin	2.0	–	5.5	V
V_{IL}	LOW-level input voltage	inputs TTL; excluding SDA pin	0	–	0.7	V
		5 V tolerant inputs TTL; including SDA pin	0	–	0.8	V
V_{OH}	HIGH-level output voltage	I_{OH} = –4 mA; $V_{DD(I/O)}$ = 3.3 V				
		10 ns slew rate outputs	2.9	–	–	V
		4 mA outputs	2.9	–	–	V
V_{OL}	LOW-level output voltage	10 ns slew rate outputs; I_{OL} = 4 mA; $V_{DD(I/O)}$ = 3.3 V	–	–	0.4	V
		4 mA outputs; I_{OL} = 4 mA	–	–	0.4	V
		SDA output; I_{OL} = 3 mA; $V_{DD(I/O)}$ = 3.3 V	–	–	0.4	V
I_{LI}	input leakage current	Schmitt trigger input without pull-down; excluding 5 V tolerant pins				
		$V_I = V_{SS(I/O)}$	–	–	–1	µA
		$V_I = V_{DD(I/O)}$	–	–	1	µA
		Schmitt trigger input without pull-down; 5 V tolerant pins only				
		V_I = 5 V	–	–	4.5	µA
		V_I = 0 V	–	–	–4.5	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{OL(Z)}$	3-state leakage current	$V_I = V_{SS(I/O)}$; 3-state outputs without pull-down; excluding 5 V tolerant pins	–	–	–1	µA
		$V_I = V_{DD(I/O)}$; 3-state outputs; excluding 5V tolerant pins	–	–	1	µA
		V_I = 5 V; 3-state outputs and open-drain outputs without pull-down; 5 V tolerant pins only	–	–	64	µA
V_{hys}	Schmitt trigger hysteresis	Schmitt trigger inputs; excluding SDA pin	0.4	–	–	V
		Schmitt trigger inputs; 5 V tolerant pins only	0.3	–	–	V
		pin SDA; $V_{DD(I/O)}$ = 3.3 V	0.15	–	–	V
$I_{DD(q)}$	digital quiescent current	V_{DDD} = 2.62 V; $V_{DD(I/O)}$ = 3.47 V; note 1	–	–	1	mA
$I_{I(pd)}$	input pull-down current	$V_{DD} < V_i < V_{DD(I/O)}$; all pins with pull-down	15	50	100	µA
Analog parameters						
V_{DDA1}	analog supply voltage		2.38	2.5	2.62	V
V_{VREFAD}	common-mode reference voltage	V_{VREFAD} is determined by V_{VADCP} and V_{VADCN} [$V_{VADCP} - V_{VADCN}$]	45	50	55	%
Z_O	output impedance pin VREFAD	$I_O < 2$ mA	–	10	100	Ω
$V_{DD(IF)}$	IF_AD supply voltage		2.38	2.5	2.62	V
V_{VREFIF}	IF_AD reference voltage		–	0.775	1	V
V_{DAC}	DAC supply voltage		2.38	2.5	2.62	V
V_{VDACP}	DAC positive reference voltage	$V_{DDA2} - V_{VDACN}$	–	100	–	%
$Z_{O(DAC)}$	DAC output impedance	pins LRV, RRV, LFV and RFV	0.65	0.9	1.2	kΩ
$I_{ADC(pos)}$	ADC reference current		–	180	–	µA
$V_{DD(OSC)}$	oscillator supply voltage		2.38	2.5	2.62	V
Regulator						
$V_{DD(REG)}$	regulator supply voltage	PMOST BSH207 in application	2.5	2.58	2.66	V
$V_{DD(REG)(ctrl)}$	regulator control range	$V_{DD(REG)}$ = 3.3 V	1	–	3.3	V

Note

1. $I_{DD(q)}$ quiescent device current testing is a proven technique to increase device quality. The testing will be performed in several different logic states, but no guarantee can be given that the current will stay below the specified maximum value in every arbitrary static device state.

10 AC CHARACTERISTICS

Positive current flows into the device; 3.13V ≤ $V_{DD(I/O)}$, $V_{DD(REG)}$ ≤ 3.47 V; 2.38V ≤ V_{DDA}, V_{DDD}, $V_{DD(OSC)}$, $V_{DD(IF)}$ ≤ 2.62 V; T_{amb} = –40 °C to +85 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog inputs						
DIFFERENTIAL MEASUREMENTS VIA AUDIOAD_1 AND AUDIOAD_2; B = 20 kHz						
PSRR	power supply rejection ratio	V_i = 0.1 V (peak); f_i = 1 kHz	35	–	–	dB
α_{ct}	cross-talk between pins AIN(x)	$V_{AIN(x)}$ = 0.5 V (RMS); f_i = 15 kHz; ADIFF(x) path measured	–	–	–70	dB
Pins ADIFF_LP, ADIFF_LN, ADIFF_RP and ADIFF_RN						
$V_{i(dif)(rms)}$	differential input voltage (RMS value)	nominal digital output level –2.5 dB	0.85	1	1.15	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1 kHz; V_i = 1 V (RMS)				
		0 dB input level	–	–	–75	dB
		–60 dB input level	–	–	–25	dB
R_i	input resistance		45	57	72	kΩ
α_{cs}	channel separation	$V_{AIN(x)}$ = 0.5 V (RMS); f_i = 15 kHz; ADIFF(x) path measured	–	–	–70	dB
$V_{o(ub)}$	left and right unbalance	V_i = 1 V (RMS); f_i = 1 kHz	–0.5	–	+0.5	dB
CMRR	common mode rejection ratio	f_i = 1 kHz; V_i = 0.1 V	40	–	–	dB
CMIR	common mode input range	f_i = 1 kHz; V_i = 0.5 V (RMS)	1.0	–	1.5	V
f_{res}	frequency response	f_c at –3 dB	20	–	–	kHz
SINGLE-ENDED MEASUREMENTS VIA AUDIOAD_1 AND AUDIOAD_2; B = 20 kHz						
PSRR	power supply rejection ratio	V_i = 0.1 V (p); f_i = 1 kHz	45	–	–	dB
Pins ADIFF_LP, ADIFF_LN, ADIFF_RP, ADIFF_RN, AIN1_L, AIN1_R, AIN2_L and AIN2_R						
α_{ct}	cross-talk	V_i = 0.5 V (RMS); f_i = 15 kHz; AIN(x) path measured	–	–	–70	dB
α_{cs}	channel separation	V_i = 0.5 V (RMS); f_i = 15 kHz; AIN(x) path measured	–	–	–60	dB
Pins AIN1_L, AIN1_R, AIN2_L and AIN2_R						
$V_{i(rms)}$	input voltage (RMS value)	nominal digital output level –2.5 dB	0.4	0.5	0.6	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1 kHz; V_i = 0.5 V (RMS)				
		0 dB input level	–	–	–75	dB
		–60 dB input level	–	–	–25	dB
R_i	input resistance		45	57	72	kΩ
$V_{o(ub)}$	left and right unbalance	V_i = 0.5 V (RMS); f_i = 1 kHz	–0.5	–	+0.5	dB
CMRR	common mode rejection ratio	f_i = 1 kHz; V_i = 0.1 V	40	–	–	dB
CMIR	common mode input range	f_i = 1 kHz; V_i = 0.5 V (RMS)	1.0	–	1.5	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{res}	frequency response	f_c at −3 dB	20	–	–	kHz
MPX; PINS AIN1_L, AIN2_L ADIFF_LP AND ADIFF_LN; SINGLE-ENDED AND DIFFERENTIAL INPUTS MEASUREMENT VIA AUDIOAD_1 AND AUDIOAD_2 LEFT						
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1 kHz; V_i = 0.5 V (RMS); single-ended; V_i = 1 V (RMS); differential; B = 40 kHz	–	−75	−70	dB
		f_i = 1 kHz; V_i = 0.5 mV (RMS); single-ended; V_i = 1 mV (RMS); differential; B = 40 kHz	–	−15	−10	dB
RDS; PINS AIN1_R, AIN2_R ADIFF_RP AND ADIFF_RN; SINGLE-ENDED AND DIFFERENTIAL INPUTS MEASUREMENT VIA AUDIOAD_1 AND AUDIOAD_2 RIGHT						
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 57 kHz; B = 4 kHz; V_i = 0.5 V (RMS); single-ended; V_i = 1 V (RMS); differential; 0 dB input level; reference level = V_i	–	–	−65	dB
		f_i = 57 kHz; B = 4 kHz; V_i = 0.5 mV (RMS); single-ended; V_i = 1 mV (RMS); differential; −60 dB input level; reference level = V_i	–	–	−5	dB
PINS MONO1_P, MONO1_N, MONO2_P AND MONO2_N; DIFFERENTIAL MEASUREMENTS VIA AUXAD_2						
$V_{i(dif)(rms)}$	differential input voltage (RMS value)	f_i = 1 kHz; nominal digital output level = −5 dB	0.4	0.5	0.6	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1 kHz; B = 4 kHz				
		V_i = 0.5 V (RMS); 0 dB input level	–	–	−45	dB
		V_i = 50 mV (RMS)	–	–	−35	dB
PSRR	power supply rejection ratio	amplitude = 0.1 V (p); f_i = 1 kHz	15	–	–	dB
R_i	input resistance		90	120	150	kΩ
CMRR	common mode rejection ratio	f_i = 1 kHz; V_i = 0.1 V	40	–	–	dB
CMIR	common mode input range	f_i = 1 kHz	1.0	–	1.5	V
f_{res}	frequency response	f_c at −3 dB	32	–	–	kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PINS MONO1_P, MONO1_N, MONO2_P AND MONO2_N; DIFFERENTIAL MEASUREMENTS VIA AUDIOAD_1 AND AUDIOAD_2						
$V_{i(dif)(rms)}$	differential input voltage (RMS value)	f_i = 1 kHz; nominal digital output level −2.5 dB	0.4	0.5	0.6	V
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1 kHz; B = 4 kHz				
		V_i = 0.5 V (RMS); 0 dB input level	–	–	−70	dB
		V_i = 0.5 mV (RMS); −60 dB input level	–	-	−25	dB
PSRR	power supply rejection ratio	V_i = 0.1 V (p-p); f_i = 1 kHz	30	–	–	dB
R_i	input resistance		90	120	150	kΩ
CMRR	common mode rejection ratio	f_i = 1 kHz; V_i = 0.10 V	40	–	–	dB
CMIR	common mode input range	f_i = 1 kHz	1.0	–	1.5	V
f_{res}	frequency response	f_c at −3 dB	20	–	–	kHz
Analog inputs; pins IFSS1 and IFSS2 single-ended measurements via AUXAD_1 and AUXAD_2; B = 32 kHz						
V_i	input voltage	$V_{VADCP} - V_{VADCN}$ = 2.5 V	2.35	2.5	2.65	V
V_{offset}	offset voltage		−150	+20	+150	mV
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1 kHz				
		V_i = 90 % × V_R (p-p)	–	–	−45	dB
		V_i = 9 % × V_R (p-p)	–	−34	−28	dB
R_i	input resistance	f_s = 5.4 MHz	500	–	–	kΩ
f_{res}	frequency response	f_c at −3 dB	32	–	–	kHz
PINS IF_IN1, IF_IN2, IF_AD1 AND IF_AD2						
$V_{i(FS)(p-p)}$	full-scale input voltage (peak-to-peak value)	nominal digital output level 0 dB				
		f_i = 451 kHz	0.82	0.96	1.09	V
		f_i = 10.701 MHz; includes influence of $f_{c(LPF)}$	0.815	1.04	1.16	V
V_{offset}	offset voltage	ADC + buffer + dither	−100	–	+100	mV
R_i	input resistance		16	20	24	kΩ
HD_{AM}	AM harmonic distortion	−34 dB (FS); measurement with respect to 0 dB (FS)				
		f_i = 225.500 kHz	–	–	−52	dB
		f_i = 150.333 kHz	–	–	−52	dB
ID_{AM}	AM intermodulation distortion	f_1 = 430 kHz; −12 dB (FS); f_2 = 411 kHz; −22 dB (FS); measurement with respect to 0 dB (FS)	–	–	−82	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
HD_{FM}	FM harmonic distortion	measurement with respect to 0 dB (FS)				
		f_i = 10.7802 MHz; −6 dB (FS)	–	–	−40	dB
		f_i = 5.3505 MHz; −10 dB (FS)	–	–	−44	dB
		f_i = 3.567 MHz; −10 dB (FS)	–	–	−44	dB
		f_i = 10.833 MHz; −9 dB (FS)	–	–	−66	dB
ID_{FM}	FM intermodulation distortion	−12 dB (FS); measurement with respect to 0 dB (FS); f_1 = 10.833 MHz; f_2 = 10.967 MHz	–	–	−67	dB
S/N_{AM}	AM signal-to-noise ratio narrow-band	f_1 = 451 kHz; f_2 = 534.809 kHz; V_i = 85.3 mV (RMS); B = 6 kHz; measurement with respect to 0 dB (FS); DITGAIN = 8	83	88	–	dB
S/N_{FM}	FM signal-to-noise ratio narrow-band	f_1 = 10.701 MHz; f_2 = 10.89255 MHz; V_i = 171 mV (RMS); B = 180 kHz; measurement with respect to 0 dB (FS); DITGAIN = 8	65	72	–	dB
PSRR	power supply rejection ratio	V_i = 0.1 V (p); f_i = 1 kHz	3	6	–	dB
$\alpha_{ct(FM)}$	FM cross-talk	f_i = 10.701 MHz; amplitude = −12 dB (FS); measurement with respect to 0 dB (FS)	–	–	−39	dB
$\alpha_{ct(AM)}$	AM cross-talk	f_i = 451 kHz; amplitude = −12 dB (FS); measurement with respect to 0 dB (FS)	–	–	−47	dB
$R_{i(IF\_VG)}$	input resistance pin IF_VG		–	400	–	Ω
Analog IF_AD dither DAC						
$V_{dither(p-p)}$	dither level (peak-to-peak)	DITGAIN = 15	56	70	84	mV
Analog IF_AD dither gain DAC						
G_{step}	number of gain steps		–	16	–	
G_{res}	gain resolution		3.5	4.4	5.3	$\frac{mV}{steps}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DAC measurements; 0 dB via I^2S-bus; minimum AC impedance on DAC outputs = 100 kΩ; filter capacitance on DAC outputs = 3.3 nF; B = 20 Hz to 20 kHz, Mixer muted						
PSRR	power supply rejection ratio pin V_{DDA2}	f_{ripple} = 1 kHz; V_{ripple} = 0.1 V (p-p); C_{VDACP} = 22 μF	3	6	–	dB
ΔV_{DAC}	deviation in output level of the front DAC voltage outputs with respect to the average of the front outputs	amplitude = 0 dB (FS); f_i = 1 kHz				
		pins RRV and LRV	–0.38	–	+0.38	dB
		pins RFV and LFV	–0.38	–	+0.38	dB
PINS RRV, LRV, RFV AND LFV						
$m_{(f\text{-}r)}$	matching of the front to rear averages	amplitude = 0 dB (FS); f_i = 1 kHz	–0.5	–	+0.5	dB
α_{ct}	crosstalk between the four DAC output voltages	amplitude = 0 dB; f_i = 1 kHz; one output digital silence; three others 0 dB (FS); for all combinations	–	–70	–60	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_i = 1 kHz; all four DAC outputs driven				
		0 dB (FS); all mixers muted	–	–80	–75	dB
		–60 dB (FS)	–	–45	–40	dB
		0 dB (FS); all mixers on and set to 0 dB	–	–	–60	dB
DS	digital silence	all zero digital input with respect to 0 dB (FS)	–	–110	–105	dB
$V_{o(DAC)(rms)}$	DAC output voltage at maximum signal (RMS value)	AC impedance ≥ 100 kΩ; f_i = 1 kHz; V_{DDA2} = 2.5 V	0.74	0.75	0.77	V
Analog MIX output; pins RRV, LRV, RFV AND LFV						
THD	total harmonic distortion summer input	f_i = 1 kHz; gain setting = 0 dB				
		V_i = 0.50 V (RMS)	–	–	–40	dB
		V_i = 0.5 mV (RMS)	–	–	–20	dB
SPDIF measurements; pins SPDIF1 and SPDIF2						
$V_{i(p\text{-}p)}$	input voltage level (peak-to-peak value)		0.2	0.5	2.5	V
R_i	input resistance		–	7	–	kΩ
$V_{i(hys)}$	input hysteresis		–	30	–	mV
Quartz crystal oscillator measurements; pins OSC_IN and OSC_OUT; $V_{DD(OSC)}$ = 2.5 V; f_i = 4 MHz						
$Z_{o(xtal)}$	crystal oscillator output impedance	V_i = 20 mV (RMS)	400	–	–	Ω
G_{xtal}	oscillator gain	V_i = 20 mV (RMS)	12	–	–	mA/V
ΔI_{xtal}	oscillator level dependent current difference	V_i = 20 mV and 200 mV (RMS)	2	–	–	mA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital output rise and fall times; T_{amb} = 25 °C; C_L = 30 pF						
$t_{o(r)}$	output rise time LOW-to-HIGH transition	10 ns slew rate outputs	–	10	–	ns
		4 mA outputs	–	5	–	ns
$t_{o(f)}$	output fall time HIGH-to-LOW transition	10 ns slew rate outputs	–	10	–	ns
		4 mA outputs	–	5	–	ns
$t_{o(f)(SDA)}$	output fall time HIGH-to-LOW transition pin SDA	C_b = 10 pF to 400 pF	20 + 0.1C_b		250	ns
I^2S-bus inputs and outputs (see Fig.29)						
$T_{cy(BCK)}$	I^2S-bus bit clock cycle time	f_s = 48 kHz; pins EXT_IIS_BCK1 and EXT_IIS_BCK2	81.3	–	–	ns
$t_{s;DAT}$	data set-up time	pins EXT_IIS_IO1 and EXT_IIS_IO2	10	–	–	ns
		pins IIS_IN1, IIS_IN2, IIS_IN3, IFP_IIS_IN1, IFP_IIS_I2O6 and IFP_IIS_I3O4	22.9	–	–	ns
$t_{h;DAT}$	data hold time	pins EXT_IIS_IO1 and EXT_IIS_IO2	5	–	–	ns
		pins IIS_IN1, IIS_IN2, IIS_IN3, IFP_IIS_IN1, IFP_IIS_I2O6 and IFP_IIS_I3O4	0	–	–	ns
$t_{d;DAT}$	data delay time	pins IIS_OUT1, IIS_OUT2, IIS_OUT3, EXT_IIS_WS1, EXT_IIS_BCK1, EXT_IIS_IO1, EXT_IIS_WS2, EXT_IIS_BCK2 and EXT_IIS_IO2	–	–	27	ns
$t_{s;WS}$	word select set-up time	pins EXT_IIS_WS1 and EXT_IIS_WS2	10	–	–	ns
$t_{h;WS}$	word select hold time	pins EXT_IIS_WS1 and EXT_IIS_WS2	2	–	–	ns
$t_{d;WS}$	word select delay time	pins IIS_WS1 and IFP_IIS_WS	–	–	27	ns
RDS inputs and outputs; pins RDS_DATA and RDS_BCK; see Figs 30**,** 31**,** 32 and 33						
T_{TDAV}	data valid period	DAVA and DAVB mode	24.5	26.0	27.0	RDS bit periods
		DAVC mode	49.0	52.0	54.0	RDS bit periods
t_{DAVNL}	time data available signal is LOW	DAVA, DAVB and DAVC mode	11.25	12.0	12.5	RDS bit periods
t_{sr}	clock set-up time		100	–	–	µs

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{pr}	period time		–	842	–	µs
t_{hr}	clock HIGH time		220	–	640	µs
t_{lr}	clock LOW time		220	–	640	µs
t_{dr}	data hold time		100	–	–	µs
t_{wb}	wait time (burst mode)		1	–	–	µs
T_{pb}	period time (burst mode)		2	–	–	µs
t_{hb}	clock HIGH time (burst mode)		1	–	–	µs
t_{lb}	clock LOW time (burst mode)		1	–	–	µs
I^2C-bus inputs and outputs; pins SCL and SDA; value referenced to V_{IH} minimum and V_{IL} maximum levels; see Fig.28						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{BUF}	bus free time between a STOP and START condition		1.3	–	–	µs
$t_{HD;STA}$	hold time (repeated) START condition		0.6	–	–	µs
t_{LOW}	LOW period of the SCL clock		1.3	–	–	µs
t_{HIGH}	HIGH period of the SCL clock		0.6	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.6	–	–	µs
$t_{HD;DAT}$	data hold time		0	–	0.9	µs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
t_r	rise time of both SDA and SCL signals	C_b = total capacitance of one bus line in pF				
		f_{SCL} = 400 kHz	$20 + 0.1C_b$	–	300	ns
		f_{SCL} = 100 kHz	$20 + 0.1C_b$	–	1000	ns
t_f	fall time of both SDA and SCL signals	C_b = total capacitance of one bus line in pF	$20 + 0.1C_b$	–	300	ns
$t_{SU;STO}$	set-up time for STOP condition		0.6	–	–	µs
C_b	capacitive load for each bus line		–	–	400	pF
t_{SP}	pulse width of spikes which must be suppressed by the input filter		0	–	50	ns

10.1 Timing diagrams

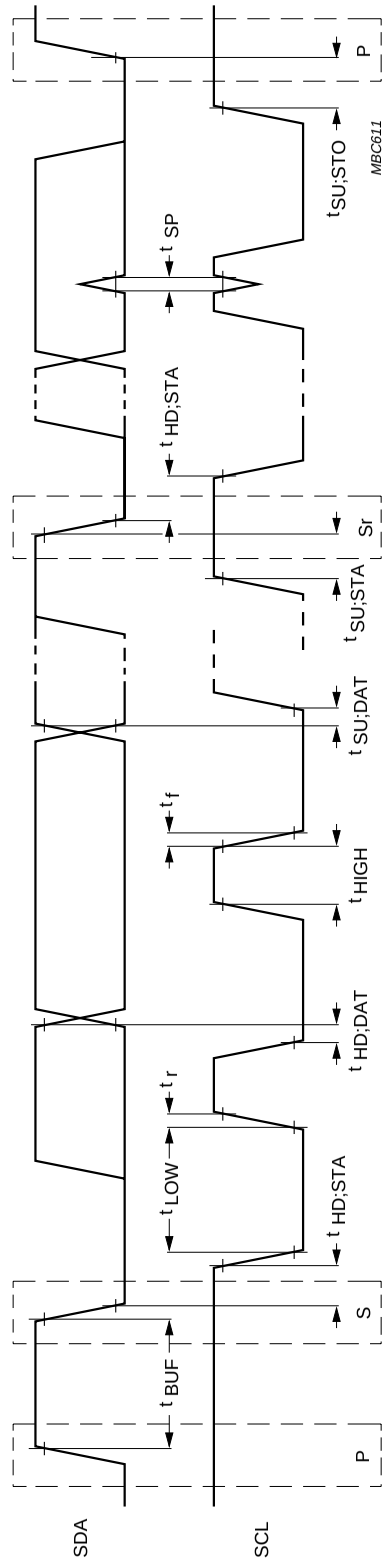


Fig.28 Definition of timing on the I²C-bus.

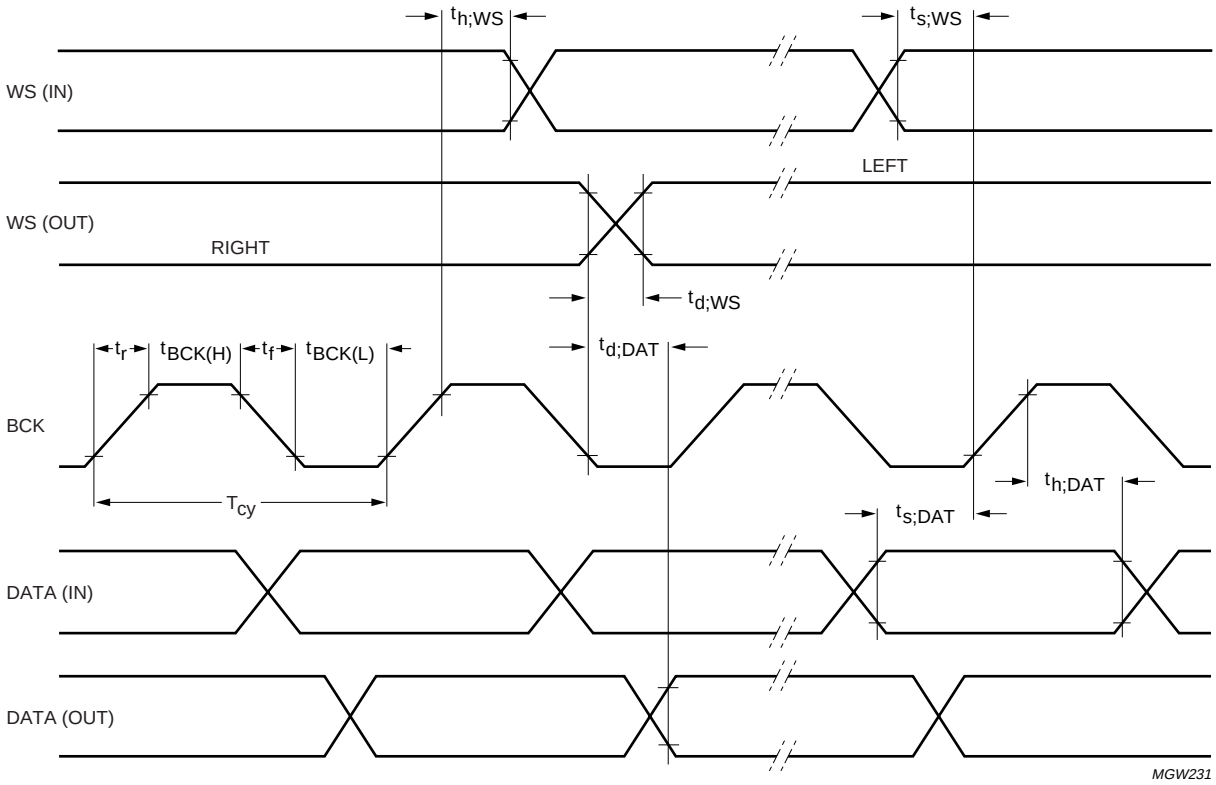


Fig.29 I^2S-bus timing diagram for digital audio inputs/outputs.

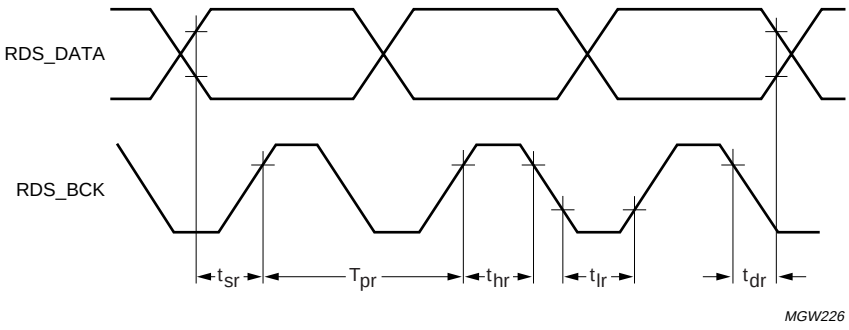


Fig.30 RDS timing diagram in direct output mode.

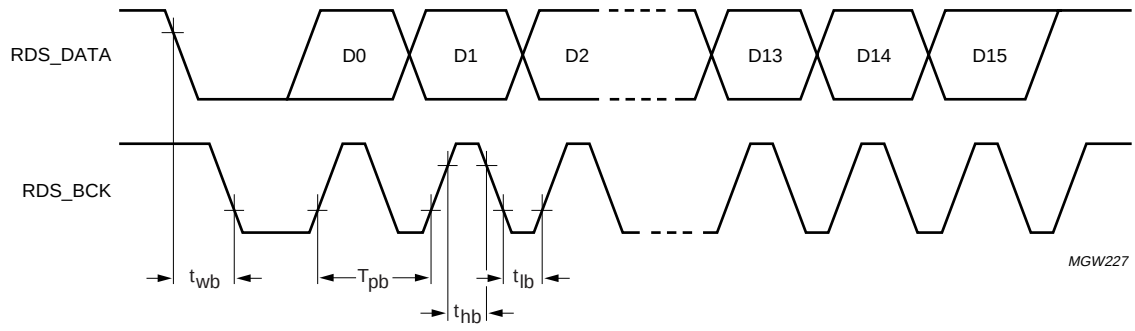


Fig.31 Timing diagram of interface signals between RDS function and microcontroller in buffered output mode.

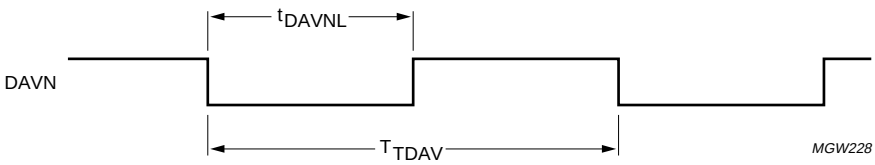


Fig.32 RDS data available signal (DAVN); no I^2C-bus request during DAVN LOW time (decoder is synchronized).

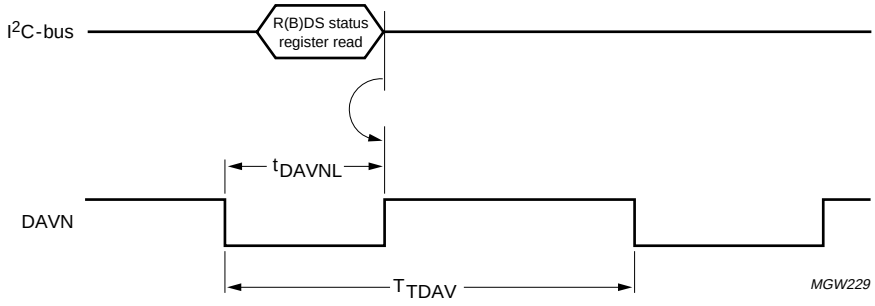


Fig.33 RDS data available signal (DAVN); DAVN LOW timing shorten by data request via I²C-bus (decoder is synchronized).

11 I²C-BUS CONTROL

General description of the I²C-bus format in a booklet can be obtained at Philips Semiconductors, International Marketing and Sales.

For the external control of the chip a fast I²C-bus is implemented. This is a 400 kHz bus which is downward compatible with the standard 100 kHz bus. There are two different types of control instructions:

- Instructions to control the DSP programs, programming the coefficient RAM and reading the values of parameters
- Instructions controlling the DATA I²S-bus flow, like source selection and clock speed.

11.1 I²C-bus protocol

The bidirectional I²C-bus interface acts as a slave transceiver while an external microcontroller acts as a master transceiver. Communication between the MPI and the microcontroller is based on the I²C-bus protocol. The data transfer on the I²C-bus is shown in Fig.34.

The I²C-bus has two lines: a Serial Clock line SCL and a Serial Data line SDA. Because the I²C-bus is a multi-master bus, arbitration between different master devices is achieved by using a START condition. The master device pulls the open-drain data line LOW while the clock line remains HIGH. After the bus has been ‘won’ in this way, data is transmitted serially in packets of 8 bits plus an extra clock pulse for an acknowledgement flag from the receiving device.

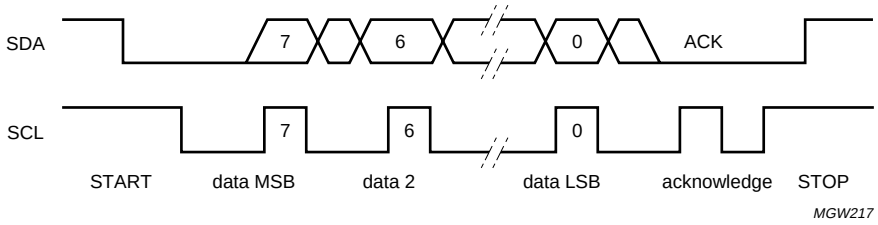


Fig.34 I²C-bus interface data transfer sequence.

11.1.1 PROTOCOL OF THE I²C-BUS COMMANDS

The SAA7724H acts as a slave receiver or slave transmitter; therefore the clock signal is only an input signal. The data signal is a bidirectional open-drain line at the IC pin level. The SAA7724H slave address has a subaddress bit A0 (bit 1) which allows the device to have 1 or 2 different addresses. The least significant bit (bit 0) represents the read/write mode.

The read and write I²C-bus commands are illustrated in Figs 35 to 40, showing SDA. The I²C-bus interface will generate a negative acknowledge on the SDA line in the event that the data transfer was not completed successfully.

After generating a START condition, the master device has to transmit a slave address. The slave I²C-bus interface responds to its own address (given in the first data byte) by sending an acknowledgement to the master device. The direction flag (bit 0) is always transmitted in this first byte so that the slave knows in which mode it has to operate. Initially, the I²C-bus interface receives a 16-bit address (2 bytes over the I²C-bus) which represents the starting memory address for the data transfer.

In the event that a read command is received before the address register has been written, a negative acknowledgement will be generated.

In the write mode, the transfer of data words continues until the master device stops the transfer with a STOP condition (P). In the read mode, the data transfer continues until a negative acknowledgement and STOP condition is generated by the master. In the read mode the last word will not be transmitted to the I²C-bus while the I²C-bus interface is stopped by the master.

When reading from or writing to an invalid address a negative acknowledge will be generated after the first data byte, and the master must then send a STOP condition. An acknowledge is generated on all memory locations if selected. Also, within a given boundary, an acknowledge will be generated when selected, although the physical size of the memory may not be that large. These are the reserved locations in the I²C-bus memory map. A negative acknowledge will only be generated in unused spaces of the I²C-bus map.

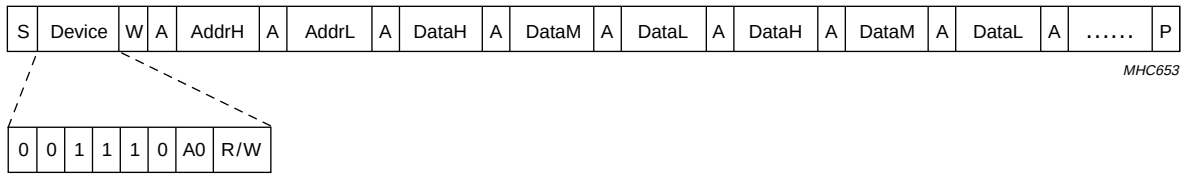


Fig.35 Write cycle EPICS (XRAM).

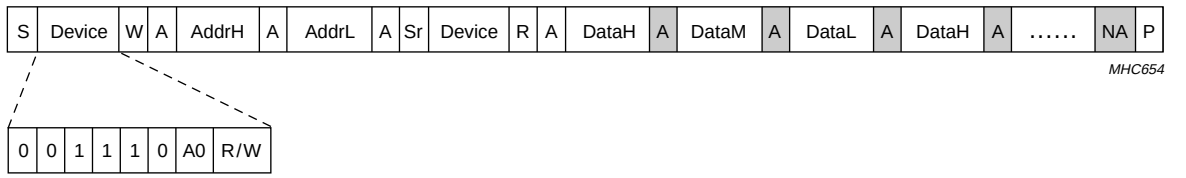


Fig.36 Read cycle EPICS (XRAM).

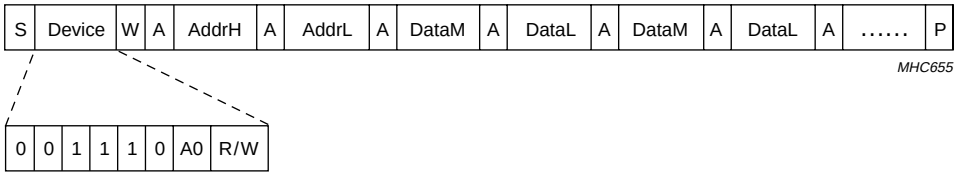


Fig.37 Write cycle EPICS (YRAM).

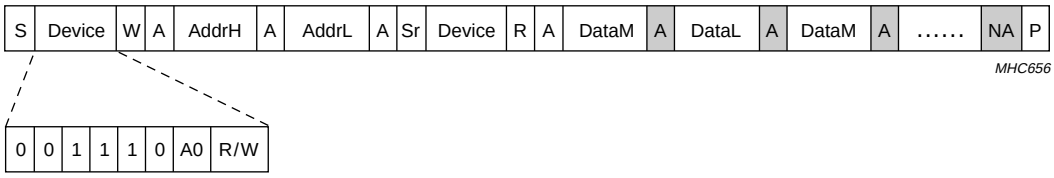


Fig.38 Read cycle EPICS (YRAM).

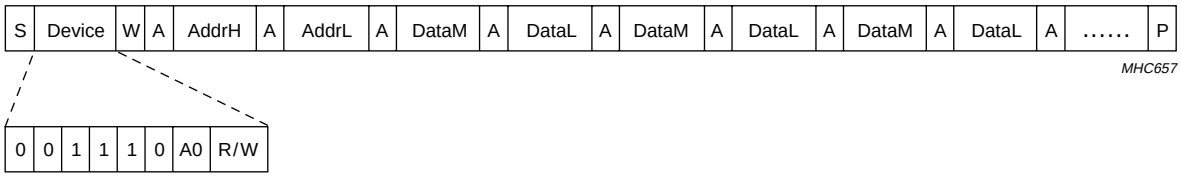


Fig.39 Write cycle IFP.

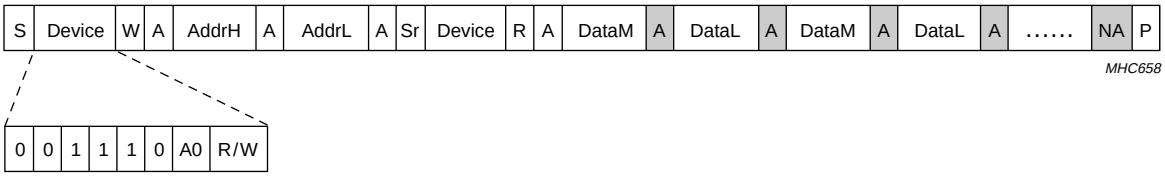


Fig.40 Read cycle IFP.

Table 19 I^2C-bus symbol description

SYMBOL	DESCRIPTION
S	START condition
Sr	repeated START condition
P	STOP condition
R	read bit (1)
W	write bit (0)
A	acknowledge from slave (SAA7724H)
A	acknowledge from master (microcontroller)
NA	negative acknowledge from master to stop the data transfer
Device	device address
AddrH and AddrL	address memory map
DataH, DataM and DataL	data of XRAM (3 bytes)
DataM and DataL	data of YRAM or IFP (2 bytes)

11.2 MPI data transfer formats

Table 20 Data transfer formats; note 1

TRANSFER	FROM		TO	
Y transfer MPI → YRAM	I^2C-bus:	XXXXM----------L	YRAM:	M----------L
Y transfer YRAM → I^2C-bus	YRAM:	M----------L	I^2C-bus:	XXXXM----------L
X transfer I^2C-bus → XRAM	I^2C-bus:	M----------L	XRAM:	M----------L
X transfer XRAM → I^2C-bus	XRAM:	M----------L	I^2C-bus:	M----------L
transfer I^2C-bus → IFP	I^2C-bus:	M----------L	IFP:	M----------L
transfer IFP → I^2C-bus	IFP_DATA_R:	M----------L	I^2C-bus:	M----------L

Note

1. M = MSB, L = LSB and X = don't care.

11.3 Reset initialization

With a synchronous reset the SAA7724H will turn to their idle position (state 0), the address counter is set to zero and the SDA_OUT line remains high-impedance. For the SDA line an asynchronous reset is also implemented which is connected directly to the $\overline{\text{RESET}}$ pin. During the asynchronous reset period the internal SDA_OUT line remains HIGH which results in a high-impedance SDA line. These two resets should have an overlap to have a proper initialization. It is also possible to reset the internal I²C-bus registers separately, and these registers will be set to their default values.

11.4 Defined I²C-bus address

The I²C-bus address is defined for location: 001110P; the least significant bit is a programmable bit with the external pin A0_pin. Two possible options are available with this pin:

- If A0 = 0 the following addresses are available:
  - Write: 00111000 = 38h
  - Read: 00111001 = 39h.
- If A0 = 1 the following addresses are available:
  - Write: 00111010 = 3Ah
  - Read: 00111011 = 3Bh.

11.5 I²C-bus memory map specification

The I²C-bus memory map contains all defined I²C-bus bits related to RDS, SRC and EPICS control and allocates EPICS, SRC and IFP RAM sizes.

The memory spaces belonging to the AUDIO_EPICS are referred to as EPICS registers, and memory spaces belonging to the SRC/RDS EPICS are referred to as SRC registers.

The RDS registers control the RDS1 and RDS2 blocks simultaneously while providing each RDS1 and RDS2 block with its own decoded data and status registers: the memory map is given in Table 21. Detailed memory map locations of the hardware registers related to the I²C-bus EPICS control are given in Table 23 and the I²C-bus RDS control are given in Table 24.

Table 21 I²C-bus memory map; notes 1 and 2

BLOCK	START (HEX)	END (HEX)	NAME	NUMBER OF WORDS × BIT WIDTH (DEBUG PART)	ACCESS
–	E000	FFFF	not used	–	–
SRC	B880	DFFF	reserved	–	–
SRC	B800	B87F	SRC_YRAM	128 × 12	R/W
SRC	B000	B7FF	reserved	–	–
SRC	AFFF	AFFF	IIC_SRC_PC	1 × 24	R/W
SRC	AFFE	AFFE	IIC_SRC_STAT	1 × 24	R/W
SRC	A300	AFFD	reserved	–	–
SRC	A000	A2FF	SRC_XRAM	768 × 24	R/W
–	9000	9FFF	reserved	–	–
–	6030	8FFF	not used	–	–
Global	602F	602F	IIC_DSP_CTR	1 × 24	R/W
–	6010	602E	not used	–	–
RDS	6000	600F	RDS 1 and 2 registers	12 × 16	see Table 24
EPICS	5FFF	5FFF	IIC_SILICON_ID	1 × 32	read
EPICS	4000	5FFE	reserved	–	–
–	3000	3FFF	not used	–	–
IFP	2C64	2FFF	IFP registers	all 16-bit width	R/W

BLOCK	START (HEX)	END (HEX)	NAME	NUMBER OF WORDS × BIT WIDTH (DEBUG PART)	ACCESS
–	1400	2C63	reserved	–	–
IFP	2C00	2C63	FP_RAM	100 × 16	R/W
IFP	2700	2BFF	reserved	–	–
IFP	2600	26FF	VY3_RAM	256 × 16	R/W
IFP	2500	25FF	VX3_RAM	256 × 16	R/W
IFP	2400	24FF	VY2_RAM	256 × 16	R/W
IFP	2300	23FF	VX2_RAM	256 × 16	R/W
IFP	2200	22FF	VY1_RAM	256 × 16	R/W
IFP	2100	21FF	VX1_RAM	256 × 16	R/W
IFP	2081	20FF	reserved	–	–
IFP	2080	2080	IIC_SWB_ERR_STAT	1 × 16	R/W
IFP	2000	207F	SWB_RAM	128 × 16	R/W
EPICS	1400	1FFF	reserved	–	–
EPICS	1000	13FF	EPICS_YRAM	1024 × 12	R/W
EPICS	0FFF	0FFF	IIC_EPICS_PC	1 × 24	R/W
EPICS	0FFE	0FFE	IIC_EPICS_STAT	1 × 24	R/W
EPICS	0FF0	0FFD	EPICS registers	14 × 24	R/W
EPICS	0E00	0FEF	reserved	–	–
EPICS	0000	0DFF	EPICS_XRAM	3584 × 24	R/W

Notes

1. At all ‘reserved’ spaces an acknowledge (ACK) will be generated.
2. At all ‘not used’ spaces a negative acknowledge (NACK) will be generated.

Table 22 I^2C-bus memory map SRC_EPICS hardware register overview

LOCATION (HEX)	REGISTER NAME	# USED BITS	READ/WRITE
AFFF	IIC_SRC_PC	24	R/W
AFFE	IIC_SRC_STAT	24	R/W

Table 23 I^2C-bus memory map AUDIO_EPICS hardware register overview

LOCATION (HEX)	REGISTER NAME	# USED BITS	READ/WRITE
0FFF	IIC_EPICS_PC	24	R/W
0FFE	IIC_EPICS_STAT	24	R/W
0FFD	IIC_DSPIO_CONF	9	R/W
0FFC	IIC_SEL	20	R/W
0FFB	IIC_IFAD_SEL	10	R/W
0FFA	IIC_HOST	12	R/W

LOCATION (HEX)	REGISTER NAME	# USED BITS	READ/WRITE
0FF9	IIC_SPDIF_STAT	13	read
0FF8	IIC_SUM	13	R/W
0FF7	IIC_EPICS_START_ADDR	16	R/W

Table 24 I²C-bus memory map RDS hardware register overview

LOCATION (HEX)	REGISTER NAME	# USED BITS	READ/WRITE
600F and 600E	not used	–	–
600D	IIC_RDS2_CTR	11	write
600C	IIC_RDS2_SET	15	write
600B	IIC_RDS2_CNT	16	read
600A	IIC_RDS2_PDAT	16	read
6009	IIC_RDS2_LDAT	16	read
6008	IIC_RDS2_STAT	8	read
6007 and 6006	not used	–	–
6005	IIC_RDS1_CTR	11	write
6004	IIC_RDS1_SET	15	write
6003	IIC_RDS1_CNT	16	read
6002	IIC_RDS1_PDAT	16	read
6001	IIC_RDS1_LDAT	16	read
6000	IIC_RDS1_STAT	8	read

Table 25 I²C_EPICS_STAT status register (0FFEh)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 13	–	0h	internal flags
12 and 11	F12 and F11	–	not used
10	F10	0	SPDIF2 lock status 0: not locked 1: locked
9	F9	0	SPDIF1 lock status 0: not locked 1: locked
8	F8	0	DSPIO8 status 0: input 1: output
7	F7	0	DSPIO7 status 0: input 1: output
6	F6	0	DSPIO6 status 0: input 1: output

BIT	SYMBOL	DEFAULT	DESCRIPTION
5	F5	0	DSPIO5 status 0: input 1: output
4	F4	0	DSPIO4 status 0: input 1: output
3	F3	0	DSPIO3 status 0: input 1: output
2	F2	0	DSPIO2 status 0: input 1: output
1	F1	0	DSPIO1 status 0: input 1: output
0	F0	0	DSPIO0 status 0: input 1: output

Table 26 IIC_DSPIO_CONF configuration register (0FFDh)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 9	–	–	not used
8	config_DSPIO8	0	port configuration for DSPIO8 0: input 1: output
7	config_DSPIO7	0	port configuration for DSPIO7 0: input 1: output
6	config_DSPIO6	0	port configuration for DSPIO6 0: input 1: output
5	config_DSPIO5	0	port configuration for DSPIO5 0: input 1: output
4	config_DSPIO4	0	port configuration for DSPIO4 0: input 1: output
3	config_DSPIO3	0	port configuration for DSPIO3 0: input 1: output

BIT	SYMBOL	DEFAULT	DESCRIPTION
2	config_DSPIO2	0	port configuration for DSPIO2 0: input 1: output
1	config_DSPIO1	0	port configuration for DSPIO1 0: input 1: output
0	config_DSPIO0	0	port configuration for DSPIO0 0: input 1: output

Table 27 IIC_SEL selection register (0FFCh)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 20	–	–	not used
19	ch2_dc_offset	1	DC offset filter for audio channel 2 0: disable 1: enable
18	ch1_dc_offset	1	DC offset filter for audio channel 1 0: disable 1: enable
17	aux2_sel_lev_voice	0	select behavioural of the compensation filter for AUX channel 2 0: level inputs 1: voice inputs
16	aux1_sel_lev_voice	0	select behavioural of the compensation filter for AUX channel 1 0: level inputs 1: voice inputs
15	ch2_wide_narrow	0	select bandwidth for audio channel 2 0: audio + RDS information 1: only audio data
14	ch1_wide_narrow	0	select bandwidth for audio channel 1 0: audio + RDS information 1: only audio data
13	sel_SPDIF2_IIS2	0	select input for SRC2 0: SPDIF 2 1: EXT_IIS2
12	sel_SPDIF1_IIS1	0	select input for SRC1 0: SPDIF 1 1: EXT_IIS1
11 and 10	aic3[1:0]	11	analog input control 3; see Table 6
9	s2	1	AD normal/differential selection 2; see Table 4
8	intref2	0	AD internal reference 2; see Table 4
7 and 6	aic2[1:0]	01	analog input control 2; see Table 5

BIT	SYMBOL	DEFAULT	DESCRIPTION
5	refc2	1	AD reference control 2; see Table 4
4	s1	0	AD normal/differential selection 1; see Table 4
3	intref1	0	AD internal reference 1; see Table 4
2 and 1	aic1[1:0]	00	analog input control 1; see Table 5
0	refc1	0	AD reference control 1; see Table 4

Table 28 IIC_IFAD_SEL selection register (0FFBh)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 10	–	–	not used
9	ifad2_power	1	controls activity of IFAD2 0: power low 1: power on
8	ifad1_power	1	controls activity of IFAD1 0: power low 1: power on
7 to 4	dith_gain_2[3:0]	0000	control gain of IF-AD dither source 2
3 to 0	dith_gain_1[3:0]	0000	control gain of IF-AD dither source 1

Table 29 IIC_HOST register (0FFAh)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 20	–	–	not used
19	src2_ext_sel_out	0	selects the external output port for SRC2 0: EXT_IIS1 1: EXT_IIS2
18	src1_ext_sel_out	1	selects the external output port for SRC1 0: EXT_IIS1 1: EXT_IIS2
17	src2_int_ext_out	0	selects the output destination for SRC2 0: internal (audio epics) 1: external (Ext_iis)
16	src1_int_ext_out	0	selects the output destination for SRC1 0: internal (audio epics) 1: external (Ext_iis)
15	src2_int_ext_in	1	selects the input source for SRC2 0: internal (audio epics) 1: external (Ext_iis/Spdif)
14	src1_int_ext_in	1	selects the input source for SRC1 0: internal (audio epics) 1: external (Ext_iis/Spdif)

BIT	SYMBOL	DEFAULT	DESCRIPTION
13	en_ifp_iis_bck	0	enable ifp_iis_bck 0: disable 1: enable
12	iboc_mode	0	selects outputs of IF decimation paths to come out at IFP_IIS ports 0: disable 1: enable
11 to 9	ext_host_io_ format2[2:0]	000	input data format for EXT_IIS2 port; see Table 10
8 to 6	ext_host_io_ format1[2:0]	000	input data format for EXT_IIS1 port; see Table 10
5	en_host_io	0	port output enable for IIS_OUT port 0: disable. IIS_OUT1, IIS_OUT2 and IIS_OUT3 set to zero; IIS_WS and IIS_BCK 3-stated 1: all pins enabled
4 to 2	host_io_format[2:0]	000	host input/output data format for I^2S-bus port; see Table 12
1	–	–	not used
0	en_256FS	0	$256 \times f_s$ clock output 0: disable 1: enable

Table 30 IIC_SPDIF_STAT status register (0FF9h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 17	–	–	not used
16	IFP_Status	–	IFP_Status 0: disabled 1: enabled
15 and 14	–	–	not used
13 and 12	SPDIF2_ accuracy[1:0]	–	accuracy of sampling frequency of SPDIF2 channel 00: level II 10: level III 01: level I 11: reserved
11 and 10	SPDIF2_fs[1:0]	-	audio sampling frequency of SPDIF2 channel 00: 44.1 kHz 10: 48 kHz 01: reserved 11: 32 kHz
9	SPDIF2_emphasis	–	equalization of SPDIF2 channel 0: no pre-emphasis present 1: 50/15 μs pre-emphasis present

BIT	SYMBOL	DEFAULT	DESCRIPTION
8	SPDIF2_content	–	contents of SPDIF2 channel 0: normal audio mode 1: data mode
7 and 6	–	–	not used
5 and 4	SPDIF1_ accuracy[1:0]	–	accuracy of sampling frequency of SPDIF1 channel 00: level II 10: level III 01: level I 11: reserved
3 and 2	SPDIF1_fs[1:0]	–	audio sampling frequency of SPDIF1 channel 00: 44.1 kHz 10: 48 kHz 01: reserved 11: 32 kHz
1	SPDIF1_emphasis	–	equalization of SPDIF1 channel 0: no pre-emphasis present 1: 50/15 µs pre-emphasis present
0	SPDIF1_content	–	contents of SPDIF1 channel 0: normal audio mode 1: data mode

Table 31 IIC_SUM summer register (0FF8h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 13	–	–	not used
12	rrm	0	DAC summer RR enable; see Table 9
11	rlm	0	DAC summer RL enable; see Table 9
10	frm	0	DAC summer FR enable; see Table 9
9	flm	0	DAC summer FL enable; see Table 9
8	mixc	0	DAC summer input selection 0: MONO1 1: MONO2
7	ifin2_inpsel	0	select IFAD for IFIN2 input from IFP 0: for IF_AD2 1: for IF_AD1
6	ifin1_inpsel	0	select IFAD for IFIN1 input from IFP 0: for IF_AD1 1: for IF_AD2
5 to 0	volmix[5:0]	000000	DAC summer volume setting; see Table 8

Table 32 IIC_EPICS_START_ADDR address register (0FF7h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 16	–	–	not used
15 to 0	start_addr[15:0]	0000h	start address for the AUDIO_EPICS; can be programmed before releasing ‘epics_pc_reset’ bit; see Table 33

Table 33 IIC_DSP_CTR control register (602Fh)

BIT	SYMBOL	DEFAULT	DESCRIPTION
23 to 19	–	–	not used
18 and 17	pll2_clksel[1:0]	01	choose PLL2 clock selection switch 00: low range 01: mid range
16 and 15	pll1_clksel[1:0]	00	choose PLL1 clock selection switch 00: low range 01: mid range
14 to 10	pll2_div[4:0]	01101	choose PLL2 division factor
9 to 5	pll1_div[4:0]	10000	choose PLL1 division factor
4	pll2_bypass	0	bypass option for SRC_EPICS; this is an evaluation mode only 0: PLL2 1: OSCIN_CLK
3	pll1_bypass	0	bypass option for AUDIO_EPICS clock; warning: the OSCIN_CLK is only used for evaluation; it is functionally not a valid setting 0: PLL2 1: OSCIN_CLK
2	–	–	not used
1	src_pc_reset	1	program counter for SRC_EPICS reset 0: no reset 1: reset; program counter will always be set to 0000h
0	epics_pc_reset	1	program counter for AUDIO_EPICS reset 0: no reset 1: reset; program counter will be set to the ‘start_addr’ value; see Table 32

Table 34 IIC_SILICON_ID register (5FFFh);

BIT	SYMBOL	DEFAULT	DESCRIPTION
31 to 16	dev_number[15:0]	–	development number; decimal number
15 to 12	dev_version[3:0]	–	development version number; binary code
11 to 7	mask_version[4:0]	–	mask version number; binary code
6 to 0	romcode_ version[6:0]	–	ROM code version number; binary code

Table 35 IIC_RDS2_CTR control register (600Dh)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 11	–	–	not used
10	sel_DAVN2_RDS_Flag	0	select DAVN2 control indicator 0: use RDS2 block 1: use FLAG from IFP
9	rds2_clkout	0	see Table 36
8	rds2_clkin	1	
7 and 6	RDS2_DAC[1:0]	00	see Table 37
5	RDS2_NWSY	0	start new synchronization 0: no start 1: start
4 to 0	RDS2_MBBG[4:0]	00000	maximum bad blocks gain

Table 36 Description of bits rds2_clkout and rds2_clkin

rds2_clkout	rds2_clkin	DESCRIPTION
0	0	rds decoder
0	1	burst mode with external clock as input
1	0	rds demodulator
1	1	not allowed

Table 37 Description of bits RDS2_DAC1 and RDS0_DAC0

RDS2_DAC1	RDS2_DAC0	DESCRIPTION
0	0	standard mode
0	1	fast PI search mode
1	0	reduced data request
1	1	decoder bypass

Table 38 IIC_RDS2_SET settings register (600Ch)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15	–	–	not used
14 and 13	RDS2_SYM[1:0]	00	see Table 39
12 to 7	RDS2_MGBL[5:0]	100000	maximum good blocks lose
6	RDS2_RBDS	0	allow RBDS ‘E’ blocks 0: not allow 1: allow
5 to 0	RDS2_MBBL[5:0]	100000	maximum bad blocks lose

Table 39 Description of bits RDS2_SYM1 and RDS2_SYM0

RDS2_SYM1	RDS2_SYMO	DESCRIPTION
0	0	no error correction
0	1	maximum 2 bits burst error
1	0	maximum 5 bits burst error
1	1	no error correction

Table 40 IIC_RDS2_CNT counter register (600Bh)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 10	RDS2_BBC[5:0]	000000	bad blocks counter
9 to 5	RDS2_GBC[4:0]	00000	good blocks counter (only 5 MSBs are available)
4 to 2	RDS2_PBIN[2:0]	111	previous block identifier
1 and 0	RDS2_EPB[1:0]	00	error status previously received block; see Table 41

Table 41 Description of bits RDS2_EPB1 and RDS2_EPB0

RDS2_EPB1	RDS2_EPB0	DESCRIPTION
0	0	no errors detected
0	1	maximum 2 bits
1	0	maximum 5 bits
1	1	uncorrectable

Table 42 IIC_RDS2_PDAT register (600Ah)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 0	RDS2_PDAT[15:0]	0000h	previously processed block data

Table 43 IIC_RDS2_LDAT register (6009h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 0	RDS2_LDAT[15:0]	0000h	last processed block data

Table 44 IIC_RDS2_STAT status register (6008h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 8	–	–	not used
7	RDS2_SYNC	0	synchronization found 0: no synchronization 1: synchronization
6	RDS2_DOFL	0	data overflow flag 0: no overflow 1: overflow

BIT	SYMBOL	DEFAULT	DESCRIPTION
5	RDS2_RSTD	0	reset detected 0: no reset 1: reset
4 to 2	RDS2_LBIN[2:0]	111	last block identification
1 and 0	RDS2_ELB[1:0]	00	error status last block; see Table 45

Table 45 Description of bits RDS2_ELB1 and RDS2_ELB0

RDS2_ELB1	RDS2_ELB0	DESCRIPTION
0	0	no errors detected
0	1	maximum 2 bits
1	0	maximum 5 bits
1	1	uncorrectable

Table 46 IIC_RDS1_CTR control register (6005h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 11	–	–	not used
10	sel_RDS_CLK1_DAVN2	0	select usage for pin RDS_CLK1_DAVN2; pin is used for DAVN2 and IFP flag usage (depending on state of sel_DAVN2_RDS_Flag); otherwise pin is used as RDS_CLK1 for RDS1 block 1: DAVN2 and IFP flag usage 0: RDS_CLK1
9	rds1_clkout	0	see Table 47
8	rds1_clkin	1	
7 and 6	RDS1_DAC[1:0]	00	see Table 48
5	RDS1_NWSY	0	start new synchronization 0: no start 1: start
4 to 0	RDS1_MBBG[4:0]	00000	max bad blocks gain

Table 47 Description of bits rds1_clkout and rds1_clkin

rds1_clkout	rds1_clkin	DESCRIPTION
0	0	decoder
0	1	burst mode with external clock as input
1	0	demodulator
1	1	not allowed

Table 48 Description of bits RDS1_DAC1 and RDS1_DAC0

RDS1_DAC1	RDS1_DAC0	DESCRIPTION
0	0	standard mode
0	1	fast PI search mode
1	0	reduced data request
1	1	decoder bypass

Table 49 IIC_RDS1_SET settings register (6004h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15	–	–	not used
14 and 13	RDS1_SYM[1:0]	00	see Table 50
12 to 7	RDS1_MGBL[5:0]	100000	maximum good blocks lose
6	RDS1_RBDS	0	allow RBDS ‘E’ blocks 0: not allowed 1: allowed
5 to 0	RDS1_MBBL[5:0]	100000	maximum bad blocks lose

Table 50 Description of bits RDS1_SYM1 and RDS1_SYM0

RDS1_SYM1	RDS1_SYM0	DESCRIPTION
0	0	no error correction
0	1	maximum 2 bits burst error
1	0	maximum 5 bits burst error
1	1	no error correction

Table 51 IIC_RDS1_CNT counter register (6003h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 10	RDS1_BBC[5:0]	000000	bad blocks counter
9 to 5	RDS1_GBC[4:0]	00000	good blocks counter (only 5 MSBs are available)
4 to 2	RDS1_PBIN[2:0]	111	previous block identifier
1 and 0	RDS1_EPB[1:0]	00	error status previously received block; see Table 52

Table 52 Description of bits RDS1_EPB1 and RDS1_EPB0

RDS1_EPB1	RDS1_EPB0	DESCRIPTION
0	0	no errors detected
0	1	maximum 2 bits
1	0	maximum 5 bits
1	1	uncorrectable

Table 53 IIC_RDS1_PDAT register (6002h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 0	RDS1_PDAT[15:0]	0000h	previously processed block data

Table 54 IIC_RDS1_LDAT register (6001h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 0	RDS1_LDAT[15:0]	0000h	last processed block data

Table 55 IIC_RDS1_STAT status register (6000h)

BIT	SYMBOL	DEFAULT	DESCRIPTION
15 to 8	–	-	not used
7	RDS1_SYNC	0	synchronization found 0: no synchronization 1: synchronization
6	RDS1_DOFL	0	data overflow flag 0: no overflow 1: overflow
5	RDS1_RSTD	0	reset detected 0: no reset 1: reset
4 to 2	RDS1_LBIN[2:0]	111	last block identification
1 and 0	RDS1_ELB[1:0]	00	error status last block; see Table 56

Table 56 Description of bits RDS1_ELB1 and RDS1_ELB0

RDS1_ELB1	RDS1_ELB0	DESCRIPTION
0	0	no errors detected
0	1	maximum 2 bits
1	0	maximum 5 bits
1	1	uncorrectable

12 I²S-BUS CONTROL

12.1 Basic system requirements

The inter-IC sound (I²S-bus) was developed by Philips to facilitate communications between the ever increasing number of digital audio processing ICs in a typical audio system. The bus only has to handle audio data, while the other signals such as sub-coding and control are transferred separately. To minimize the number of pins required and to keep wiring simple, a 3-line serial bus is used consisting of a line for two time-multiplexed data channels, a word select line and a clock line.

Since the transmitter and receiver have the same clock signal for data transmission, the transmitter as the master, has to generate the bit clock, word select signal and data. In complex systems however, there may be several transmitters and receivers which makes it difficult to define the master. In such systems there is usually a system master controlling digital audio data-flow between the various ICs. Transmitters then have to generate data under the control of an external clock, and so act as a slave. Figure 41 illustrates some simple system configurations and the basic interface timing. Note that the system master can be combined with a transmitter or receiver, and it may be enabled or disabled under software control or by pin programming.

As shown in Fig.41, the bus has three lines:

- Continuous serial clock (SCK)
- Word Select (WS)
- Serial Data (SD).

The device generating SCK and WS is the master.

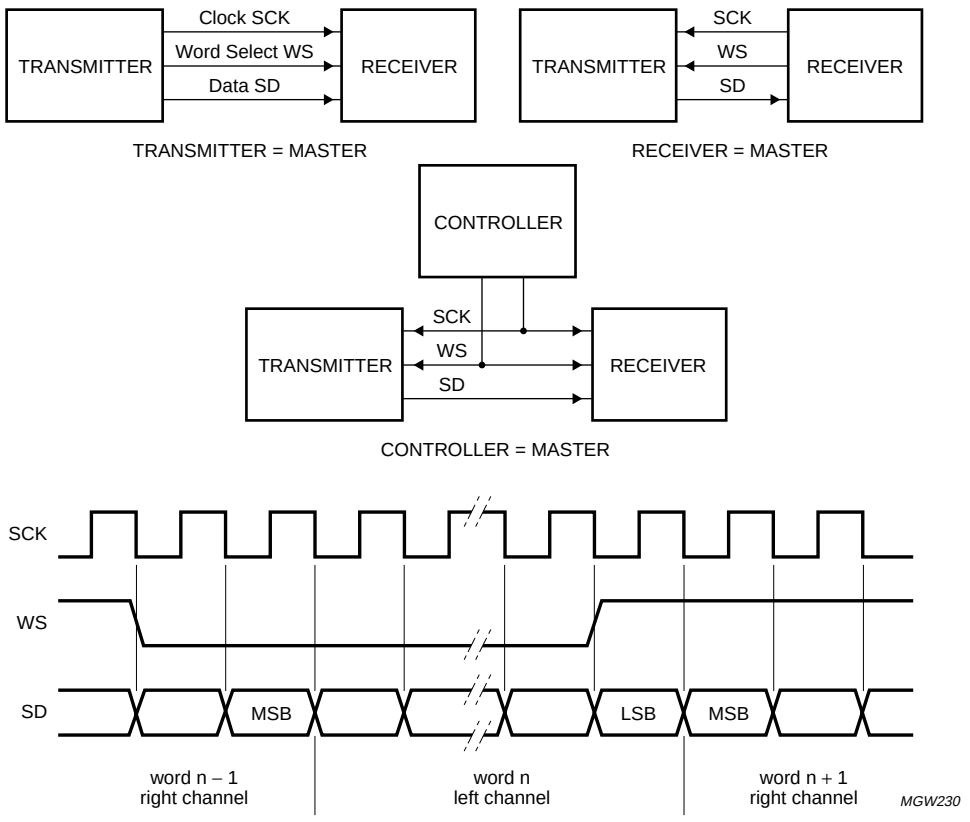


Fig.41 Simple system configurations and basic interface timing.

12.2 Serial data

Serial data is transmitted in twos complement with the MSB first. The MSB is transmitted first because the transmitter and receiver may have different word lengths. It is not necessary for the transmitter to know how many bits the receiver can handle, nor does the receiver need to know how many bits are being transmitted.

When the system word length is greater than the transmitter word length, the word is truncated (least significant bits are set to 0) for data transmission. If the receiver is sent more bits than it's word length, the bits after the LSB are ignored. However, if the receiver is sent fewer bits than it's word length the missing bits are set to zero internally. Therefore, the MSB has a fixed position whereas the position of the LSB depends on the word length. The transmitter always sends the MSB of the next word one clock period after the WS changes.

Serial data sent by the transmitter may be synchronized with either the trailing (HIGH-to-LOW) or the leading (LOW-to-HIGH) edge of the clock signal. However, the serial data must be latched into the receiver on the leading edge of the serial clock signal so there are some restrictions when transmitting data that is synchronized with the leading edge.

12.3 Word select

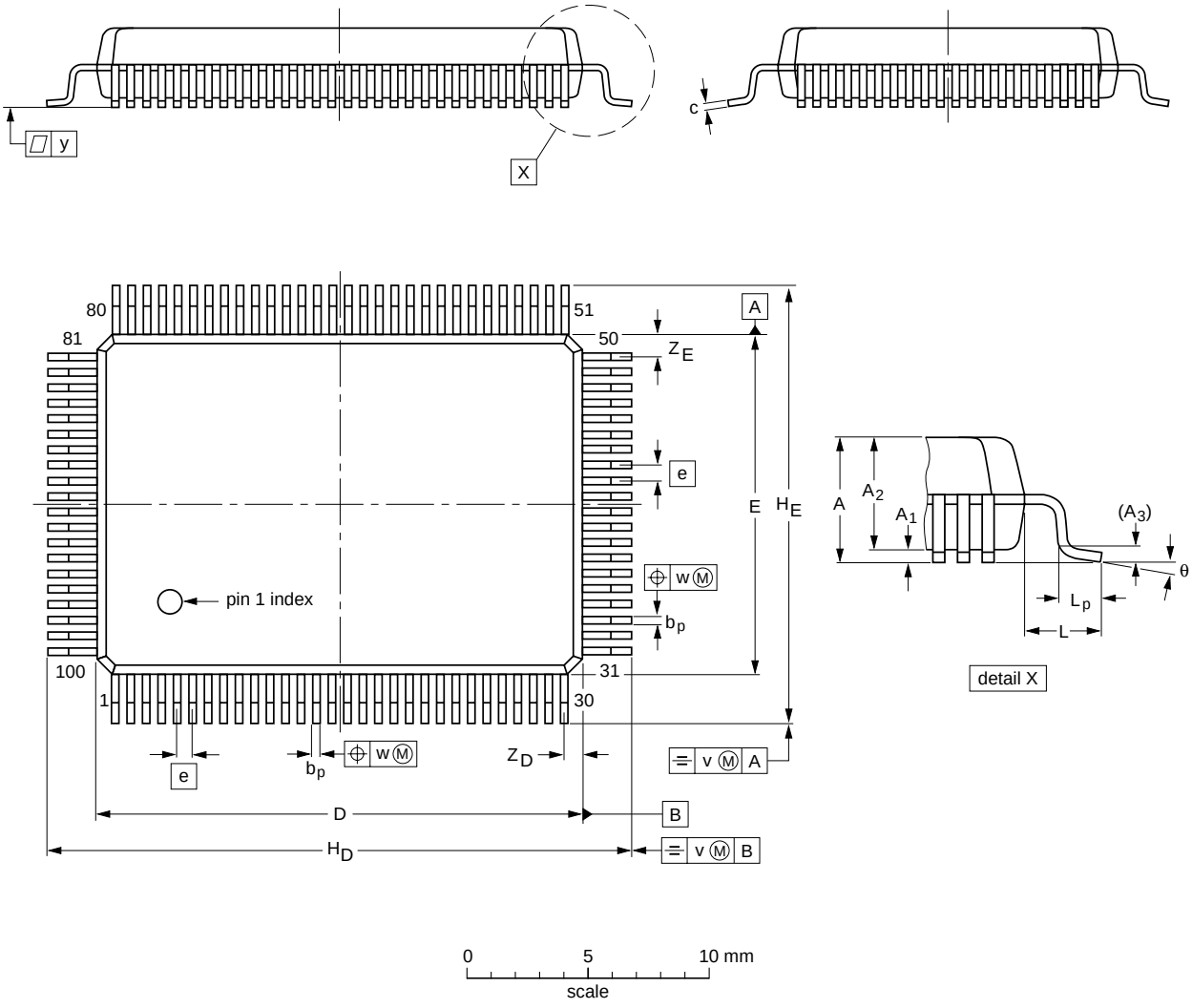
The word select line indicates the channel being transmitted:

- WS = 0: channel 1 (left)
- WS = 1: channel 2 (right).

WS may change either on a trailing or leading edge of the serial clock, but it doesn't need to be symmetrical. In the slave, this signal is latched on the leading edge of the clock signal. The WS line changes one clock period before the MSB is transmitted. This allows the slave transmitter to derive synchronous timing of the serial data that will be set up for transmission. Furthermore, it enables the receiver to store the previous word and clear the input for the next word (see Fig.41).

13 PACKAGE OUTLINE

QFP100: plastic quad flat package; 100 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT317-3**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.4	0.45 0.25	2.90 2.65	0.25	0.40 0.25	0.25 0.14	20.1 19.9	14.1 13.9	0.65	24.2 23.6	18.2 17.6	1.95	1.0 0.73	0.2	0.15	0.1	0.8 0.4	1.0 0.6	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT317-3		MO-112				~~99-12-15~~ 03-02-25

14 SOLDERING

14.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

14.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

14.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

14.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

15 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16 DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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18 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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