MICRON TECHNOLOGY, INC.

MT4LD(T)164A (X), MT8LD264A (X), MT16LD464A (X)
1, 2, 4 MEG x 64 DRAM MODULES

DRAM MODULE

1, 2, 4 MEG x 64

8, 16, 32 MEGABYTE, NONBUFFERED,
3.3V, EDO OR FAST PAGE MODE

FEATURES

- 168-pin, dual-in-line memory module (DIMM)
- Nonbuffered
- High-performance CMOS silicon-gate process
- Single +3.3V ±0.3V power supply
- All device pins are TTL-compatible
- Refresh modes: RAS# ONLY, CAS#-BEFORE-RAS# (CBR), HIDDEN
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- 1,024-cycle refresh (10 row-, 10 column-addresses) [MT4LD(T)164A (X)]
  2,048-cycle refresh (11 row-, 10 column-addresses) [MT8LD264A (X)]
  2,048-cycle refresh (11 row-, 11 column-addresses) [MT16LD464A (X)]
- 5V-tolerant inputs and I/Os (5.5V maximum V_{IH} level)
- Serial Presence-Detect (SPD)

OPTIONS / MARKING

• Timing	
60ns access	-6
70ns access	-7
• Components	
SOJ	D
TSOP (1 Meg x 64 only)	DT
• Packages	
168-pin DIMM (gold)	G
• Access Cycle	
FAST PAGE MODE	Blank
EDO PAGE MODE	X

KEY TIMING PARAMETERS

EDO Operating Mode

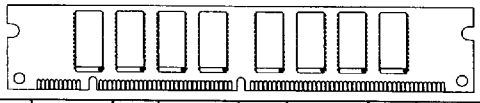
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-6	105ns	60ns	25ns	30ns	15ns	12ns
-7	125ns	70ns	30ns	35ns	20ns	12ns

FPM Operating Mode

SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{RP}
-6	110ns	60ns	35ns	30ns	15ns	40ns
-7	130ns	70ns	40ns	35ns	20ns	50ns

PIN ASSIGNMENT (Front View)
168-Pin DIMM

(DE-9) 1 Meg x 64 SOJ version
(DE-11) 1 Meg x 64 TSOJ version
(DE-12) 2 Meg x 64 (shown), (DE-10) 4 Meg x 64



PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL	PIN #	SYMBOL
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	OE2#	86	DQ32	128	RFU
3	DQ1	45	RAS2#	87	DQ33	129	NC
4	DQ2	46	CAS2#	88	DQ34	130	CAS6#
5	DQ3	47	CAS3#	89	DQ35	131	CAS7#
6	Vcc	48	WE2#	90	Vcc	132	RFU
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	RFU	104	DQ47	146	RFU
21	NC	63	NC	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	WE0#	69	DQ24	111	RFU	153	DQ56
28	CAS0#	70	DQ25	112	CAS4#	154	DQ57
29	CAS1#	71	DQ26	113	CAS5#	155	DQ58
30	RAS0#	72	DQ27	114	NC	156	DQ59
31	OE0#	73	Vcc	115	RFU	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	NC*/A10	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	RFU	167	SA2
42	RFU	84	Vcc	126	RFU	168	Vcc

*1 Meg x 64 version only

PART NUMBERS

PART NUMBER	DESCRIPTION
MT4LD164AG-xx	1 Meg x 64 FPM, SPD, Nonbuffered, SOJ
MT4LD164AG-xx X	1 Meg x 64 EDO, SPD, Nonbuffered, SOJ
MT4LDT164AG-xx	1 Meg x 64 FPM, SPD, Nonbuffered, TSOP
MT4LDT164AG-xx X	1 Meg x 64 EDO, SPD, Nonbuffered, TSOP
MT8LD264AG-xx	2 Meg x 64 FPM, SPD, Nonbuffered, SOJ
MT8LD264AG-xx X	2 Meg x 64 EDO, SPD, Nonbuffered, SOJ
MT16LD464AG-xx	4 Meg x 64 FPM, SPD, Nonbuffered, SOJ
MT16LD464AG-xx X	4 Meg x 64 EDO, SPD, Nonbuffered, SOJ

xx = speed, SPD = serial presence-detect

GENERAL DESCRIPTION

The MT4LD(T)164A (X), MT8LD264A (X) and MT16LD464A (X) are randomly accessed 8MB, 16MB and 32MB solid-state memories organized in a x64 configuration. During READ or WRITE cycles, each bit is uniquely addressed through the 20/21/22 address bits, which are entered 10/11 bits (A0-A10) at RAS# time and 10/11 bits (A0-A10) at CAS# time.

FAST PAGE MODE

FAST PAGE MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST PAGE MODE cycle is always initiated with a row-address strobed-in by RAS# followed by a column-address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST PAGE MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (^tCP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

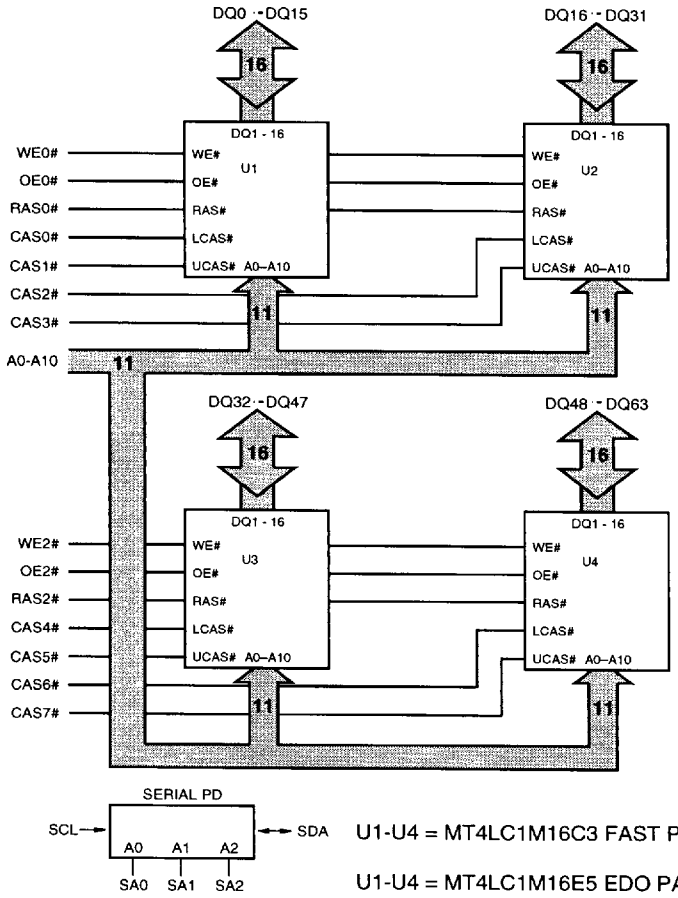
FAST PAGE MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate similar to FAST PAGE MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z.

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^tOFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last (reference the MT4LC4M4E8 DRAM data sheet for additional information on EDO functionality).

SERIAL PRESENCE-DETECT EEPROM

This module incorporates Serial Presence Detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM. This nonvolatile storage device contains data programmed by Micron that identifies the module type and various DRAM organization and timing parameters. System READ/WRITE operations to the EEPROM device occur via a standard I^2C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0) which provide the EEPROM device address. The EEPROM device operates with a Vcc of 3.3V ±0.3V.

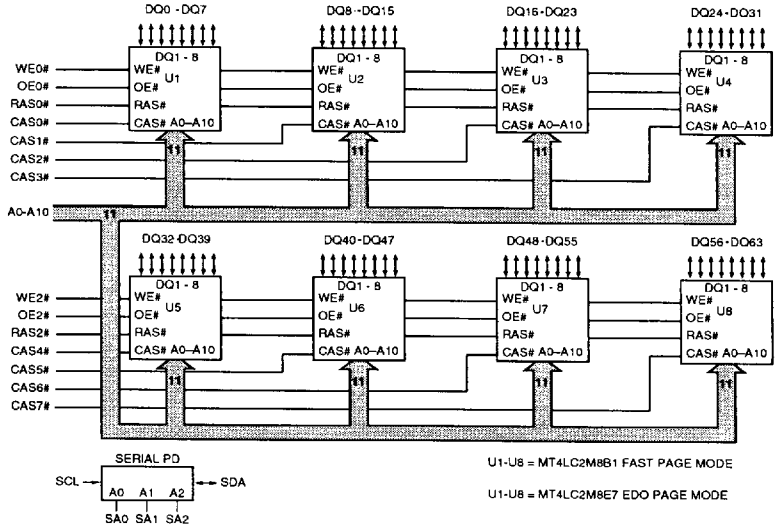
FUNCTIONAL BLOCK DIAGRAM
MT4LD(T)164A (X) (8MB)



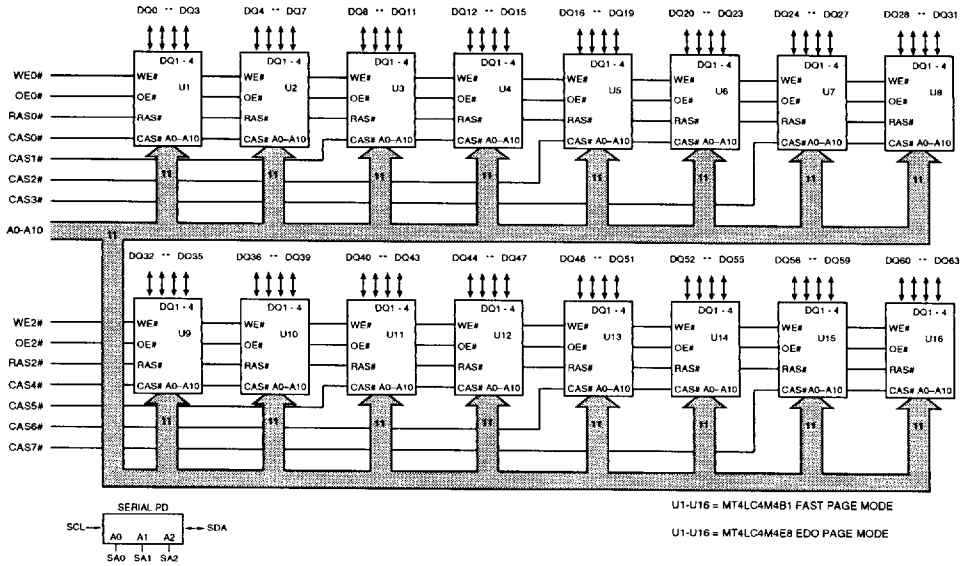
U1-U4 = MT4LC1M16C3 FAST PAGE MODE

U1-U4 = MT4LC1M16E5 EDO PAGE MODE

FUNCTIONAL BLOCK DIAGRAM
MT8LD264A (X) (16MB)



FUNCTIONAL BLOCK DIAGRAM
MT16LD464A (X) (32MB)



SERIAL PRESENCE-DETECT EEPROM
ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs	V_{IH}	V_{CC} x .7	V_{CC} x .5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}	-1.0	V_{CC} x .3	V	
OUTPUT LOW VOLTAGE, I_{OUT} = 3mA	V_{OL}		0.4	V	
INPUT LEAKAGE CURRENT, V_{IN} = GND to V_{CC}	I_{LI}		10	µA	
OUTPUT LEAKAGE CURRENT, V_{OUT} = GND to V_{CC}	I_{LO}		10	µA	
STANDBY CURRENT SCL = SDA = V_{CC} -0.3V, All other inputs = GND or V_{CC} 3.3V +10%	I_{SB}		30	µA	
POWER SUPPLY CURRENT SCL clock frequency = 100 KHz	I_{CC}		2	mA	

SERIAL PRESENCE-DETECT EEPROM
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	t_{AA}	0.3	3.5	µs	
Time the bus must be free before a new transition can start	t_{BUF}	4.7		µs	
Data-out hold time	t_{DH}	300		ns	
SDA and SCL fall time	t_{F}		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		µs	
Start condition hold time	$t_{HD:STA}$	4		µs	
Clock HIGH period	t_{HIGH}	4		µs	
Noise suppression time constant at SCL, SDA inputs	t_{I}		100	ns	
Clock LOW period	t_{LOW}	4.7		µs	
SDA and SCL rise time	t_{R}		1	µs	
SCL clock frequency	t_{SCL}		100	KHz	
Data-in setup time	$t_{SU:DAT}$	250		ns	
Start condition setup time	$t_{SU:STA}$	4.7		µs	
Stop condition setup time	$t_{SU:STO}$	4.7		µs	
WRITE cycle time	t_{WR}		10	ms	31

SERIAL PRESENCE-DETECT MATRIX

	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BYTE 0: NUMBER OF BYTES USED BY MICRON								
128	1	0	0	0	0	0	0	0
BYTE 1: TOTAL NUMBER OF SPD MEMORY BYTES								
256	0	0	0	0	1	0	0	0
BYTE 2: MEMORY TYPE								
FAST PAGE MODE	0	0	0	0	0	0	0	1
EDO PAGE MODE	0	0	0	0	0	0	1	0
BYTE 3: NUMBER OF ROW ADDRESSES								
10 - (8MB)	0	0	0	0	1	0	1	0
11 - (16MB, 32MB)	0	0	0	0	1	0	1	1
BYTE 4: NUMBER OF COLUMN ADDRESSES								
10 - (8MB, 16MB)	0	0	0	0	1	0	1	0
11 - (32MB)	0	0	0	0	1	0	1	1
BYTE 5: NUMBER OF BANKS								
1	0	0	0	0	0	0	0	1
BYTE 6: DATA WIDTH								
x64	0	1	0	0	0	0	0	0
BYTE 7: DATA WIDTH (continued)								
NONE	0	0	0	0	0	0	0	0
BYTE 8: VOLTAGE INTERFACE								
LVTTL	0	0	0	0	0	0	0	1
BYTE 9: RAS# ACCESS TIME								
60ns	0	0	1	1	1	1	0	0
70ns	0	1	0	0	0	1	1	0
BYTE 10: CAS# ACCESS TIME								
15ns	0	0	0	0	1	1	1	1
20ns	0	0	0	1	0	1	0	0
BYTE 11: MODULE CONFIGURATION TYPE								
NON-PARITY	0	0	0	0	0	0	0	0
BYTE 12: REFRESH RATES								
NORMAL (15.625µs)	0	0	0	0	0	0	0	0

NOTE: 1. "1"/"0": Serial Data, "driven to HIGH" / "driven to LOW."

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
30, 45	RAS0#, RAS2#	Input	Row-Address Strobe: RAS# is used to clock-in the 10/11 row-address bits. Two RAS# inputs allow for one x64 bank or two x32 banks.
28, 29, 46, 47, 112, 113, 130, 131	CAS0#-7#	Input	Column-Address Strobe: CAS# is used to clock-in the 10/11 column-address bits, enable the DRAM output buffers and strobe the data inputs on WRITE cycles. Eight CAS# inputs allow byte access control for any memory bank configuration.
27, 48	WE0#, WE2#	Input	Write Enable: WE# is the READ/WRITE control for the DQ pins. WE0# controls DQ0-DQ31. WE2# controls DQ32-DQ63. If WE# is LOW prior to CAS# going LOW, the access is an EARLY WRITE cycle. If WE# is HIGH while CAS# is LOW, the access is a READ cycle, provided OE# is also LOW. If WE# goes LOW after CAS# goes LOW, then the cycle is a LATE WRITE cycle. A LATE WRITE cycle is generally used in conjunction with a READ cycle to form a READ-MODIFY-WRITE cycle.
31, 44	OE0#, OE2#	Input	Output Enable: OE# is the input/output control for the DQ pins. OE0# controls DQ0-DQ31. OE2# controls DQ32-DQ63. These signals may be driven, allowing LATE WRITE cycles.
33-38, 117-121	A0-A10	Input	Address Inputs: These inputs are multiplexed and clocked by RAS# and CAS#.
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/O: For WRITE cycles, DQ0-DQ63 act as inputs to the addressed DRAM location. BYTE WRITEs may be performed by using the corresponding CAS# select (x64 mode only). For READ access cycles, DQ0-DQ63 act as outputs for the addressed DRAM location.
42, 62, 111, 115, 125, 126, 128, 132, 146	RFU	—	RFU: These pins should be left unconnected (reserved for future use).
6, 18, 26, 40, 41, 49, 59, 73,84, 90, 102, 110, 124, 133, 143, 157, 168	Vcc	Supply	Power Supply: +3.3V ±0.3V
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	Vss	Supply	Ground
82	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
83	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
165-167	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.

TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	OE#	ADDRESSES		DATA-IN/OUT
						^tR	^tC	DQ0-63
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO/FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
	Any Cycle (X version)	L	L→H	H	L	n/a	n/a	Data-Out
EDO/FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO/FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS#-ONLY REFRESH		H	X	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data-Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Pin Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs, NC or I/O pins
Relative to V_{SS} ..... -1V to +5.5V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 8W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3.0	3.6	V	
Input High (Logic 1) Voltage, all inputs		V_{IH}	2.0	5.5	V	2
Input Low (Logic 0) Voltage, all inputs		V_{IL}	-1.0	0.8	V	2
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ 5.5V (All other pins not under test = 0V)	CAS0#-CAS7#	I_{I1}	-4	4	µA	
	A0-A10	I_{I2}	-32	32	µA	
	WE0#,2#,OE0#,2#	I_{I3}	-16	16	µA	
	RAS0#,2#	I_{I4}	-16	16	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	DQ0-DQ63	I_{OZ}	-10	10	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

			MAX			
PARAMETER/CONDITION	**SYMBOL**	**SIZE**	**-6**	**-7**	**UNITS**	**NOTES**
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	8MB 16MB 32MB	8 16 32	8 16 32	mA	
STANDBY CURRENT: (CMOS) (RAS# = CAS# = V_{CC} -0.2V)	I_{CC2}	8MB 16MB 32MB	2 4 8	2 4 8	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC3}	8MB 16MB 32MB	680 1,040 1,920	620 960 1,760	mA	3, 25
OPERATING CURRENT: FAST PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{CC4}	8MB 16MB 32MB	400 720 1,440	360 640 1,280	mA	3, 25
OPERATING CURRENT: EDO PAGE MODE (X version only) Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^tPC = ^tPC [MIN])	I_{CC5} (X only)	8MB 16MB 32MB	560 960 1,760	520 880 1,600	mA	3, 25
REFRESH CURRENT: RAS# ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^tRC = ^tRC [MIN])	I_{CC6}	8MB 16MB 32MB	640 1,040 1,920	580 960 1,760	mA	3, 25
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^tRC = ^tRC [MIN])	I_{CC7}	8MB 16MB 32MB	600 1,040 1,920	560 960 1,760	mA	3, 4

CAPACITANCE

		MAX				
PARAMETER	**SYM**	**8MB**	**16MB**	**32MB**	**UNITS**	**NOTES**
Input Capacitance: A0-A10	C_{I1}	26	48	90	pF	2
Input Capacitance: WE0#, WE2#, OE0#, OE2#, RAS0#, RAS2#	C_{I2}	18	34	64	pF	2
Input Capacitance: CAS0# - CAS7#	C_{I3}	10	10	18	pF	2
Input Capacitance: SCL, SA0-SA2	C_{I4}	6	6	6	pF	2
Input/Output Capacitance: DQ0-DQ63, SDA	C_{IO}	10	10	10	pF	2

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35	ns	
Column-address hold time (referenced to RAS#)	tAR	50		55		ns	
Column-address setup time	tASC	0		0		ns	
Row-address setup time	tASR	0		0		ns	
Column-address to WE# delay time	tAWD	55		60		ns	23
Access time from CAS#	tCAC		15		20	ns	14
Column-address hold time	tCAH	10		15		ns	
CAS# pulse width	tCAS	15	10,000	20	10,000	ns	
CAS# hold time (CBR REFRESH)	tCHR	15		15		ns	4
CAS# to output in Low-Z	tCLZ	3		3		ns	26
CAS# precharge time	tCP	10		10		ns	15
Access time from CAS# precharge	tCPA		35		40	ns	
CAS# to RAS# precharge time	tCRP	5		5		ns	
CAS# hold time	tCSH	60		70		ns	
CAS# setup time (CBR REFRESH)	tCSR	5		5		ns	4
CAS# to WE# delay time	tCWD	40		45		ns	23
Write command to CAS# lead time	tCWL	15		20		ns	
Data-in hold time	tDH	10		15		ns	22
Data-in hold time (referenced to RAS#)	tDHR	45		55		ns	
Data-in setup time	tDS	0		0		ns	22
Output disable	tOD	3	15	3	20	ns	
Output enable	tOE		15		20	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	tOEH	15		20		ns	
Output buffer turn-off delay	tOFF	3	15	3	20	ns	19, 26
OE# setup prior to RAS# during HIDDEN REFRESH cycle	tORD	0		0		ns	

FAST PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
FAST-PAGE-MODE READ or WRITE cycle time	tPC	35		40		ns	
FAST-PAGE-MODE READ-WRITE cycle time	tPRWC	85		95		ns	
Access time from RAS#	tRAC		60		70	ns	13
RAS# to column-address delay time	tRAD	15	30	15	35	ns	17
Row-address hold time	tRAH	10		10		ns	
Column-address to RAS# lead time	tRAL	30		35		ns	
RAS# pulse width	tRAS	60	10,000	70	10,000	ns	
RAS# pulse width (FAST PAGE MODE)	tRASP	60	100,000	70	100,000	ns	
Random READ or WRITE cycle time	tRC	110		130		ns	
RAS# to CAS# delay time	tRCD	20	45	20	50	ns	16
Read command hold time (referenced to CAS#)	tRCH	0		0		ns	18
Read command setup time	tRCS	0		0		ns	
Refresh period (1,024 cycles)	tREF		16		16	ms	
Refresh period (2,048 cycles)	tREF		32		32	ms	
RAS# precharge time	tRP	40		50		ns	
RAS# to CAS# precharge time	tRPC	0		0		ns	
Read command hold time (referenced to RAS#)	tRRH	0		0		ns	18
RAS# hold time	tRSH	15		20		ns	
READ WRITE cycle time	tRWC	150		180		ns	
RAS# to WE# delay time	tRWD	85		95		ns	23
Write command to RAS# lead time	tRWL	15		20		ns	
Transition time (rise or fall)	tT	3	50	3	50	ns	
Write command hold time	tWCH	10		15		ns	
Write command hold time (referenced to RAS#)	tWCR	45		55		ns	
WE# command setup time	tWCS	0		0		ns	23
Write command pulse width	tWP	10		15		ns	
WE# hold time (CBR REFRESH)	tWRH	10		10		ns	
WE# setup time (CBR REFRESH)	tWRP	10		10		ns	

EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	tAA		30		35	ns	
Column-address setup to CAS# precharge during writes	tACH	15		15		ns	
Column-address hold time (referenced to RAS#)	tAR	45		50		ns	
Column-address setup time	tASC	0		0		ns	
Row-address setup time	tASR	0		0		ns	
Column-address to WE# delay time	tAWD	55		60		ns	23
Access time from CAS#	tCAC		15		20	ns	14
Column-address hold time	tCAH	10		12		ns	
CAS# pulse width	tCAS	12	10,000	12	10,000	ns	
CAS# hold time (CBR REFRESH)	tCHR	10		12		ns	4
CAS# to output in Low-Z	tCLZ	0		0		ns	
Data output hold after CAS# LOW	tCOH	3		3		ns	
CAS# precharge time	tCP	10		10		ns	15
Access time from CAS# precharge	tCPA		35		40	ns	
CAS# to RAS# precharge time	tCRP	5		5		ns	
CAS# hold time	tCSH	50		55		ns	
CAS# setup time (CBR REFRESH)	tCSR	5		5		ns	4
CAS# to WE# delay time	tCWD	35		40		ns	23
Write command to CAS# lead time	tCWL	15		15		ns	
Data-in hold time	tDH	10		12		ns	22
Data-in hold time (referenced to RAS#)	tDHR	45		55		ns	
Data-in setup time	tDS	0		0		ns	22
Output disable	tOD	0	15	0	15	ns	
Output enable	tOE		15		20	ns	
OE# hold time from WE# during READ-MODIFY-WRITE cycle	tOEH	12		12		ns	
OE# HIGH hold time from CAS# HIGH	tOEHC	10		10		ns	
OE# HIGH pulse width	tOEP	10		10		ns	
OE# LOW to CAS# HIGH setup time	tOES	5		5		ns	
Output buffer turn-off delay	tOFF	3	15	3	15	ns	19
OE# setup prior to RAS# during HIDDEN REFRESH cycle	tORD	0		0		ns	19
EDO-PAGE-MODE READ or WRITE cycle time	tPC	25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	tPRWC	75		85		ns	
Access time from RAS#	tRAC		60		70	ns	13
RAS# to column-address delay time	tRAD	12	30	12	35	ns	17
Row-address hold time	tRAH	10		10		ns	
Column-address to RAS# lead time	tRAL	30		35		ns	
RAS# pulse width	tRAS	60	10,000	70	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	tRASP	60	125,000	70	125,000	ns	
Random READ or WRITE cycle time	tRC	105		125		ns	
RAS# to CAS# delay time	tRCD	14	45	14	50	ns	16
Read command hold time (referenced to CAS#)	tRCH	0		0		ns	18
Read command setup time	tRCS	0		0		ns	
Refresh period (1,024 cycles)	tREF		16		16	ms	
Refresh period (2,048 cycles)	tREF		32		32	ms	

EDO PAGE MODE
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

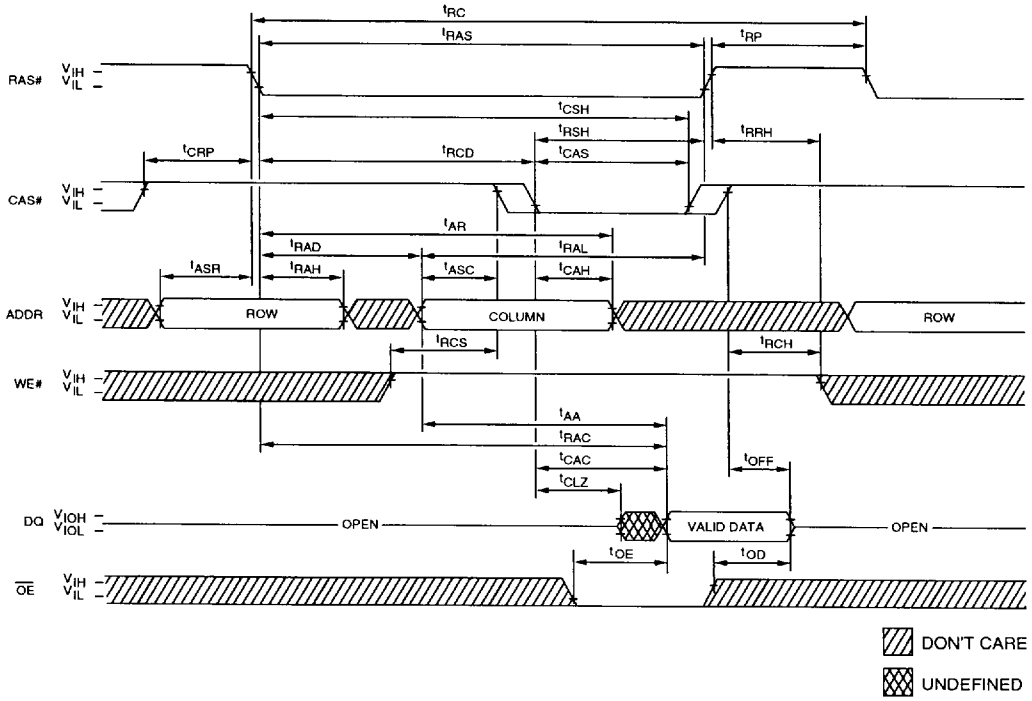
(Notes: 5, 6, 7, 8, 9, 10, 11, 12) (Vcc = +3.3V ±0.3V)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	UNITS	NOTES
RAS# precharge time	tRP	40		50		ns	
RAS# to CAS# precharge time	tRPC	5		5		ns	
Read command hold time (referenced to RAS#)	tRRH	0		0		ns	18
RAS# hold time	tRSH	13		15		ns	
READ WRITE cycle time	tRWC	145		170		ns	
RAS# to WE# delay time	tRWD	80		90		ns	23
Write command to RAS# lead time	tRWL	15		15		ns	
Transition time (rise or fall)	tT	2	50	2	50	ns	
Write command hold time	tWCH	10		12		ns	
Write command hold time (referenced to RAS#)	tWCR	45		55		ns	
WE# command setup time	tWCS	0		0		ns	
Output disable delay from WE# (CAS# HIGH)	tWHZ	0	13	0	15	ns	
Write command pulse width	tWP	10		12		ns	
WE# pulse width for output disable when CAS# HIGH	tWPZ	10		12		ns	
WE# hold time (CBR REFRESH)	tWRH	10		10		ns	
WE# setup time (CBR REFRESH)	tWRP	10		10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.0V ±0.3V; f = 1 MHz.
3. I_{CC} is dependent on output loading. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
6. An initial pause of 100µs is required after power-up, followed by eight RAS# refresh cycles (RAS# ONLY or CBR with WE# HIGH) before proper device operation is assured. The eight RAS# cycle wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 5ns for FAST PAGE MODE and 2.5ns for EDO PAGE MODE.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. If CAS# = V_{IH}, data output is High-Z.
11. If CAS# = V_{IL}, data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
13. Assumes that ^{t}RCD < ^{t}RCD (MAX). If ^{t}RCD is greater than the maximum recommended value shown in this table, ^{t}RAC will increase by the amount that ^{t}RCD exceeds the value shown.
14. Assumes that ^{t}RCD ≥ ^{t}RCD (MAX).
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^{t}CP.
16. Operation within the ^{t}RCD (MAX) limit ensures that ^{t}RAC (MAX) can be met. ^{t}RCD (MAX) is specified as a reference point only; if ^{t}RCD is greater than the specified ^{t}RCD (MAX) limit, access time is controlled exclusively by ^{t}CAC.
17. Operation within the ^{t}RAD (MAX) limit ensures that ^{t}RAC (MIN) and ^{t}CAC (MIN) can be met. ^{t}RAD (MAX) is specified as a reference point only; if ^{t}RAD is greater than the specified ^{t}RAD (MAX) limit, access time is controlled exclusively by ^{t}AA.
18. Either ^{t}RCH or ^{t}RRH must be satisfied for a READ cycle.
19. ^{t}OFF (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The maximum current ratings are based with the memory operating or being refreshed in the x64 mode. The stated maximums may be reduced by approximately one-half when used in the x32 mode.
22. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. ^{t}WCS, ^{t}RWD, ^{t}AWD and ^{t}CWD are not restrictive operating parameters. ^{t}WCS applies to EARLY WRITE cycles. ^{t}RWD, ^{t}AWD and ^{t}CWD apply to READ-MODIFY-WRITE cycles. If ^{t}WCS ≥ ^{t}WCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^{t}RWD ≥ ^{t}RWD (MIN), ^{t}AWD ≥ ^{t}AWD (MIN) and ^{t}CWD ≥ ^{t}CWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. ^{t}WCS, ^{t}RWD, ^{t}CWD and ^{t}AWD are not applicable in a LATE WRITE cycle.
24. Refresh current increases if ^{t}RAS is extended beyond its minimum specification.
25. Column-address changed once each cycle.
26. The 3ns minimum parameter guaranteed by design.
27. Measured with the specified current load and 100pf.
28. ^{t}CAC (MIN), ^{t}CPA (MIN) and ^{t}AA (MIN) are for reference only to help aid the user as to when to expect the earliest data to be accessed. Only ^{t}CAC (MAX), ^{t}CPA (MAX) and ^{t}AA (MAX) are guaranteed.
29. For FAST PAGE MODE option, ^{t}OFF is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, ^{t}OFF on an EDO option is determined by the latter of the RAS# and CAS# signal to transition HIGH.
30. Applies to both EDO and FAST PAGE MODE modules.
31. The SPD EEPROM WRITE cycle time (^{t}WR) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.

READ CYCLE
(FAST PAGE MODE Module)

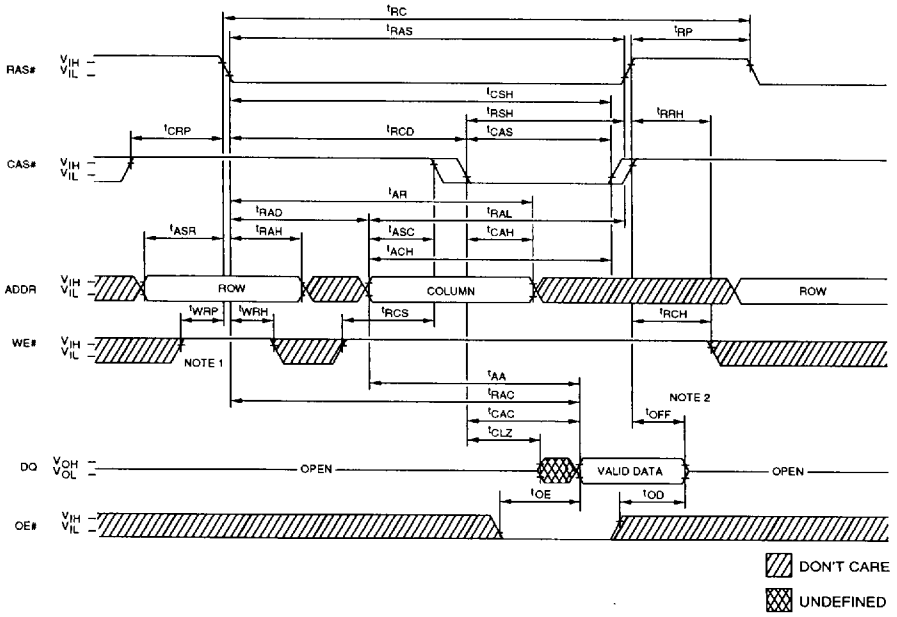


FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	3		3		ns
tCRP	5		5		ns
tCSH	60		70		ns
tOD	3	15	3	20	ns
tOE		15		20	ns
tOFF	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	110		130		ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

READ CYCLE
(EDO PAGE MODE Module)



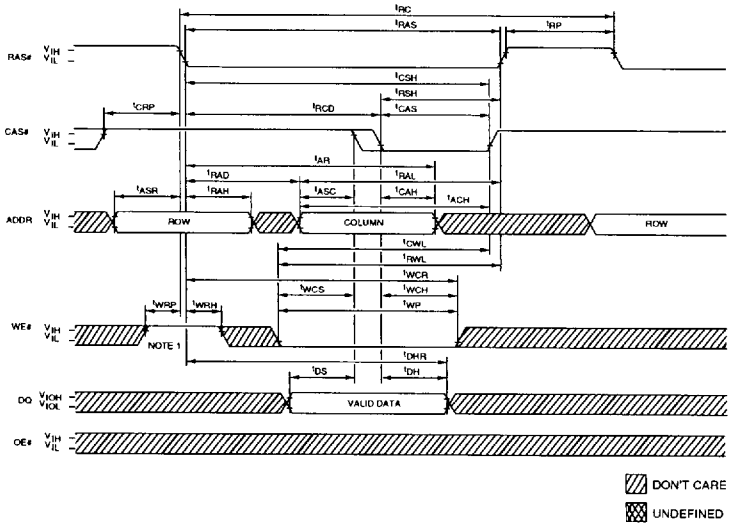
NOTE:
1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. tOFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tACH	15		15		ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCAS	12	10,000	12	10,000	ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	50		55		ns
tOD	0	15	0	15	ns
tOE		15		15	ns
tOFF	3	15	3	15	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC	105		125		ns
tRCD	14	45	14	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	13		15		ns
tWRH	10		10		ns
tWRP	10		10		ns

EARLY WRITE CYCLE [30]



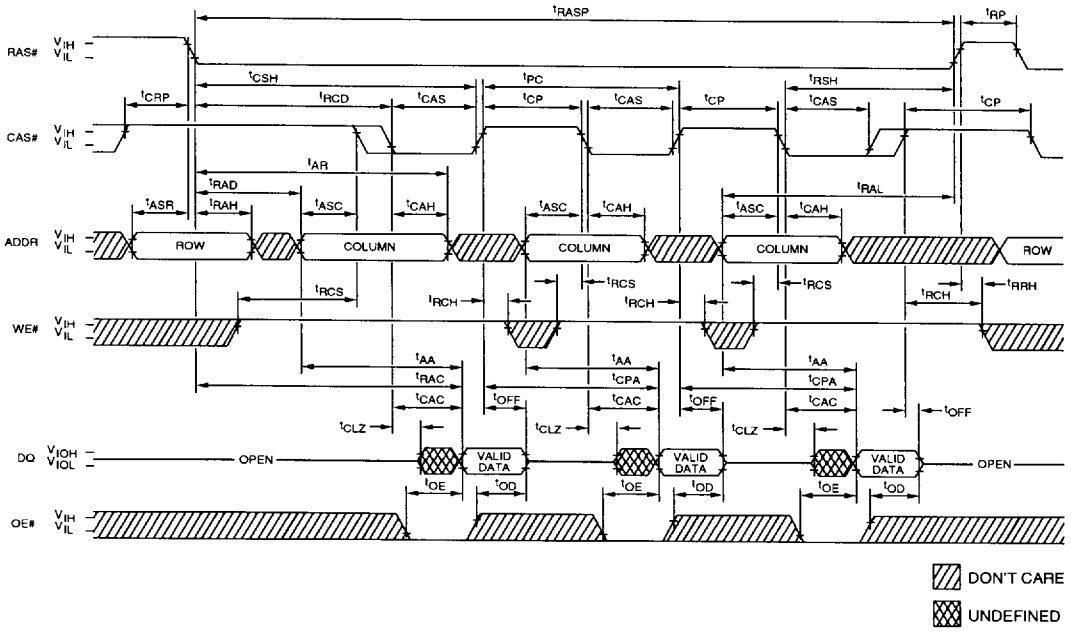
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tACH EDO)	15		15		ns
tAR (FPM)	50		55		ns
tAR (EDO)	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH (FPM)	10		15		ns
tCAH (EDO)	10		12		ns
tCAS (FPM)	15	10,000	20	10,000	ns
tCAS (EDO)	12	10,000	12	10,000	ns
tCRP	5		5		ns
tCSH (FPM)	60		70		ns
tCSH (EDO)	50		55		ns
tCWL (FPM)	15		20		ns
tCWL (EDO)	15		15		ns
tDH (FPM)	10		15		ns
tDH (EDO)	10		12		ns
tDHR	45		55		ns
tDS	0		0		ns
tRAD (FPM)	15	30	15	35	ns
tRAD (EDO)	12	30	12	35	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC (FPM)	110		130		ns
tRC (EDO)	105		125		ns
tRCD (FPM)	20	45	20	50	ns
tRCD (EDO)	14	45	14	50	ns
tRP	40		50		ns
tRSH (FPM)	15		20		ns
tRSH (EDO)	13		15		ns
tRWL (FPM)	15		20		ns
tRWL (EDO)	15		15		ns
tWCH (FPM)	10		15		ns
tWCH (EDO)	10		12		ns
tWCR	45		55		ns
tWCS	0		0		ns
tWP (FPM)	10		15		ns
tWP (EDO)	10		12		ns
tWRH	10		10		ns
tWRP	10		10		ns

FAST-PAGE-MODE READ CYCLE

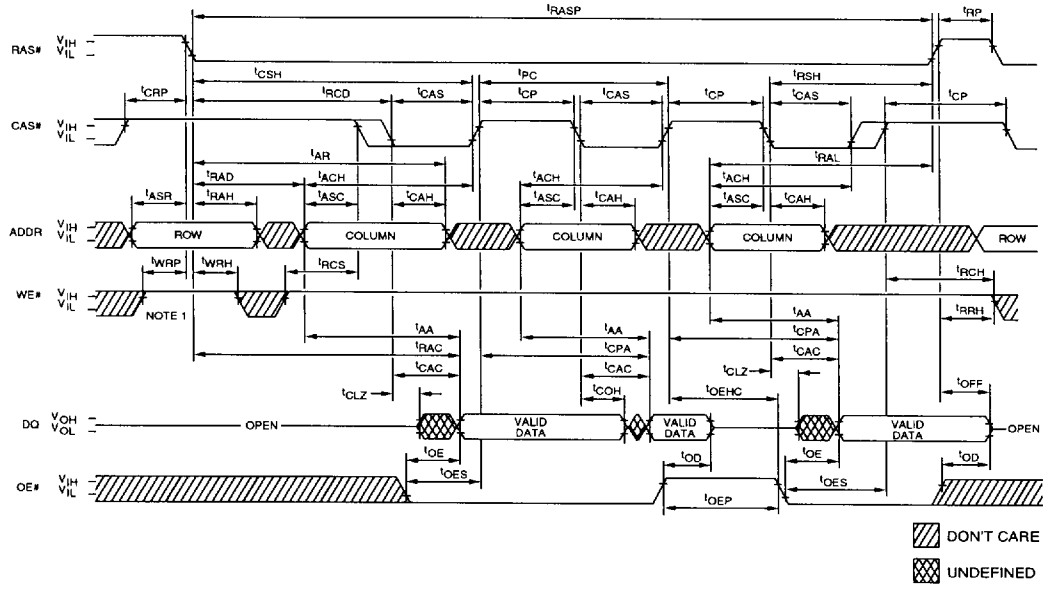


FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	3		3		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	5		5		ns
tCSH	60		70		ns
tOD	3	15	3	20	ns
tOE		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOFF	3	15	3	20	ns
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRRH	0		0		ns
tRSH	15		20		ns

EDO-PAGE-MODE READ CYCLE



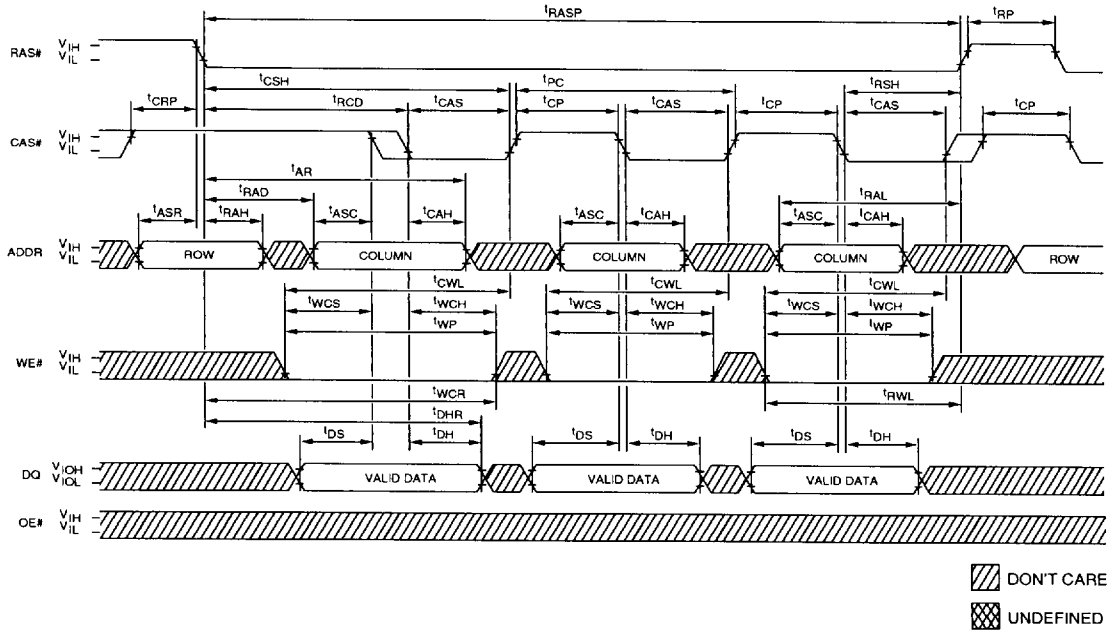
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}AA		30		35	ns
^{t}ACH	15		15		ns
^{t}AR	45		50		ns
^{t}ASC	0		0		ns
^{t}ASR	0		0		ns
^{t}CAC		15		20	ns
^{t}CAH	10		12		ns
^{t}CAS	12	10,000	12	10,000	ns
^{t}CLZ	0		0		ns
^{t}COH	3		3		ns
^{t}CP	10		10		ns
^{t}CPA		35		40	ns
^{t}CRP	5		5		ns
^{t}CSH	50		55		ns
^{t}OD	0	15	0	15	ns
^{t}OE		15		20	ns
^{t}OEHC	10		10		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}OEP	10		10		ns
^{t}OES	5		5		ns
^{t}OFF	3	15	3	15	ns
^{t}PC	25		30		ns
^{t}RAC		60		70	ns
^{t}RAD	12	30	12	35	ns
^{t}RAH	10		10		ns
^{t}RAL	30		35		ns
^{t}RASP	60	125,000	70	125,000	ns
^{t}RCD	14	45	14	50	ns
^{t}RCH	0		0		ns
^{t}RCS	0		0		ns
^{t}RP	40		50		ns
^{t}RRH	0		0		ns
^{t}RSH	13		15		ns
^{t}WRH	10		10		ns
^{t}WRP	10		10		ns

FAST-PAGE-MODE EARLY-WRITE CYCLE

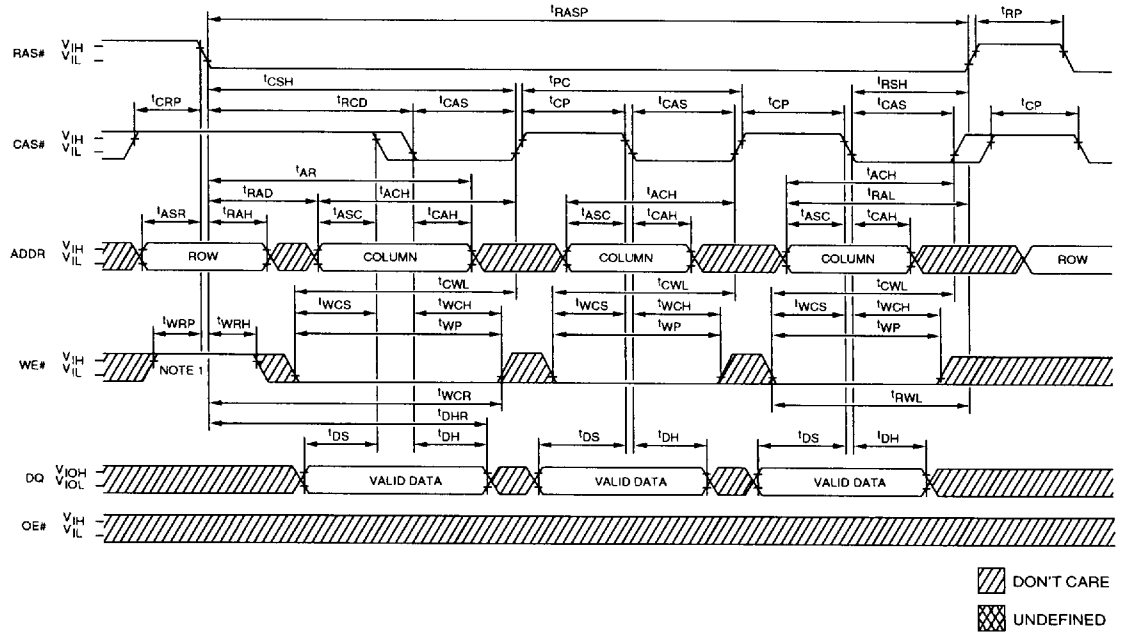


FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCP	10		10		ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDHR	45		55		ns
tDS	0		0		ns
tPC	35		40		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCR	45		55		ns
tWCS	0		0		ns
tWP	10		15		ns

EDO-PAGE-MODE EARLY-WRITE CYCLE



NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

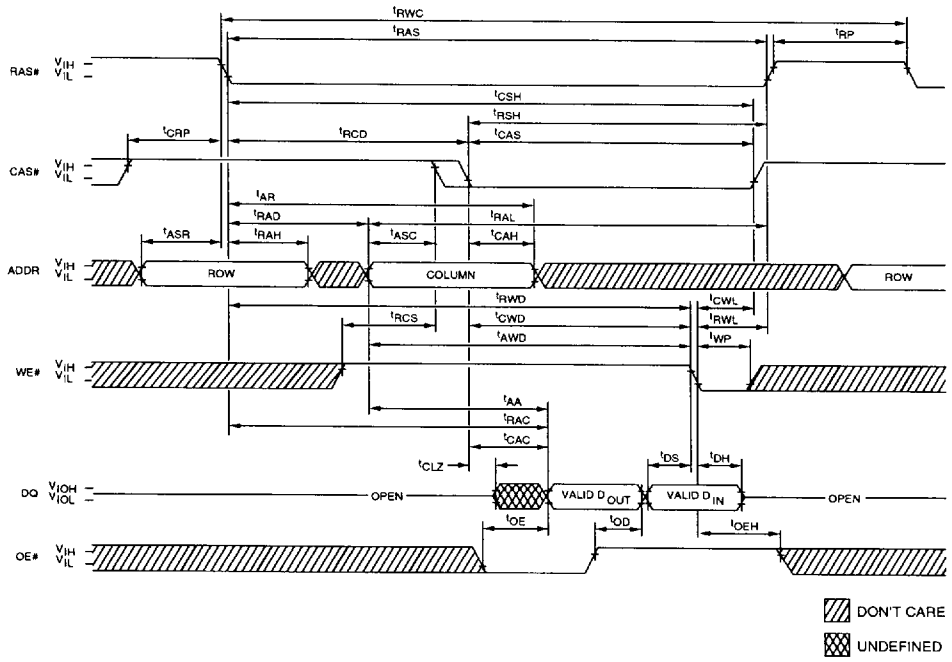
EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tACH	15		15		ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAH	10		12		ns
tCAS	12	10,000	12	10,000	ns
tCP	10		10		ns
tCRP	5		5		ns
tCSH	50		55		ns
tCWL	15		15		ns
tDH	10		12		ns
tDHR	45		55		ns
tDS	0		0		ns
tPC	25		30		ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	125,000	70	125,000	ns
tRCD	14	45	14	50	ns
tRP	40		50		ns
tRSH	13		15		ns
tRWL	15		15		ns
tWCH	10		12		ns
tWCR	45		55		ns
tWCS	0		0		ns
tWP	10		12		ns
tWRH	10		10		ns
tWRP	10		10		ns

READ WRITE CYCLE

(LATE WRITE and READ-MODIFY-WRITE cycles)

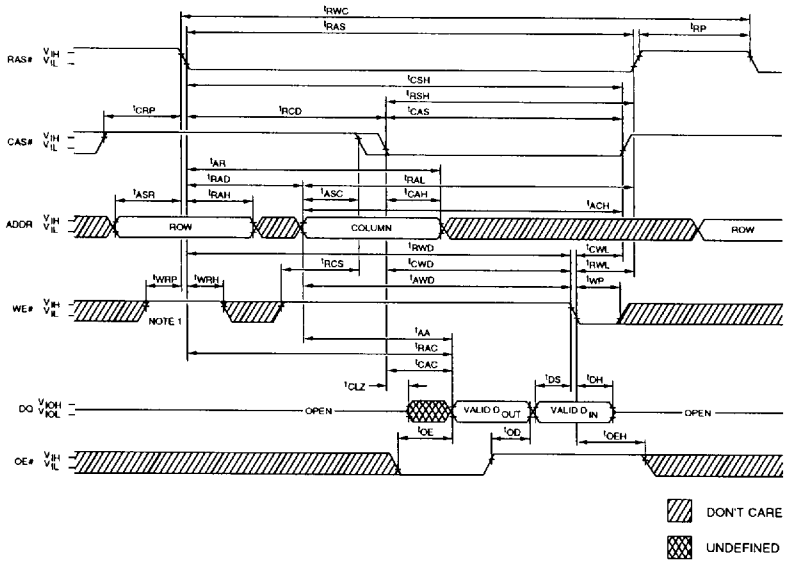


FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	55		60		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	3		3		ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWD	40		45		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns
tOD	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOE		15		20	ns
tOEH	15		20		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWC	150		180		ns
tRWD	85		95		ns
tRWL	15		20		ns
tWP	10		15		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



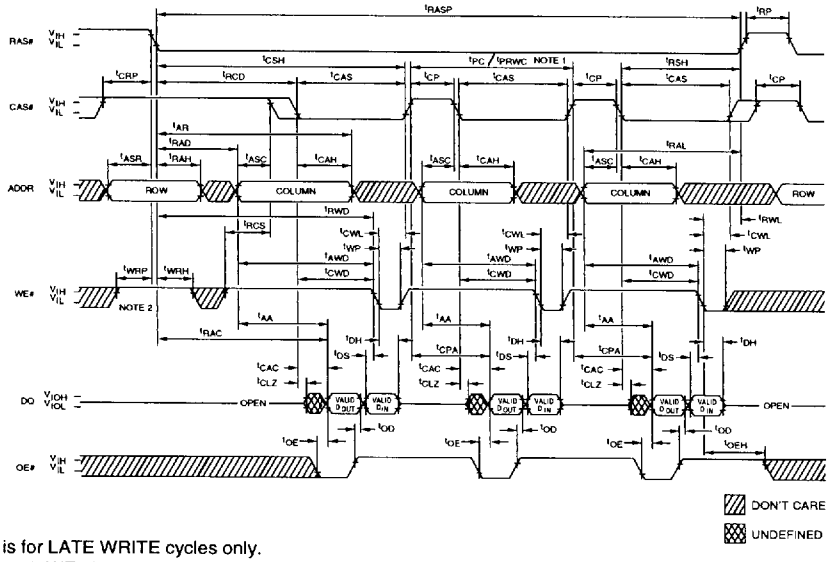
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tACH	15		15		ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	55		60		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCAS	12	10,000	12	10,000	ns
tCLZ	0		0		ns
tCRP	5		5		ns
tCSH	50		55		ns
tCWD	35		40		ns
tCWL	15		15		ns
tDH	10		12		ns
tDS	0		0		ns
tOD	0	15	0	15	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOE		15		20	ns
tOEH	12		12		ns
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRCD	14	45	14	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	13		15		ns
tRWC	145		170		ns
tRWD	80		90		ns
tRWL	15		15		ns
tWP	10		12		ns
tWRH	10		10		ns
tWRP	10		10		ns

FPM-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



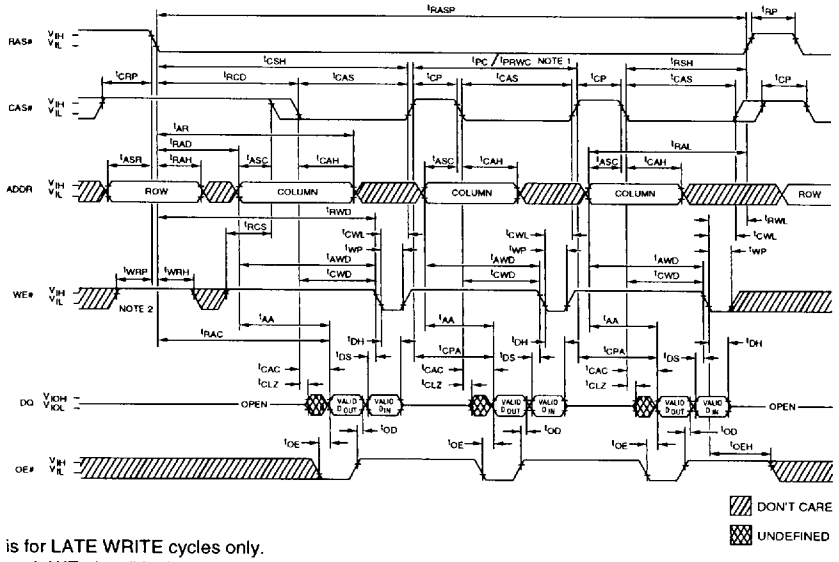
NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	55		60		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	3		3		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWD	40		45		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns
tOD	3	15	3	20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOE		15		20	ns
tOEH	15		20		ns
tPC	35		40		ns
tPRWC	85		95		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWD	85		95		ns
tRWL	15		20		ns
tWP	10		15		ns
tWRH	10		10		ns
tWRP	10		10		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



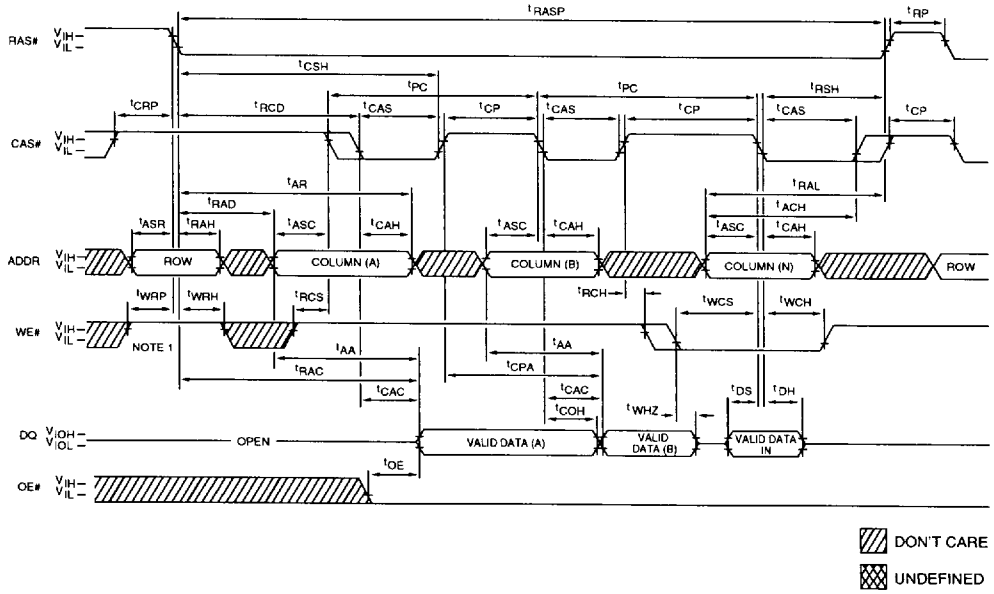
NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tAWD	55		60		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCAS	12	10,000	12	10,000	ns
tCLZ	0		0		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	5		5		ns
tCSH	50		55		ns
tCWD	35		40		ns
tCWL	15		15		ns
tDH	10		12		ns
tDS	0		0		ns
tOD	0	15	0	15	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOE		15		20	ns
tOEH	12		12		ns
tPC	25		30		ns
tPRWC	75		85		ns
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	125,000	70	125,000	ns
tRCD	14	45	14	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	13		15		ns
tRWD	80		90		ns
tRWL	15		15		ns
tWP	10		12		ns
tWRH	10		10		ns
tWRP	10		10		ns

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



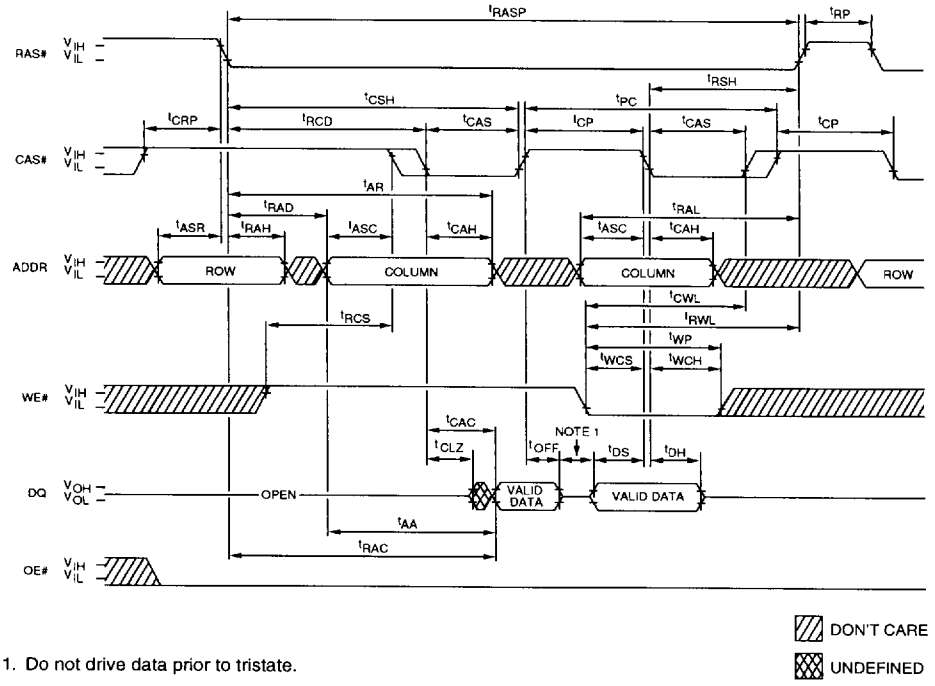
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tACH	15		15		ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCAS	12	10,000	12	10,000	ns
tCOH	3		3		ns
tCP	10		10		ns
tCPA		35		40	ns
tCRP	5		5		ns
tCSH	50		55		ns
tDH	10		12		ns
tDS	0		0		ns
tOE		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tPC	25		30		ns
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	125,000	70	125,000	ns
tRCD	14	45	14	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	13		15		ns
tWCH	10		12		ns
tWCS	0		0		ns
tWHZ	0	13	0	15	ns
tWRH	10		10		ns
tWRP	10		10		ns

FAST-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



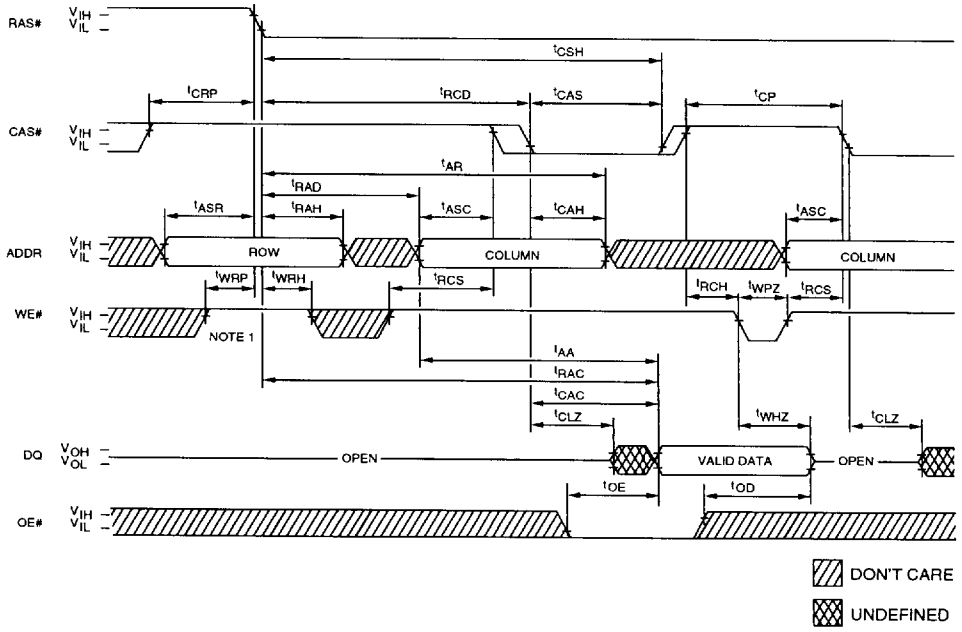
NOTE: 1. Do not drive data prior to tristate.

FAST PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tAA		30		35	ns
tAR	50		55		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		15		ns
tCAS	15	10,000	20	10,000	ns
tCLZ	3		3		ns
tCP	10		10		ns
tCRP	5		5		ns
tCSH	60		70		ns
tCWL	15		20		ns
tDH	10		15		ns
tDS	0		0		ns
tOFF	3	15	3	20	ns

	-6		-7		
SYM	**MIN**	**MAX**	**MIN**	**MAX**	**UNITS**
tPC	35		40		ns
tRAC		60		70	ns
tRAD	15	30	15	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRASP	60	100,000	70	100,000	ns
tRCD	20	45	20	50	ns
tRCS	0		0		ns
tRP	40		50		ns
tRSH	15		20		ns
tRWL	15		20		ns
tWCH	10		15		ns
tWCS	0		0		ns
tWP	10		15		ns

EDO READ CYCLE
(with WE#-controlled disable)



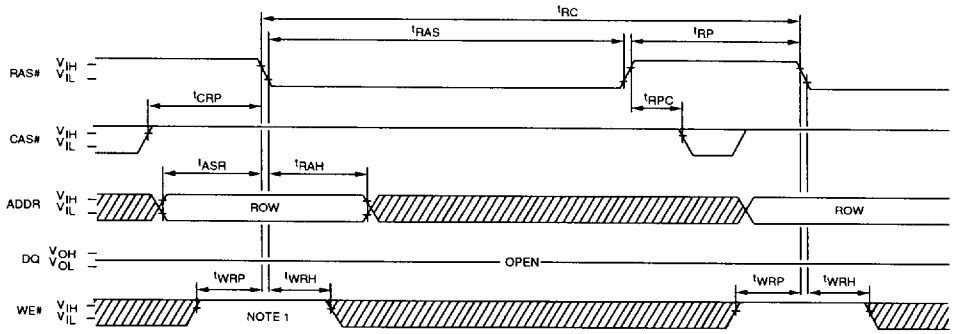
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH	10		12		ns
tCAS	12	10,000	12	10,000	ns
tCLZ	0		0		ns
tCP	10		10		ns
tCRP	5		5		ns
tCSH	50		55		ns
tOD	0	15	0	15	ns

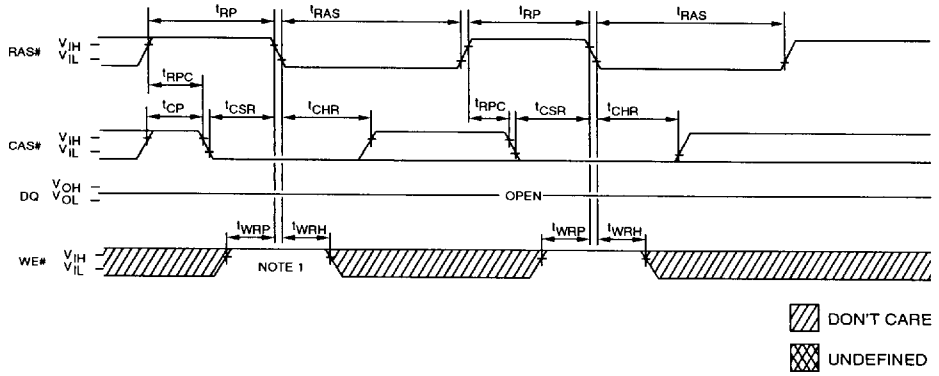
	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOE		15		20	ns
tRAC		60		70	ns
tRAD	12	30	12	35	ns
tRAH	10		10		ns
tRCD	14	45	14	50	ns
tRCH	0		0		ns
tRCS	0		0		ns
tWHZ	0	13	0	15	ns
tWPZ	10		12		ns
tWRH	10		10		ns
tWRP	10		10		ns

RAS#-ONLY REFRESH CYCLE [30]



CBR REFRESH CYCLE [30]

(Addresses, OE# = DON'T CARE)



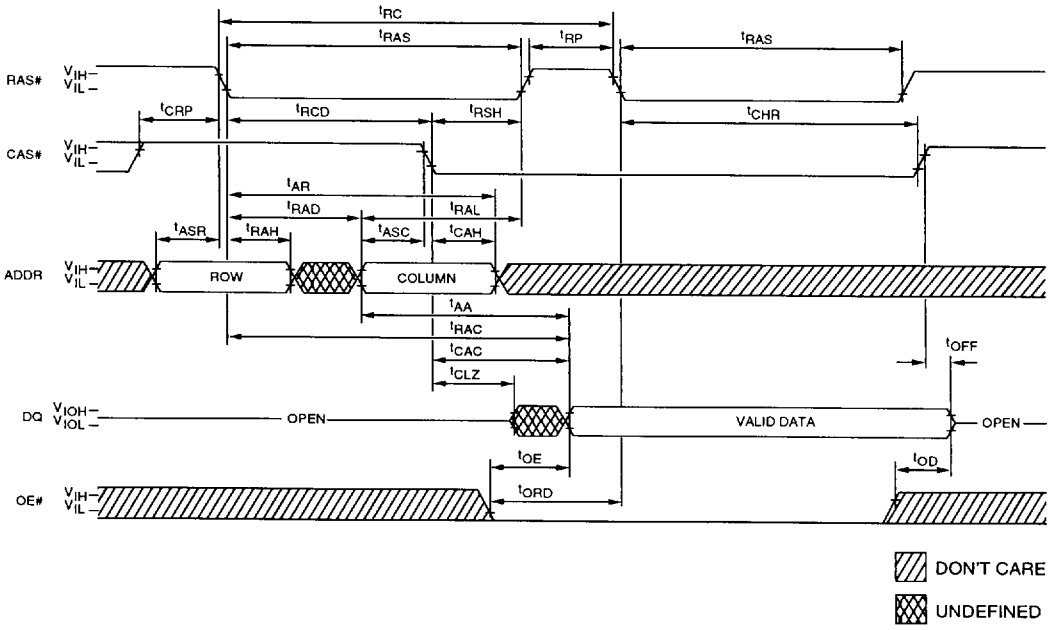
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}ASR	0		0		ns
^{t}CHR (FPM)	15		15		ns
^{t}CHR (EDO)	10		12		ns
^{t}CP	10		10		ns
^{t}CRP	5		5		ns
^{t}CSR	5		5		ns
^{t}RAH	10		10		ns
^{t}RAS	60	10,000	70	10,000	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
^{t}RC (FPM)	110		130		ns
^{t}RC (EDO)	105		125		ns
^{t}RP	40		50		ns
^{t}RPC (FPM)	0		0		ns
^{t}RPC (EDO)	5		5		ns
^{t}WRH	10		10		ns
^{t}WRP	10		10		ns

HIDDEN REFRESH CYCLE [20, 30]
(WE# = HIGH; OE# = LOW)

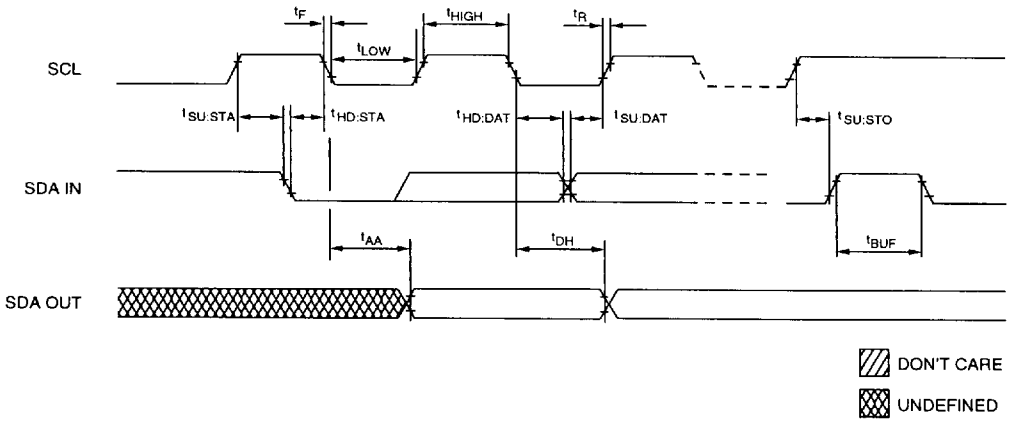


FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tAA		30		35	ns
tAR (FPM)	50		55		ns
tAR (EDO)	45		50		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		15		20	ns
tCAH (FPM)	10		15		ns
tCAH (EDO)	10		12		ns
tCHR (FPM)	15		15		ns
tCHR (EDO)	10		12		ns
tCLZ (FPM)	3		3		ns
tCLZ (EDO)	0		0		ns
tCRP	5		5		ns
tOD (FPM)	3	15	3	20	ns
tOD (EDO)	0	15	0	15	ns
tOE		15		20	ns

	-6		-7		
SYM	MIN	MAX	MIN	MAX	UNITS
tOFF (FPM)	3	15	3	20	ns
tOFF (EDO)	3	15	3	15	ns
tORD	0		0		ns
tRAC		60		70	ns
tRAD (FPM)	15	30	15	35	ns
tRAD (EDO)	12	30	12	35	ns
tRAH	10		10		ns
tRAL	30		35		ns
tRAS	60	10,000	70	10,000	ns
tRC (FPM)	110		130		ns
tRC (EDO)	105		125		ns
tRCD (FPM)	20	45	20	50	ns
tRCD (EDO)	14	45	14	50	ns
tRP	40		50		ns
tRSH (FPM)	15		20		ns
tRSH (EDO)	13		15		ns

SPD EEPROM



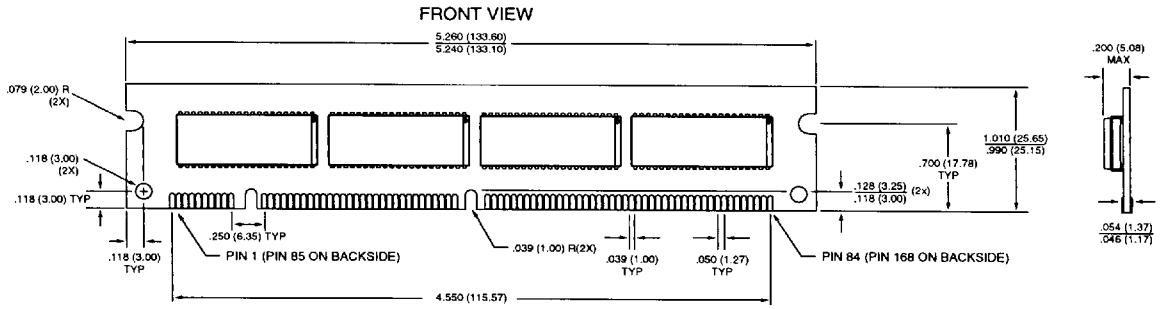
SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYM	MIN	MAX	UNITS
tAA	0.3	3.5	µs
tBUF	4.7		µs
tDH	300		ns
tF		300	ns
tHD:DAT	0		µs
tHD:STA	4		µs
tHIGH	4		µs
tI		100	ns

SYM	MIN	MAX	UNITS
tLOW	4.7		µs
tR		1	µs
tSCL		100	KHz
tSU:DAT	250		ns
tSU:STA	4.7		µs
tSU:STO	4.7		µs
tWR		10	ms

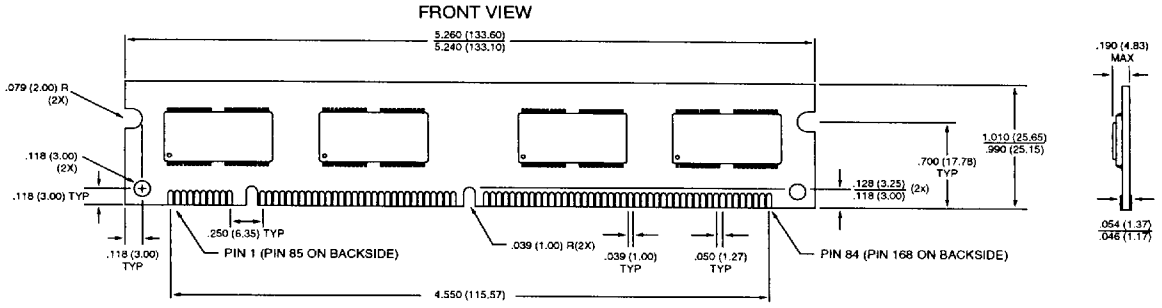
168-PIN DIMM

DE-9



168-PIN TSOP DIMM

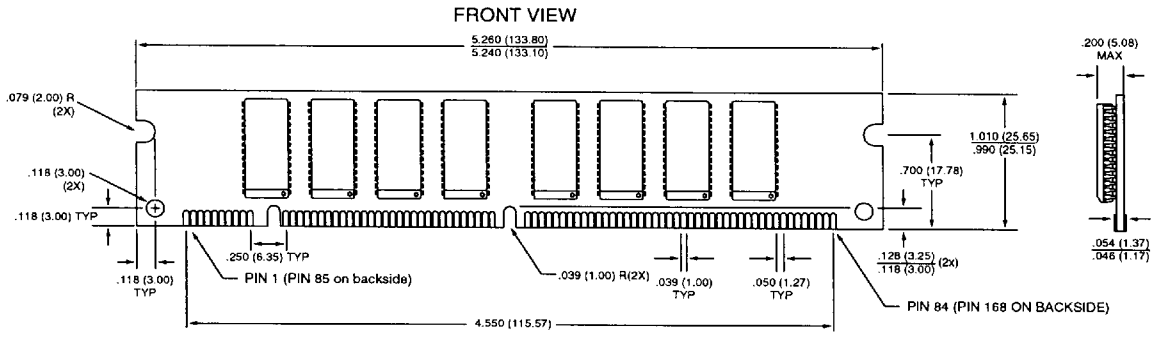
DE-11



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

168-PIN DIMM

DE-12



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

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