LXT9784

Low-Power Octal PHY

Datasheet

The LXT9784 is an eight-port Fast Ethernet PHY Transceiver supporting IEEE 802.3 10Mbps and 100Mbps physical layer applications. It provides both a Reduced Media Independent Interface (RMII) and a Serial Media Independent Interface (SMII) for switching and other independent port applications. In RMII mode, each PHY has a discrete exposed RMII interface, and in SMII mode a discrete exposed SMII interface. All network ports provide a Twisted-Pair (TP) interface for a 10/100BASE-TX connection.

The LXT9784 provides three discrete LED driver outputs for each port. The device supports both half- and full-duplex 10Mbps and 100Mbps operation, and requires only a single 3.3V power supply. For low power applications the devices may be powered by a single 3.0V power supply. Advanced design techniques result in very low power requirements.

The LXT9784 also supports an auto-MDIX feature as well as an integrated Hardware Integrity (HWI) feature that utilizes a Time Domain Reflectometry (TDR) technique to locate and report problems with the cable plant.

Product Features

- Eight IEEE 802.3 Standard-compliant 10BASE-T or 100BASE-TX ports with integrated filters.
- Automatic MDI/MDIX switch over capability.
- Integrated Hardware Integrity (HWI): device ports detect and report cabling problems via MDIO.
- Uses 1:1 magnetic device for 10/100 Mbps operation, allowing low-cost design.
- Supports both IEEE 802.3u Auto-Negotiation and parallel detection operation.
- Controls all 8 ports through one single IEEE 802.3 Standard compliant MII management bus.
- Automatic polarity correction at 10M data rate.
- Robust baseline wander correction for improved 100BASE-TX performance.
- Eight Reduced MII (RMII) and Serial MII (SMII) ports for independent PHY port operation.
- Low power consumption, 3.0V and 3.3V operation.
- 324-lead PBGA package.
  - —LXT9784BC - Commercial (0° to 70°C ambient).
  - —LXT9784BE - Extended (-40° to 85°C ambient).

As of January 15, 2001, this document replaces the Level One document *LXT9784 Low-Power Octal PHY Datasheet.*

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Datasheet

Contents

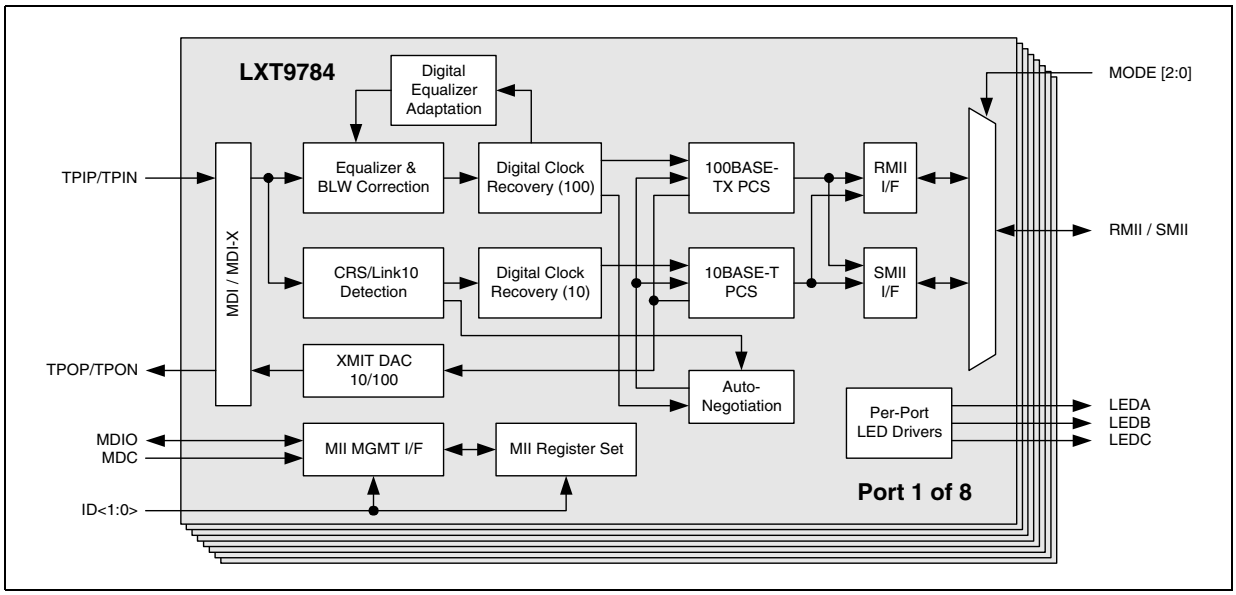
Figures

Tables

Revision History

Revision	Date	Description

Figure 1. LXT9784 Block Diagram



1.0 Pin Assignments and Signal Descriptions

Figure 2. LXT9784 Ball Assignments - RMII Mode

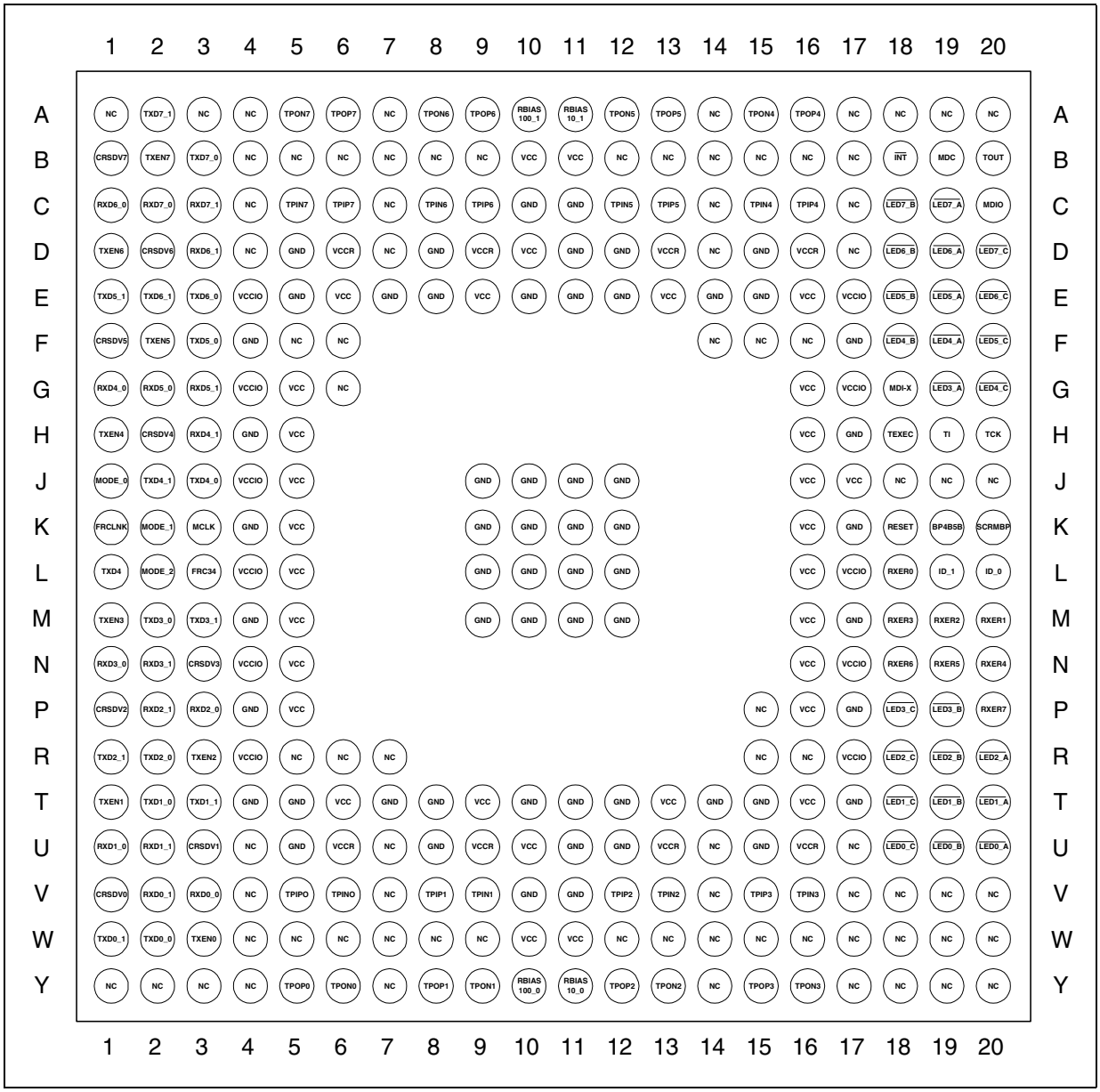


Figure 3. LXT9784 Ball Assignments - SMII Mode

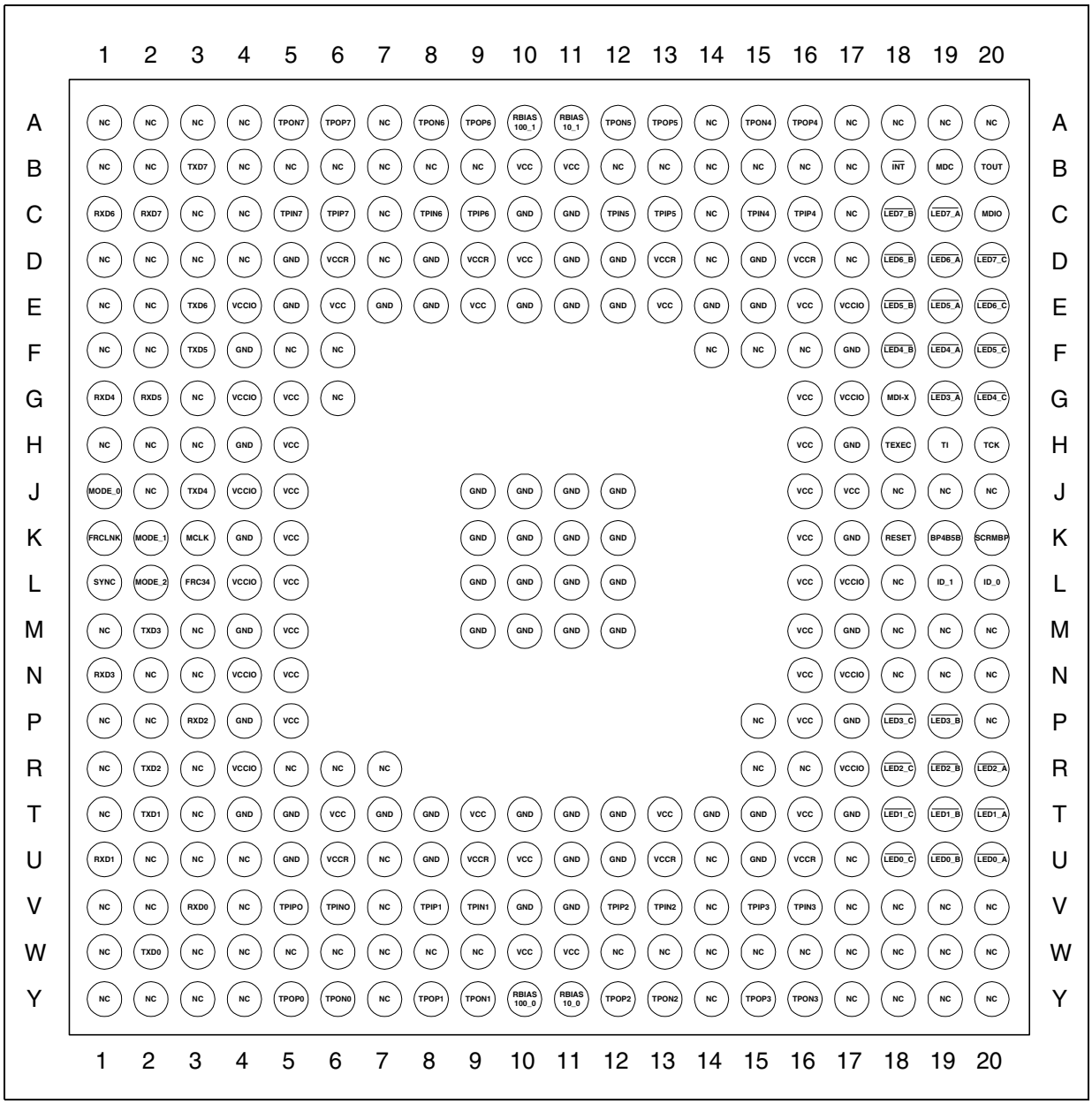


Table 1. Signal Types

Type	Name	Definition
I	Input	Standard input only signal.
O	Output	Standard output-only signal.
I/O	Bidirectional	This is an input and output ball.

Table 1. Signal Types

Type	Name	Definition
OD	Open-drain output	This open drain ball allows multiple devices to share this signal as a wired-ORed.
OZ	Tri-state output	High impedance
PU	Internal weak pull-up	Input ball, external pull-up device is not required.
PD	Internal weak pull-down	Input ball, external pull-down device is not required.
EPU	External pull up	Pull this ball up to 3.3V through a 10K ohm resistor.
EPD	External pull down	Pull this ball down to ground through a 10K ohm resistor.
MLT	Multi-level analog I/O	Presented on MDI balls while in 100M mode of operation.
A_PWR	Power (analog)	Connect the marked balls to separate analog planes.
NC	No Connect	This ball is not used and can be left floating.

Table 2. Numeric Pad Assignments

Ball	Symbol	Type[1]	Reference for Full Description
A1	-	NC	-
A2	TXD7_1 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	-
A3	-	NC	-
A4	-	NC	-
A5	TPON7	MLT	Table 3 on page 22
A6	TPOP7	MLT	Table 3 on page 22
A7	-	NC	-
A8	TPON6	MLT	Table 3 on page 22
A9	TPOP6	MLT	Table 3 on page 22
A10	RBIAS100_1	I	Table 7 on page 25
A11	RBIAS10_1	I	Table 7 on page 25
A12	TPON5	MLT	Table 3 on page 22
A13	TPOP5	MLT	Table 3 on page 22
A14	-	NC	-
A15	TPON4	MLT	Table 3 on page 22
A16	TPOP4	MLT	Table 3 on page 22
A17	-	NC	
A18	-	NC	-
A19	-	NC	-
A20	-	NC	-
B1	CRSDV7 (RMII)	O	Table 3 on page 22
	Not Used (SMII)	NC	-

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
B2	TXEN7 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
B3	TXD7_0 (RMII)	I	Table 9 on page 27
	TXD7 (SMII)	I	Table 9 on page 27
B4	-	NC	-
B5	-	NC	-
B6	-	NC	-
B7	-	NC	-
B8	-	NC	-
B9	-	NC	-
B10	VCC		Table 6 on page 24
B11	VCC		Table 6 on page 24
B12	-	NC	-
B13	-	NC	
B14	-	NC	
B15	-	NC	
B16	-	NC	
B17	-	NC	
B18	$\overline{\text{INT}}$	OD	Table 7 on page 25
B19	MDC	I	Table 4 on page 23
B20	TOUT	O	Table 7 on page 25
C1	RXD6_0 (RMII)	O	Table 8 on page 26
	RXD6 (SMII)	O	Table 9 on page 27
C2	RXD7_0 (RMII)	O	Table 8 on page 26
	RXD7 (SMII)	O	Table 9 on page 27
C3	RXD7_1 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
C4	-	NC	
C5	TPIN7	MLT	Table 3 on page 22
C6	TPIP7	MLT	Table 3 on page 22
C7	-	NC	
C8	TPIN6	MLT	Table 3 on page 22
C9	TPIP6	MLT	Table 3 on page 22
C10	GND		
C11	GND		
C12	TPIN5	MLT	Table 3 on page 22
C13	TPIP5	MLT	Table 3 on page 22

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
C14	-	NC	
C15	TPIN4	MLT	Table 3 on page 22
C16	TPIP4	MLT	Table 3 on page 22
C17	-	NC	
C18	$\overline{\text{LED7\_B}}$	O	Table 5 on page 23
C19	$\overline{\text{LED7\_A}}$	O	Table 5 on page 23
C20	MDIO	I/O	Table 4 on page 23
D1	TXEN6 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
D2	CRSDV6 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
D3	RXD6_1 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
D4	-	NC	
D5	GND		
D6	VCCR	A_PWR	
D7	-	NC	
D8	GND		
D9	VCCR	A_PWR	
D10	VCC		
D11	GND		
D12	GND		
D13	VCCR	A_PWR	
D14	-	NC	
D15	GND		
D16	VCCR	A_PWR	
D17	-	NC	
D18	$\overline{\text{LED6\_B}}$	O	Table 5 on page 23
D19	$\overline{\text{LED6\_A}}$	O	Table 5 on page 23
D20	$\overline{\text{LED7\_C}}$	O	Table 5 on page 23
E1	TXD5_1 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
E2	TXD6_1 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
E3	TXD6_0 (RMII)	I	Table 8 on page 26
	TXD6 (SMII)	I	Table 9 on page 27
E4	VCCIO		

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
E5	GND		
E6	VCC		
E7	GND		
E8	GND		
E9	VCC		
E10	GND		
E11	GND		
E12	GND		
E13	VCC		
E14	GND		
E15	GND		
E16	VCC		
E17	VCCIO		
E18	$\overline{\text{LED5\_B}}$	O	Table 5 on page 23
E19	$\overline{\text{LED5\_A}}$	O	Table 5 on page 23
E20	$\overline{\text{LED6\_C}}$	O	Table 5 on page 23
F1	CRSDV5 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
F2	TXEN5 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
F3	TXD5_0 (RMII)	I	Table 8 on page 26
	TXD5	I	Table 9 on page 27
F4	GND		
F5	-	NC	
F6	-	NC	
F14	-	NC	
F15	-	NC	
F16	-	NC	
F17	GND		
F18	$\overline{\text{LED4\_B}}$	O	Table 5 on page 23
F19	$\overline{\text{LED4\_A}}$	O	Table 5 on page 23
F20	$\overline{\text{LED5\_C}}$	O	Table 5 on page 23
G1	RXD4_0 (RMII)	O	Table 8 on page 26
	RXD4 (SMII)	O	Table 9 on page 27
G2	RXD5_0 (RMII)	O	Table 8 on page 26
	RXD5 (SMII)	O	Table 9 on page 27

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
G3	RXD5_1 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
G4	VCCIO		
G5	VCC		
G6	-	NC	
G16	VCC		
G17	VCCIO		
G18	MDI-X	I-PU	Table 7 on page 25
G19	$\overline{\text{LED3\_A}}$	O	Table 5 on page 23
G20	$\overline{\text{LED4\_C}}$	O	Table 5 on page 23
H1	TXEN4 (RMII)	I	Table 8 on page 26
	NC (SMII)	PD	
H2	CRSDV4 (RMII)	O	Table 8 on page 26
	NC (SMII)	PD	
H3	RXD4_1 (RMII)	O	Table 8 on page 26
	NC (SMII)	PD	
H4	GND		
H5	VCC		
H16	VCC		
H17	GND		
H18	TEXEC	I	Table 7 on page 25
H19	TI	I	Table 7 on page 25
H20	TCK	I	Table 7 on page 25
J1	MODE_0	I	Table 7 on page 25
J2	TXD4_1 (RMII)	I	Table 7 on page 25
	Not Used (SMII)	NC	
J3	TXD4_0 (RMII)	I	Table 8 on page 26
	TXD4 (SMII)	I	Table 9 on page 27
J4	VCCIO		Table 8 on page 26
J5	VCC		
J9	GND		
J10	GND		
J11	GND		
J12	GND		
J16	VCC		
J17	VCC		
J18	-	NC	

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
J19	-	NC	
J20	-	NC	
K1	FRCLNK	I-PD	Table 7 on page 25
K2	MODE_1	I	Table 7 on page 25
K3	MCLK	I	Table 7 on page 25
K4	GND		
K5	VCC		
K9	GND		
K10	GND		
K11	GND		
K12	GND		
K16	VCC		
K17	GND		
K18	RESET	I	Table 7 on page 25
K19	BP4B5B	I-PD	Table 7 on page 25
K20	SCRMBP	I-PD	Table 7 on page 25
L1	TXD4 (RMII)	I	Table 8 on page 26
	SYNC (SMII)	I	Table 9 on page 27
L2	MODE_2	Ext-PD	Table 7 on page 25
L3	FRC34	I-PD	Table 7 on page 25
L4	VCCIO		
L5	VCC		
L9	GND		
L10	GND		
L11	GND		
L12	GND		
L16	VCC		
L17	VCCIO		
L18	RXER0 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
L19	ID_1	I-PD	Table 7 on page 25
L20	ID_0	I-PD	Table 7 on page 25
M1	TXEN3 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
M2	TXD3_0 (RMII)	I	Table 8 on page 26
	TXD3 (SMII)		Table 9 on page 27

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
M3	TXD3_1 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
M4	GND		
M5	VCC		
M9	GND		
M10	GND		
M11	GND		
M12	GND		
M16	VCC		
M17	GND		
M18	RXER3	O	Table 8 on page 26
M19	RXER2	O	Table 8 on page 26
M20	RXER1	O	Table 8 on page 26
N1	RXD3_0 (RMII)	O	Table 8 on page 26
	RXD3 (SMII)	O	Table 9 on page 27
N2	RXD3_1 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
N3	CRSDV3 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
N4	VCCIO		
N5	VCC		
N16	VCC		
N17	VCCIO		
N18	RXER6 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
N19	RXER5 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
N20	RXER4 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
P1	CRSDV2 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
P2	RXD2_1 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
P3	RXD2_0	O	Table 8 on page 26
	RXD2	O	Table 8 on page 26
P4	GND		
P5	VCC		

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
P15	-	NC	
P16	VCC		
P17	GND		
P18	LED3_C	O	Table 5 on page 23
P19	LED3_B	O	Table 5 on page 23
P20	RXER7	O	Table 8 on page 26
R1	TXD2_1 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
R2	TXD2_0 (RMII)	I	Table 8 on page 26
	TXD2 (SMII)	I	Table 9 on page 27
R3	TXEN2 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
R4	VCCIO		Table 8 on page 26
R5	-	NC	
R6	-	NC	
R7	-	NC	
R15	-	NC	
R16	-	NC	
R17	VCCIO		
R18	LED2_C	O	Table 5 on page 23
R19	LED2_B	O	Table 5 on page 23
R20	LED2_A	O	Table 5 on page 23
T1	TXEN1 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
T2	TXD1_0 (RMII)	I	Table 8 on page 26
	TXD1 (SMII)	I	Table 9 on page 27
T3	TXD1_1 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
T4	GND		
T5	GND		
T6	VCC		
T7	GND		
T8	GND		
T9	VCC		
T10	GND		
T11	GND		
T12	GND		

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
T13	VCC		
T14	GND		
T15	GND		
T16	VCC		
T17	GND		
T18	$\overline{\text{LED1\_C}}$	O	Table 5 on page 23
T19	$\overline{\text{LED1\_B}}$	O	Table 5 on page 23
T20	$\overline{\text{LED1\_A}}$	O	Table 5 on page 23
U1	RXD1_0 (RMII)	O	Table 8 on page 26
	RXD1 (SMII)	O	Table 9 on page 27
U2	RXD1_1 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
U3	CRSDV1 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
U4	-	NC	
U5	GND		
U6	VCCR	A_PWR	
U7	-	NC	
U8	GND		
U9	VCCR	A_PWR	
U10	VCC		
U11	GND		
U12	GND		
U13	VCCR	A_PWR	
U14	-	NC	
U15	GND		
U16	VCCR	A_PWR	
U17	-	NC	
U18	$\overline{\text{LED0\_C}}$	O	Table 5 on page 23
U19	$\overline{\text{LED0\_B}}$	O	Table 5 on page 23
U20	$\overline{\text{LED0\_A}}$	O	Table 5 on page 23
V1	CRSDV0 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
V2	RXD0_1 (RMII)	O	Table 8 on page 26
	Not Used (SMII)	NC	
V3	RXD0_0 (RMII)	O	Table 8 on page 26
	RXD0 (SMII)	O	Table 9 on page 27

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
V4	-	NC	
V5	TPIP0	MLT	Table 3 on page 22
V6	TPIN0	MLT	Table 3 on page 22
V7	-	NC	
V8	TPIP1	MLT	Table 3 on page 22
V9	TPIN1	MLT	Table 3 on page 22
V10	GND		
V11	GND		
V12	TPIP2	MLT	Table 3 on page 22
V13	TPIN2	MLT	Table 3 on page 22
V14	-	NC	
V15	TPIP3	MLT	Table 3 on page 22
V16	TPIN3	MLT	Table 3 on page 22
V17	-	NC	
V18	-	NC	
V19	-	NC	
V20	-	NC	
W1	TXD0_1 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	
W2	TXD0_0 (RMII)	I	Table 8 on page 26
	TXD0 (SMII)	I	Table 9 on page 27
W3	TXEN0 (RMII)	I	Table 8 on page 26
	Not Used (SMII)	NC	-
W4	-	NC	-
W5	-	NC	-
W6	-	NC	-
W7	-	NC	-
W8	-	NC	-
W9	-	NC	-
W10	VCC		-
W11	VCC		-
W12	-	NC	-
W13	-	NC	-
W14	-	NC	-
W15	-	NC	-
W16	-	NC	-
W17	-	NC	-

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 2. Numeric Pad Assignments (Continued)

Ball	Symbol	Type[1]	Reference for Full Description
W18	-	NC	-
W19	-	NC	-
W20	-	NC	-
Y1	-	NC	-
Y2	-	NC	-
Y3	-	NC	-
Y4	-	NC	
Y5	TPOP0	MLT	Table 3 on page 22
Y6	TPON0	MLT	Table 3 on page 22
Y7	-	NC	
Y8	TPOP1	MLT	Table 3 on page 22
Y9	TPON1	MLT	Table 3 on page 22
Y10	RBIAS100_0	I	Table 7 on page 25
Y11	RBIAS10_0	I	Table 7 on page 25
Y12	TPOP2	MLT	Table 3 on page 22
Y13	TPON2	MLT	Table 3 on page 22
Y14	-	NC	
Y15	TPOP3	MLT	Table 3 on page 22
Y16	TPON3	MLT	Table 3 on page 22
Y17	-	NC	-
Y18	-	NC	-
Y19	-	NC	-
Y20	-	NC	-

1. Refer to Table 1 on page 11 for Signal Type definitions.

Table 3. Network Interface Signal Descriptions

Ball ID	Signal Name	Type[1]	Signal Description
Y5, Y6	TPOP0, TPON0	MLT	**Transmit Differential Pair, Ports 0-7.** These pins transmit the serial bit-stream on an unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T mode (Manchester) or a three-level signal in 100BASE-TX mode (MLT-3). These signals interface directly with an isolation transformer.
Y8, Y9	TPOP1, TPON1		
Y12, Y13	TPOP2, TPON2		
Y15, Y16	TPOP3, TPON3		
A16, A15	TPOP4, TPON4		
A13, A12	TPOP5, TPON5		
A9, A8	TPOP6, TPON6		
A6, A5	TPOP7, TPON7		

1. Refer to Table 1 on page 11 for Signal Type Definitions.

Table 3. Network Interface Signal Descriptions (Continued)

Ball ID	Signal Name	Type[1]	Signal Description
V5, V6	TPIP0, TPIN0	MLT	**Receive Differential Pair, Ports 0-7.** These pins receive the serial bit-stream on an unshielded twisted pair (UTP) cable. The differential pair is a two-level signal in 10BASE-T mode (Manchester) or a three-level signal in 100BASE-TX mode (MLT-3). These signals interface directly with an isolation transformer.
V8, V9	TPIP1, TPIN1		
V12, V13	TPIP2, TPIN2		
V15, V16	TPIP3, TPIN3		
C16, C15	TPIP4, TPIN4		
C13, C12	TPIP5, TPIN5		
C9, C8	TPIP6, TPIN6		
C6, C5	TPIP7, TPIN7		
1. Refer to Table 1 on page 11 for Signal Type Definitions.			

Table 4. MDIO Signal Descriptions

Ball ID	Signal Name	Type[1]	Signal Description
C20	MDIO	I/O	**Management Data Input/Output.** The MDIO signal is a bi-directional data pin for the Management Data Interface. When this signal is not used, a pull-up resistor is required.
B19	MDC	I	**Management Data Clock.** The MDC signal functions as a clock reference for the MDIO signal. MDC can operate at a maximum frequency of 3 MHz. When this signal is not used, a pull-up resistor is required.
1. Refer to Table 1 on page 6 for Signal Type Definitions.			

Table 5. LED Signal Descriptions

Ball ID	Signal Name	Type[1]	Signal Description
U20	$\overline{\text{LED0\_A}}$	O	**Link/Activity LED, Ports 0-7.** With a good link the output is Low. The output blinks at a rate related to the utilization.
T20	$\overline{\text{LED1\_A}}$		
R20	$\overline{\text{LED2\_A}}$		
G19	$\overline{\text{LED3\_A}}$		
F19	$\overline{\text{LED4\_A}}$		
E19	$\overline{\text{LED5\_A}}$		
D19	$\overline{\text{LED6\_A}}$		
C19	$\overline{\text{LED7\_A}}$		
1. O = Output. Refer to Table 1 for additional Signal Type Definitions.			

Table 5. LED Signal Descriptions (Continued)

Ball ID	Signal Name	Type[1]	Signal Description
U19	LED0_B	O	**Speed LED, Ports 0-7.** Indicates speed of operation. The output is Low for 100 Mbps, and High for 10 Mbps.
T19	LED1_B		
R19	LED2_B		
P19	LED3_B		
F18	LED4_B		
E18	LED5_B		
D18	LED6_B		
C18	LED7_B		
U18	LED0_C	O	**Collision LED, Ports 0-7.** When in RMII or SMII modes of operation, the output blinks Low with collisions stretch rate of 10 ms.
T18	LED1_C		
R18	LED2_C		
P18	LED3_C		
G20	LED4_C		
F20	LED5_C		
E20	LED6_C		
D20	LED7_C		

1. O = Output. Refer to Table 1 for additional Signal Type Definitions.

Table 6. Power Supply Signal Descriptions

Ball ID	Symbol	Type	Signal Description
D6, D9, D13, D16, U6, U9, U13, U16	VCCR	Analog	**Receiver Power Supply.** +3.3V supply for core analog circuits.
E4, E17, G4, G17, J4, L4, L17, N4, N17, R4, R17	VCCI/O	Digital	**I/O Power Supply.** +3.3V supply for core digital circuits.
B10, B11, D10, E6, E9, E13, E16, G5, G16, H5, H16, J5, J16, J17, K5, K16, L5, L16, M5, M16, N5, N16, P5, P16, T6, T9, T13, T16, U10, W10, W11	VCC	A/D	**Primary Power Supply.** +3.3V supply for all circuits except Receiver and I/O.
C10, C11, D8, D5, D11, D12, D15, E5, E7, E8, E10,E11,E12, E14, E15, F4, F17, H4, H17, J9, J10, J11, J12, K4, K9, K10, K11, K12, K17, L9, L10, L11, L12, M4, M9, M10, M11, M12, M17, P4, P17, T4, T5, T7, T8, T10,T11, T12, T14, T15, T17, U5, U8, U11, U12, U15, V10, V11	GND	Return	Ground. Power supply return.

Table 7. Miscellaneous Signal Descriptions

Ball ID	Signal Name	Type[1]	Description
Y11, A11	RBIAS10_0 RBIAS10_1	B	**Bias Reference Resistor 10.** A 464 Ω 1% resistor should be connected from this pin to ground. This determines the current source in 10M mode.
Y10, A10	RBIAS100_0 RBIAS100_1	B	**Bias Reference Resistor 100.** A 619 Ω 1% resistor should be connected from this pin to ground. This determines the current source in 100M mode.
K3	MCLK	I	**Master Clock.** The LXT9784 master input clock, 35/65 duty cycle, ±50ppm. The MCLK frequency varies, based on the mode. Mode is set by the MODE<2:0> pins. In RMII mode, MODE<2:0> = 001, MCLK = 50 MHz In SMII mode, MODE<2:0> = 010, MCLK = 125 MHz
K18	RESET	I	**Reset.** The Reset signal is active high and resets the LXT9784. A reset pulse width of at least 500µs should be used.
J1, K2, L2	MODE_0 MODE_1 MODE_2	I	**Mode of Operation.** Sets the LXT9784 mode of operation. See Table 10.
L20, L19	ID_0 ID_1	I-PD	**ID.** Sets the two most significant bits of the PHY addresses. The ID<1:0> pins are used to set the PHY addresses for accessing the PHY registers through the MII management interface.
B18	$\overline{INT}$	OD	**Link Status Interrupt.** The Link status change interrupt line.
K19	BP4B5B	I-PD	**4B5B encoder Bypass.** If BP4B5B is high, the 4B5B encoder / 5B4B decoder will be bypassed in 100 Mbps mode of operation.
K20	SCRMBP	I-PD	**Scrambler/Descrambler Bypass.** If SCRMBP is high, the scrambler/ descrambler of TP-PMD will be bypassed in 100 Mbps mode of operation.
K1	FRCLNK	I-PD	**Force Link.** When high, force good link at speed of operation.
L3	FRC34	I-PD	**Force 34 Pattern.** When high, force the 34 pattern in 100M only.
G18	MDI-X	I-PU	**MDI-X Enable.** When high, enable the MDI/MDI-X automatic detection and switch-over feature.
H19	TI	I	**Test Input.** Sets the device into manufacturing test mode (MODE<2:0>=”111”). Should be externally pulled low when not in use.
H18	TEXEC	I	**Test Execute Command.** Sets the device into async test mode (MODE<2:0>=”111”). Should be externally pulled low when not in use.
H20	TCK	I	**Test Clock.** The test clock signal. Should be externally pulled low when not in use.
B20	TOUT	O	**Test Output.** The test output port.

1. Refer to Table 1 on page 11 for Signal Type Definitions.

Table 8. RMII Mode Signal Descriptions

Ball ID	Signal Name	Type[1]	Signal Description
V1	CRSDV0	O	**Carrier Sense / Receive Data Valid, Ports 0-7.** CRS and RXDV signals of the MII interface are collapsed into one signal. This signal indicates to the LXT9784 that traffic is present on the link, and that the incoming data on the RXD<1:0> pins is valid.
U3	CRSDV1		
P1	CRSDV2		
N3	CRSDV3		
H2	CRSDV4		
F1	CRSDV5		
D2	CRSDV6		
B1	CRSDV7		
L18	RXER0	O	**Receive Error, Ports 0-7.** The RXER signal indicates to the LXT9784 that an error has occurred during frame reception.
M20	RXER1		
M19	RXER2		
M18	RXER3		
N20	RXER4		
N19	RXER5		
N18	RXER6		
P20	RXER7		
V2, V3	RXD0_1, RXD0_0	O	**Receive Data, Ports 0-7.** In 100 Mbps and 10 Mbps mode, data is transferred across these two lines.
U2, U1	RXD1_1, RXD1_0		
P2, P3	RXD2_1, RXD2_0		
N2, N1	RXD3_1, RXD3_0		
H3, G1	RXD4_1, RXD4_0		
G3, G2	RXD5_1, RXD5_0		
D3, C1	RXD6_1, RXD6_0		
C3, C2	RXD7_1, RXD7_0		
W1, W2	TXD0_1, TXD0_0	I	**Transmit Data, Ports 0-7.** In 100 Mbps and 10 Mbps mode, data is transferred across these two lines
T3, T2	TXD1_1, TXD1_0		
R1, R2	TXD2_1, TXD2_0		
M3, M2	TXD3_1, TXD3_0		
J2, J3	TXD4_1, TXD4_0		
E1, F3	TXD5_1, TXD5_0		
E2, E3	TXD6_1, TXD6_0		
A2, B3	TXD7_1, TXD7_0		

1. Refer to Table 1 on page 11 for Signal Type Definitions.

Table 8. RMII Mode Signal Descriptions (Continued)

Ball ID	Signal Name	Type[1]	Signal Description
W3	TXEN0	I	**Transmit Enable, Ports 0-7.** The transmit enable signal indicates to the LXT9784 that valid data is present on the TXD[1:0] pins of the appropriate port.
T1	TXEN1		
R3	TXEN2		
M1	TXEN3		
H1	TXEN4		
F2	TXEN5		
D1	TXEN6		
B2	TXEN7		
L1	TXD4	I	**Fifth Transmit Data Bit.** When the LXT9784 is in a 4B5B by-pass mode, the TXD4 pin is used as the fifth transmit data bit of all eight ports. This signal allows for limited symbol interface functionality.
1. Refer to Table 1 on page 11 for Signal Type Definitions.			

Table 9. SMII Mode Signal Descriptions

Ball ID	Signal Name	Type[1]	Signal Description
V3	RXD0	O	**Receive Data and Control, Ports 0-7.** Receive data stream, that contains all of the information found on the receive path of the standard MII.
U1	RXD1		
P3	RXD2		
N1	RXD3		
G1	RXD4		
G2	RXD5		
C1	RXD6		
C2	RXD7		
W2	TXD0	I	**Transmit Data and Control, Ports 0-7.** Transmit data stream, that contains all of the information found on the transmit path of the standard MII.
T2	TXD1		
R2	TXD2		
M2	TXD3		
J3	TXD4		
F3	TXD5		
E3	TXD6		
B3	TXD7		
L1	SYNC	I	**Synchronization.** Defines the SMII segment boundaries.
1. Refer to Table 1 on page 11 for Signal Type Definitions.			

Table 10. Unused Pins

Ball ID	Symbol	Type	Description
A1,A3,A4,A7,A14,A17,A18,A,19,A20, B4,B5,B6,B7,B8,B9,B12,B13,B14,B15, B16,B17,C4,C7,C14,C17,D4,D7,D14, D17,F5,F6,F14,F15,F16,G6,J18,J19,J20, P15,R5,R6,R7,R15,R16,U4,U7,U14,U17,V4, V7, V14, V17,V18,V19,V20,W4,W5,W6, W7,W8,W9,W12,W13,W14,W15,W16, W17,W18,W19,W20,Y1,Y2,Y3,Y4,Y7, Y14,Y17,Y18,Y19,Y20.	NC	**RMII** Mode	No Connection- These pins are not used in RMII mode and should not be connected.
A1,A2,A3,A4,A7,A14,A17,A18,A,19, A20,B1,B2,B4,B5,B6,B7,B8,B9,B12,B13, B14,B15,B16,B17,C3,C4,C7,C14,C17, D1,D2,D3,D4,D7,D14,D17,E1,E2,F1,F2, F5,F6,F14,F15,F16,G3,G6,J2,J18,J19,J20,L18,M1,M 3,N2,N3,N18,N19,N20,P1,P2, P15,R1,R3,R5,R6,R7,R15,R16,T1,T3,U2,U4,U7,U14, U17,V1,V2,V4,V7, V14, V17,V18,V19,V20,W1,W3,W4,W5,W6,W7, W8, W9,W12,W13,W14,W15,W16, W17,W18,W19,W20,Y1,Y2,Y3,Y4,Y7, Y14,Y17,Y18,Y19,Y20.	NC	**SMII** Mode	No Connection- These pins are not used in SMII mode and should not be connected.

2.0 Functional Description

2.1 Introduction

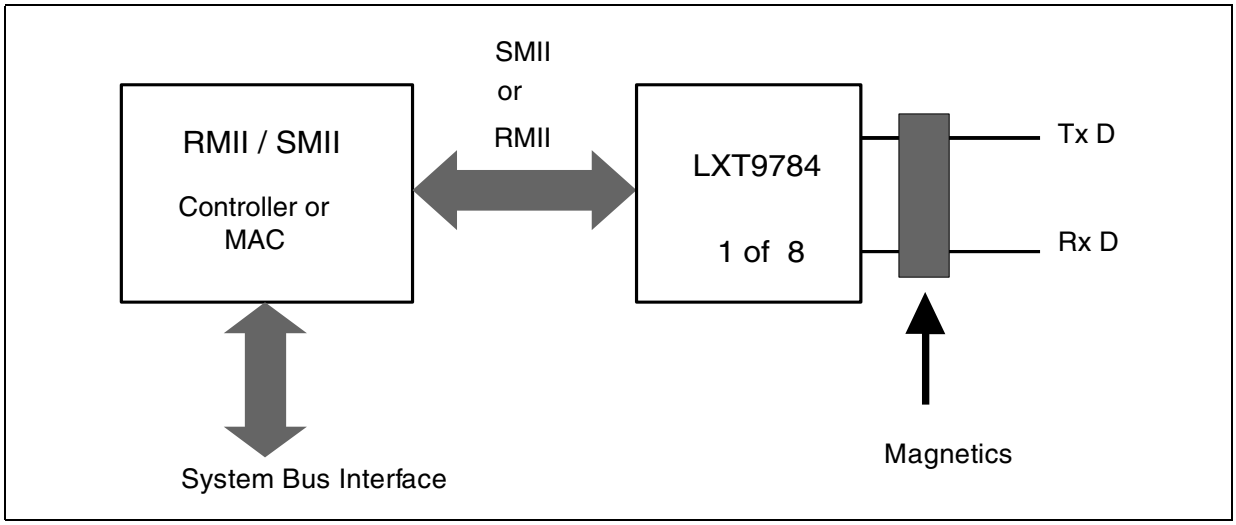
The LXT9784 is a single chip transceiver device containing eight independent 10/100 Ethernet transceivers with RMII and/or SMII Interfaces. The LXT9784 supports per-port speed auto-configuration. Each of the eight PHYs represents a highly-integrated, physical-layer interface solution designed for 10Mbps and/or 100 Mbps Ethernet systems based on the IEEE 802.3 Standard 10BASE-T and 100BASE-TX specifications.

100BASE-TX is an IEEE 802.3 Standard physical layer specification for use over two pairs of Category 5 unshielded twisted-pair (UTP CAT 5) or Type 1 shielded twisted pair (STP Type 1) cable. 100BASE-TX defines a signaling scheme not only for 100 Mbps, but also provides CSMA/CD compatibility with the 10Mbps IEEE 802.3 Standard 10BASE-T signaling standard.

Each PHY of the LXT9784 complies with the IEEE 802.3u Auto-Negotiation section, and with the IEEE 802.3x Full- Duplex Flow Control section. The interface to each PHY complies with the current RMII and SMII specifications.

The LXT9784 PHYs incorporate all active circuitry required to interface 10/100 Mbps Ethernet controllers and CSMA/CD MAC components to 100BASE-TX and 10BASE-T networks. Each PHY supports a direct glue less interface to all standard RMII or SMII components. Figure 4 shows how the LXT9784 PHY fits into a typical 10/100 Mbps Ethernet switch design.

Figure 4. LXT9784 PHY in a 10/100 Mbps Ethernet Solution



2.2 LXT9784 Configuration

The LXT9784 has a common Management Data Interface (MDI) for the eight PHYs. This is a serial interface and complies with the IEEE 802.3Standard MII for MDC and MDIO signals. In all modes of operation the PHYs can be configured individually using the MII management interface.

The PHYs can individually auto-negotiate with their link partners, and thereby auto-configure their speeds of operation. The MDI/MDIX auto-switching configuration is done prior to Auto-Negotiation.

The RMII or SMII mode is selected by mode select balls MODE<2:0>.

Three balls select the general operation of the device. Table 11 shows the balls settings for the different modes of operation.

Table 11. LXT9784 Modes of Operation

Mode Pins			MII Mode	MCLK Frequency
2[1]	1	0		
0	0	0	Reserved	
0	**0**	**1**	**RMII**	**50 MHz**
0	**1**	**0**	**SMII**	**125 MHz**
0	1	1	Reserved	
1	0	0	Reserved	
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Manufacturing Test Mode	

1. MODE 2 pin must be set to zero for normal operation.

2.3 100BASE-TX Mode

2.3.1 100BASE-TX Receiver

Each receive subsection of the LXT9784 PHYs accepts 100BASE-TX MLT-3 data on TPIP*n* and TPIN*n* (where "*n*" is the port number). Due to the advanced digital signal processing design techniques employed, the PHYs accurately receive valid data from CAT5 UTP and type 1 STP cable over distances well in excess of 100 meters.

2.3.1.1 Digital Adaptive Equalizer

The distorted MLT-3 signal at the end of the wire is restored by the equalizer. The equalizer filter coefficients are digitally adapted based on the shape of the received signal, equalizing the signal to exceed IEEE specification bit error rate (BER) performance for transmission over 100 meters of CAT 5 twisted pair.

2.3.1.2 Receive Clock and Data Recovery

The clock recovery circuit uses advanced DSP technology to compensate for signal distortion and jitter. The circuitry recovers the 125 MHz clock and data from the equalizer output and presents the data to the NRZI-to-NRZ converter.

2.3.1.3 Baseline Wander Correction

The baseline wander effect is the wandering of the DC offset of the receive signal. The wander of the DC offset happens when the 100BASE-TX data is not DC-balanced. Baseline wander can greatly reduce BER performance. The LXT9784 Equalizer has an automatic baseline wander correction circuit, thereby preserving outstanding BER performance in case of extreme baseline wander conditions.

2.3.1.4 Decoder

The LXT9784 PHYs first convert the data from the clock recovery circuitry to NRZ format. The NRZ serial data stream is assembled to 5-bit symbols, de-scrambled and aligned to symbol boundaries. The de-scrambling is based on synchronization to the transmitted Idle pattern generated by an 11-bit LFSR during idle. The data is then decoded at the 5B/4B decoder.

2.3.1.5 100BASE-TX Receive Framing

The LXT9784 PHYs do not differentiate between the fields of the MAC frame containing preamble, SFD, data and CRC. During 100 Mbps reception, the PHY detects Start-of-Stream Delimiter (SSD) (/J/K/) and End-of-Stream Delimiter ESD) (/T/R/) pairs. The PHY strips those symbols from the data stream before passing the packet to the MAC. CRSDV*n* is asserted on a detection of a non-idle symbol.

2.3.1.6 100BASE-TX RMII Data Reception

When the receive medium is idle, CRSDV*n* is de-asserted and the data on RXD*n*_<1:0> is “00”. When carrier is detected, CRSDV*n* signal asserts asynchronously. After the internal FIFO is half full, the PHY transfers two bits of recovered data on RXD*n*_<1:0> at each clock period, synchronous to MCLK.

If the PHY has additional bits to present on RXD*n*_<1:0> (accumulated in the FIFO) after CRSDV*n* initial de-assertion, then CRSDV*n* toggles at 25 MHz, starting on a nibble boundary.

See Figure 5

If false carrier is detected (bad SSD), then RXD*n*_<1:0> will be “10” until the end of the receive event. See Figure 6.

2.3.1.7 100BASE-TX SMII Data Reception

The data is signaled in ten-bit segments, where each segment represents a new byte of data. Each segment is delimited by a SYNC pulse (every 10 clocks).

RXD_[7:0] in the serial bit stream are used to convey packet data, receive error status from the previous frame, and PHY status, decoded by two SMII control bits (CRS and RX_DV). See Table 12 for bit definitions. Figure 7 shows the SMII receive data stream.

When the receive medium is busy receiving a frame, SMII control bit CRS is asserted. RX_ER (inter-frame status bit RXD0) is asserted if during a frame reception the internal FIFO overflows or underflows.

If false carrier is detected (bad Start-of-Stream Delimiter), then inter-frame status bit RXD6 is asserted.

2.3.1.8 100BASE-TX Receive Error Detection and Reporting

In 100BASE-TX mode, the PHYs detect errors in the receive data in a number of ways. Any of the following conditions is considered an error:

- If the SSD ("JK") symbol is not fully detected after idle
- If an invalid symbol is detected at the 4B/5B decoder
- If IDLE is detected in the middle of a frame (before "TR" symbol pair are detected)

When any of the above error conditions occurs, the PHY immediately indicates a receive error for reception. In RMII mode the PHY asserts RXER*n*, and in SMII mode the PHY asserts the RXD_0 status bit.

Figure 5. RMII Data Reception

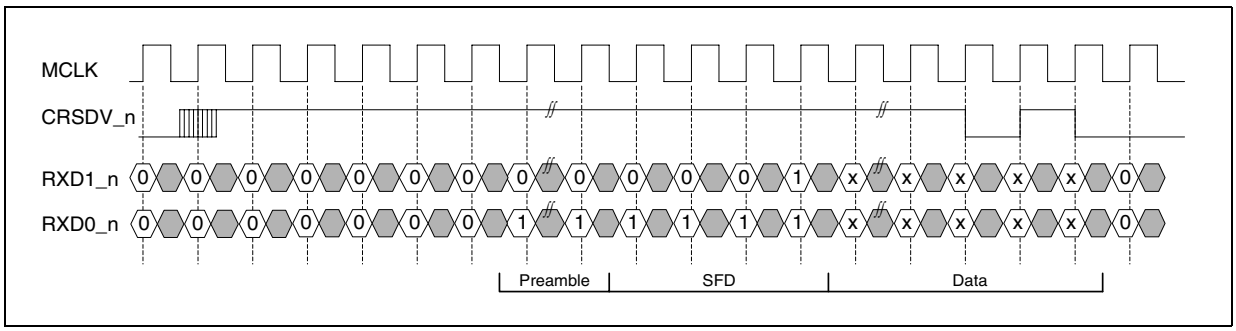


Figure 6. False Carrier Detect

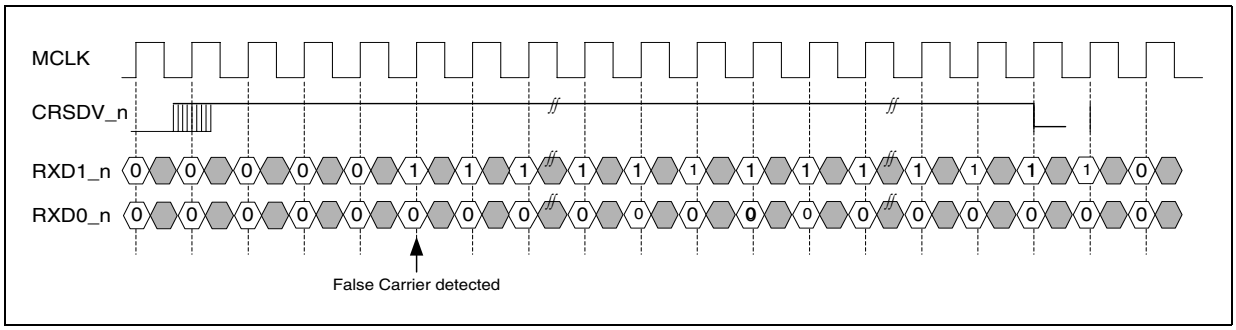
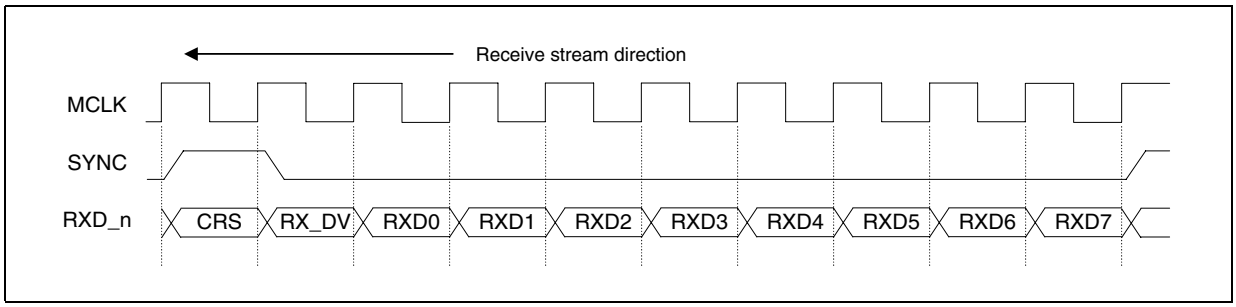


Table 12. SMII RXD_[7:0] Contents

CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
X	O	receive error status, from previous frame	Speed 0 = 10Mbps 1=100Mbps	Duplex 0=down 1 = up	Link 0=down 1 = up	Jabber 0 =OK 1=error	Upper Nibble 0 = invalid 1 = valid	False Carrier Detect	1
X	1	One Data Byte (two MII data nibbles)							

Figure 7. SMII Received Serial Data Stream



2.3.2 100BASE-TX Transmitter

The transmit subsection of the LXT9784 PHY device accepts di-bit data on TXD*n*_[1:0] (RMII interface) or serial stream data on TXD*n* (SMII interface) while TXEN*n* is asserted (High). The data is assembled into nibbles and passed to the 4B/5B encoder as long as TXEN*n* is active.

The 4B/5B encoder compiles the data into 5-bit-wide parallel symbols. These symbols are scrambled and serialized into a 125 Mbps bit stream, converted by the analog transmit driver into an MLT-3 waveform format, and transmitted onto the unshielded twisted pair (UTP) or Type 1 shielded twisted pair (STP) wire.

2.3.2.1 100BASE-TX 4B/5B Encoder

The 4B/5B encoder complies with the IEEE 802.3u 100BASE-TX standard. Four bits at a time are accepted and encoded according to the TX 4B/5B look-up table. The lookup table matches a 5-bit code to each 4-bit code. Refer to Table 12.

2.3.2.2 100BASE-TX Scrambler and MLT-3 Encoder

Data is scrambled in 100BASE-TX to reduce electromagnetic emissions during long transmissions of high-frequency data codes. The scrambler logic accepts 5 bits from the 4B/5B encoder block, then presents scrambled data to the MLT-3 encoder. The LXT9784 PHYs implement the 11-bit Stream Cipher scrambler as adopted by the ANSI XT3T9.5 committee for unshielded twisted-pair operation. The cipher equation used is: X[n] = X[n-11] + X[n-9] (mod 2).

The encoder receives the scrambled NRZ data stream from the scrambler and encodes the stream into MLT-3 for presentation to the driver. MLT3 is similar to NRZI coding, but three levels are output instead of two. There are three output levels +, 0 and -. When an NRZ “0” arrives at the input of the encoder, the last output level is maintained unchanged (either +, 0 or -) When an NRZ “1” arrives at the input of the encoder, the output steps to the next level. The order of steps is “-,0,+,0,-,0...” See Figure 8.

Figure 8. NRZ to MLT-3 encoding diagram

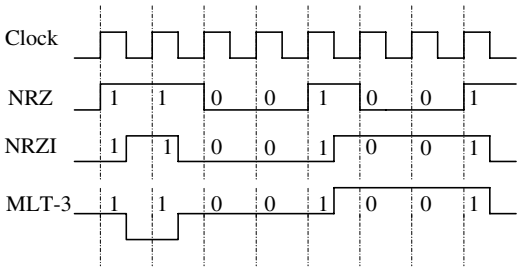


Table 13. 4B/5B Coding

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
	0 0 0 0	0	1 1 1 1 0	Data 0
	0 0 0 1	1	0 1 0 0 1	Data 1
	0 0 1 0	2	1 0 1 0 0	Data 2
	0 0 1 1	3	1 0 1 0 1	Data 3
	0 1 0 0	4	0 1 0 1 0	Data 4
	0 1 0 1	5	0 1 0 1 1	Data 5
	0 1 1 0	6	0 1 1 1 0	Data 6
DATA	0 1 1 1	7	0 1 1 1 1	Data 7
	1 0 0 0	8	1 0 0 1 0	Data 8
	1 0 0 1	9	1 0 0 1 1	Data 9
	1 0 1 0	A	1 0 1 1 0	Data A
	1 0 1 1	B	1 0 1 1 1	Data B
	1 1 0 0	C	1 1 0 1 0	Data C
	1 1 0 1	D	1 1 0 1 1	Data D
	1 1 1 0	E	1 1 1 0 0	Data E
	1 1 1 1	F	1 1 1 0 1	Data F
IDLE	undefined	I [1]	1 1 1 11	Idle. Used as inter-stream fill code
	0 1 0 1	J [2]	1 1 0 0 0	Start-of-Stream Delimiter (SSD), part 1 of 2
CONTROL	0 1 0 1	K [2]	1 0 0 0 1	Start-of-Stream Delimiter (SSD), part 2 of 2
	undefined	T [3]	0 1 1 0 1	End-of-Stream Delimiter (ESD), part 1 of 2
	undefined	R [3]	0 0 1 1 1	End-of-Stream Delimiter (ESD), part 2 of 2
	undefined	H [4]	0 0 1 0 0	Transmit Error. Used to force signaling errors
	undefined	Invalid	0 0 0 0 0	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

Table 13. 4B/5B Coding (Continued)

Code Type	4B Code 3 2 1 0	Name	5B Code 4 3 2 1 0	Interpretation
	undefined	Invalid	0 0 0 0 1	Invalid
	undefined	Invalid	0 0 0 1 0	Invalid
INVALID	undefined	Invalid	0 0 0 1 1	Invalid
	undefined	Invalid	0 0 1 0 1	Invalid
	undefined	Invalid	0 1 0 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	0 1 1 0 0	Invalid
	undefined	Invalid	1 0 0 0 0	Invalid
	undefined	Invalid	1 1 0 0 1	Invalid

1. The /I/ (Idle) code group is sent continuously between frames.
2. The /J/ and /K/ (SSD) code groups are always sent in pairs; /K/ follows /J/.
3. The /T/ and /R/ (ESD) code groups are always sent in pairs; /R/ follows /T/.
4. An /H/ (Error) code group is used to signal an error condition.

2.3.2.3 Transmit Driver

The TPOP*n* and TPON*n* lines are implemented with a highly slope-controlled driver that meets the TP-PMD specifications. The driver either sinks, floats, or drives the TPOP*n* and TPON*n* outputs with 20 ma of current, depending on whether the ternary signal is -1, 0, or +1. The magnetics external to the LXT9784 converts this current to voltage levels of 2.0 Vptp, as required by the TP-PMD specification.

There are four inputs (RBIAS10_0, RBIAS10_1, and RBIAS100_0, RBIAS100_1) to the LXT9784 that must have external resistor connections to set up voltage biases for the internal analog section of the LXT9784 PHYs. RBIAS10_0 and RBIAS100_0 provide the bias for PHYs 0 through 3. RBIAS10_1 and RBIAS100_1 provide the bias for PHYs 4 through 7.

2.3.2.4 100BASE-TX Transmit Framing

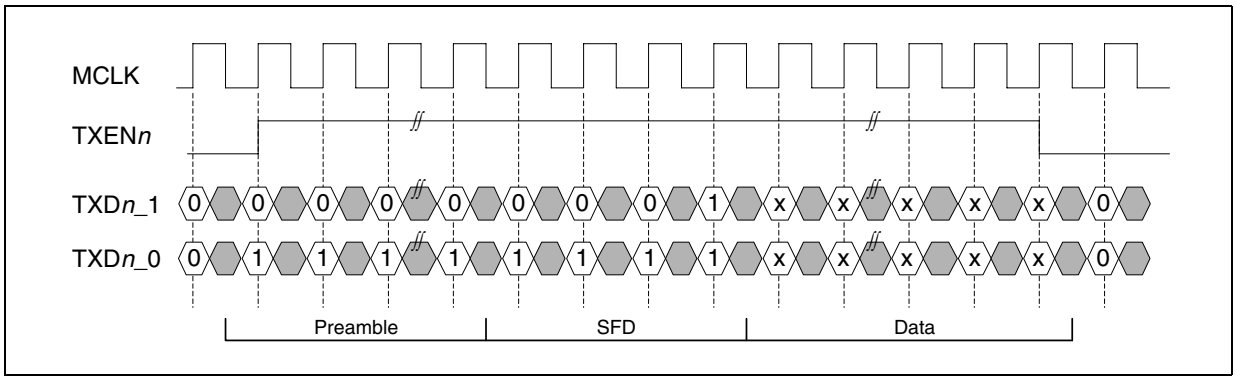
The LXT9784 PHYs do not differentiate between the fields of the MAC frame containing preamble, SFD, data and CRC. When TXEN*n* is asserted, the PHY accepts di-bit data on the RMII TXD*n*_[1:0] lines, or serial stream data on the SMII TXD*n* line.

The PHY encodes the data, and sends it out onto the wire. The PHY substitutes the first byte of the preamble with the "JK" symbol pair, encodes all other pieces of data according to the 4B/5B lookup table, and adds the "TR" code after the end of the packet (de-assertion of TXEN*n* transmit enable indication). The PHY scrambles and serializes the data into a 125 Mbps stream, encodes it as MLT-3, and drives it onto the wire. If TXER bit in the SMII control word is asserted while TXEN*n* bit is active, the LXT9784 transmits an invalid "H" symbol.

100BASE-TX RMII Data Transmission

When TXEN*n* is de-asserted, the data on TXD*n*_[1:0] shall be "00" to indicate idle. When TXEN*n* asserts, the PHY accepts di-bit data on the TXD*n*_[1:0] lines. See Figure 9.

Figure 9. RMII Data Transmission

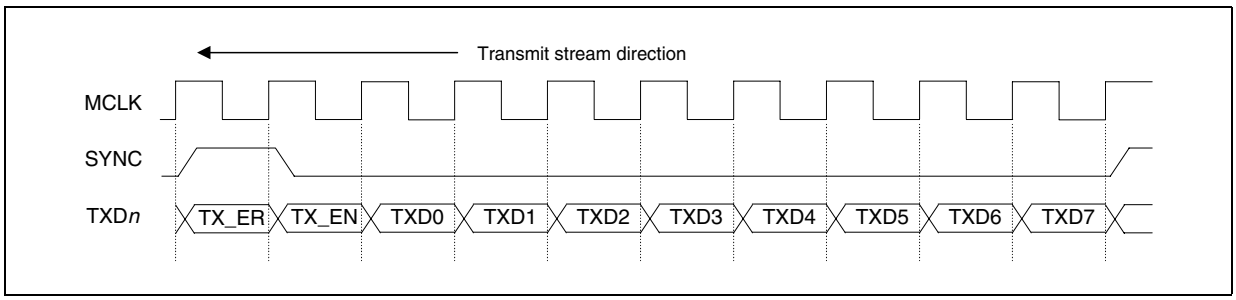


100BASE-TX SMII Data Transmission

The data is signaled in ten-bit segments, where each segment represents a new byte of data. Each segment is delimited by a SYNC pulse (every 10 clocks).

When TX_EN in the serial bit stream is de-asserted, then TXD[7:0] are the inter-frame control bits (for a direct MAC to MAC connection). When the TX_EN bit asserts, the PHY accepts the data stream on the TXD*n* line. Figure 10 shows the format of the SMII transmit serial stream.

Figure 10. SMII Transmit Data Serial Stream



2.4 10BASE-T Mode

2.4.1 10BASE-T Receiver

2.4.1.1 10BASE-T Manchester Decoder

The LXT9784 PHYs perform Manchester decoding and timing recovery when in 10BASE-T mode. The Manchester-encoded data stream is decoded from TPIP*n* and TPIN*n* to separate Receive Clock and Receive Data signals from the differential signal. This data is assembled to nibbles and transferred to the RMII/SMII.

10BASE-T RMII Data Reception

RMII data is transferred in di-bits at a 50 MHz rate. Therefore the data on RXD*n*_<1:0> is changed every 10 clock cycles.

10BASE-T SMII Data Reception

SMII data is signaled in ten-bit segments. Each segment is delimited by a SYNC pulse (every 10 clocks). In 10BASE-T mode, the data rate is one-tenth the 100 Mbps rate, therefore each segment is repeated ten times so that every 10 segments represent a new byte of data.

2.4.1.2 10BASE-T Receive Buffer and Filter

In 10 Mbps mode, data is received on TPIP*n* and TPIN*n*, after passing through isolation transformers. The filters implemented inside each LXT9784 PHY for 10BASE-T operation are tuned for supporting a single magnetics that are shared with the 100BASE-TX side. The receive buffer distinguishes valid receive data, link test pulses, and the idle condition, according to the requirements of the 10BASE-T standard. The filters are responsible for noise immunity, data acceptance and rejection conditions.

The filter rejects the differential pulses listed next. These rejectable single-cycle sine waves are discarded only if they are preceded by 4-bit times (400 ns) of silence. All other activity is determined to be either data, link test pulses, auto-negotiation fast link pulses, or the idle condition of peak magnitude less than 300 mV.

- Differential pulses with a peak magnitude of less than 300 mV.
- Continuous sinusoids with a differential amplitude less than 6.2 V peak to peak and frequency less than 2 MHz.
- Sine waves of a single cycle duration, starting with phase 0 or 180, that have a differential amplitude less than 6.2 V peak to peak and a frequency of at least 2 MHz and not more than 16 MHz.

2.4.1.3 10BASE-T Error Detection and Reporting

In 10BASE-T mode, the LXT9784 can detect errors in the receive data. As error is defined only in cases that TP-IDLE is not detected at the end of the frame (200 ns without mid-bit transitions).

2.4.1.4 10BASE-T Link Integrity

The link integrity in 10 Mbps works with link pulses. Each LXT9784 PHY senses and differentiates those link pulses from fast link pulses and from 100BASE-TX idles. For link pulse and for 100BASE-TX idles, the PHY uses parallel detection of the respective technology.

For fast link pulses, the PHY uses auto-negotiation. The 10BASE-T link pulses or NLPs are driven on the TPO*n* line. The link beat pulse is also used to determine if the receive pair polarity is reversed. If reversed the polarity is corrected internally.

2.4.1.5 10BASE-T Jabber Control Function

Each LXT9784 PHY contains a jabber control function that when enabled, inhibits transmission after a specified time window. The jabber timer is set to a value between 26.2 and 39 ms. When the PHY detects continuous transmission for longer than this time, it prevents further transmissions from going out in the wire until it detects that the MAC TXEN*n* signal (in RMII mode) or the TX_EN signal (in SMII mode) has been inactive for at least 314 ms.

2.4.1.6 10BASE-T Full Duplex

The LXT9784 PHYs support 10 Mbps full duplex by disabling the collision and the carrier sense functions. This allows each LXT9784 PHY to transmit and receive simultaneously, achieving up to 20 Mbps of network bandwidth. The configuration is done through auto-negotiation.

2.4.2 10BASE-T Transmit

2.4.2.1 10BASE-T Manchester Encoder

When TXEN*n* is asserted, the PHY accepts di-bit data on the RMII TXD*n*_[1:0] lines, or serial stream data on the SMII TXD*n* line. After the clocked data is serialized into a 10 Mbps serial stream, the 20 MHz clock performs the Manchester encoding. The Manchester code always has a mid-bit transition. If the data to be transmitted is "1", then the transition is from low to high. If the value is "0" then the transition is from high to low. The boundary transition (such as between cell times) occurs only when the data changes from bit to bit: if "10" then the change is from high to low; if "01" then the change is from low to high.

10BASE-T RMII Data Transmission

The data is transferred in di-bits at a 50 MHz rate. Therefore the data on TXD*n*_[1:0] is valid for 10 clock cycles for each di-bits.

10BASE-T SMII Data Transmission

The data is signaled in ten-bit segments. Each segment is delimited by a SYNC pulse (every 10 clocks). In 10M mode, the data rate is one-tenth the 100M rate, therefore each segment is repeated ten times so that every 10 segments represent a new byte of data.

2.4.2.2 10BASE-T Driver and Filter

Since 10BASE-T and 100BASE-TX have different filtration needs, both filters are implemented inside the chip. This allows the two technologies to share the same magnetics. The LXT9784 supports both technologies through one pair of TPOP*n* and TPON*n* pins and by externally sharing the same magnetics.

In 10 Mbps mode, the LXT9784 PHYs begin transmitting the serial Manchester bit stream within 3 bit times (300 ns) after the assertion TXEN*n*. In 10-Mbps mode the line drivers use a pre-distortion algorithm to improve jitter tolerance. The line drivers reduce their drive level during the second half of “wide” (100 ns) Manchester pulses and maintain a full drive level during all narrow (50 ns) pulses and the first half of the wide pulses. The LXT9784’s advanced wave-shaping circuitry prevents overcharging during wide pulses, a major source of jitter.

2.5 MDI/MDI-X Function

When connecting Ethernet devices together, there are two types of cables in use: straight-through and crossed-over cables. In a typical connection, DTE to Switch, cross-over is implemented in the Switch MAU. In this case a straight-through cable is required. However, in case that a connection is required between two MAUs of the same type, then an external cross-over cable is required. In

cases that the cable type does not match the two ends MAUs configurations, replacement of the cable is required. With the MDI/MDI-X feature enabled, switching is performed automatically by the LXT9784, to adjust the MAU to the cable type.

This advanced feature enables auto-correction of a specific wiring problem of incorrect cabling with respect to crossed-over versus straight-through cables. The LXT9784 PHY can identify the cable connection type and adjust its MDI port to the cable by switching between the TPO and TPI pairs. The auto switching is done prior to the auto-negotiation algorithm.

Table 14 shows the standard DTE straight-through RJ-45 port configuration, with the transmit pair on contacts 1 and 2, and the receive pair on contacts 3 and 6. Table 15 shows the MAU configuration of a crossed-over RJ-45 port.

2.5.1 MDI/MDI-X Auto Switching Activation

The external MDI-X input, sampled during reset, enables or disables auto-switching. When this input is externally pulled up, or left unconnected, auto-switching is enabled. When MDI-X is externally pulled down, auto switching is disabled. In the case that auto-switching was disabled during reset, after reset the MDI-X pin is used to configure the connection type (straight-through or crossed-over). A “1” forces a crossed-over connection, a “0” forces a straight-through connection.

2.5.2 MDI/MDI-X Algorithm

In the case that auto-switching was enabled during reset, the PHY attempts to detect link activity in a given configuration (MDI or MDI-X) for a duration of 80 - 100 ms. If no link activity is detected during this slot time, the PHY waits a random amount of time greater then 80 ms, and switches the MDI pairs to the other configuration.

Table 14. Straight-through Pin Assignments

Contact	MDI Signal
1	TDP_*n*
2	TDN_*n*
3	RDP_*n*
4	Not used
5	Not used
6	RDN_*n*
7	Not used
8	Not used

Table 15. Crossed-over Pin Assignments

Contact	MDI Signal
1	RDP_*n*
2	RDN_*n*
3	TDP_*n*
4	Not used

Table 15. Crossed-over Pin Assignments

Contact	MDI Signal
5	Not used
6	TDN_*n*
7	Not used
8	Not used

2.6 Hardware Control Interface

The LXT9784 can be configured for unmanaged applications, using external pins (hardware control) as described in the following paragraphs.

2.6.1 MDI-X (MDI Crossover)

During RESET, enables the auto-switch feature. If this feature was disabled, then after reset the MDI-X pin controls the manual MDI/MDI-X switching.

- When MDI-X = 1, the MDI port is forced to MDI-X (cross- over mode).
- When MDI-X = 0, the MDI port is forced to MDI (straight-through mode).

2.6.2 FRCLNK (Force Link)

During RESET:

- When FRCLNK = 1, it *forces good link* (PHY reg17, bit 11), *link integrity* (PHY reg17, bit 1), and *disables auto-negotiation* (PHY reg0, bit 12)
- When FRCLNK = 0, Normal Operation.

If FRCLNK was set, then after reset the FRCLNK pin will control speed selection (PHY reg0, bit 13), where:

- When FRCLNK = 1, it forces 100 Mbps.
- When FRCLNK = 0, it forces 10 Mbps.

The FRCLNK pin and bit 11 in PHY register 11'h are ORed together.

2.6.3 FRC34 (Force 34 Transmit Pattern)

The FRC34 pin and bit 12 in PHY register 11'h are ORed together.

2.6.4 BP4B5B (4B/5B Bypass)

To enter 4B/5B bypass mode, this pin must be set high after the end of reset. During reset, this pin must be pulled down to ensure proper operation of the LXT9784.

The BP4B5B pin and bit 14 in PHY register 11'h are ORed together. This pin bypasses the 4B5B encoder/decoder in the transmit and receive sections. In 4B5B bypass mode the data is transmitted in 5-bit symbols. In RMII mode, the fifth bit (MSB) of all eight ports is driven through the TXD4 pin. The TXD4 pin is a static pin and should be pulled up or pulled down. In SMII mode, TXER represents the fifth bit.

2.6.5 SCRMBP (Scrambler Bypass)

In order to enter scrambler by-pass this pin must be set high after the end of reset. During reset this pin must be pulled-down to ensure proper operation of the LXT9784.

The SCRMBP pin and bit 15 in PHY register 11'h are ORed together.

2.7 PHY Addresses

The ID<1:0> pins are used to set the PHY addresses for the MII management interface.

The PHYs are assigned consecutive addresses in increasing order, starting with PHY0. The address of PHY0 is determined by the setting of ID<1:0>. This allows up to

four LXT9784s to be connected on a single MII management bus. Up to thirty-two ports are available when using all the combinations of ID<1:0>. Table 16 shows the internal PHY addresses for each of the possible combinations of ID<1:0>.

Table 16. PHY Addresses

ID_1	ID_0	PHY0	PHY1	PHY2	PHY3	PHY4	PHY5	PHY6	PHY7
0	0	00000	00001	00010	00011	00100	00101	00110	00111
0	1	01000	01001	01010	01011	01100	01101	01110	01111
1	0	10000	10001	10010	10011	10100	10101	10110	10111
1	1	11000	11001	11010	11011	11100	11101	11110	11111

2.8 Link Status Interrupt

The LXT9784 provides an open-drain interrupt pin ($\overline{INT}$), which is driven low by the LXT9784 when one or more of it's internal PHYs has a change in link status. Figure 11 is a simplified diagram of the interrupt structure.

When $\overline{INT}$ is driven low, all of the PHY interrupt registers should be read, to determine which port or ports caused the interrupt (Refer to Table 51). Once a PHY interrupt bit has been read, it is self-cleared. The interrupt line becomes inactive only after reading the Link Status Interrupt bits of all the PHYs that caused the interrupt. In the case of more than one PHY having an interrupt pending, $\overline{INT}$ remains asserted until after reading the last PHY with a Link Status Interrupt bit set to "1".

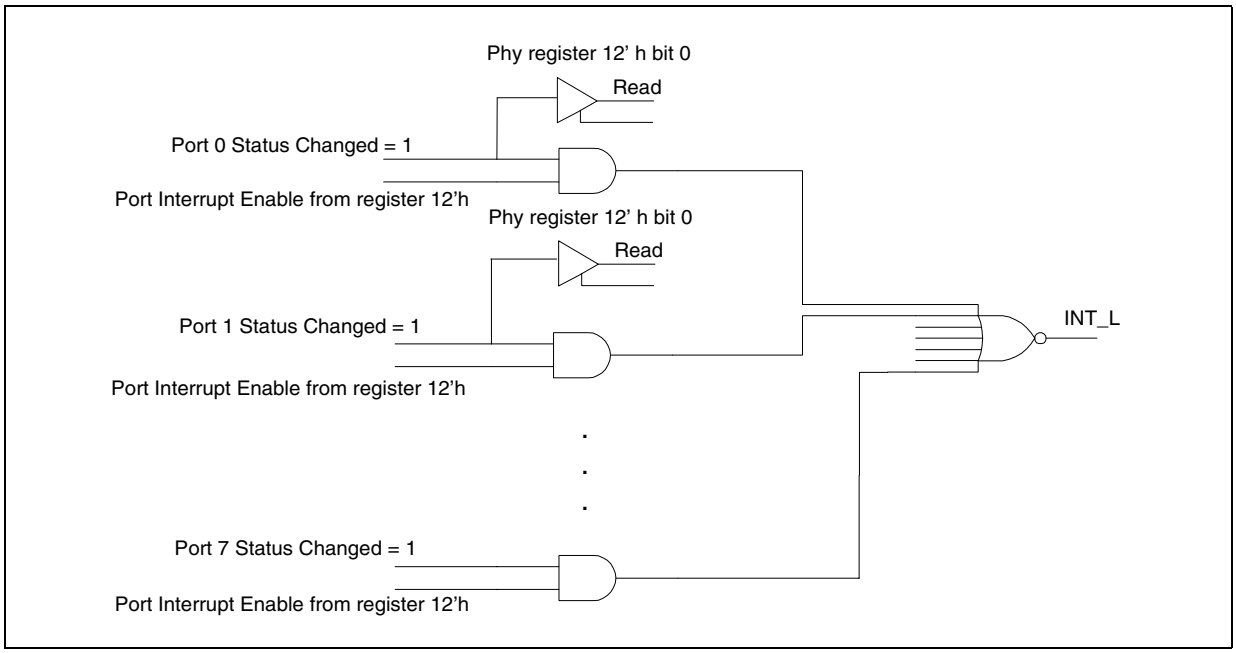
If during the procedure of reading the interrupt registers a new change of link status occurred on a PHY which has already been accessed, the interrupt line remains asserted after completing the read procedure.

This feature can be used instead of polling the PHYs for link status change.

2.9 Reset

When the LXT9784 RESET signal is asserted (active high) all internal circuits are reset. The PHY can also be reset individually via the PHY register reset bit (register 0 ’h bit 15). Device clock should be stable and running prior to HW RESET. Reset must be asserted for a minimum of 500 µs for proper operation after de-assertion.

Figure 11. Simplified Interrupt Structure



2.10 LED Operation

The LXT9784 has three pins per port dedicated to driving the LEDs. These drivers can indicate link/activity, speed, and collision. The drivers also indicate that the PHY port was disabled by management. The activity LED in this mode is triggered by both transmit and receive activities. All three drivers are active Low.

The algorithm for computing media utilization is an average of the activity on the media over the time of 8 maximum length packets, with minimum IPG spacing. The utilization is averaged over:

(8 packets * 1518 bytes * 8 bytes/bit * bit time) + (8 IPG * 96 bits * bit time)

The percent utilization is indicated by a specific frequency on the $\overline{\text{LED}n\text{\_A}}$ (as shown in Table 17) for a period of 600 ms (LED refresh rate), based on the activity of the prior 600 ms period.

In case the port is disabled, register 0.10 = 1, drivers $\overline{\text{LED}n\text{\_A}}$ and $\overline{\text{LED}n\text{\_B}}$ blink in unison, at a rate of 1 Hz, 500 ms on and 500 ms off. Eliminate the indication of PHY port disable by setting the PHY register 1B’h, bit 4. There is full controllability on all drivers through PHY register 1B’h, bits [2:0].

The $\overline{\text{LED}n\text{\_B}}$ state is frozen when a link is lost and is changed only after the link is re-established.

During reset, all LED drivers are active for approximately 2 seconds, then turned off.

Table 17. LED Functionality

LED driver	Function	Description
$\overline{\text{LED}n\_\text{A}}$	link **solid** /activity **blink**	With a good link the output is low, the output toggles at a rate related to the utilization. Refer to Table 18 for the actual numbers.
$\overline{\text{LED}n\_\text{B}}$	speed	The output is low for 100 Mbps, high for 10 Mbps
$\overline{\text{LED}n\_\text{C}}$	collision	The output blinks low with collisions stretch rate of 10 ms.
1. *n* indicates Port Number.		

Table 18. Activity LED Blink Rates

Percent Utilization	Blink Rate [1]	Frequency
0-5%	slow	3 Hz
5-30%	medium	5 Hz
+30%	fast	7 Hz
1. Note: Duty Cycle = 50%		

2.11 MII Management Interface Operation

The LXT9784 provides PHY status and accepts PHY management information via the MII management interface. This is accomplished via read and write operations to various registers according to the IEEE802.3u Standard. A read or write of a particular register is called a management frame, which is sent serially over the MDIO pin synchronous to MDC at a maximum rate of 3 MHz. Read and write cycles are from the perspective of the controller. Therefore, the controller would always drive the Start, Opcode, PHY Address and Register Address on to the MDIO pin. For a write, the controller would also drive the transition bits and data. For a read, the LXT9784 drives the transition bits and data onto the MDIO pin. The controller should drive address and data on the falling edge of MDC and the LXT9784 latches that data on the rising edge of MDC. The PHY addresses in the LXT9784 can be configured from 0-31. The management frame structure is shown in Table 19.

This structure allows a controller or other management hardware, to query a PHY for status of the link, auto-negotiation registers, or configure the PHY to one of many modes. Table 20 defines the protocol terms.

When MDIO and MDC are not in use, they should be connected to pull-up devices.

Table 19. MII Management Frame Format

Function	Preamble	Start Frame	Opcode	PHY Adr	Reg adr	Turnaround	Data	Idle
READ	1...1	10	10	AAAAA	RRRRR	Z0	D[15:0]	Z
WRITE	1...1	01	01	AAAAA	RRRRR	10	D[15:0]	Z

Table 20. Glossary of Protocol Terms

Term	Definition
Preamble	Sequence of 32 contiguous logic one bits on the MDIO pin at the beginning of each transaction with corresponding cycles on the MDC clock pin for synchronization of the PHY.
Start	A start of Frame pattern of “01”
Opcode	An Operation Code which can assume one of two values: 10 Read instruction. 01 Write instruction.
PHY Adr	5-bit address of the PHY device with MSB transmitted first, which provides support for 32 unique PHY addresses.
Reg Adr	5-bit address of the specific register within the PHY device with MSB transmitted first. This provides support for 32 unique registers.
Turnaround	A two-bit turnaround time during which no device actively drives the MDIO signal on a read cycle. During a read transaction the PHY should not drive MDIO in the first bit time and the drive a zero in the second bit time. During a write transaction a "10" pattern is driven to PHY.
Data	16 bits of data driven by the PHY on read transaction, and will be driven to PHY on write transaction. In either case, the MSB is transmitted first.
Idle	The IDLE condition on MDIO is a high impedance state. The MDIO driver is disabled and the PHY should pull-up the MDIO line to logic one.

2.12 Test Port Operation

The LXT9784 can be set to one of two manufacturing testing modes, depending on TI, TEXEC, and TCK input pins combination, as shown in Table 20.

The MODE[2:0] pins are used to enable the manufacturing testing modes, and should be set to "111".

The test mode can be used only for manufacturing testing.

Table 21. Test Mode Configuration

Mode Select Pins [1]			Test Enable Pins			Mode	Comments
2	1	0	TCK	TI	TEXEC		
0	0	1	X	X	X	RMII	Normal System Mode
0	1	0	X	X	X	SMII	
1	1	1	0	0	1	NAND Tree (+ Hi Z)	Manufacturing test mode
1	1	1	0	1	0	XNOR Tree (+ Hi Z)	
1. Note: All other combinations are “reserved” and should not be used.							

2.12.1 NAND-Tree Test

This command connects all the outputs of the input-buffers in the device periphery into a NAND-Tree scheme. All the I/O and outputs, except for MODE[2:0], TI, TEXEC, TCK, INT, and TOUT pins, are put into a Tri-State mode.

There are two NAND-Tree chains, with two separate inputs, assigned to UCA1 (Chain 1) and COLED (chain 2), and two separate outputs, assigned to INT (Chain 1) and TOUT (Chain 2) respectively.

To enable NAND-tree manufacturing test mode, set MODE[2:0] = "111", TCK = "0", TI = "0", TEXEC = "1" and power-up or reset the chip. Toggling the chain input pin will be reflected at the chain output after a delay of about 20ns.

2.12.2 XNOR-Tree Test

This command connects all the outputs of the input-buffers in the device periphery into a XNOR-Tree scheme. All the I/O and outputs, except for MODE[2:0], TI, TEXEC, TCK, INT, and TOUT pins, are put into a Tri-State mode.

There are two XNOR-Tree chains, with two separate inputs, assigned to UCA1 (Chain 1) and COLED (chain 2), and two separate outputs, assigned to INT (Chain 1) and TOUT (Chain 2), respectively.

In order to set up the device into XNOR tree manufacturing test mode set MODE[2:0] = "111", TCK = "0", TI = "1", TEXEC = "0" and power-up or reset the chip. Toggling the chain input pin will be reflected at the chain output after a delay of about 20 ns.

2.12.3 NAND/XNOR Tree Chain Order

A combination of “111” on the MODE_[2:0] pins indicates that the LXT9784 is configured to an asynchronous test mode (NAND-TREE or XNOR-TREE). Test pins combinations for the asynchronous test modes are:

MODE_[2:0] = “111”, TCK = “0”, TI= “0”, TEXEC =”1” for NAND - TREE

MODE_[2:0] = “111”, TCK = “0”, TI= “1”, TEXEC =”0” for XNOR - TREE

The NAND-TREE / XNOR-TREE commands connect all outputs of the *input-buffers* in the device periphery into a
NAND-TREE / XNOR-TREE scheme. All the input/output pins and output pins except for: MODE_[2.0], TI, TEXEC, TCK, INT#, and TOUT pins are put into a Tri-State mode.

There are two NAND-TREE / XNOR-TREE chains, with two separate outputs, assigned to INT# (Chain 1) and TOUT (Chain 2).

The following table lists the chains order / direction (pin no. 1 in the chain, is the farthest from the NAND-TREE / XNOR-TREE outputs).]

Table 22. Test Scan Chain

Chain Order	Ball ID	Chain #1	Ball ID	Chain #2
1	W1	TXD0_1	W18	NC
2	W2	TXD0_1	W19	NC
3	W3	TXEN0	W20	NC
4	V1	CRSDV0	V18	NC
5	V2	RXD0_1	V19	NC

Table 22. Test Scan Chain (Continued)

Chain Order	Ball ID	Chain #1	Ball ID	Chain #2
6	V3	RXD0_0	V20	NC
7	U1	RXD1_0	U18	LED0-C#
8	U2	RXD1_1	U19	LED0_B#
9	U3	CRSDV1	U20	LED0_A#
10	T1	TXEN1	T18	LED1_C#
11	T2	TXD1_0	T19	LED1_B#
12	T3	TXD1_1	T20	LED1_A#
13	R1	TXD2_1	R18	LED2_C#
14	R2	TXD2_0	R19	LED2_B#
15	R3	TXEN2	R20	LED2_A#
16	P1	CRSDV2	P18	LED3_C#
17	P2	RXD2_1	P19	LED3_B#
18	P3	RXD2_0	P20	RXER7
19	N1	RXD3_0	N18	RXER6
20	N2	RXD3_1	N19	RXER5
21	N3	CRSDV3	N20	RXER4
22	M1	TXEN3	M18	RXER3
23	M2	TXD3_0	M19	RXER2
24	M3	TXD3_1	M20	RXER1
25	L1	TXD4	L18	RXER0
26	L3	FRC34	L19	ID_1
27	K3	MCLK	L20	ID_0
28	K1	FRCLNK	K18	RESET
29	J2	TXD4_1	K19	BP4B5B
30	J3	TXD4_0	K20	SCRMBP
31	H1	TXEN4	J18	NC
32	H2	CRSDV4	J19	NC
33	H3	RXD4_1	J20	NC
34	G1	RXD4_0	G18	MDIX
35	G2	RXD5_0	G19	LED3_A#
36	G3	RXD5_1	G20	LED4_C#
37	F1	CRSDV5	F18	LED4_B#
38	F2	TXEN5	F19	LED4_A#
39	F3	TXD5_0	F20	LED5_C#
40	E1	TXD5_1	E18	LED5_B#
41	E2	TXD6_1	E19	LED5_A#
42	E3	TXD6_0	E20	LED6_C#
43	D1	TXEN6	D18	LED6_B#

Table 22. Test Scan Chain (Continued)

Chain Order	Ball ID	Chain #1	Ball ID	Chain #2
44	D2	CRSDV6	D19	LED6_A#
45	D3	RXD6_1	D20	LED7_C#
46	C1	RXD6_0	C18	LED7_B#
47	C2	RXD7_0	C19	LED7_A#
48	C3	RXD7_1	C20	MDIO
49	B1	CRSDV7	B19	MDC
50	B2	TXEN7	-	-
51	B3	TXD7_0	-	-
52	A2	TXD7_1	-	-
NAND-TREE / XNOR-TREE Output	B18	INT#	B20	TOUT

3.0 Application Information

3.1 Magnetics

Table 23 lists of magnetics modules available from various vendors. All modules listed support both 10M and 100M operation.

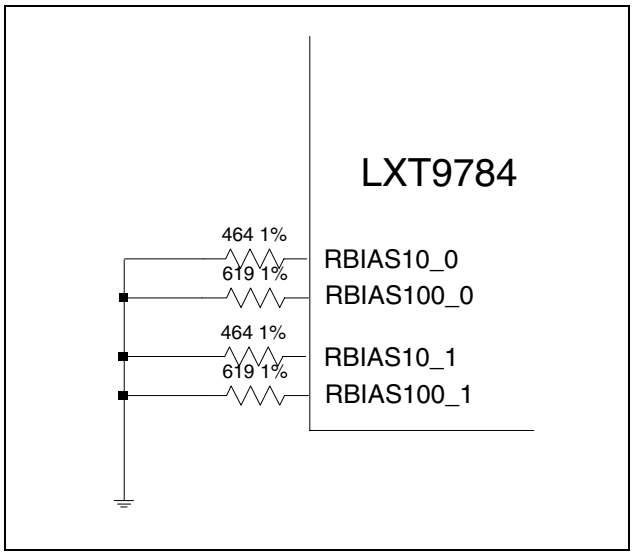
Table 23. Magnetics Module Vendor

Vendor	Model/Type
Bel Fuse	0558-5999-N7 (quad)
Pulse Engineering	H1141T (single)
	H1140T (quad)

3.2 Analog References (RBIAS)

The four RBIAS inputs (RBIAS10_0, RBIAS10_1, and RBIAS100_0, RBIAS100_1) must have external resistor connections. The inputs are sensitive to the resistor value and some experimentation is required to select the correct values for any given layout. Resistors of 1% tolerance are to be used. See Figure 12 for a circuit example.

Figure 12. Typical RBIAS Circuit



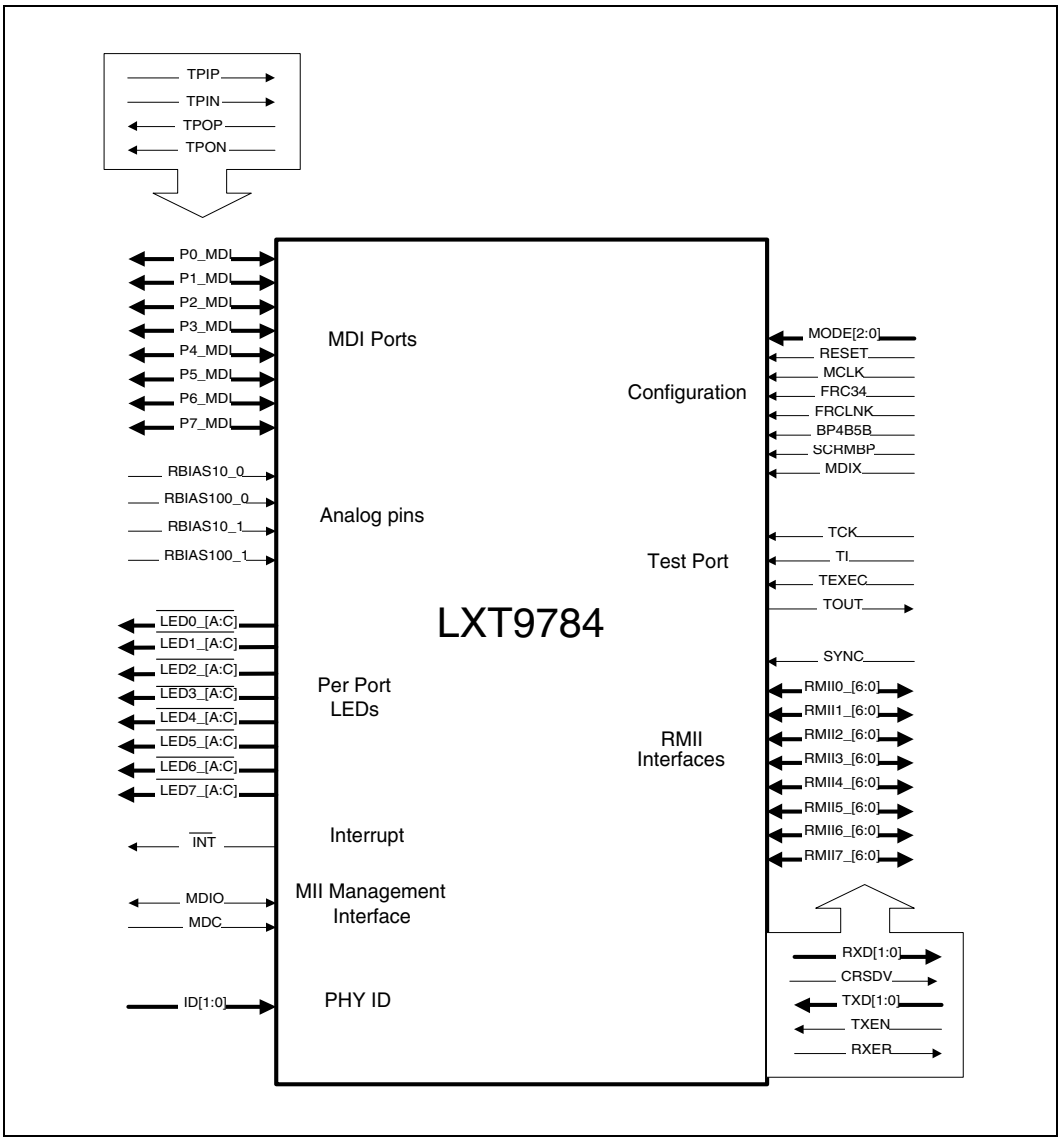
3.3 RMII Applications

The RMII ports provide eight low pin-count interfaces between the eight PHYs and an ASIC switch, as an alternative to the SMII interface. The RMII interface is composed of seven signals per port, and a global reference clock.

3.3.1 RMII Clock

In RMII mode of operation, the master input clock (MCLK) frequency should be 50 MHz ± 50 ppm, with a duty-cycle between 35% and 65% inclusive.

Figure 13. Typical RMII Application



3.4 SMII Applications

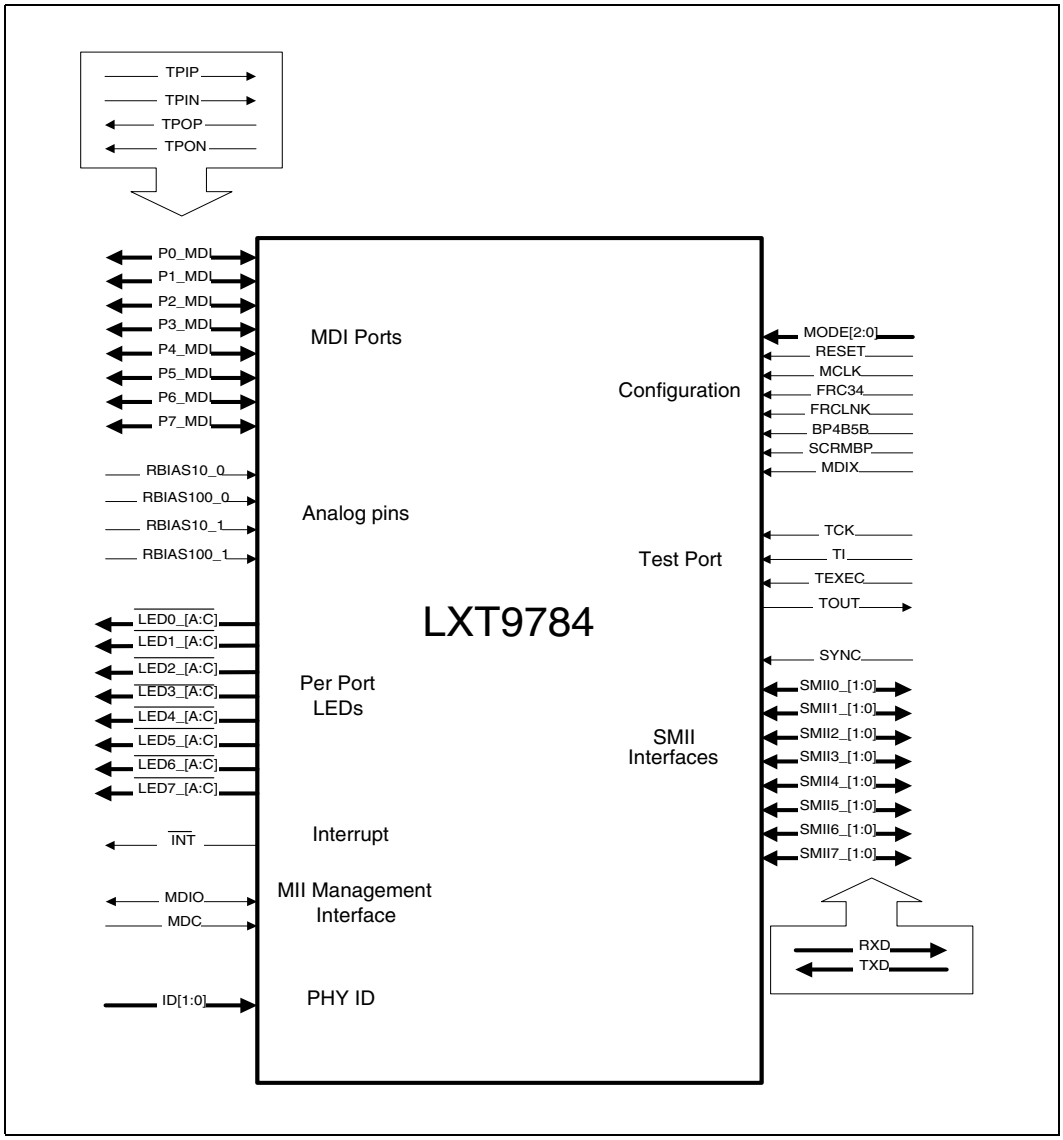
The SMII ports provide eight low pin-count interfaces between the LXT9784's eight PHYs and an ASIC switch, as an alternative to the RMII interface. The SMII interface is composed of two signals per port, a global synchronization signal, and a global reference clock.

Data and control bits are transmitted and received serially synchronous to MCLK, in ten bit segments delimited by a pulse on SYNC, on RXD*n* and TXD*n* respectively.

3.4.1 SMII Clock

In SMII mode of operation, the master input clock (MCLK) frequency should be 125 MHz, ± 50ppm, with a duty-cycle between 35% and 65% inclusive.

Figure 14. Typical SMII Application



4.0 Test Specifications

Note: Table 24 through Table 41 and Figure 15 through Figure 27 represent the performance specifications of the LXT9784 and are guaranteed by test, except where noted, by design. The minimum and maximum values listed in Table 26 through Table 41 are guaranteed over the recommended operating conditions specified in Table 25.

Table 24. Absolute Maximum Ratings

Parameter		Minimum	Maximum	Units
Temperature Under Bias	Ambient - Commercial	0	+ 100	°C
	Ambient - Extended	-40	+ 100	°C
	Case - Commercial	0	+ 120	°C
	Case - Extended	-40	+ 120	°C
Supply Voltage with respect to V_{SS}		-0.5	+ 3.45	V
Outputs Voltages		-0.5	+ 3.45	V
Input Voltages		-1.0	+ 3.45	V
Caution: Exceeding these values may cause permanent damage.				
Caution: Functional operation under these conditions is not implied.				
Caution: Exposure to maximum rating conditions for extended periods may affect device reliability.				

Table 25. Operating Conditions

Parameter	Symbol	Min	Typ[1]	Max[2]	Units	Condition
Recommended Operating Temperatures - Commercial	TOPA	0		70	C	Ambient
	TOPC	0		105	C	Case
Recommended Operating Temperatures - Extended	TOPA	- 40		85	C	Ambient
	TOPC	- 40		120	C	Case
Recommended Supply Voltage - Commercial	V_{CC}	2.85	3.0 / 3.3	3.45	V	
Recommended Supply Voltage - Extended	Vcc	3.15		3.45	V	
Current Consumption	I_{CC}	-	680 /750	775	mA	100 Mbps, RMII Mode
		-	635 / 680	-		10 Mbps, RMII Mode
		-	715 / 800	850		100Mbs, SMII Mode
		-	710 / 760	-		10Mbs, SMII Mode
Power Dissipation	P	-	-	334	mW	Per port 100Mbps RMII Mode
		-	-	367		Per port 100Mbps SMII Mode
			1.0		W	Auto-Negotiation
1. Tested at a supply voltage of 3.0V/3.3V. 2. Tested at a supply voltage of 3.45V.						

4.1 DC Characteristics

Table 26. Clock DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Input Low Voltage (TTL)	V_{IL}			0.8	V	
Input High Voltage (TTL)	V_{IH}	2.0			V	
Input Leakage Currents	I_{ILIH}			± 10	µA	0< Vin< Vcc
Input Capacitance	C_{IN}			8	pF	See Note 1.
1. Characterized, not tested. Valid for digital pins only.						

Table 27. RMII/SMII and General Interface[1] DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Input Low Voltage (TTL)	V_{IL}			0.8	V	
Input High Voltage (TTL)	V_{IH}	2.0			V	
Output Low Voltage	V_{OL}			0.4	V	I_{out} = 4 mA
Output High Voltage	V_{OH}	2.4			V	I_{out} = -4 mA
Input Leakage Current	I_{ILIH}			± 10	µA	0< Vin< Vcc
Input Capacitance	C_{IN}			8	pF	Note 2.
1. “General Interface” refers to the following: MII management, configuration and PHY ID. 2. Characterized, not tested. Valid for digital pins only.						

Table 28. LED DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Output Low Voltage	V_{OLLED}			0.7	V	I_{out} = 10 mA
Output High Voltage	V_{OHLED}	Vcc - 0.7			V	I_{out} = -10 mA

Table 29. 10BASE-T Receiver Voltage/Current DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Input Differential Resistance	R_{ID10}	10			kΩ	DC. Note 1.
Input Differential Accept Peak Voltage	V_{IDA10}	585		3100	mV	5 MHz ≤ f ≤ 10 MHz
Input Differential Reject Peak Voltage	V_{IDR10}			300	mV	5 MHz ≤ f ≤ 10 MHz
Input Common Mode Voltage	V_{ICM10}		Vcc/2		V	
1. This value is measured across the receive differential pins, TPIP and TPIN.						

Table 30. 10BASE-T Transmitter Voltage/Current DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Output differential Peak Voltage	V_{OD10}	2.2		2.8	V	R_L= 100 Ω Note 1.
Line Driver Supply Peak Current per port	I_{CCT10}		57		mA	R_{BIAS10}= 464 Ω Notes 2 and 3.

1. R_L is the resistive load across the transmit differential pins, TPOP and TPON.
2. Current is measured on all Vcc pins @ Vcc = 3.3 V.
3. Transmitter current is measured with a 1:1 transformer. Transmitter peak current is governed by the following equation: maximum differential output peak voltage divided by the load resistance value.

Table 31. 100BASE-TX Receiver Voltage/Current DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Condition
Input Differential Resistance	R_{ID100}	10			kΩ	DC. Note 1.
Input Differential Accept Peak Voltage	V_{IDA100}	500		1200	mV	
Input Differential Reject Peak Voltage	V_{IDR100}			100	mV	
Input Common Mode Voltage	V_{ICM100}		Vcc/2		V	

1. This value is measured across the receive differential pins, TPIP and TPIN.

Table 32. 100BASE-TX Transmitter Voltage/Current DC Characteristics

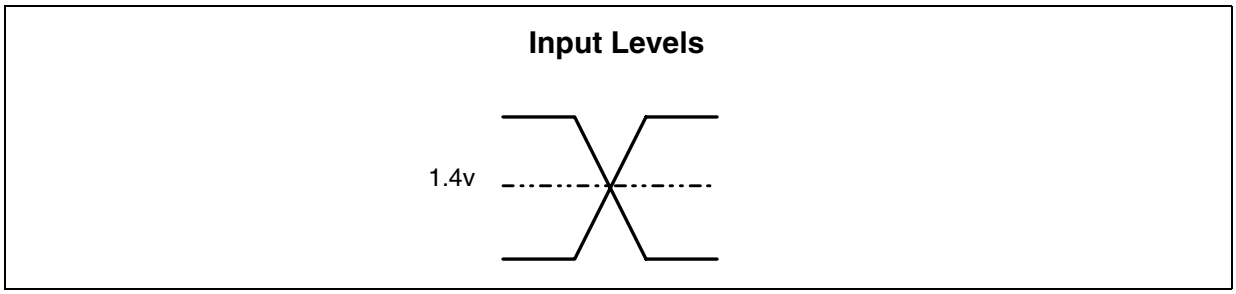
Parameter	Symbol	Min	Typ	Max	Units	Condition
Output differential Peak Voltage	V_{OD100}	0.95	1.00	1.05	V	R_L= 100 Ω Note 1.
Line Driver Supply Peak Current per port	I_{CCT100}		20		mA	$R_{BIAS100}$= 619 Ω Notes 2 and 3.

1. R_L is the resistive load across the transmit differential pins, TPOP and TPON.
2. Current is measured on all Vcc pins @ Vcc = 3.3 V.
3. Transmitter current is measured with a 1:1 transformer. Transmitter peak current is governed by the following equation: maximum differential output peak voltage divided by the load resistance value.

4.2 AC Characteristics

Figure 15 defines the conditions under which timing measurements are done. The design must guarantee proper operation for voltage swings and slew rates that exceed the specified test conditions.

Figure 15. AC Testing Level Conditions



4.2.1 Common Characteristics

Figure 16. MDC Clock AC Timing

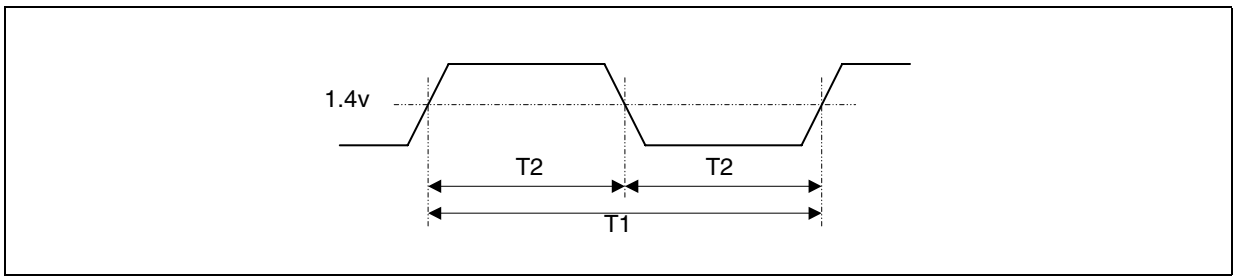


Table 33. MII Management Clock Specifications

Parameter	Symbol	Min	Typ	Max	Units	Condition
MDC Frequency	*f*	0		3.0	MHz	
MDC clock period	T1	300			ns	
MDC duty cycle	T2	35		65	%	

Figure 17. MII Management Timing Parameters: MDC/MDIO

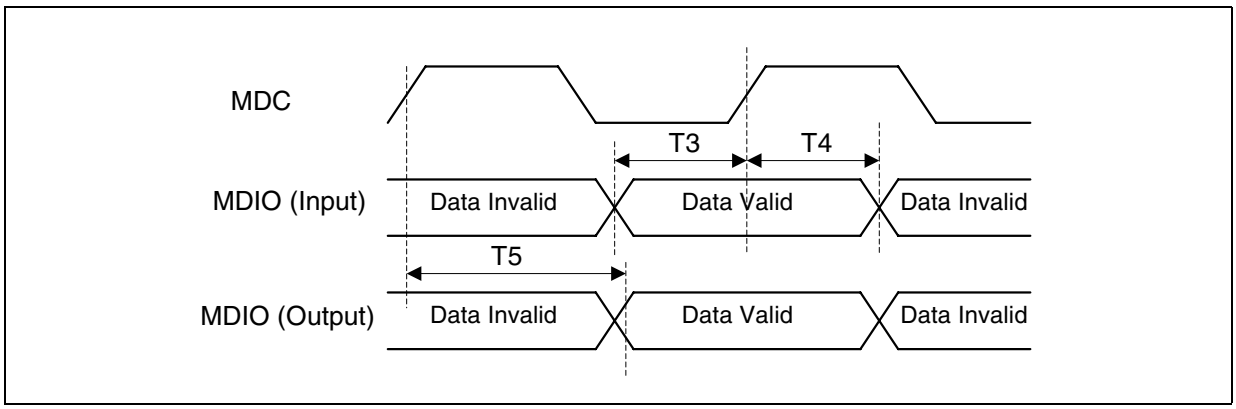


Table 34. MII Management Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Condition
MDIO setup time to MDC rising edge	T3	10			ns	
MDIO hold time from MDC rising edge	T4	10			ns	
MDIO valid from MDC rising edge	T5	0		200	ns	

Figure 18. Normal Link Pulse Timings

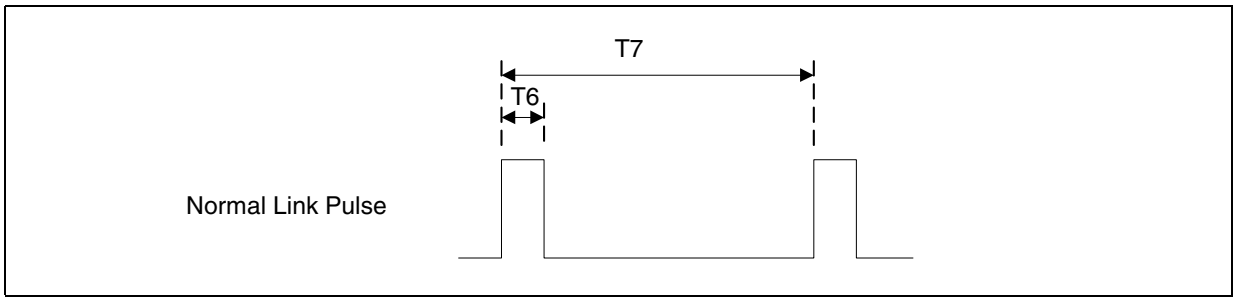


Table 35. 10BASE-T Normal Link Pulse (NLP) Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Condition
NLP width	T6		100		ns	10 Mbps
NLP Period	T7	8	16	24	ms	10 Mbps

Figure 19. Fast Link Pulse Timings

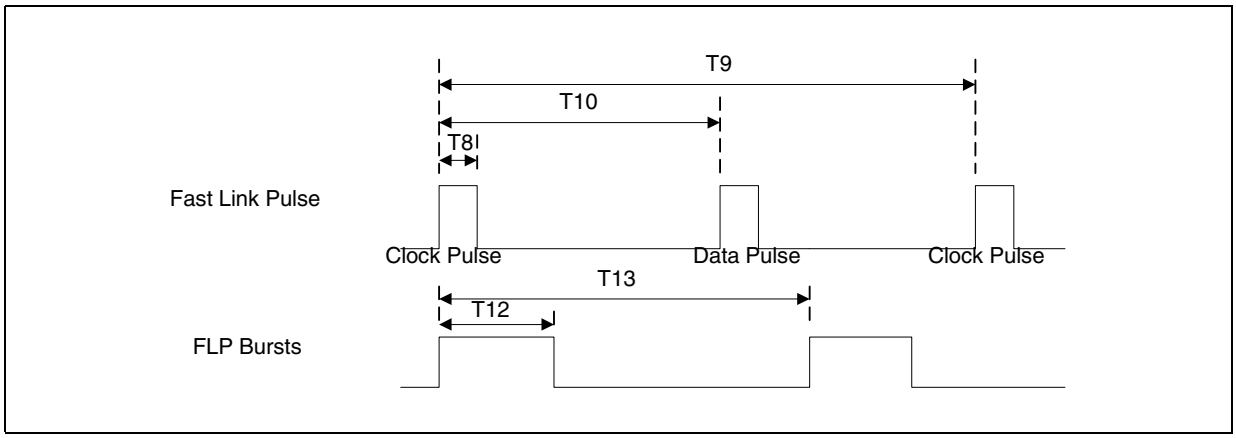


Table 36. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Condition
FLP width (clock/data)	T8		100		ns	
Clock pulse to clock pulse period	T9	111	125	139	µs	
Clock pulse to Data pulse period	T10	55.5	62.5	69.5	µs	

Table 36. Auto-Negotiation Fast Link Pulse (FLP) Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Condition
Number of pulses in one burst	T11	17		33	#	
Burst width	T12		2		ms	
FLP Burst period	T13	8	16	24	ms	

Table 37. 100BASE-TX Transmitter AC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Condition
TPOP/TPON Differential Output Peak Jitter	T_{JIT}			1400	ps	HLS data

4.3 RMII Interface

Figure 20. RMII AC Testing Level Conditions

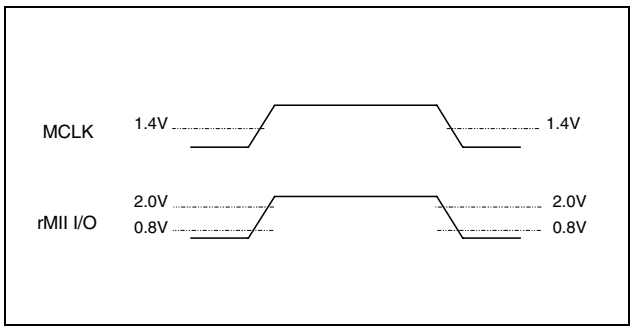


Figure 21. RMII Rise and Fall Timings

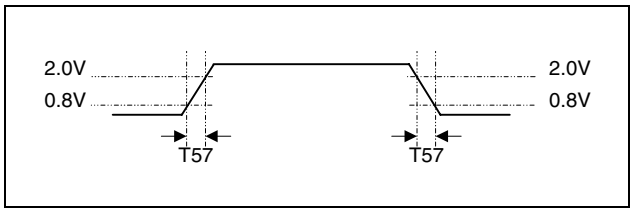


Figure 22. RMII Timing Parameters

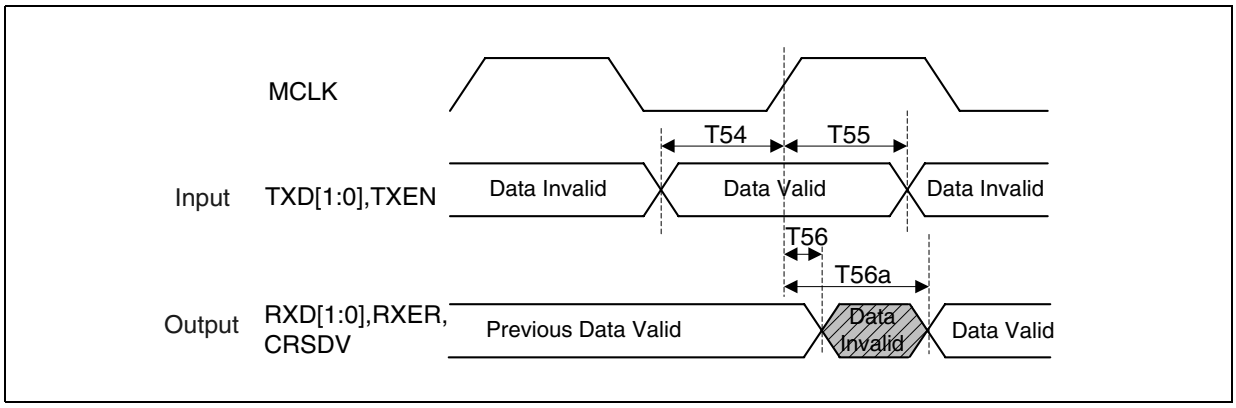


Table 38. RMII Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Condition
TXD[1:0],TXEN Data setup to MCLK rising edge	T54 (T_{RMSU})	4			ns	
TXD[1:0],TXEN Data hold to MCLK rising edge	T55 (T_{RMHD})	2			ns	
RXD[1:0], RXER,CRSDV min valid time	T56 (T_{RMVLM})	3			ns	
RXD[1:0], RXER,CRSDV max valid time	T56a (T_{RMVLX})			14	ns	
TXD[1:0],TXEN,RXD[1:0], RXER,CRSDV rise and fall time	T57 (T_{RMFR})	1		5	ns	

4.4 SMII Interface

Figure 23. SMII Mode - AC Testing Level Conditions

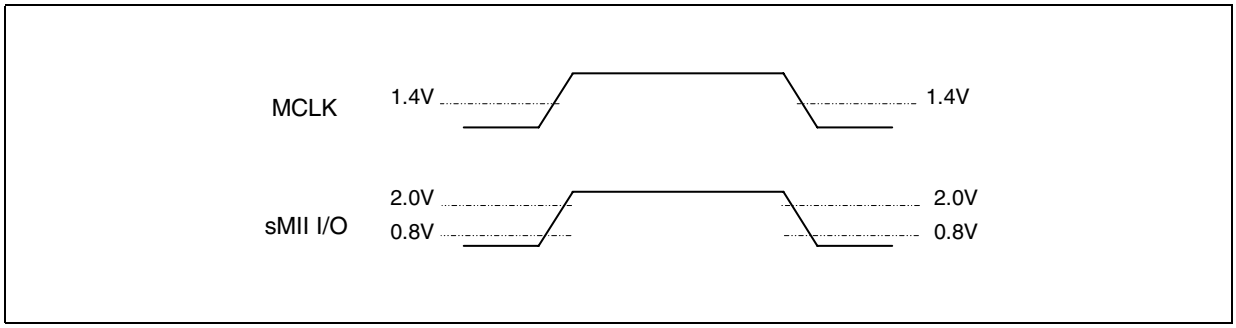


Figure 24. SMII Timing Parameters

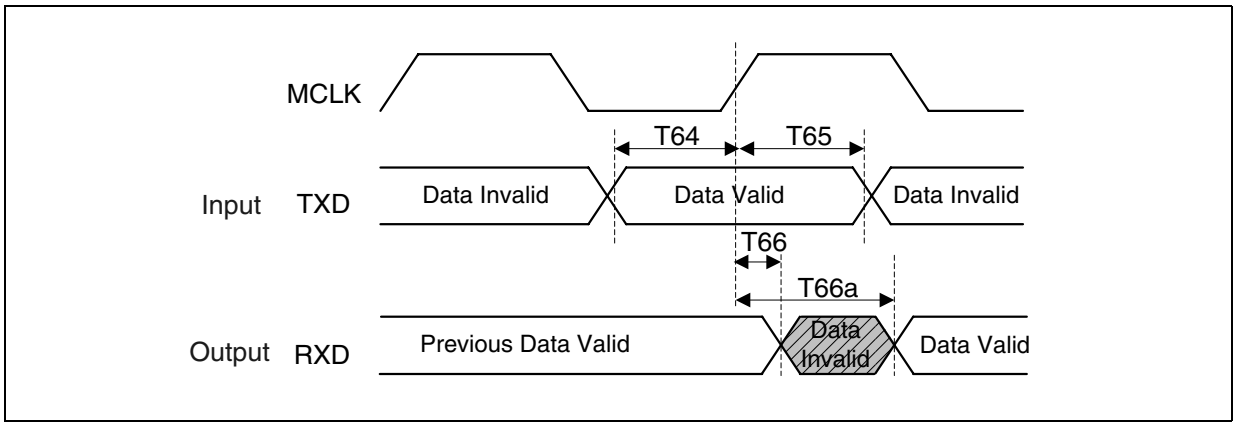


Table 39. SMII Interface Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Condition
TXD setup to MCLK rising edge	T64 (T_{SMSU})	1.5			ns	
TXD hold from MCLK rising edge	T65 (T_{SMHD})	1			ns	
RXD min. Valid time	T66 (T_{SMVLM})	2			ns	
RXD max. Valid time	T66a (T_{SMVLx})			5	ns	

4.5 Reset Timing Parameters

Figure 25. Reset Timing Parameters

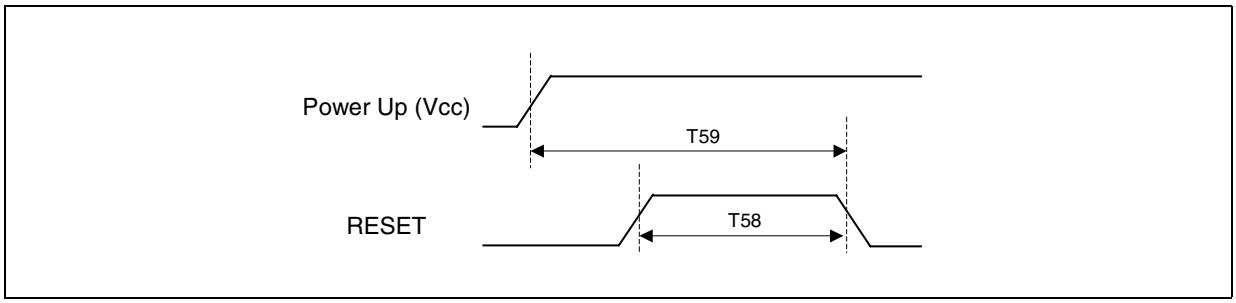


Table 40. Reset Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units	Condition
Reset pulse width	T58 (T_{RST_WID})	500			µs	
Power Up to falling edge of Reset	T59 (T_{POP_RST})	1000			µs	

4.6 Clock Specifications

4.6.1 MCLK Specifications

MCLK is the LXT9784 master clock. It is externally sourced by an oscillator. Table 41 defines the LXT9784 requirements from this signal.

Figure 26. Master Clock Specifications

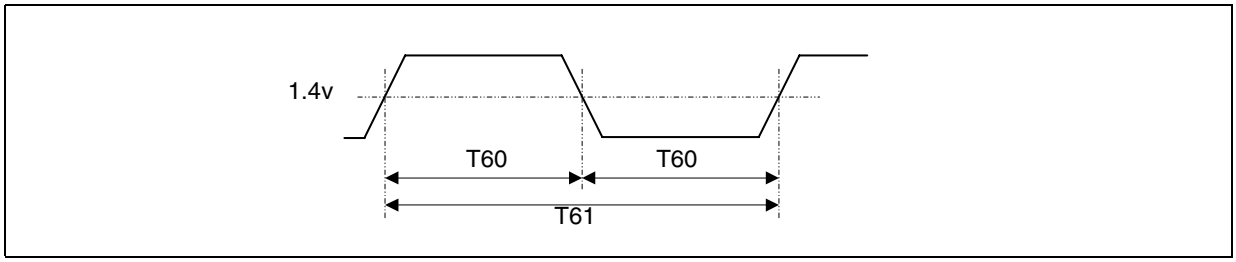


Figure 27. Master Clock Slope Specifications

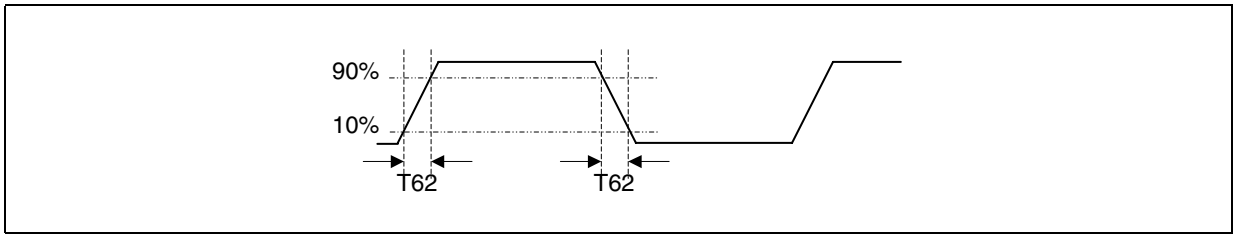


Table 41. MCLK Specifications

Parameter	Symbol	Min	Typ	Max	Units	Condition
MCLK Duty Cycle	T60 (T_{MCLK_DC})	35		65	%	
MCLK period	T61 (T_{MCLK_PR})		20		ns	**RMII** Mode - 50 MHz
MCLK period	T61 (T_{MCLK_PR})		8		ns	**SMII** Mode - 125 MHz
MCLK slope	T62 (T_{MCLK_SL})	3			V/ns	
MCLK jitter	T63 (T_{MCLK_JIT})			100	ps	Peak

1. The MCLK frequency shall be ±50 PPM.
2. Trace characteristic impedance (Z_0), 60W ±10%.

5.0 Register Definitions

The PHY registers can be accessed through the MII management interface.

Table 42 defines the bit type designations used in the following tables.

Table 42. Bit Type Designations

Designator	Definition
SC	Self Cleared
RO	Read Only
P	external Pin affects content
LL	Latch Low
LH	Latch High.

Table 43. Control Register (Register 0) Bit Definitions

Bit(s)	Name	Description	Type[1]
0.15	Reset	Sets the status and control register of the PHY to their default states and is self-clearing. The PHY returns a value of “1” when this register is read until the reset process has completed and accepts a read or write transaction. 1 = PHY reset. default 0 = normal operation.	RW SC
0.14	Loopback	Enable loopback of transmit data to the receive data path. The PHY receive circuitry is isolated from the network. Note that this may cause the de-scrambler to lose synchronization and produce 560 ns of “dead time”. 1 = Loopback enabled. default 0 = Loopback disabled (normal operation).	RW
0.13	Speed Selection	Controls speed when auto-negotiation is disabled. default 1 = 100 MBPS 0 = 10 MBPS	RW P
0.12	Auto-Negotiation Enable	Bits 0.13 & 0.8 (Speed Selection and Duplex Mode, respectively) are ignored when auto-negotiation is enabled. Bits 4.12:5 (Technology Ability Field) depends on the PHY ability (Register 0) to define the preferred link configuration. default 1 = auto-negotiation enable. 0 = auto-negotiation disable.	RW P
0.11	Power Down	1 = Analog section *only* power-down enabled. default 0 = Power-down disabled (normal operation).	RW
0.10	Isolate	Allows the PHY to isolate the Media Independent Interface. The PHY doesn't respond on the both transmit and receive activities. 1 = Logical isolate of internal MII interface. default 0 = Normal operation.	RW

1. Refer to Table 42 for Type definitions.

Table 43. Control Register (Register 0) Bit Definitions (Continued)

Bit(s)	Name	Description	Type[1]
0.9	Restart Auto-Negotiation	Restarts the auto-negotiation process and is self cleared after 300 ns 1 = Restart auto-negotiation process. default 0 = normal operation.	RW SC
0.8	Duplex Mode	Controls the duplex mode when auto-negotiation is disabled. If the PHY reports that it only able to operate in one duplex mode (via bits 1.15:11), the value of this bit shall correspond to the mode which the PHY can operate. When the PHY is placed in Loopback mode, the behavior of the PHY shall not be affected by the status of this bit, bit 0.8. 1 = Full Duplex. default 0 = Half Duplex.	RW
0.7	Collision Test	Force collision in response to the assertion of TXEN. 1 = Force COL. default 0 = disable Collision signal test.	RW
0.6:0	Reserved	Constant “0”.	RO

1. Refer to Table 42 for Type definitions.

Table 44. Status Register (Register 1) Bit Definitions

Bit(s)	Name	Description	Type[1]
1.15	100BASE-T4	Constant 0 = PHY not able to perform 100BASE-T4.	RO
1.14	Reserved	Constant “0”.	RO
1.13	100BASE-TX Half Duplex	1 = PHY able to perform half duplex 100BASE-TX 0 = PHY not able to operate in 100BASE-TX	RO
1.12	Reserved	Constant “0”.	RO
1.11	10 Mbps Half Duplex	1 = PHY able to operate at 10 Mbps in half duplex mode 0 = PHY not able to operate in 10BASE-T	RO
1.10:7	Reserved	Constant “0”.	RO
1.6	MF Preamble Suppression	Constant 0 = PHY will not accept management frames with preamble suppressed.	RO
1.5	Auto-Negotiation Complete	1 = Auto-Negotiation process completed default 0 = Auto-Negotiation process has not completed.	RO
1.4	Remote Fault	Constant 0 = no remote fault condition detected	RO
1.3	Reserved	Constant 0	RO
1.2	Link Status	1 = Valid link has been established. default 0 = Invalid link detected.	RO LL SC
1.1	Jabber Detect	This bit has meaning only in 10 Mbps mode. 1 = Jabber condition detected. default 0 = No jabber condition detected.	RO LH SC
1.0	Extended Capability	Constant 1 = Extended register capabilities enabled	RO

1. Refer to Table 42 for Type definitions.

Table 45. PHY Identifier Register (Register 2) Bit Definitions

Bit(s)	Name	Description	Type[1]
2.15:0	PHY ID (word MSB)	Value: 02A8 ‘h	RO
1. RO = Read Only.			

Table 46. PHY Identifier Register (Register 3) Bit Definitions

Bit(s)	Name	Description	Type[1]
3.15:0	PHY ID (word LSB)	Value: 0250 ‘h	RO
1. RO = Read Only.			

Table 47. Auto-Negotiation Advertisement Register (Register 4) Bit Definitions

Bit(s)	Name	Description	Type[1]
4.15	Next Page	Constant 0 = Transmitting primary capability data page.	RO
4.14	Reserved	Constant “0”.	RO
4.13	Remote Fault	1 = Indicates link partner’s remote fault. default 0 = No remote fault.	RW
4.12:5	Technology Ability Field	An 8-bit field containing information indicating supported technologies specific to the Selector Field value.	RW
4.12	Reserved	Ignore.	R/W
4.11	Reserved	Ignore	R/W
4.10	Pause	1 = Pause operation enabled for full-duplex links. 0 = Pause operation disabled.	R/W
4.9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. (The LXT9784 does not support 100BASE-T4 but allows this bit to be set to advertise in the Auto-Negotiation sequence for 100BASE-T4 operation. An external 100BASE-T4 transceiver could be switched in if this capability is desired.)	R/W
4.8	100BASE-TX full-duplex	1 = Port is 100BASE-TX full duplex capable. 0 = Port is not 100BASE-TX full duplex capable.	R/W
4.7	100BASE-TX	1 = Port is 100BASE-TX capable. 0 = Port is not 100BASE-TX capable.	R/W
4.6	10BASE-T full-duplex	1 = Port is 10BASE-T full duplex capable. 0 = Port is not 10BASE-T full duplex capable.	R/W
4.5	10BASE-T	1 = Port is 10BASE-T capable. 0 = Port is not 10BASE-T capable.	R/W
4.4:0	Selector Field	A 5-bit field identifying the type of message to be sent via Auto-Negotiation. default 00001’b (IEEE Standard 802.3)	RO
1. Refer to Table 42 on page 60 for Type definitions.			

Table 48. Auto-Negotiation Link Partner Ability Register (Base Page) (Register 5) Bit Definitions

Bit(s)	Name	Description	Type[1]
5.15	Next Page	Reflects the PHY's link partner's Auto-Negotiation ability	RO
5.14	Acknowledge	Indicates that the PHY has successfully received its link partner's Auto-Negotiation advertising ability.	RO
5.13	Remote Fault	Reflects the PHY's link partner's Auto-Negotiation ability.	RO
5.12:5	Technology Ability Field	Reflects the PHY's link partner's Auto-Negotiation ability.	RO
5.12	Reserved	Ignore.	RO
5.11	Reserved	Ignore	RO
5.10	Pause	1 = Link Partner is Pause capable. 0 = Link Partner is not Pause capable.	RO
5.9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	RO
5.8	100BASE-TX full duplex	1 = Link Partner is 100BASE-TX full duplex capable. 0 = Link Partner is not 100BASE-TX full duplex capable.	RO
5.7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	RO
5.6	10BASE-T full duplex	1 = Link Partner is 10BASE-T full duplex capable. 0 = Link Partner is not 10BASE-T full duplex capable.	RO
5.5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	RO
5.4:0	Selector Field	Reflects the PHY's link partner's Auto-Negotiation ability.	RO

1. RO = Read Only.

Table 49. Auto-Negotiation Expansion Register (Register 6) Bit Definitions

Bit(s)	Name	Description	Type[1]
Bit(s)	Name	Description	R/W
6:15:5	Reserved	Constant "0".	RO
6.4	Parallel detection fault	1 = Fault detected via parallel detection (multiple link fault occurred). default 0 = No fault detected via the parallel detection.	RO LH SC
6.3	Link Partner Next Page Able	1 = Link Partner is Next Page able. default 0 = Link Partner is not Next Page able.	RO
6.2	Next Page Able	Constant 0 = Local device is not Next Page able.	RO
6.1	Page Received	1 = New Page received. default 0 = New Page not received.	RO LH SC
6.0	Link Partner Auto-Negotiation Able	1 = Link Partner is Auto-Negotiation able default 0 = Link Partner is not Auto-Negotiation able	RO

1. Refer to Table 42 on page 60 for Type definitions.

Note: Registers 8-15 are IEEE reserved

Table 50. Register 16 (10 Hex) Status and Control

Bit(s)	Name	Description	Type[1]
Bit(s)	Name	Description	R/W
16.15:14	Reserved	Constant “0”.	RO
16.13	Reserved	Constant “0”.	RW
16.12	Reserved	Constant “0”.	RO
16.11	Receive De-Serializer In-Sync Indication	Indicates status of the 100BASE-TX Receive De-Serializer In-Sync Indication.	RO
16.10	100BASE-TX Power-Down	Indicates the power state of 100BASE-TX. 1 = Power-Down. 0 = Normal operation.	RO
16.9	10BASE-T Power-Down	Indicates the power state of 10BASE-T. 1= Power-Down. 0= Normal operation.	RO
16.8	Polarity	Indicates 10BASE-T polarity. 1 = Reverse polarity. 0 = normal polarity.	RO
16.7	Reserved	Must be set to zero during write.	RO
16.6:2	PHY Address	Value determined by ID[1:0] and PHY port number (which of 8)	RO
16.1	Speed	Indicates the Auto-Negotiation result. 1 = 100 Mbps. 0 = 10 Mbps.	RO
16.0	Full Duplex	Indicates the Auto-Negotiation result. 1 = Full Duplex. 0 = Half Duplex.	RO
1. Refer to Table 42 on page 60 for Type definitions.			

Table 51. Register 17 (11 Hex) Special Control

Bit(s)	Name	Description	Type[1]
17.15	Scrambler By-pass	Scrambler by-pass control. 1 = By-pass Scrambler. default 0 = Normal Operation.	RW P
17.14	By-pass 4B/5B	1= 4 bit to 5 bit encoder by-pass. default 0 = Normal Operation.	RW P
17.13	Force Transmit H-Pattern	1 = Force transmit H-pattern. default 0 = Normal Operation.	RW
17.12	Force 34 Transmit Pattern	1 = Force 34 transmit pattern. default 0 = Normal Operation.	RW P
17.11	Good Link	1 = 100BASE-TX good link indication forcing to ASD output. default 0 = Normal operation.	RW P
17.10	Reserved	Must be set to zero during write	RW
1. Refer to Table 42 on page 60 for Type definitions.			

Table 51. Register 17 (11 Hex) Special Control (Continued)

Bit(s)	Name	Description	Type[1]
17.9	Carrier Sense Disable	Controls the RX100 CRS disable function 1 = CRS disable. default 0 = CRS enable.	RW
17.8	Reserved	Must be set to zero during write	RW
17.7	Auto-Negotiation Loopback	1 = Auto-Negotiation Loopback. default 0 = Auto-Negotiation normal mode.	RW
17.6	MDI Tri-state	1 = MDI Tri-state (transmit driver tri-states) default 0 = Normal operation	RW
17.5	Force Polarity	1 = Reversed polarity default 0 = Normal polarity operation.	RW
17.4	Auto Polarity Disable	1 = Auto Polarity disabled. default 0 = Auto Polarity enabled.	RW
17.3	SQE Disable	1 = 10BASE-T squelch test disabled. default 0 = Normal squelch operation	RW
17.2	Extended Squelch	Extended Squelch control. 1 = 10BASE-T extended squelch control enabled. 0 = 10BASE-T extended squelch control disabled.	RW
17.1	Link Integrity Disable	1 = Link disabled. default 0 = Normal Link Integrity operation.	RW P
17.0	Jabber Function Disable	1 = Jabber disabled. default 0 = Normal Jabber operation.	RW

1. Refer to Table 42 on page 60 for Type definitions.

Table 52. Register 18 (12 Hex) PHY Interrupt Register

Bit(s)	Name	Description	Type[1]
18.15:2	Reserved	Constant “0”.	RO
18.1	Interrupt Enable	Enables the assertion of a specific PHY Interrupt line. However, bit 0 is not masked, and the interrupt bit will remain visible. 1 = enable the assertion of the interrupt line. default 0 = disable the interrupt line.	RW
18.0	Link Status Interrupt	Reflects the PHY link integrity changing. The bit is self-cleared after any read cycle. 1 = a change on PHY link status was detected.	RO SC

1. Refer to Table 42 on page 60 for Type definitions.

Table 53. Reg 19 (13 Hex) 100 BASE-TX RCV False Carrier Counter

Bit(s)	Name	Description	Type[1]
19[15:0]	False Carrier Sense	A 16 bit counter that increments for each false carrier event (bad SSD). The counter stops when full (and does not roll over.) Self clears on read.	RO SC

1. Refer to Table 42 on page 60 for Type definitions.

Table 54. Reg 20 (14 Hex) 100BASETx Receive Disconnect Counter

Bit(s)	Name	Description	Type[1]
20[15:0]	Disconnect Event	A 16 bit counter that increments for each disconnect event. The counter stops when full (and does not roll over). Self clears on read. Two or more consecutive False carrier events causes this counter to increment.	RO SC
1. RO = Read Only; SC = Self Cleared.			

Table 55. Reg 21 (15 Hex) 100BASETx Receive Error Frame Counter

Bit(s)	Name	Description	Type[1]
21[15:0]	Receive Error Frame	A 16 bit counter that increments once per frame for any receive error condition, such as a symbol error or premature end of frame, in that frame. The counter stops when full (and does not roll over). Self clears on read.	RO SC
1. RO = Read Only; SC = Self Cleared.			

Table 56. Reg 22 (16 Hex) Receive Symbol Error Counter

Bit(s)	Name	Description	Type[1]
22[15:0]	Symbol Error Counter	A 16-bit counter that increments for each symbol error. The counter stops when full (and does not roll over). Self clears on read.	RO SC
1. RO = Read Only; SC = Self Cleared.			

Table 57. Reg 23 (17 Hex) 100BASETx Receive Premature End of Frame Error Counter

Bit(s)	Name	Description	Type[1]
23[15:0]	Premature End of Frame	A 16-bit counter that increments for each premature end of frame event. The counter stops when full (and does not roll over). Self clears on read. A frame without a “TR” at the end is considered a premature end of frame event.	RO SC
1. RO = Read Only; SC = Self Cleared.			

Table 58. Reg 24 (18 Hex) 10BASET Receive End of Frame Error Counter

Bit(s)	Name	Description	Type[1]
24[15:0]	End of Frame Counter	A 16-bit counter which increments for each end of frame error event. The counter stops when full (and does not roll over). Self clears on read.	RO SC
1. RO = Read Only; SC = Self Cleared.			

Table 59. Reg 25 (19 Hex) 10BASET Transmit Jabber Detect Counter

Bit(s)	Name	Description	Type[1]
25[15:0]	Jabber detect counter	A 16-bit counter which increments for each jabber detection event. The counter stops when full (and does not roll over). Self clears on read.	RO SC
1. RO = Read Only; SC = Self Cleared.			

Table 60. Reg 26 (1A Hex) Reserved

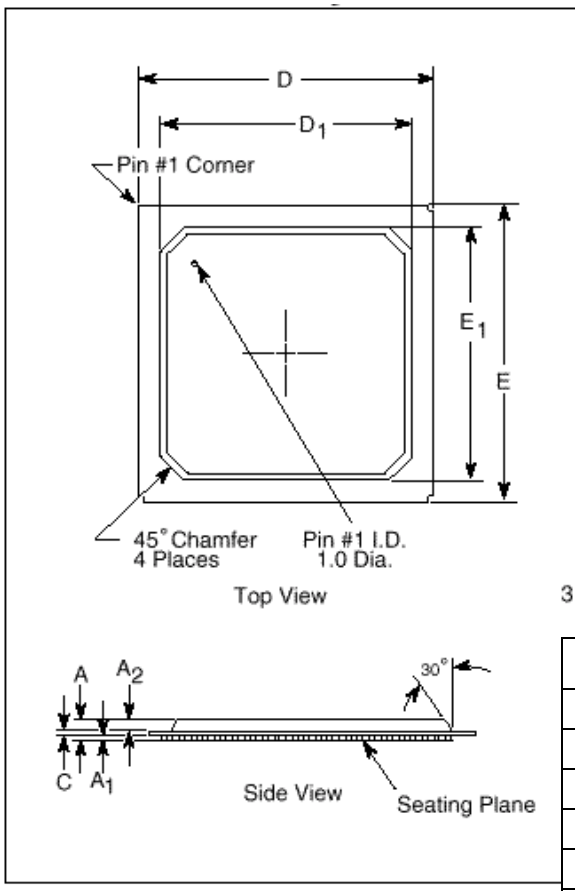
Bit(s)	Name	Description	Type[1]
26[15:0]	Reserved	Data read from this should be ignored.	RO
1. RO = Read Only.			

Table 61. Register 27 (1B Hex) PHY Special Control

Bit(s)	Name	Description	Type[1]
27.15:5	Reserved	Constant “0”.	RO
27.4	LED Blink	1 = LED blink disabled. default 0 = LED blink enabled (normal operation).	RW
27.3	100RX Jabber Enable	Enables carrier sense disconnection while PHY in jabber at 100Mbps. 1 = Carrier sense disconnection enabled. default 0 = Carrier sense disconnection disabled.	RO
27.2:0	LED Switch Control	[2:0] LEDA LEDB LEDC 000 Link/Activity Speed Collision (RMII, SMII modes) 001 Collision Speed Speed 010 Link Speed Speed 011 Collision Speed Activity 100 OFF Speed OFF 101 ON Speed OFF 110 OFF Speed ON 111 ON Speed ON	RW
1. RO = Read Only; RW = Read/Write.			

6.0 Mechanical Specifications

Figure 28. Package Specifications



	Parameter	Min	Max
N	Ball Count	324	
A	Overall Height	1.94	2.32
A_1	Stand Off	0.50	0.70
A_2	Encapsulation Height	1.12	1.22
D	Package Body Length	26.80	27.20
D_1	Encapsulant Length	23.75	24.25
S_1	Outer Ball Center to Edge of Body	1.44 REF	
B	Ball Diameter	0.60	0.90
C (2L/4L)	Substrate Thickness	.32/.52	.40/.60
E	Ball Pitch	1.27mm	
1. All dimensions in millimeters			