IMI145156

INTERNATIONAL MICROCIRCUITS INC

CMOS LSI
SERIAL INPUT PLL FREQUENCY SYNTHESIZER

T-50-17

PRODUCT FEATURES

- >30 MHz Typical Input Capability @ V_{DD} = 5V
- On- or Off-Chip Reference Oscillator Operation with Buffered Output
- Compatible with the SPI (Serial Peripheral Interface) on CMOS MCU's
- Lock Detect Signal
- Two Open-Drain Switch Outputs
- Dual Modulus/Serial Programming
- 8 User-Selectable ÷R Values: 8, 64, 128, 256, 640, 1000, 1024, 2048
- ÷N Range = 3 to 1023; ÷A Range = 0 to 127
- Linearized Digital Phase Detector Enhances Transfer Function Linearity
- Two Error Signal Options: Single-Ended (3-State), Double-Ended
- Packaging Options Include: Plastic and Ceramic Dual-In-Line, Plastic J-Leaded, and Ceramic Leadless Chip Carriers, and Small-Outline Packages. Die are available for Hybrid Applications.
- Grades Available Include: Commercial, Military Operating Range, and Military Screened

PRODUCT DESCRIPTION

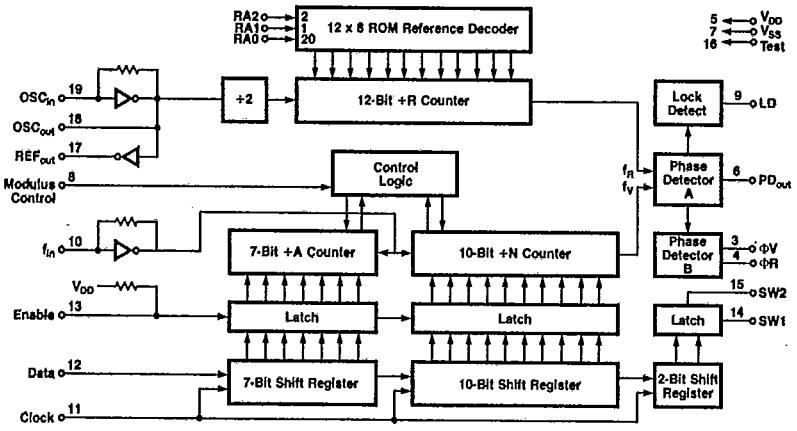
The IMI145156 is one of a family of LSI PLL frequency synthesizers from International Microcircuits. In the 20-pin ceramic or plastic dual-in-line packages, this product is pin-for-pin compatible with the MC145156, and can be used as a direct replacement with identical or superior operating characteristics. This product can be alternatively packaged to meet your needs. MIL-STD-883 screening is available for high-reliability applications.

The IMI145156 is programmed by a clocked, serial input 19-bit data stream. The device features a reference oscillator, selectable-reference divider, digital-phase detector, 10-bit programmable ÷N counter and 7-bit programmable ÷A counter, and the necessary shift register and latch circuitry for accepting the serial input data. When combined with a loop filter and VCO, the IMI145156 can provide all the remaining functions for a PLL frequency synthesizer operating up to the device's frequency limit. For higher VCO frequency operation, a down mixer or a dual modulus prescaler can be used between the VCO and IMI145156.

The IMI145155, IMI145156, IMI145157, and IMI145158 CMOS PLL frequency synthesizers have serial programmable inputs with a single or dual modulus capability, transmit/receive offsets, selection of phase detector type, and choice of reference divider integer values.

If your application requires additional features, please contact our factory. Our engineers can quickly design a product to meet your requirements.

BLOCK DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +10	Vdc
Input Voltage, All Inputs	V_{in}	−0.5 to V_{DD} +0.5	Vdc
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

(Voltage Referenced to V_{SS})

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, V_{in} and V_{out} should be constrained to the range:

$$V_{SS} < (V_{in} \text{ or } V_{out}) < V_{DD}$$

Unused inputs must always be tied to an appropriate logic voltage level (either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD}	−55°C		−40°C		25°C			85°C		125°C		Units
			Min	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max	
Power Supply Voltage	V_{DD}	—	3	8	3	8	3	—	8	3	8	3	8	Vdc
Output Voltage V_{in} = V_{DD} or 0	V_{OL}	3	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	Vdc
		5	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	
		8	—	0.05	—	0.05	—	0	0.05	—	0.05	—	0.05	
V_{in} = 0 or V_{DD}	V_{OH}	3	2.95	—	2.95	—	2.95	3	—	2.95	—	2.95	—	
		5	4.95	—	4.95	—	4.95	5	—	4.95	—	4.95	—	
		8	7.95	—	7.95	—	7.95	8	—	7.95	—	7.95	—	
Input Voltage V_O = 2.5 or 0.5	V_{IL}	3	—	0.9	—	0.9	—	1.35	0.9	—	0.9	—	0.9	Vdc
V_O = 4.5 or 0.5		5	—	1.5	—	1.5	—	2.75	1.5	—	1.5	—	1.5	
V_O = 7.5 or 1.5		8	—	2.4	—	2.4	—	3.65	2.4	—	2.4	—	2.4	
V_O = 0.5 or 2.5	V_{IH}	3	2.1	—	2.1	—	2.1	1.65	—	2.1	—	2.1	—	
V_O = 0.5 or 4.5		5	3.5	—	3.5	—	3.5	2.75	—	3.5	—	3.5	—	
V_O = 1.5 or 7.5		8	5.6	—	5.6	—	5.6	4.45	—	5.6	—	5.6	—	
Output Current V_{OH} = 2.7	I_{OH}	3	−1.6	—	−1.6	—	−1.4	−2.0	—	−0.8	—	−0.8	—	mAdc
V_{OH} = 4.6		5	−2.4	—	−2.4	—	−2.0	−2.8	—	−1.6	—	−1.6	—	
V_{OH} = 7.5		8	−4.8	—	−1.6	—	−3.6	−4.6	—	−2.8	—	−2.8	—	
V_{OH} = 2.7 REF_{out}	I_{OH}	3	−0.5	—	−0.45	—	−0.35	—	—	−0.28	—	−0.28	—	
V_{OH} = 4.6 only		5	−1.1	—	−1.00	—	−0.60	—	—	−0.50	—	−0.50	—	
V_{OH} = 7.5		8	−1.7	—	−1.55	—	−1.10	—	—	−0.90	—	−0.90	—	
V_{OH} = 2.7 OSC_{out}	I_{OH}	3	−0.17	—	−0.16	—	−.125	—	—	−.090	—	−.090	—	
V_{OH} = 4.6 only		5	−0.30	—	−0.28	—	−.225	—	—	−0.18	—	−0.18	—	
V_{OH} = 7.5		8	−0.35	—	−0.34	—	−.300	—	—	−0.25	—	−0.25	—	
V_{OL} = 0.3	I_{OL}	3	1.6	—	1.6	—	1.4	2.0	—	0.8	—	0.8	—	
V_{OL} = 0.4		5	2.4	—	2.4	—	2.0	2.8	—	1.6	—	1.6	—	
V_{OL} = 0.5		8	4.8	—	4.8	—	3.6	4.6	—	2.8	—	2.8	—	
V_{OL} = 0.3 REF_{out}	I_{OL}	3	0.6	—	0.55	—	0.42	—	—	0.28	—	0.28	—	
V_{OL} = 0.4 only		5	1.1	—	1.00	—	0.90	—	—	0.70	—	0.70	—	
V_{OL} = 0.5		8	2.2	—	2.10	—	1.70	—	—	1.40	—	1.40	—	
V_{OL} = 0.3 OSC_{out}	I_{OL}	3	0.320	—	0.310	—	0.250	—	—	0.180	—	0.180	—	
V_{OL} = 0.4 only		5	0.480	—	0.470	—	0.400	—	—	0.300	—	0.300	—	
V_{OL} = 0.5		8	0.600	—	0.580	—	0.500	—	—	0.400	—	0.400	—	
Input Current Enable	I_{IL}	8	—	−400	—	−400	—	−90	−200	—	−170	—	−170	
f_{in}, OSC_{in}	I_{IN}	8	—	±50	—	±50	—	±10	±25	—	±22	—	±22	
Other Inputs	I_{IH}	8	—	±0.3	—	±0.3	—	±.00001	±0.1	—	±1.0	—	±1.0	μAdc
Input Capacitance	C_{in}	3–8	—	10	—	10	—	6	10	—	10	—	10	pF
Output Capacitance	C_{out}	3–8	—	10	—	10	—	6	10	—	10	—	10	pF
3-State Leakage Current PD_{out}	I_L	8	—	±0.1	—	±0.1	—	±0.0001	±0.1	—	±10	—	±10	μAdc
Quiescent Current (Static)	I_{DD}	8	—	150	—	150	—	40	150	—	150	—	150	μAdc

SWITCHING CHARACTERISTICS

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Units
Output Rise and Fall Time OSC_{out} REF_{out}	t_{TLH} t_{THL}	3	—	30	40	ns
		5	—	20	30	
		8	—	10	20	
Others		3	—	15	20	
		5	—	10	15	
		8	—	5	10	
Propagation Delay Time f_{in} to Modulus Control	t_{PLH} t_{PHL}	3	—	55	125	ns
		5	—	40	80	
		8	—	25	50	
Propagation Delay Time Enable to SW1, SW2	t_{PHL}	3	—	40	100	ns
		5	—	30	60	
		8	—	20	40	
Setup Time Data to Clock	t_{SU}	3	50	20	—	ns
		5	40	10	—	
		8	30	9	—	
Clock to Enable	t_{SU}	3	100	30	—	ns
		5	50	15	—	
		8	30	10	—	
Hold Time Clock to Data	t_H	3	10	5	—	ns
		5	15	8	—	
		8	20	10	—	
Recovery Time Enable to Clock	t_{REC}	3	10	−2	—	ns
		5	15	−3	—	
		8	20	−3	—	
Output Pulse Width PHIR, PHIV with f_R in Phase with f_V	$t_{WH(O)}$	3	70	250	500	ns
		5	40	150	300	
		8	30	100	200	
Input Rise and Fall Times OSC_{in}, f_{in}	t_{TLH} t_{THL}	3	—	10	5	μs
		5	—	5	2	
		8	—	2	0.5	
Input Pulse Width Clock, Enable	t_W	3	60	30	—	ns
		5	50	25	—	
		8	40	20	—	

(TA = −55°C to +125°C, C_L = 50 pF)

FREQUENCY CHARACTERISTICS

Characteristic	Symbol	Division Ratio	V_{DD}	−55°C to 125°C Max	Typical	−40°C to 85°C Max	Units
Operating Frequency f_{in} OSC_{in} Input=SQ Wave V_{DD}-V_{SS} or Sinewave 500mVP-P	f_{max}	≥10	3	10	28	11	MHz
			5	15	30	17	
			8	20	30	21	
		3*	3	3.5	12	4	
			5	5	16	6	
			8	8	24	9	

*NOTE: This frequency applies only to f_{in} input.

PIN DESCRIPTIONS

RA0, RA1, RA2 (Pins 20, 1, and 2) – These three inputs establish a code defining one of eight possible divide values for the total reference divider, as defined by the table below.

Reference Address Code			Total Divide Value
RA2	RA1	RA0	
0	0	0	8
0	0	1	64
0	1	0	128
0	1	1	256
1	0	0	640
1	0	1	1000
1	1	0	1024
1	1	1	2048

ΦR, ΦV (Pins 3 and 4) – These phase detector outputs can be combined externally for a loop error signal. A single-ended output is also available for this purpose (see PD_{out}).

If frequency f_V is greater than f_R or if the phase of f_V is leading, then error information is provided by ΦV pulsing low. ΦR remains essentially high.

If the frequency of f_V is less than f_R or if the phase of f_V is lagging, then error information is provided by ΦR pulsing low. ΦV remains essentially high.

If the frequency of $f_V = f_R$ and both are in phase, both ΦV and ΦR remain high except for a small minimum time period when both pulse low in phase.

V_{DD} (Pin 5) – Positive power supply.

PD_{out} (Pin 6) – Three state output of phase detector for use as loop error signal. Double-ended outputs are also available for this purpose (see ΦV and ΦR).

Frequency $f_V > f_R$ or f_V leading: negative pulses
Frequency $f_V < f_R$ or f_V lagging: positive pulses
Frequency $f_V = f_R$ and phase coincidence: High-Impedance state.

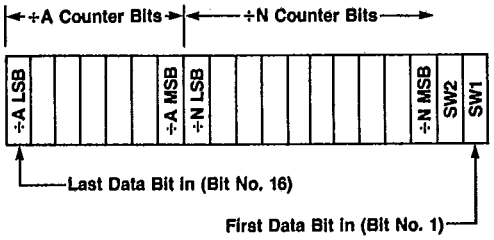
V_{SS} (Pin 7) – Circuit ground.

MODULUS CONTROL (Pin 8) – Signal generated by the on-chip control logic circuitry for controlling an external dual modulus pre-scaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the ÷A counter has counted down from its programmed value. At this time, modulus control goes high and remains high until the ÷N counter has counted the rest of the way down from its programmed value (N – A additional counts since both ÷N and ÷A are counting down during the first portion of the cycle). Modulus control is then set back low, the counters preset to their respective programmed values, and the above sequence repeated. This provides for a total programmable divide value (N_T)=N*P+A, where P and P+1 represent the dual modulus prescaler divide values respectively for low and high modulus control levels; N the number programmed into the ÷N counter, and A the number programmed into the ÷A counter.

LD (Pin 9) – Lock detector signal. High level when loop is locked (f_R, f_V same phase and frequency). Pulses low when loop is out of lock.

f_{in} (Pin 10) – Input to the positive edge triggers ÷N and ÷A counters, f_{in} is typically derived from a dual modulus prescaler and is AC coupled into Pin 10. For larger amplitude signals (standard CMOS logic levels) DC coupling may be used.

CLOCK, DATA (Pins 11 and 12) – Shift register clock and data input. Each low-to-high transition clocks one bit into the on-chip 19-bit shift register. The data is presented on the DATA input at the time of the positive clock transition. The DATA input provides programming information for the 10-bit ÷N counter, the 7-bit ÷A counter, and the two switch signals SW1 and SW2. The entry format is as follows:



ENABLE (Pin 13) – When high (1) transfers contents of the shift register into the latches, and to the programmable counter inputs and the switch outputs SW1 and SW2. When low (0) inhibits the above action and allows changes to be made in the shift register data without affecting the counter programming and switch outputs. An on-chip- pull-up establishes a continuously high level for ENABLE when no external signal is applied to Pin 13.

SW1, SW2 (Pins 14 and 15) – SW1 and SW2 provide latched open drain outputs corresponding to data bits numbers one and two. These will typically be used for band switch functions. A logic one will cause the output to assume a high-impedance state, while a logic zero will cause an output logic zero.

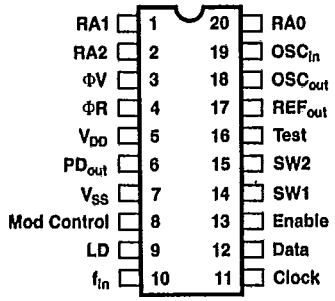
TEST (Pin 16) – Used in manufacturing. Must be left open or tied to V_{SS}.

REF_{out} (Pin 17) – Buffered output of on-chip reference oscillator or externally provided reference-input signal.

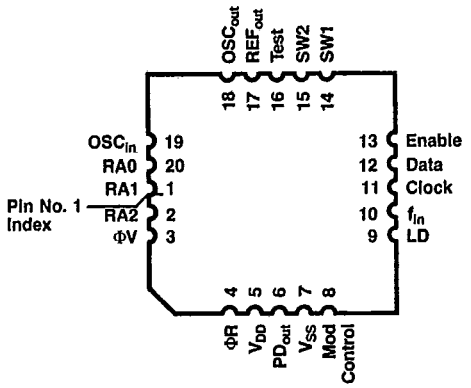
OSC_{out}, OSC_{in} (Pins 18 and 19) – These pins form an on-chip reference oscillator when connected to terminals of an external parallel resonant crystal. Frequency-setting capacitors of appropriate value must be connected from OSC_{in} to ground and OSC_{out} to ground. OSC_{in} may also serve as input for an externally generated reference signal. This signal will typically be AC coupled to OSC_{in}, but for larger amplitude signals (standard CMOS logic levels) DC coupling may also be used. In the external reference mode, no connection is required to OSC_{out}.

CONNECTION DIAGRAMS

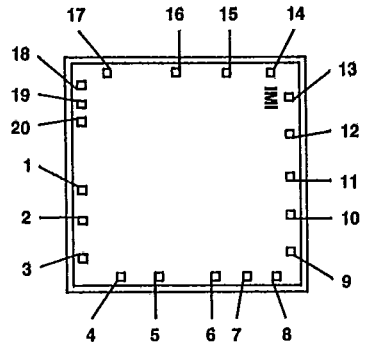
DUAL-IN-LINE PACKAGES



CHIP CARRIER



DIE LAYOUT



NOTE: Pin numbers correspond to DIP pin-out.

ORDERING INFORMATION

VALID COMBINATIONS:

IMI145156020**PB**
IMI145156020**QB**
IMI145156020**XB**
IMI145156020**ST**
IMI145156020**SK**
IMI145156020**LT**
IMI145156020**LK**
IMI145156000**DG**
IMI145156000**DQ**

For detailed ordering information see page 2.

DUAL MODULUS PRESCALING

The technique of dual modulus prescaling is well established as a method of achieving high-performance frequency synthesizer operation at high frequencies. The approach allows relatively low-frequency programmable counters to be used as high-frequency programmable counters with speed capability of several hundred MHz. This is possible without the sacrifice in system resolution and performance that would otherwise result if a fixed (single modulus) divider was used for the prescaler.

In dual modulus prescaling, the lower-speed counters must be uniquely configured. Special control logic is necessary to select the divide value P or P+1 in the prescaler for the required amount of time (see modulus control definition). The IMI145156 contains this feature, and can be used with a variety of dual modulus prescalers to allow speed, complexity, and cost to be tailored to the system requirements. Prescalers with P, P+1 divide values in the range of ÷3/÷4 to ÷128/÷129 can be controlled by the IMI145156.

DESIGN GUIDELINES APPLICABLE TO THE IMI145156

The system total divide value (N_{total}) will be dictated by the application:

$$N_{total} = \frac{\text{frequency into the prescaler}}{\text{frequency into the phase detector}} = N*P+A$$

N is the number programmed into the ÷N counter; A is the number programmed into ÷A counter. P and P+1 are two selectable divide ratios available in the two modulus prescalers. To have a range of N_{total} values in sequence, the ÷A counter is programmed from zero through P−1 for a particular value N in the ÷N counter. N is then incremented to N+1, and the ÷A is sequenced from zero through P−1 again.

There are minimum and maximum values that can be achieved for N_{total}. These are a function of P and the size of the ÷N and ÷A counters. The constraint N>A always applies. If $A_{max} = P-1$, then $N_{min} \geq P-1$; then $N_{total-min} = (P-1)P+A$ or $(P-1)P$, since A is free to assume the value of zero.

$$N_{total-max} = N_{max}*P+A_{max}$$

To maximize system frequency capability, the dual modulus prescaler's output must go from low to high after each group of P or P+1 input cycles. The prescaler should divide by P when its modulus control line is high, and by P+1 when its modulus control is low.

For the maximum frequency into the prescaler (F_{VCO} max), the value used for P must be large enough so that:

A. F_{VCO} max divided by P may not exceed the frequency capability of Pin 10 of the IMI145156.

B. The period of F_{VCO} divided by P must be greater than the sum of the times:

   a. Propagation delay through the dual modulus prescaler.

   b. Prescaler setup or release time relative to its modulus control signal.

   c. Propagation time from f_{in} to the modulus control output for the IMI145156.

A sometimes useful simplification in the IMI145156 programming code can be achieved by choosing the values for P of 8, 16, 32, 64, or 128. For these cases, the desired value to N_{total} will result when N_{total} in binary is used as the program code to the ÷N and ÷A counters in the following manner:

A. Assume the ÷A counter contains "b" bits where $2^b=P$.

B. Always program all higher order ÷A counter bits above "b" to zero.

C. Assume the ÷N counter and ÷A counter (with all the higher order bits above "b" ignored) combined into a single binary counter of 10+b bits in length. The MSB of this hypothetical counter is to correspond to the MSB of ÷N, and the LSB is to correspond to the LSB of ÷A. The system divide value, N_{total}, now results when the value of N_{total} in binary is used to program the "new" 10+b bit counter.