GM6486

33 OUTPUT LED DRIVER

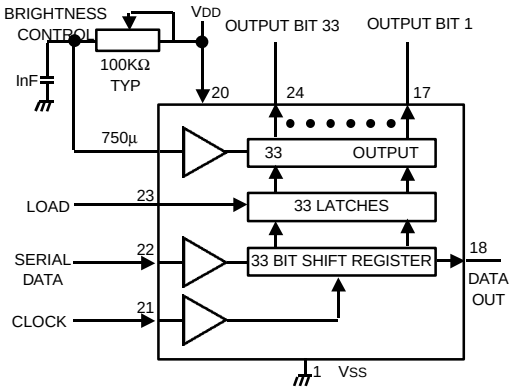
General Description

The GM6486 is a monolithic MOS integrated circuit produced with high voltage CMOS technology. It is available in a 40-pin dual in-line plastic package. A sin-gle pin controls the LED display brightness by setting a reference current through a variable resistor connect-ed to VDD or to a separated supply of 13.2V maximum.

Features

- 33 Output, 15mA Sink Capability
- Current Generator Outputs (No External Resistros Required)
- Continous Brightness Control
- Serial Data Input-Output
- External Load Input
- Cascade operation capability
- Wide supply voltage range
- TTL compatibility

Block Diagram

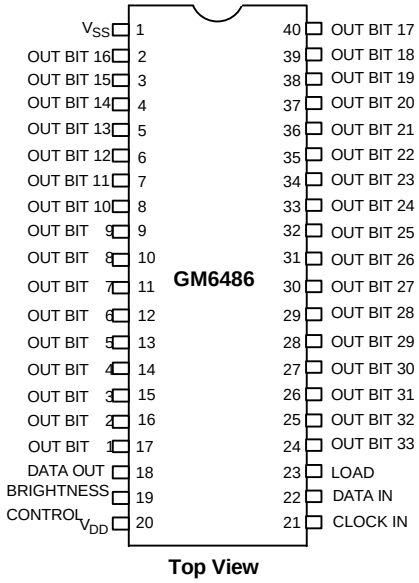


Application

- Microprocessor Displays
- Industrial control Indicator
- Relay Driver
- Instrumentation Readouts

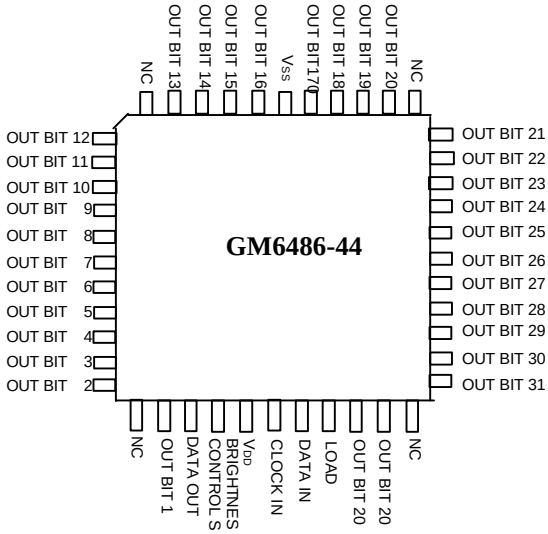
Pin Configuration

40 PIN DIP



Top View

44 PIN PLCC



Absolute Maximum Rating

SYMBOL	PARAMETER	RATINGS	UNIT
V_{DD}	Supply Voltage	-0.3 to 15	V
V_{IN}	Input Voltage	-0.3 to 15	V
V_O(off)	Off State Output Voltage	15	V
I_O	Output Sink Current	40	mA
P_{tot}	Total Package Power Dissipation	1 (at 25 °C)	W
		560 (at 85 °C)	mW
T_j	Junction Temperature	150	°C
T_{op}	Operating Temperature Range	-25 to 85	°C
T_{stg}	Storage Temperature Range	-65 to 150	°C

Electrical Characteristics

(T_{amb} within operating range, V_{DD} =4.75V to 13.2V V_{SS} =0, unless otherwise specified)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		4.75		13.2	V
I_{DD}	Supply Current	V_{DD} =13.2V All Control Inputs at V_{SS} =0V		50	1000	μA
V_{IL} V_{IH}	Input Voltage Logical "0" Level Logical "1" Level	±10μA Input Bias $4.75 \le V_{DD} \le 5.25$ V_{DD} >5.25	-0.3 2.2 V_{DD} -2		0.8 V_{DD} V_{DD}	V V V
I_b	Brightness input current (Note 1)				0.75	mA
V_b	Brightness input voltage (Pin 19)	Input Current=750 μA	3		4.3	V
V_O(off)	Off State out. Voltage				13.2	V
I_{OH} I_{OL}	Output sink current (Note 2) Segment off Segment on	 V_o = 3V V_o = 1V (Note 3) Bright in =0 μA Bright in =100 μA Bright in =750 μA	 0 2 12	 2.7 15	 10 10 4 25	 μA μA mA mA
I_O	Maximum Segment Current				40	mA

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
O_M	Output Matching (Note 4)				±20	%
V_{OL}	Data Output Logical "0" Level	I_{OUT} = 0.5mA	V_{SS}		0.4	V
V_{OH}	Logical "1" Level	I_{OUT} = 100μA	2.4		V_{DD}	V
f_C	Clock Input Frequency	(notes 5 and 6)			500	KHz
th	High Time		950			ns
t_l	Low Time		950			ns
t_{DS}	Data Input Set-up time		300			ns
t_{DH}	Hold time		300			ns
t_{DES}	Data Enable Input Set-up time		100			ns

Note: 1. With a fixed resistor on the brightness input, some variation in brightness will occur from one device to another.

2. Absolute maximum for each output should be limited to 40 mA.
3. The V_o voltage should be regulated by the user. See figures 6 and 7 for allowable V_o versus I_o operation.
4. Output matching is calculated as the percent variation (lmax+lmin)/2.
5. AC input waveform specification for test prupose: $t_r \leq 20ns$. $t_f \leq 20ns$. f=500kHz ± 10% duty cycle
6. Clock Input rise and fall times must not exceed 300ns.

Functional Description

The GM6486 is specifically designed to operate 4 digit displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 3 signals, serial data, clock and load.

The 33 data bits are latched by a positive pulse, thus providing non-multiplexed direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current of LED drivers. A 1nF capacitor should be connected to brightness control, pin 19, to prevent possible oscillation. A block diagram is shown in figure 1.

The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400 Ω nominal value.

Figure 2 and 3 show the input data format. Bit "1" is the first bit into the data input pin and it will appear on pin 17. A logical "1" at the input will turn on the appropriate LED. The LOAD signal latches the 33 bit of the shift registers into the latches. The data out pin allows for cascading the shift registers for more than 33 output drivers. When power is first applied to the chip an internal power ON reset signal is generated which resets all registers and all latches.

The first clock return the chip to its normal operation.

Figure 4 shows the timing relationship between data, clock and load.

A max clock frequency of 0.5MHz is assumed.

For applications where less number of outputs are used, it is possible to either increase the current per output or operate the part at higher than 1V V_o.

The following equation can be used for calculation.

$T_j = [(V_o) \bullet (I_{LED}) \bullet (\text{No. of segments}) + (Vdd \times 7mA)](124\,^{\circ}C/W) + Tamb$

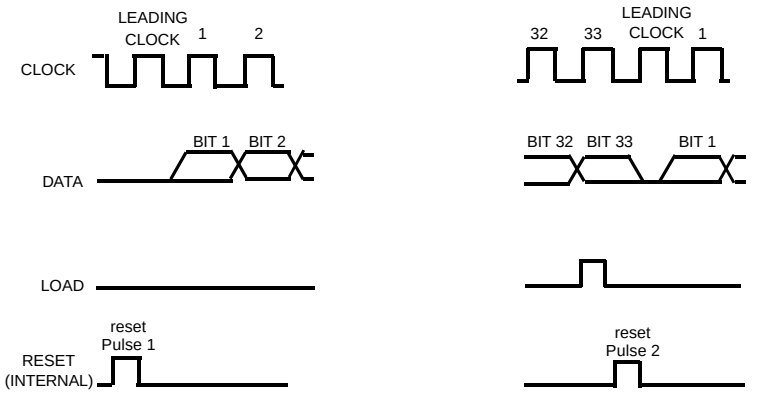
where

T_j = junction temperature (+150 °C max) 124 °C /W=thermal coefficient of package

V_o =the voltage at the LED driver outputs Temb=ambient temperature

I_{LED} =the LED current

The above equation was used to plot figure 5, 6 and 7.



- leading clock is necessary after power on and load signal high.
- reset pulse 1: internal pulse that comes after power on–effective on both shift register and latches
- reset pulse 2: internal pulse that comes load pulse–effective on shift register only.

Fig. 2. Data Input Format

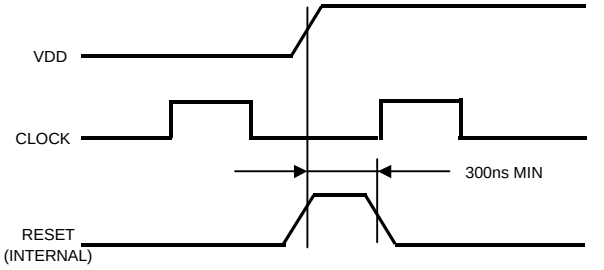


Fig. 3. Power On Reset

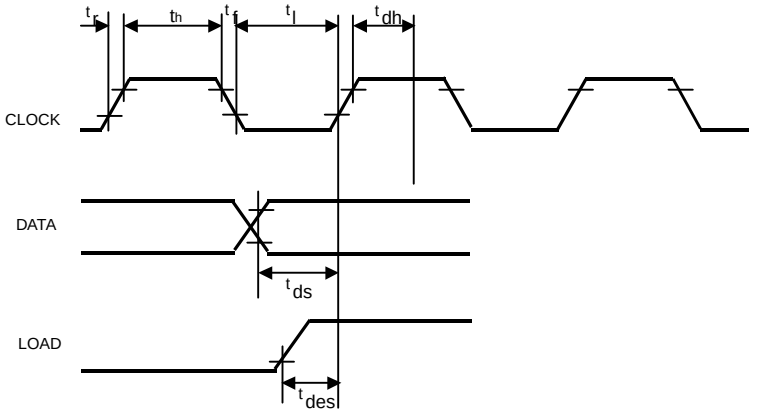


Fig. 4. Timing Diagram

Fig. 5

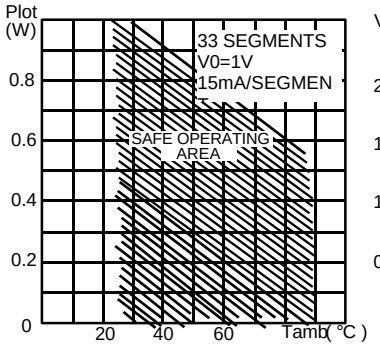


Fig. 6

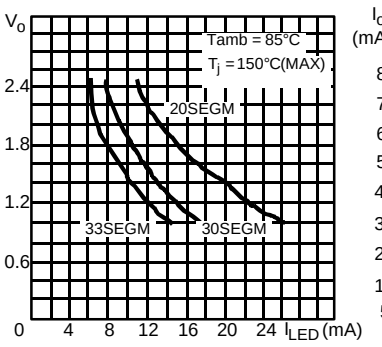
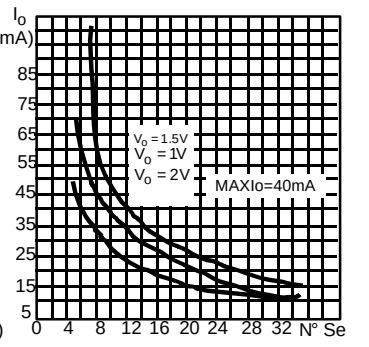
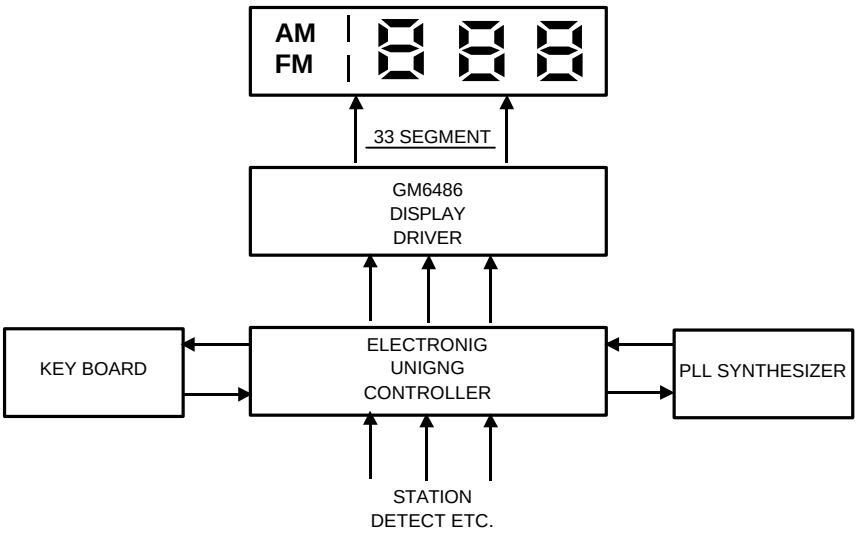


Fig. 7



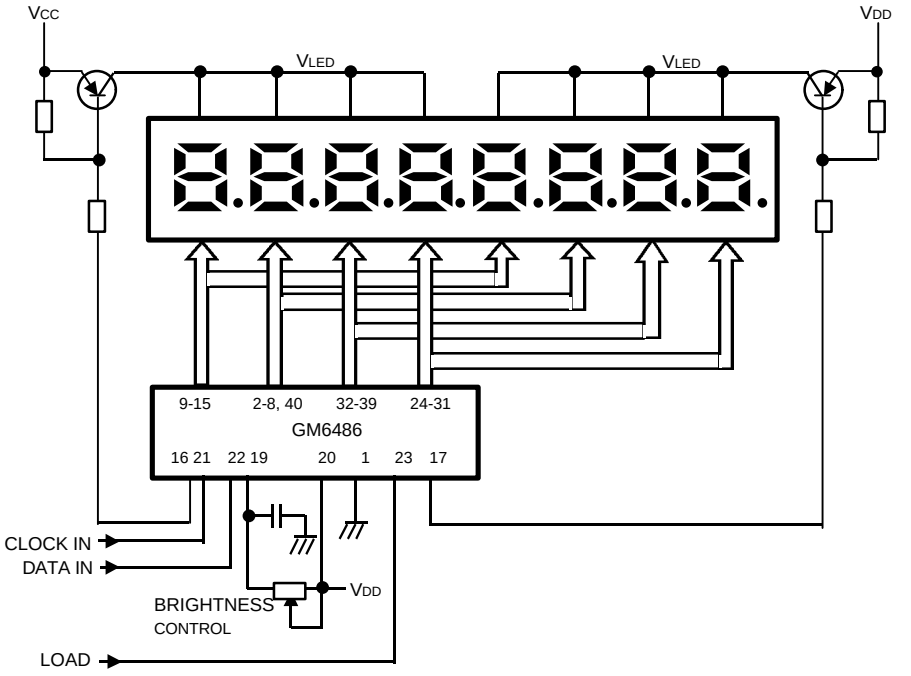
Typical Applications

Basic electronically turned Ratio or TV system



Typical Applications (Continued)

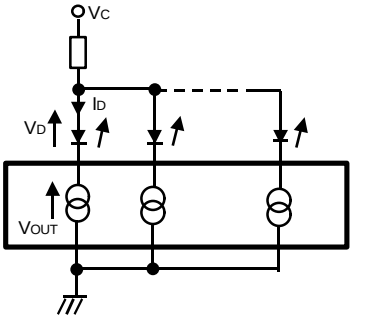
Duplexing 8 Digits with one GM6486



Power Dissipations of the IC

The power dissipation of the IC can be limited by using different configulation.

a)

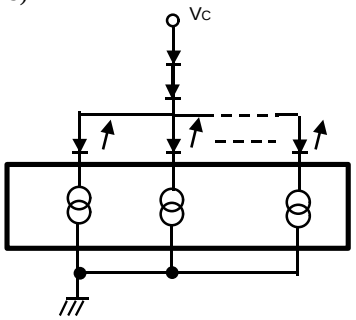


In this application R must be chosen taking into account the worst operating conditions. R is determined by the maximum number of segment activated.

$$R = \frac{V_C - V_{DMAX} - V_{OMIN}}{N_{Max} \bullet I_D}$$

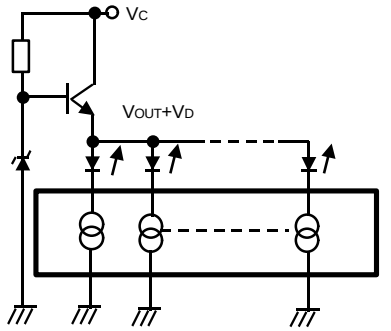
The worst case condition for the device is when roughly half of the maximum number of segments are activated. It must be checked that the total power dissipation does not exceed the absolute maximum ratings.
In critical cases more resistors can be used in conjuction with groups of segments. In this case the current variation in the single resistor is reduced and plot limited.

b)



In this configuration the drop on the serial connected diodes is quite stable if the diodes are properly chosen.
The total power dissipation of the ICs is, in first approximation, depending only on the number of segments activated.

c)



In this configuration VOUT+VD is constant. The total power dissipation of the IC depends only the number of segments activated.