

ADA4691-2/ADA4692-2

FEATURES

- Low power: 200 μ A typical, 250 μ A maximum**
- Low distortion: 0.003% THD + N**
- Low noise: 16 nV/ $\sqrt{\text{Hz}}$ typical**
- 3.9 MHz bandwidth**
- Slew rate: 1.4 V/ μ s typical**
- Offset voltage: 500 μ V typical**
- Low offset voltage drift: 4 μ V/ $^{\circ}$ C maximum**
- Very low input bias currents: 0.5 pA typical**
- 2.7 V to 5 V single supply or \pm 1.35 V to \pm 2.5 V dual supply**

APPLICATIONS

- Portable audio: MP3, PDA, smart phone, notebook**
- Portable instrumentation**
- Portable medical devices**
- Photodiode amplifiers**
- Sensor amplifiers**
- Low-side current sense**
- ADC drivers**
- Active filters**
- Sample-and-hold**
- Automotive sensors**

GENERAL DESCRIPTION

The ADA4691-2 and ADA4692-2 are dual, rail-to-rail output, single-supply amplifiers featuring low power, wide bandwidth, and low noise. The ADA4691-2 has two independent shutdown pins, allowing further reduction in supply current. These amplifiers are ideal for a wide variety of applications. Audio preamps, filters, IR/photodiode amplifiers, charge amps, and high impedance sensors all benefit from this combination of performance features.

Applications for these amplifiers include consumer audio personal players with low noise and low distortion that provide

enough gain and slew rate response over the audio band at low power. Industrial applications with high impedance sensors, such as pyroelectric sensors and other IR sensors, benefit from the high impedance input, low offset drift, and enough bandwidth and response for low gain applications.

The ADA4691-2 and ADA4692-2 are specified over the extended industrial temperature range (-40°C to $+125^{\circ}\text{C}$). The ADA4691-2 is available in a 10-lead LFCSP package, and the ADA4692-2 is available in an 8-lead SOIC package.

PIN CONFIGURATIONS

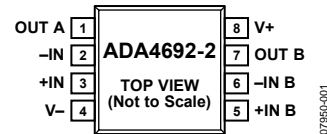


Figure 1. 8-Lead SOIC_N (R-8)

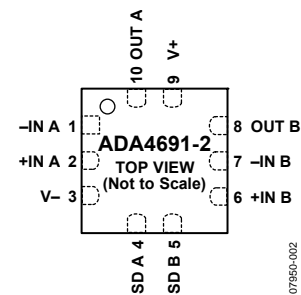


Figure 2. 10-Lead LFCSP (CP-10-11)

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REVISION HISTORY

ADA4691-2/ADA4692-2 Revision History

6/09—Rev. 0 to Rev. A

Added ADA4691-2 Information Throughout	1
Added Figure 2, Renumbered Subsequent Figures	1
Changes to Table 1	3
Changes to Table 2	4
Changes to Table 4	6
Changes to Captions for Figure 40, Figure 41, Figure 43, Figure 44	13
Added Shutdown Operations Section	15
Updated Outline Dimensions	16
Changes to Ordering Guide	16

ADA4692-2 Revision History

3/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—2.7 V OPERATION

$V_{SY} = 2.7\text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = -0.3\text{ V to }+1.6\text{ V}$ $V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	2.5	mV
Input Bias Current	I_B			0.5	5	pA
ADA4691		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			350	pA
ADA4692		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			325	pA
Input Offset Current	I_{OS}			1	5	pA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			225	pA
Input Voltage Range		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-0.3		+1.6	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.3\text{ V to }+1.6\text{ V}$	70	90		dB
ADA4691		$V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$	62			dB
ADA4692		$V_{CM} = -0.1\text{ V to }+1.6\text{ V}; -40^\circ\text{C} < T_A < +125^\circ\text{C}$	70			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_{OUT} = 0.5\text{ V to }2.2\text{ V}$	90	100		dB
ADA4691		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	80			dB
ADA4692		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	85			
ADA4691		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	67			dB
ADA4692		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	73			
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$R_L = 600\ \Omega$, $V_{OUT} = 0.5\text{ V to }2.2\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	85	95		dB
Input Capacitance	C_{IN}			0.8	3	$\mu\text{V}/^\circ\text{C}$
Differential Mode	C_{INDM}			2.5		pF
Common Mode	C_{INCM}			7		pF
Logic High Voltage (Enabled)	V_{IH}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+1.6			V
Logic Low Voltage (Power-Down)	V_{IL}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			0.5	V
Logic Input Current (Per Pin)	I_{IN}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$, $0\text{ V} \leq V_{SD} \leq 2.7\text{ V}$			1	μA
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$ to GND $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.65	2.67		V
		$R_L = 600\ \Omega$ to GND $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.6			V
		$R_L = 600\ \Omega$ to GND $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.55	2.59		V
		$R_L = 600\ \Omega$ to GND $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	2.5			V
Output Voltage Low	V_{OL}	$R_L = 2\text{ k}\Omega$ to V_{SY} $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		24	30	mV
		$R_L = 600\ \Omega$ to V_{SY} $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		78	95	mV
		$R_L = 600\ \Omega$ to V_{SY} $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			125	mV
Short-Circuit Current	I_{SC}	$V_{OUT} = V_{SY}$ or GND		± 15		mA
Closed-Loop Output Impedance	Z_{OUT}	$f = 1\text{ MHz}$, $A_V = -100$		372		Ω
Output Pin Leakage Current		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$, shutdown active, $V_{SD} = V_{SS}$		1		nA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to }5.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80	90		dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	75			dB
Supply Current Per Amplifier	I_{SY}	$V_{OUT} = V_{SY}/2$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		165	200	μA
ADA4691-2		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			240	μA
ADA4692-2		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			225	μA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shut down, $V_{ShutDown} = V_{SS}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		10		nA
					2	μA

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Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 600 \Omega$, $C_L = 20 \text{ pF}$, $A_v = +1$		1.1		V/ μs
Slew Rate	SR	$R_L = 2 \text{ k}\Omega$, $C_L = 20 \text{ pF}$, $A_v = +1$		1.4		V/ μs
Settling Time to 0.1%	t_s	Step = 0.5 V, $R_L = 2 \text{ k}\Omega$, 600 Ω		1		μs
Gain Bandwidth Product ADA4691	GBP	$R_L = 1 \text{ M}\Omega$, $C_L = 35 \text{ pF}$, $A_v = +1$		3.6		MHz
Gain Bandwidth Product ADA4692	GBP	$R_L = 1 \text{ M}\Omega$, $C_L = 35 \text{ pF}$, $A_v = +1$		3.9		MHz
Phase Margin	Φ_M	$R_L = 1 \text{ M}\Omega$, $C_L = 35 \text{ pF}$, $A_v = +1$		49		Degrees
Turn-on, Turn-off time		$R_L = 600 \Omega$		1		μs
NOISE PERFORMANCE						
Distortion	THD + N	$A_v = -1$, $R_L = 2 \text{ k}\Omega$, $f = 1 \text{ kHz}$, $V_{IN \text{ rms}} = 0.15 \text{ V rms}$		0.009		%
		$A_v = -1$, $R_L = 600 \Omega$, $f = 1 \text{ kHz}$, $V_{IN \text{ rms}} = 0.15 \text{ V rms}$		0.01		%
		$A_v = +1$, $R_L = 2 \text{ k}\Omega$, $f = 1 \text{ kHz}$, $V_{IN \text{ rms}} = 0.15 \text{ V rms}$		0.006		%
		$A_v = +1$, $R_L = 600 \Omega$, $f = 1 \text{ kHz}$, $V_{IN \text{ rms}} = 0.15 \text{ V rms}$		0.007		%
Voltage Noise	$e_n \text{ p-p}$	$f = 0.1 \text{ Hz to } 10 \text{ Hz}$		3.1		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1 \text{ kHz}$		16		nV/ $\sqrt{\text{Hz}}$
		$f = 10 \text{ kHz}$		13		nV/ $\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS—5 V OPERATION

$V_{SY} = 5 \text{ V}$, $V_{CM} = V_{SY}/2$, $T_A = 25^\circ\text{C}$, unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$V_{CM} = -0.3 \text{ V to } +3.9 \text{ V}$		0.5	2.5	mV
		$V_{CM} = -0.1 \text{ V to } +3.9 \text{ V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$			3.5	mV
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	5	pA
					360	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	5	pA
					260	pA
Input Voltage Range		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-0.3		+3.9	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -0.3 \text{ V to } +3.9 \text{ V}$	75	98		dB
		$V_{CM} = -0.1 \text{ V to } +3.9 \text{ V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	68			dB
		$V_{CM} = -0.1 \text{ V to } +3.9 \text{ V}$; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	75			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2 \text{ k}\Omega$, $V_O = 0.5 \text{ V to } 4.5 \text{ V}$, $V_{CM} = 0 \text{ V}$	95	110		dB
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	80			dB
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	90			dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	75			dB
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	80			dB
		ADA4691-2 and ADA46920-2	$R_L = 600 \Omega$, $V_O = 0.5 \text{ V to } 4.5 \text{ V}$, $V_{CM} = 0 \text{ V}$	90	100	
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	4	$\mu\text{V}/^\circ\text{C}$
Input Capacitance	C_{INDM}			2.5		pF
				7		pF
Logic High Voltage (Enabled)	V_{IH}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	+2.0			V
Logic Low Voltage (Power-Down)	V_{IL}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			0.8	V
Logic Input Current (Per Pin)	I_{IN}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$, $0 \text{ V} \leq V_{SD} \leq 2.7 \text{ V}$			1	μA
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2 \text{ k}\Omega$	4.95	4.97		V
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.90			V
		$R_L = 600 \Omega \text{ to GND}$	4.85	4.88		V

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Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Output Voltage Low	V_{OL}	$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $R_L = 2\text{ k}\Omega$	4.80	28	35	V mV
		$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ $R_L = 600\ \Omega$			45 110	mV mV
		$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$			140	mV
		$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$				mV
Short-Circuit Limit	I_{SC}	$V_{OUT} = V_{SY}$ or GND		± 55		mA
Closed-Loop Output Impedance	Z_{OUT}	ADA4691-2, $f = 1\text{ MHz}$, $A_V = -100$		364		Ω
Closed-Loop Output Impedance	Z_{OUT}	ADA4691-2, $f = 1\text{ MHz}$, $A_V = -100$		246		Ω
Output Pin Leakage Current		$-40^{\circ}\text{C} < T_A < +125^{\circ}\text{C}$, shutdown active, $V_{SD} = V_{SS}$		1		nA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = 2.7\text{ V to } 5.5\text{ V}$	80	90		dB
		$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$	75			dB
Supply Current per Amplifier ADA4691-2	I_{SY}	$V_{OUT} = V_{SY}/2$		180	225	μA
		$-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$			275	μA
Supply Current Shutdown Mode	I_{SD}	All amplifiers shutdown, $V_{ShutDown} = V_{SS}$ $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$		10		nA uA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$, $600\ \Omega$, $C_L = 20\text{ pF}$, $A_V = +1$		1.3		V/ μs
Settling Time to 0.1%	t_s	$V_{IN} = 2\text{ V step}$, $R_L = 2\text{ k}\Omega$ or $600\ \Omega$		1.5		μs
Gain Bandwidth Product	GBP	$R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$, $A_V = +1$		3.6		MHz
Phase Margin	Φ_M	$R_L = 1\text{ M}\Omega$, $C_L = 35\text{ pF}$, $A_V = +1$		52		Degrees
Turn-on, Turn-off time		$R_L = 600\ \Omega$		1		μs
NOISE PERFORMANCE						
Distortion	THD + N	$A_V = -1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.8\text{ V rms}$		0.008		%
		$A_V = -1$, $R_L = 600\ \Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.8\text{ V rms}$		0.006		%
		$A_V = +1$, $R_L = 2\text{ k}\Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.8\text{ V rms}$		0.003		%
		$A_V = +1$, $R_L = 600\ \Omega$, $f = 1\text{ kHz}$, $V_{IN\text{ rms}} = 0.8\text{ V rms}$		0.001		%
Voltage Noise	e_n p-p	$f = 0.1\text{ Hz to } 10\text{ Hz}$		3.2		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		16		nV/ $\sqrt{\text{Hz}}$
	e_n	$f = 10\text{ kHz}$		13		nV/ $\sqrt{\text{Hz}}$

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ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$
Input Current ¹	$\pm 10 \text{ mA}$
Shutdown Pin Rise/Fall times	50 μs maximum
Differential Input Voltage ²	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Temperature	
Storage Temperature Range	-65°C to $+150^\circ\text{C}$
Operating Temperature Range	-40°C to $+125^\circ\text{C}$
Junction Temperature Range	-65°C to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	300 $^\circ\text{C}$

¹ Input pins have clamp diodes to the supply pins. Limit the input current to 10 mA or less whenever the input signal exceeds the power supply rail by 0.3 V.

² Differential input voltage is limited to 5 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages and measured using a standard 4-layer board, unless otherwise specified.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	155	45	$^\circ\text{C}/\text{W}$
10-Lead LFCSP (CP-10-11)	88	32	$^\circ\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

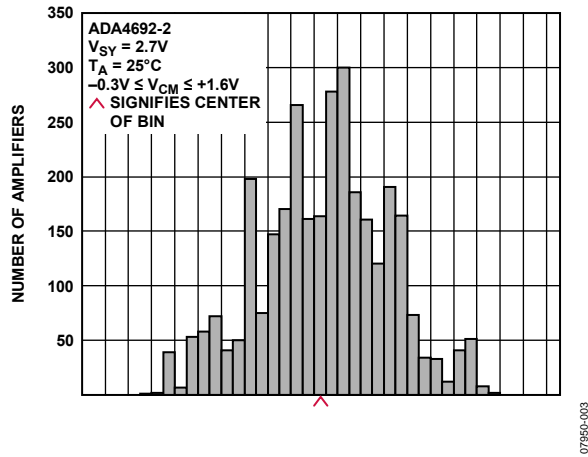


Figure 3. Input Offset Voltage Distribution

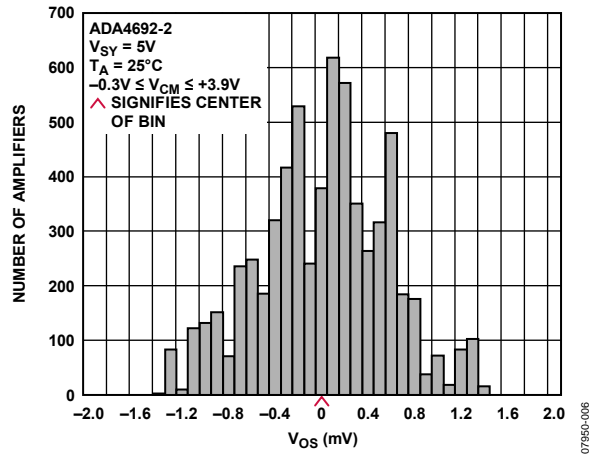


Figure 6. Input Offset Voltage Distribution

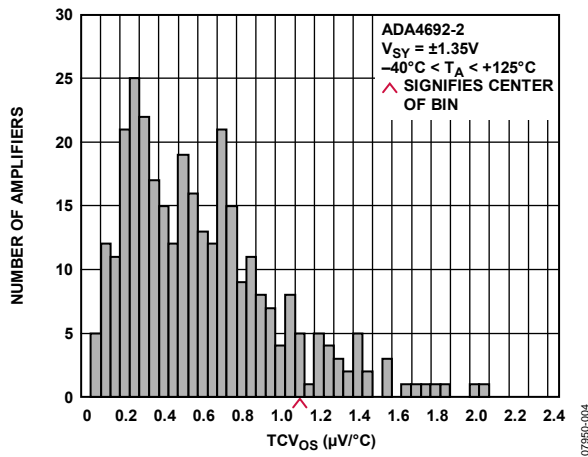


Figure 4. Input Offset Voltage Drift Distribution

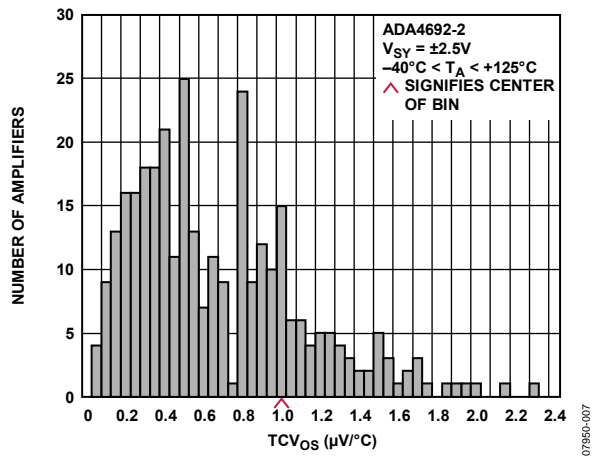


Figure 7. Input Offset Voltage Drift Distribution

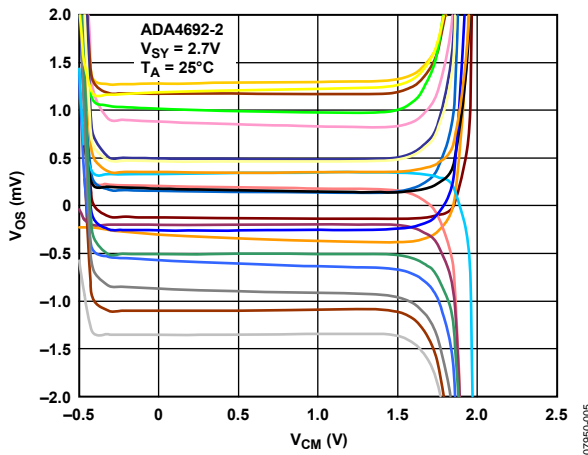


Figure 5. Input Offset Voltage vs. Common-Mode Voltage

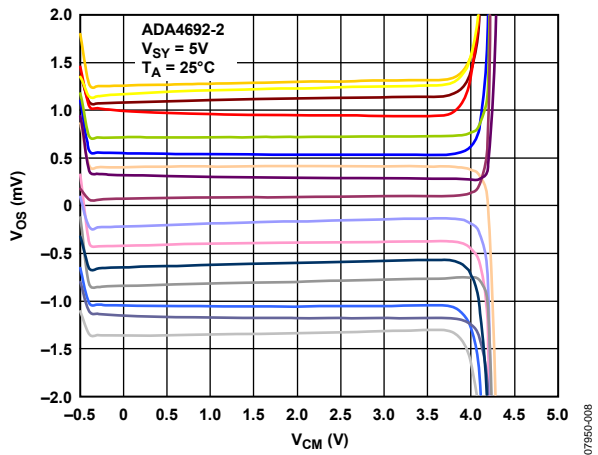


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

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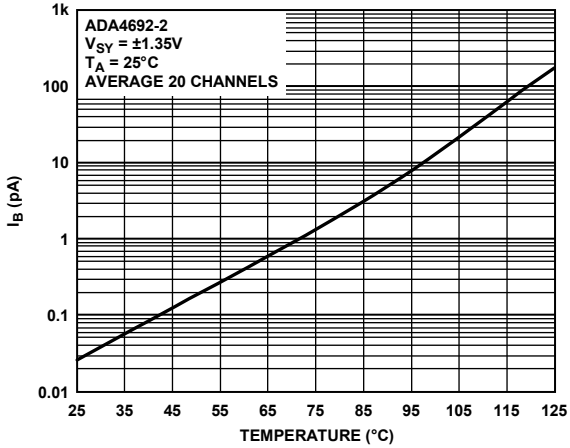


Figure 9. Input Bias Current vs. Temperature

07950-009

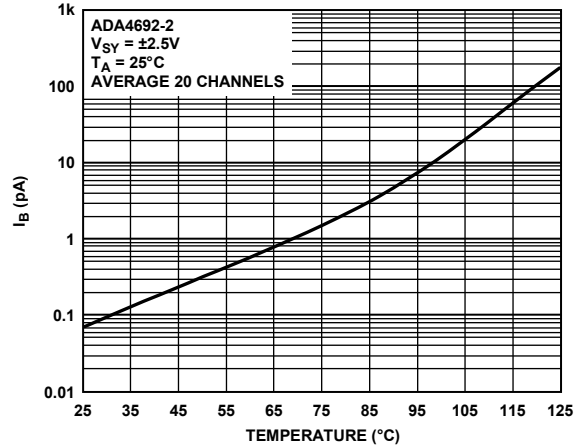


Figure 12. Input Bias Current vs. Temperature

07950-012

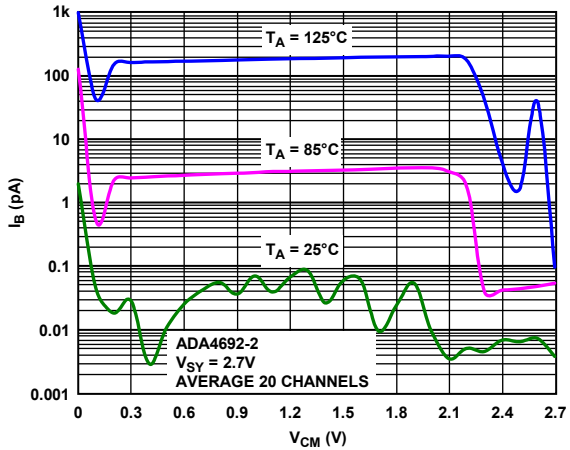


Figure 10. Input Bias Current vs. Common-Mode Voltage

07950-010

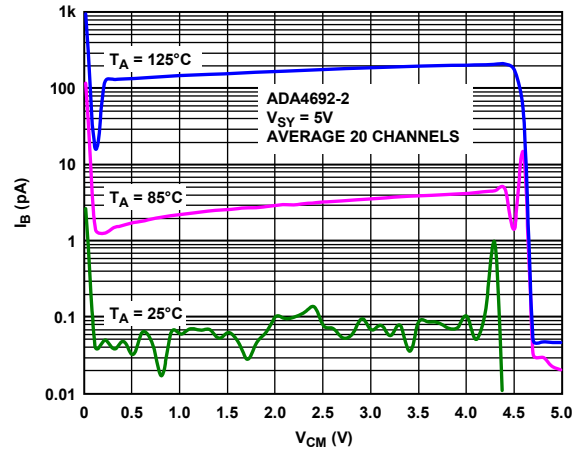


Figure 13. Input Bias Current vs. Common-Mode Voltage

07950-013

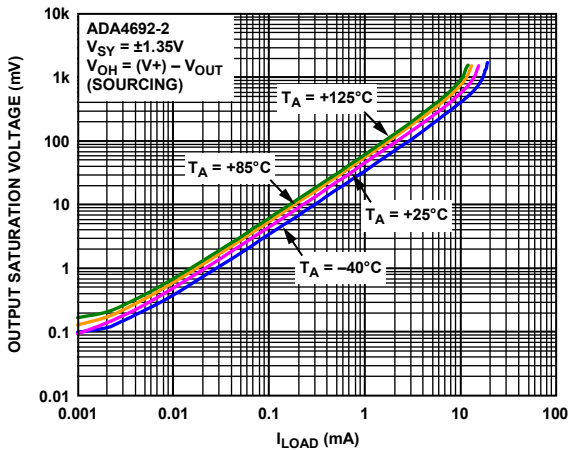


Figure 11. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

07950-011

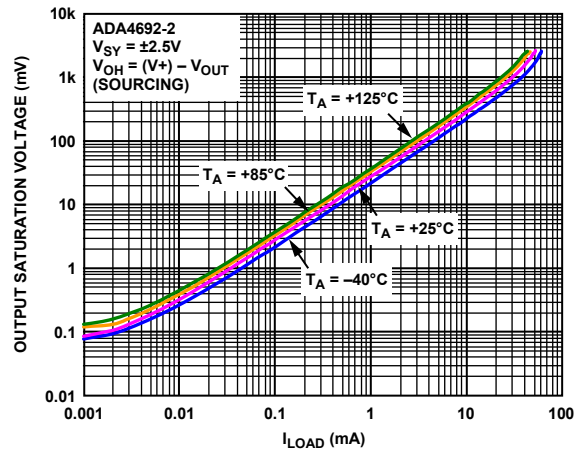


Figure 14. Output Voltage (V_{OH}) to Supply Rail vs. Load Current

07950-014

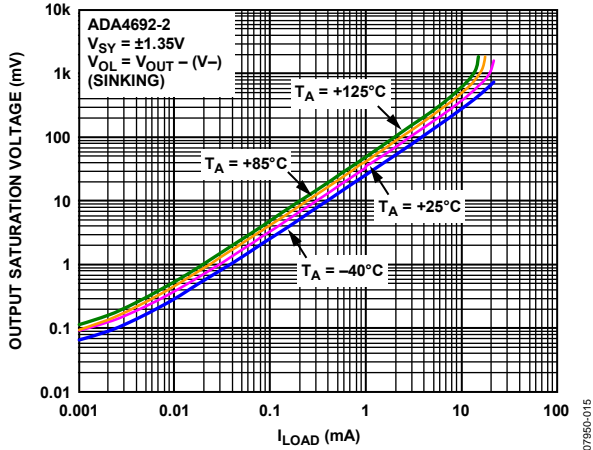


Figure 15. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

07950-015

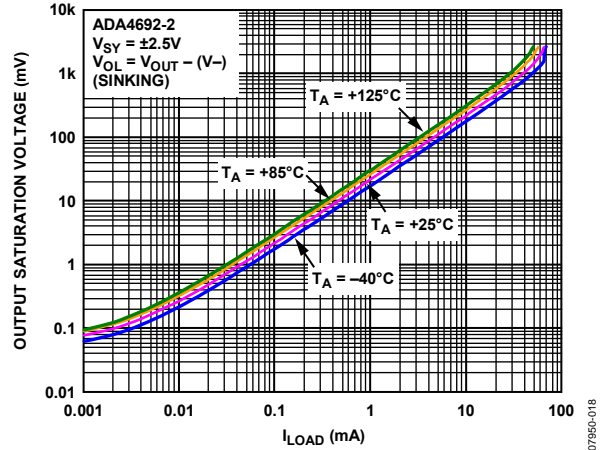


Figure 18. Output Voltage (V_{OL}) to Supply Rail vs. Load Current

07950-018

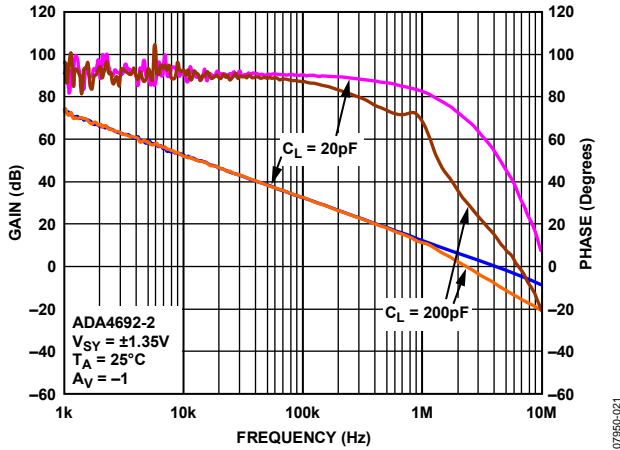


Figure 16. Open-Loop Gain and Phase vs. Frequency

07950-021

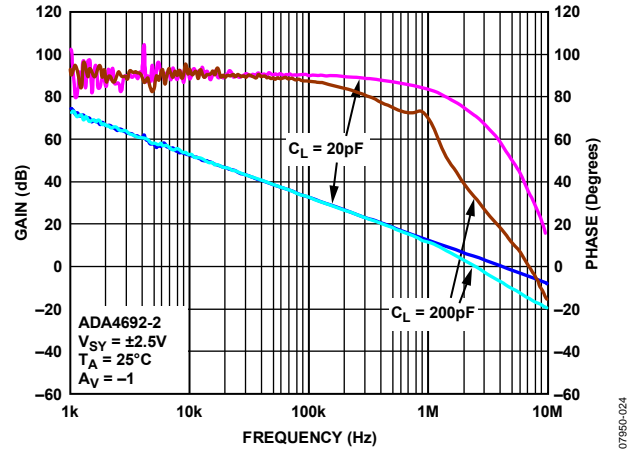


Figure 19. Open-Loop Gain and Phase vs. Frequency

07950-024

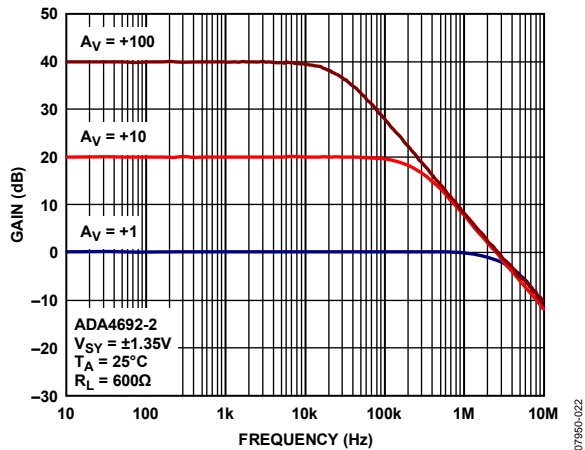


Figure 17. Closed-Loop Gain vs. Frequency

07950-022

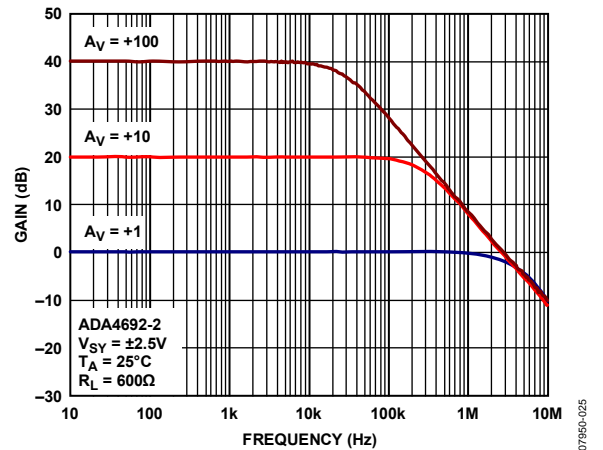


Figure 20. Closed-Loop Gain vs. Frequency

07950-025

ADA4691-2/ADA4692-2

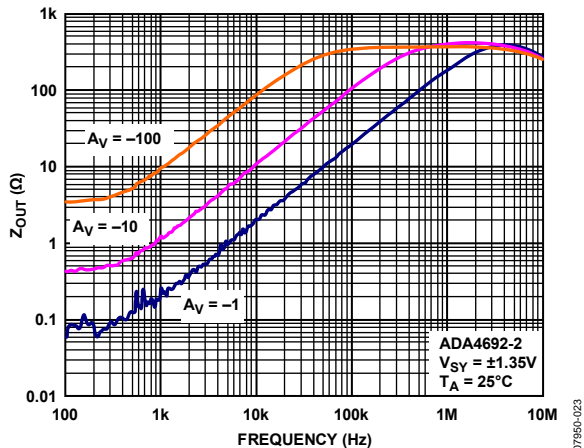


Figure 21. Output Impedance vs. Frequency

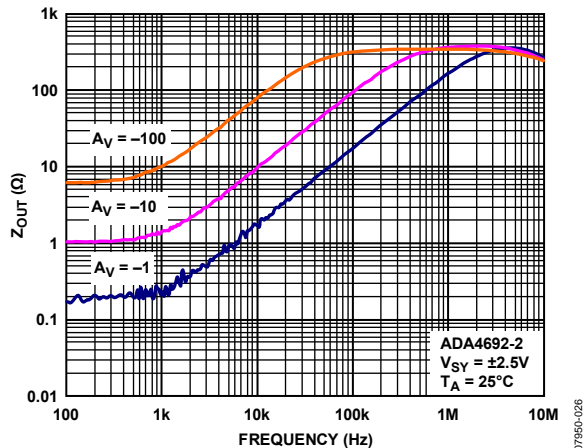


Figure 24. Output Impedance vs. Frequency

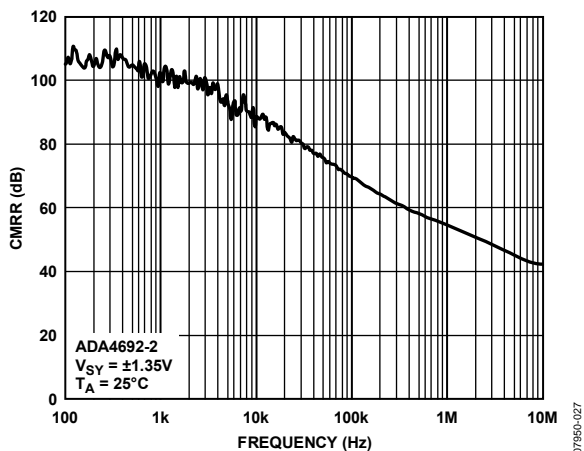


Figure 22. CMRR vs. Frequency

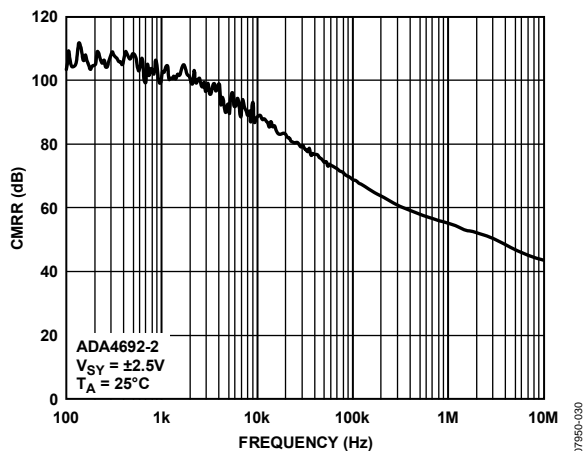


Figure 25. CMRR vs. Frequency

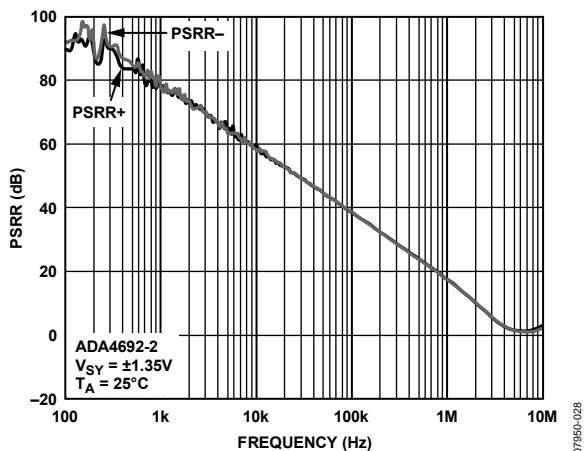


Figure 23. PSRR vs. Frequency

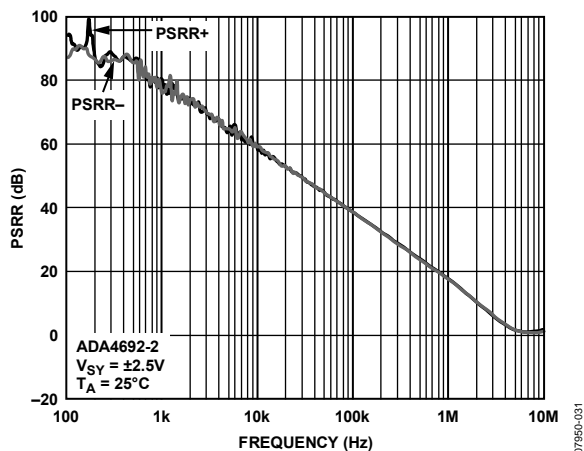


Figure 26. PSRR vs. Frequency

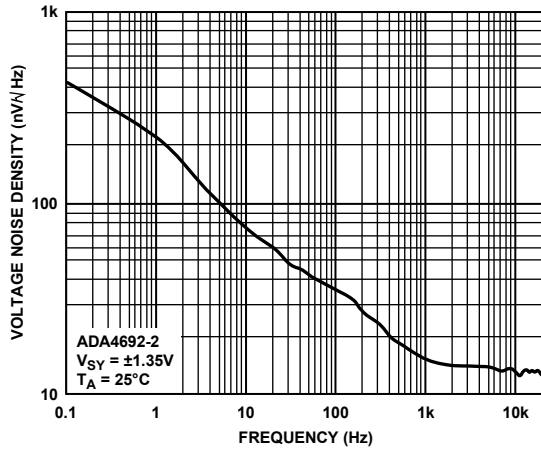


Figure 27. Voltage Noise Density vs. Frequency

07950-029

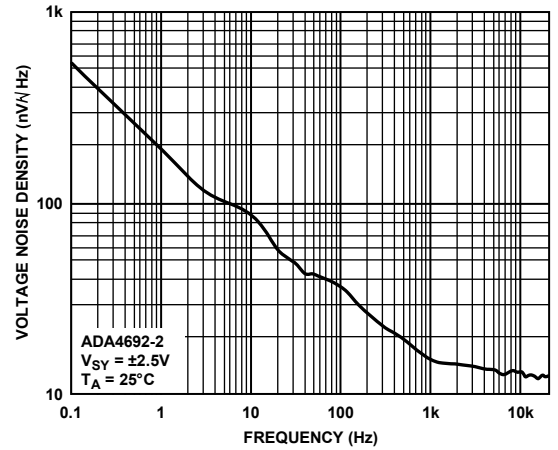


Figure 30. Voltage Noise Density vs. Frequency

07950-032

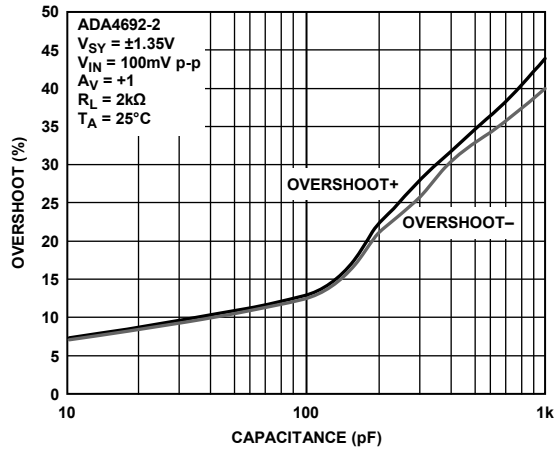


Figure 28. Small Signal Overshoot vs. Load Capacitance

07950-033

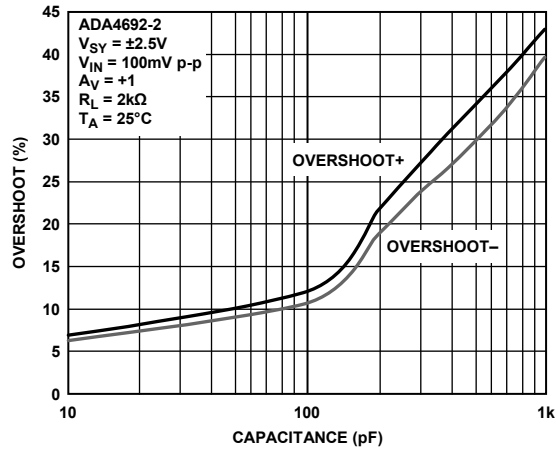


Figure 31. Small Signal Overshoot vs. Load Capacitance

07950-036

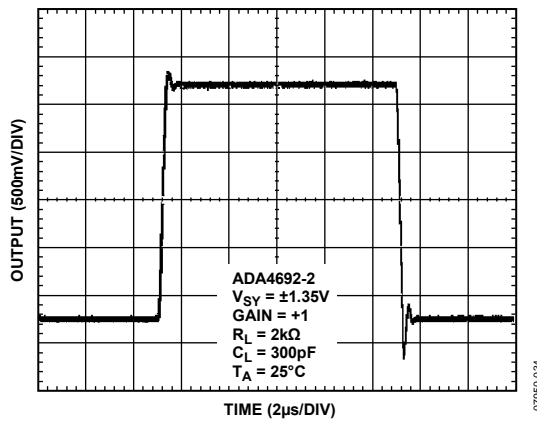


Figure 29. Large Signal Transient Response

07950-034

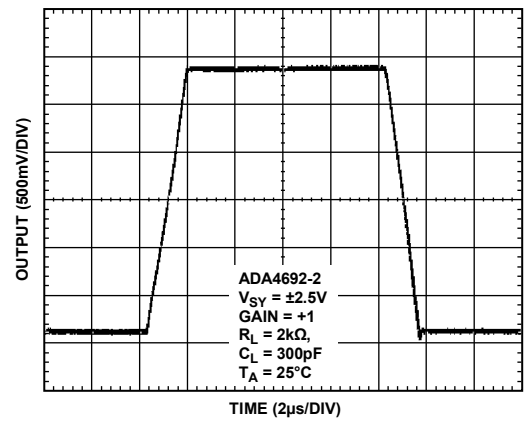


Figure 32. Large Signal Transient Response

07950-037

ADA4691-2/ADA4692-2

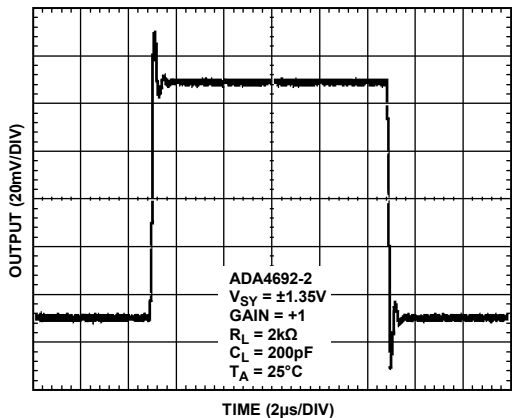


Figure 33. Small Signal Transient Response

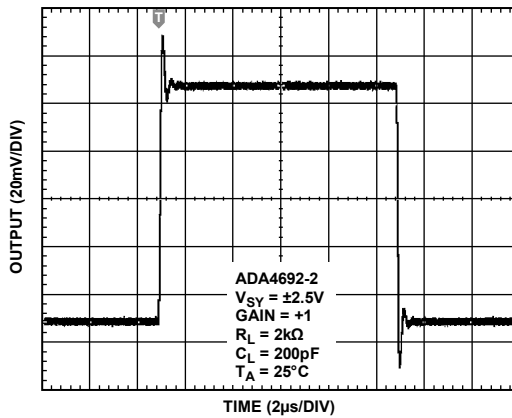


Figure 36. Small Signal Transient Response

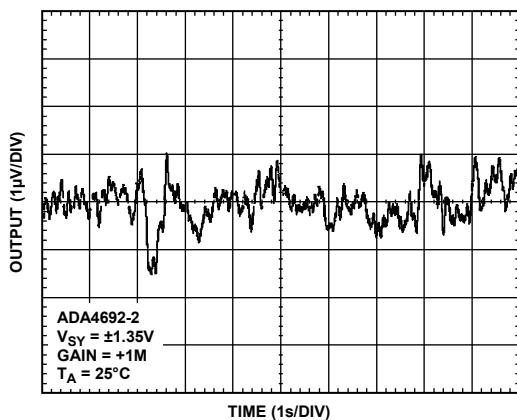


Figure 34. 0.1 Hz to 10 Hz Noise

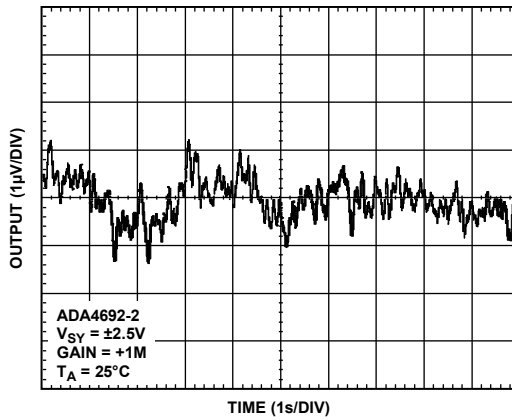


Figure 37. 0.1 Hz to 10 Hz Noise

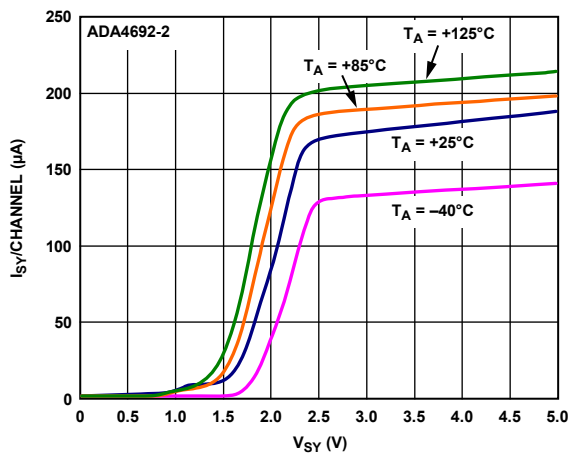


Figure 35. Supply Current per Amplifier vs. Supply Voltage

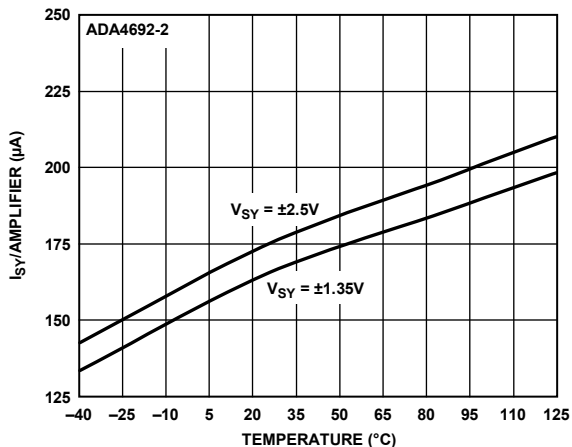


Figure 38. Supply Current per Channel vs. Temperature

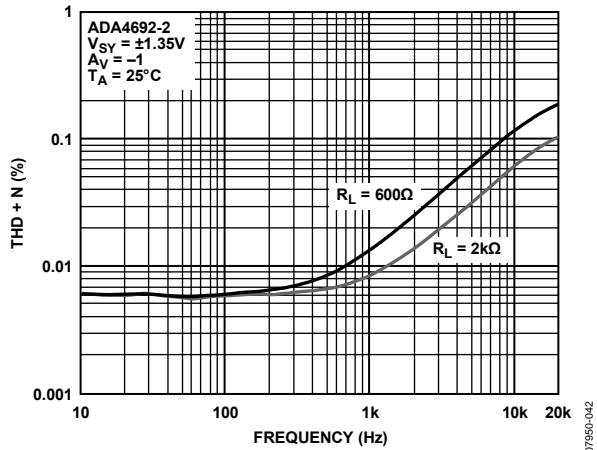


Figure 39. THD + Noise vs. Frequency

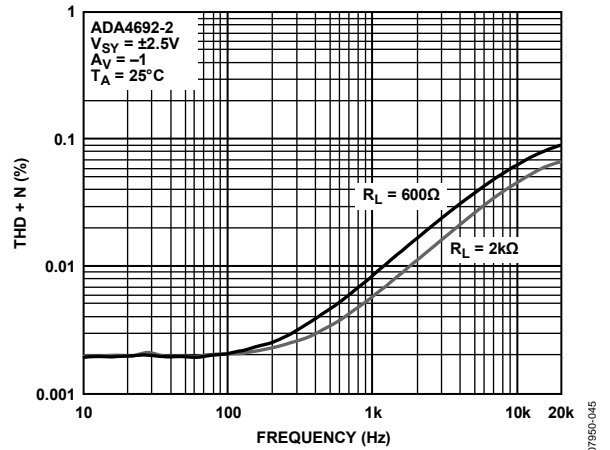


Figure 42. THD + Noise vs. Frequency

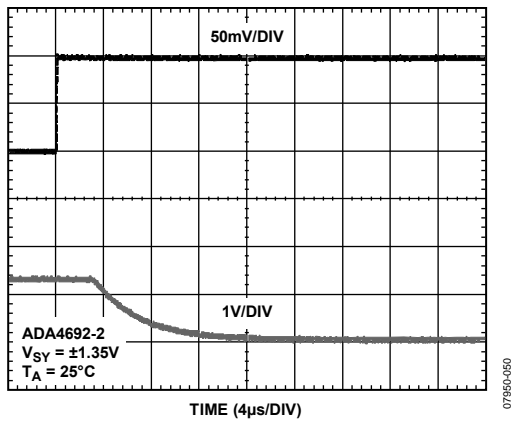


Figure 40. Positive Overload Recovery

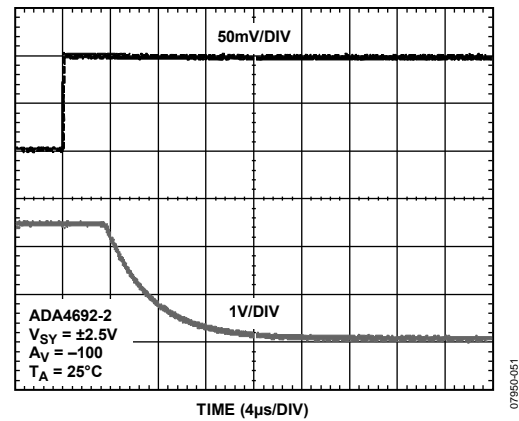


Figure 43. Positive Overload Recovery

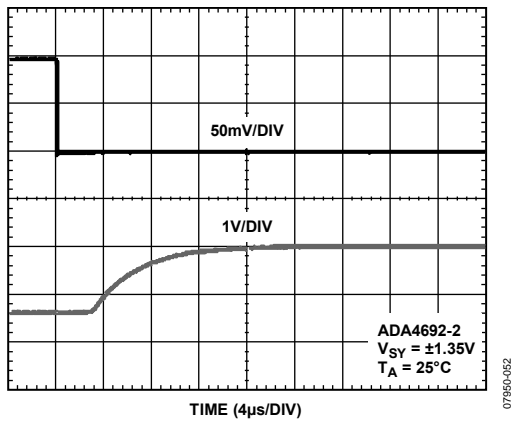


Figure 41. Negative Overload Recovery

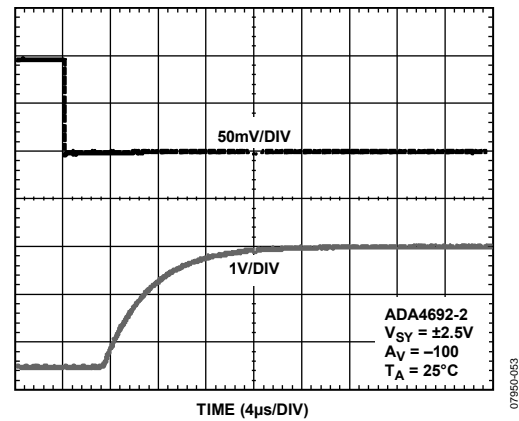


Figure 44. Negative Overload Recovery

ADA4691-2/ADA4692-2

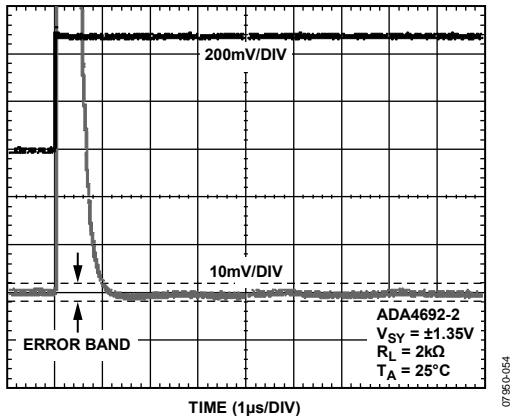


Figure 45. Positive Settling Time to 0.1%

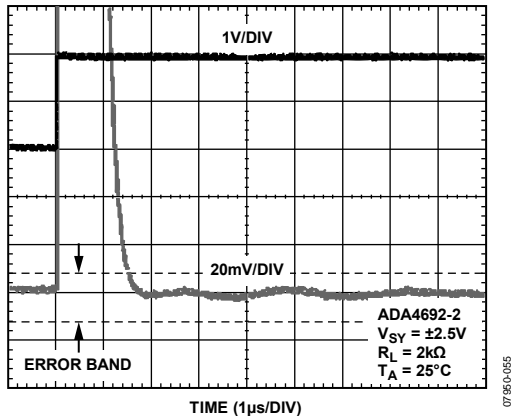


Figure 48. Positive Settling Time to 0.1%

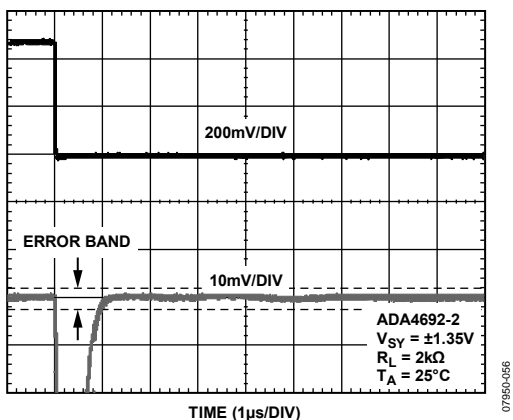


Figure 46. Negative Settling Time to 0.1%

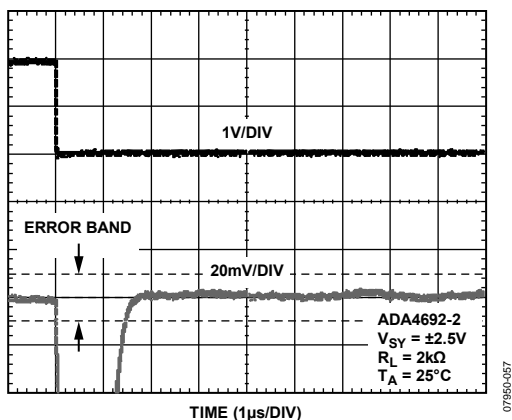


Figure 49. Negative Settling Time to 0.1%

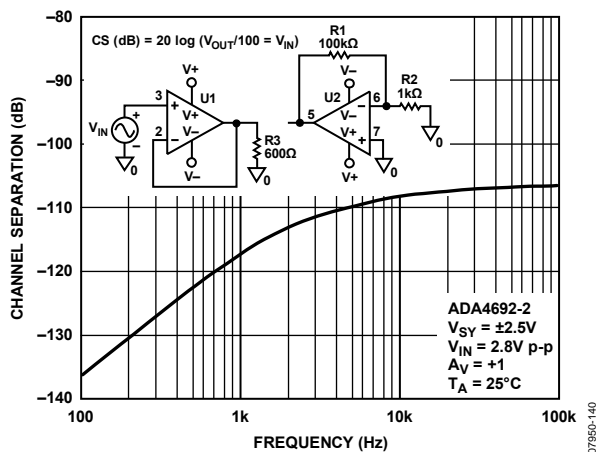


Figure 47. Channel Separation vs. Frequency

SHUTDOWN OPERATION

INPUT PIN CHARACTERISTICS

The ADA4691-2 has a classic CMOS logic inverter input for each shutdown pin, as shown in Figure 50.

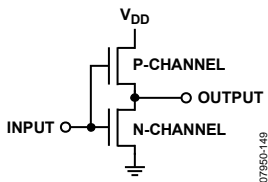


Figure 50. CMOS Inverter

With slowly changing inputs, the top transistor and bottom transistor may be slightly on at the same time, increasing the supply current. This can be avoided by driving the input with a digital logic output having fast rise and fall times. Figure 51 through Figure 53 show the supply current for both sections switching simultaneously with rise times of 1 μ s, 10 μ s, and 1 ms. Clearly, the rise and fall times should be faster than 10 μ s. Using an RC time constant to enable/disable shutdown is not recommended.

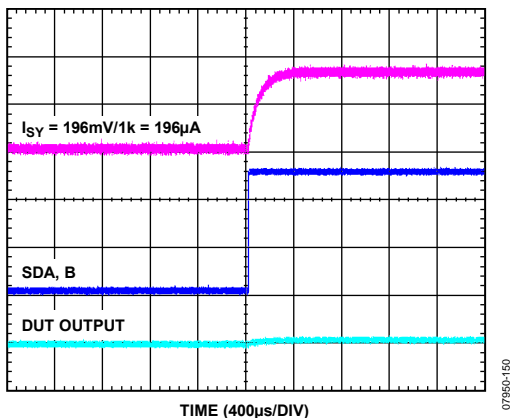


Figure 51. Shutdown Pin Rise Time = 1 μ s

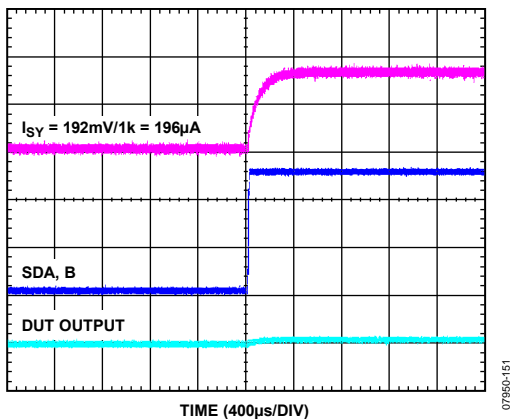


Figure 52. Shutdown Pin Rise Time = 10 μ s

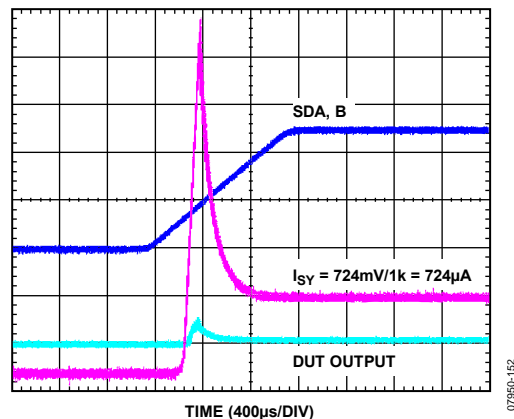


Figure 53. Shutdown Pin Rise Time = 1 ms

INPUT THRESHOLD

The input threshold is approximately 1.2 V above the V- pin when operating on ground and +5 V, and 0.9 V when operating on 2.7 V (see Figure 54 and Figure 55). The threshold is relatively stable over temperature. For operation on split supplies, the logic swing may have to be level shifted.

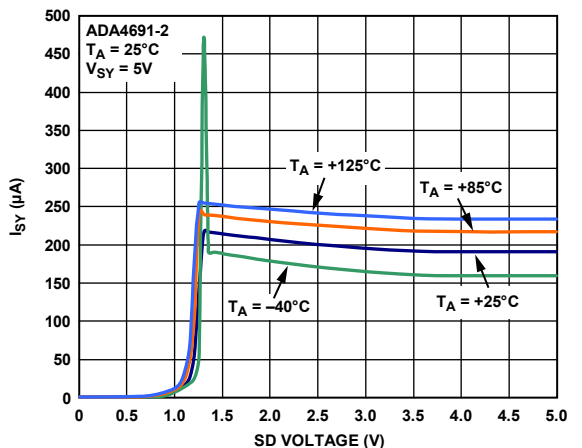


Figure 54. Supply Current vs. Temperature, $V_{SY} = 5$ V

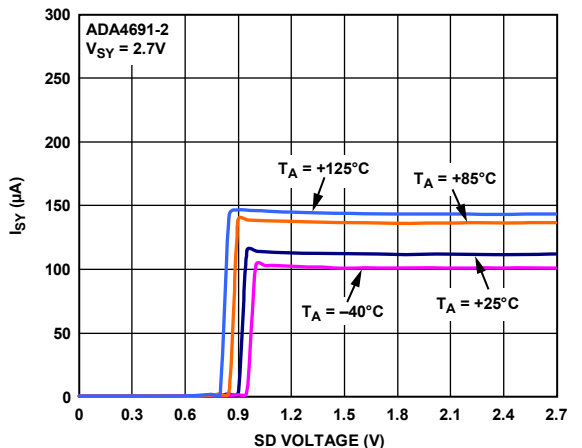
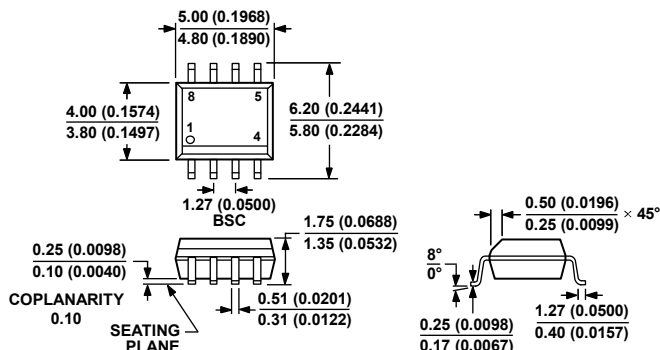


Figure 55. Supply Current vs. Temperature, $V_{SY} = 2.7$ V

ADA4691-2/ADA4692-2

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 56. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)

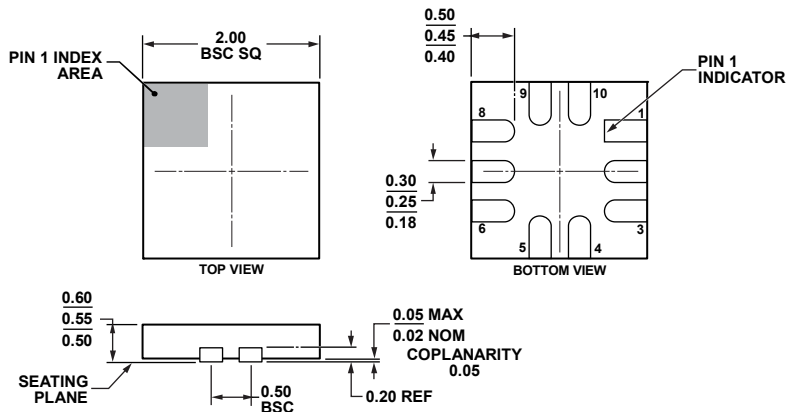


Figure 57. 10-Lead Lead Frame Chip Scale Package [LFCSP_UQ]
 2 mm x 2 mm Body, Ultra Thin Quad
 (CP-10-11)

Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Code
ADA4691-2ACPZ-R7 ¹	-40°C to +125°C	10-Lead_LFCSP_UQ	CP-10-11	A2
ADA4691-2ACPZ-RL ¹	-40°C to +125°C	10-Lead_LFCSP_UQ	CP-10-11	A2
ADA4691-2ACPZ-R2 ¹	-40°C to +125°C	10-Lead_LFCSP_UQ	CP-10-11	A2
ADA4692-2ARZ ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4692-2ARZ-R7 ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4692-2ARZ-RL ¹	-40°C to +125°C	8-Lead SOIC_N	R-8	

¹ Z = RoHS Compliant Part.