REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																					
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SHEET	15	16	17																		
REV STATUS OF SHEETS			REV																		
			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIFS OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-03-21

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 12-BIT, 1 MHZ 75 MW A/D CONVERTER W/INPUT MULTIPLEXER AND SAMPLE/HOLD, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-95593

SHEET 1 OF 17

DESC FORM 193
JUL 94

5962-E142-95

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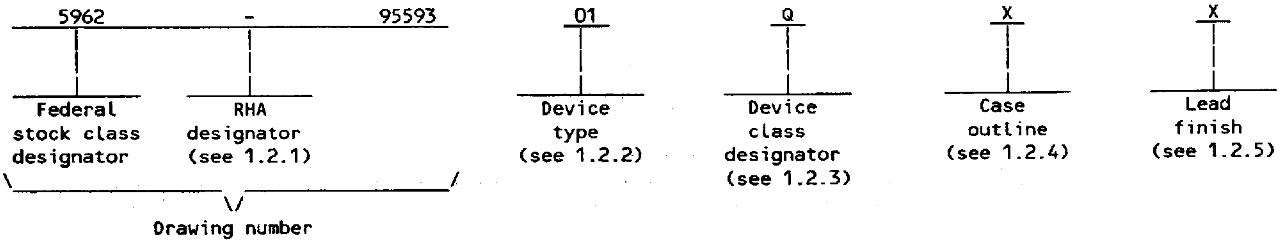
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADC12062	12-bit, 1MHz, 75 mW A/D converter with input multiplexer and sample/hold

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1	44	Quad flat package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/, 2/

Supply voltage (V_{CC} = DV_{CC} = AV_{CC}) - - - - - - - - - - - - - - -0.3 V to +6 V
Voltage at any input or output - - - - - - - - - - - - - - - -0.3 V to V_{CC} + 0.3 V
Input current at any pin 3/ - - - - - - - - - - - - - - - - 25 mA
Package input current 3/ - - - - - - - - - - - - - - - - - 50 mA
Storage temperature range (T_{STG}) - - - - - - - - - - - - - - -65°C to +150°C
Power dissipation (P_D) 4/ - - - - - - - - - - - - - - - - - 875 mW
Lead temperature (soldering,10 seconds) - - - - - - - - - - - +300°C
Junction temperature (T_J) - - - - - - - - - - - - - - - - - +150°C
Thermal resistance, junction-to-case (θ_{JC}) - - - - - - - - - 7.5°C/W
Thermal resistance, junction-to-ambient (θ_{JA}) - - - - - - - - 48°C/W

1.4 Recommended operating conditions.

Supply voltage range (DV_{CC} = AV_{CC})- - - - - - - - - - - - - - +4.5 V to +5.5 V
Ambient operating temperature range (T_A) - - - - - - - - - - -55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltages are measured with respect to GND (GND = AGND = DGND), unless otherwise specified.
3/ When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < GND or V_{IN} > V_{CC}) the absolute value of current at that pin should be limited to 25 mA or less. The 50 mA package input current limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.
4/ The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, θ_{JA} and the ambient temperature T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_J\text{max} - T_A)/\theta_{JA}$ or the number given in the Absolute maximum ratings, whichever is lower. In most cases the maximum derated power dissipation will be reached only during fault conditions.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CONVERTER CHARACTERISTICS							
Resolution	RES		1, 2, 3	01		12	Bits
Differential linearity error	DLE		1	01	-0.8	+0.8	LSB
			2, 3		-0.95	+0.95	
Integral linearity error	ILE	2/	1	01	-1.0	+1.0	LSB
			2, 3		-1.5	+1.5	
Offset error	OE		1	01	-1.25	+1.25	LSB
			2, 3		-2.0	+2.0	
Full scale error	FSE		1	01	-1.0	+1.0	LSB
			2, 3		-1.5	+1.5	
Power supply sensitivity	PSRR	$DV_{CC} = AV_{CC} = 5$ V ± 10 %	1, 2, 3	01	-1.0	+1.0	LSB
Reference resistance	R_{REF}		1, 2, 3	01	500	1000	Ω
V_{REF+} (sense) Input voltage	V_{REF+}		1, 2, 3	01		AV_{CC}	V
V_{REF-} (sense) Input voltage	V_{REF-}		1, 2, 3	01	A_{GND}		V

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-95593
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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CONVERTER CHARACTERISTICS-continued							
Input voltage range	V_{IN}	To V_{IN1}, V_{IN2}, or ADC IN	1, 2, 3	01	A_{GND} - 0.05 V	AV_{CC} + 0.05 V	V
ADC IN input leakage	I_{INL}	A_{GND} to AV_{CC} - 0.3 V	1, 2, 3	01		3	µA
MUX On-channel leakage	I_{ONL}	A_{GND} to AV_{CC} - 0.3 V	1, 2, 3	01		3	µA
MUX Off-channel leakage	I_{OFFL}	A_{GND} to AV_{CC} - 0.3 V	1, 2, 3	01		3	µA
DYNAMIC CHARACTERISTICS 3/							
Signal-to-noise plus distortion ratio	SINAD	4/	4, 5, 6	01	68.0		dB
Signal-to-noise ratio	SNR	4/, 5/	4, 5, 6	01	69.5		dB
Total harmonic distortion	THD	4/, 6/	4	01		-74	dBc
			5, 6			-70	
Effective number of Bits	ENOB	4/, 7/	4, 5, 6	01	11		Bits

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \leq T_A \leq +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DC CHARACTERISTICS							
Logical 1 input voltage	V_{IN1}	$DV_{CC} = AV_{CC} = +5.5$ V	1, 2, 3	01	2.0		V
Logical 0 input voltage	V_{IN0}	$DV_{CC} = AV_{CC} = +4.5$ V	1, 2, 3	01		0.8	V
Logical 1 input current	I_{IN1}		1, 2, 3	01		1.0	µA
Logical 0 input current	I_{IN0}		1, 2, 3	01		1.0	µA
Logical 1 output voltage	V_{OUT1}	$D_{VCC} = A_{VCC} = +4.5$ V, $I_{OUT} = -360$ µA	1, 2, 3	01	2.4		V
		$D_{VCC} = A_{VCC} = +4.5$ V, $I_{OUT} = -100$ µA	1, 2, 3		4.25		
Logical 0 output voltage	V_{OUT0}	$DV_{CC} = AV_{CC} = +4.5$ V $I_{OUT} = 1.6$ mA	1, 2, 3	01		0.4	V
TRI-STATE 0 output leakage current	I_{OUT}	Pins DB0-DB11	1, 2, 3	01		3	µA
DV_{CC} supply current	DI_{CC}		1, 2, 3	01		3	mA
AV_{CC} supply current	AI_{CC}		1, 2, 3	01		12	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC CHARACTERISTICS							
Maximum sampling rate ($1/t_{THROUGHPUT}$)	f_S		9,10,11	01	1		MHz
Conversion time (S/$\overline{H}$ low to EOC high)	t_{CONV}		9,10,11	01	600	980	ns
S/$\overline{H}$ pulse width	$t_{S/\overline{H}}$		9,10,11	01	5	550	ns
S/$\overline{H}$ low to EOC low	t_{EOC}		9,10,11	01	60	125	ns
Access time (RD low or OE high to data valid)	t_{ACC}	C_L = 100 pf	9,10,11	01		20	ns
TRI-STATE control (RD high or OE low databus TRI-STATE)	t_{1h} t_{0h}	R_L = 1 KΩ, C_L = 10 pf	9,10,11	01		40	ns
Delay from $\overline{RD}$ low to INT high	$t_{\overline{INT}H}$	C_L = 100 pf	9,10,11	01		60	ns
Delay from EOC high to INT low	$t_{\overline{INT}L}$	C_L = 100 pf	9,10,11	01		-10	ns
EOC high to new data valid	t_{UPDATE}		9,10,11	01		15	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55^{\circ}C \leq T_A \leq +125^{\circ}C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
AC CHARACTERISTICS-continued.							
Multiplexer address setup time (MUX address valid to EOC low)	t_{MS}		9,10,11	01	50		ns
Multiplexer address hold time (EOC low to MUX address invalid)	t_{MH}		9,10,11	01	50		ns
$\overline{CS}$ setup time ($\overline{CS}$ low to $\overline{RD}$ low, S/H low, or OE high)	$t_{\overline{CS}S}$		9,10,11	01	20		ns
$\overline{CS}$ hold time ($\overline{CS}$ high after $\overline{RD}$ high, S/H high, or OE low)	$t_{\overline{CS}H}$		9,10,11	01	20		ns

1/ $DV_{CC} = AV_{CC} = +5$ V, V_{REF+}(sense) = +4.096 V, V_{REF-}(sense) = A_{GND}, and $f_S = 1$ MHz.

2/ Integral linearity error is the maximum deviation from a straight line between the measured offset and full scale endpoints.

3/ $DV_{CC} = AV_{CC} = +5$ V, V_{REF+}(sense) = +4.096 V, V_{REF-}(sense) = A_{GND}, and $f_S = 1$ MHz, $R_S = 25\ \Omega$, $f_{IN} = 100$ KHz, 0 dB from fullscale.

4/ Dynamic testing of device is performed using the ADC IN input. The input multiplexer adds harmonic distortion at high frequencies.

5/ The signal-to-noise ratio is the ratio of the signal amplitude to the background noise level. Harmonics of the input signal are not included in its calculation.

6/ The contributions from the first nine harmonics are used in the calculation of the THD.

7/ Effective number of bits (ENOB) is calculated from the measured signal-to-noise plus distortion ratio (SINAD) using the equation ENOB = (SINAD - 1.76)/6.02.

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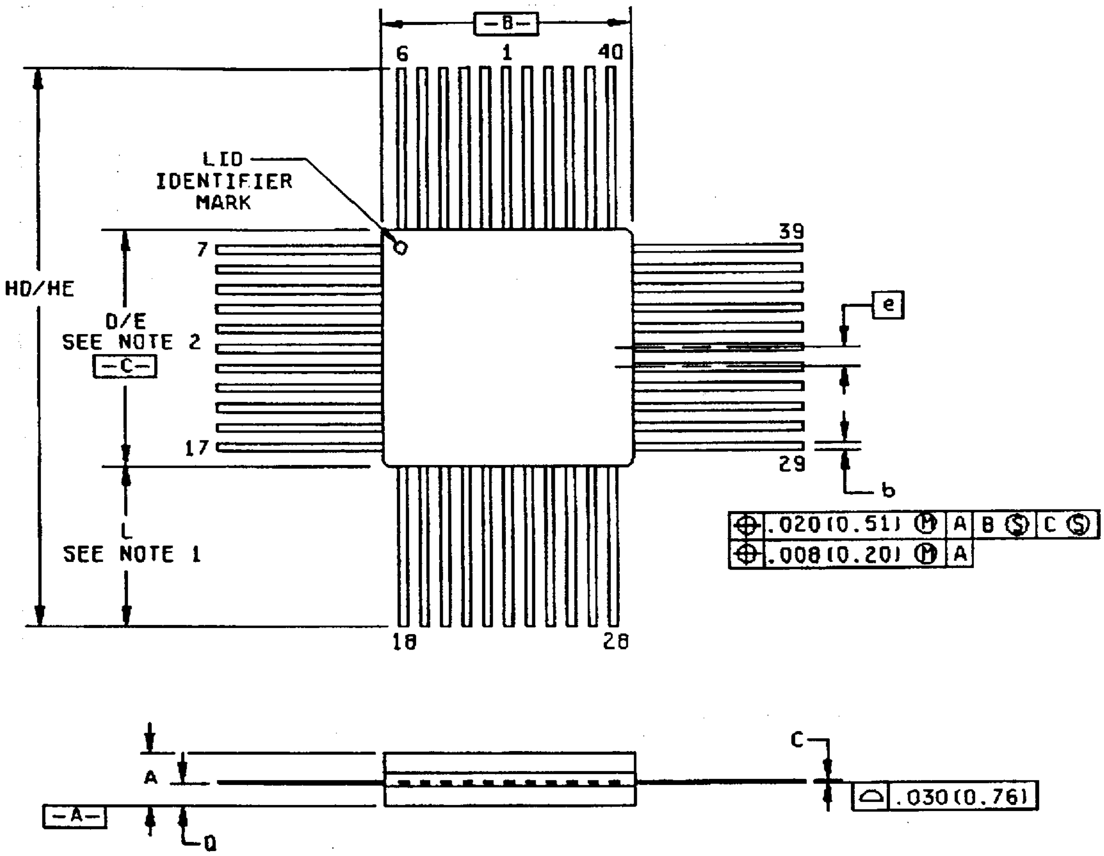


Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.108	.132	2.74	3.35
HD/HE	1.365	1.435	34.67	36.45
C	.005	.009	0.13	0.23
D/E	.575	.605	14.61	15.37
e	.050bsc		1.27bsc	
L	.395	.415	10.03	10.54
Q	.044	.060	1.12	1.52
b	.017	.023	.43	.58

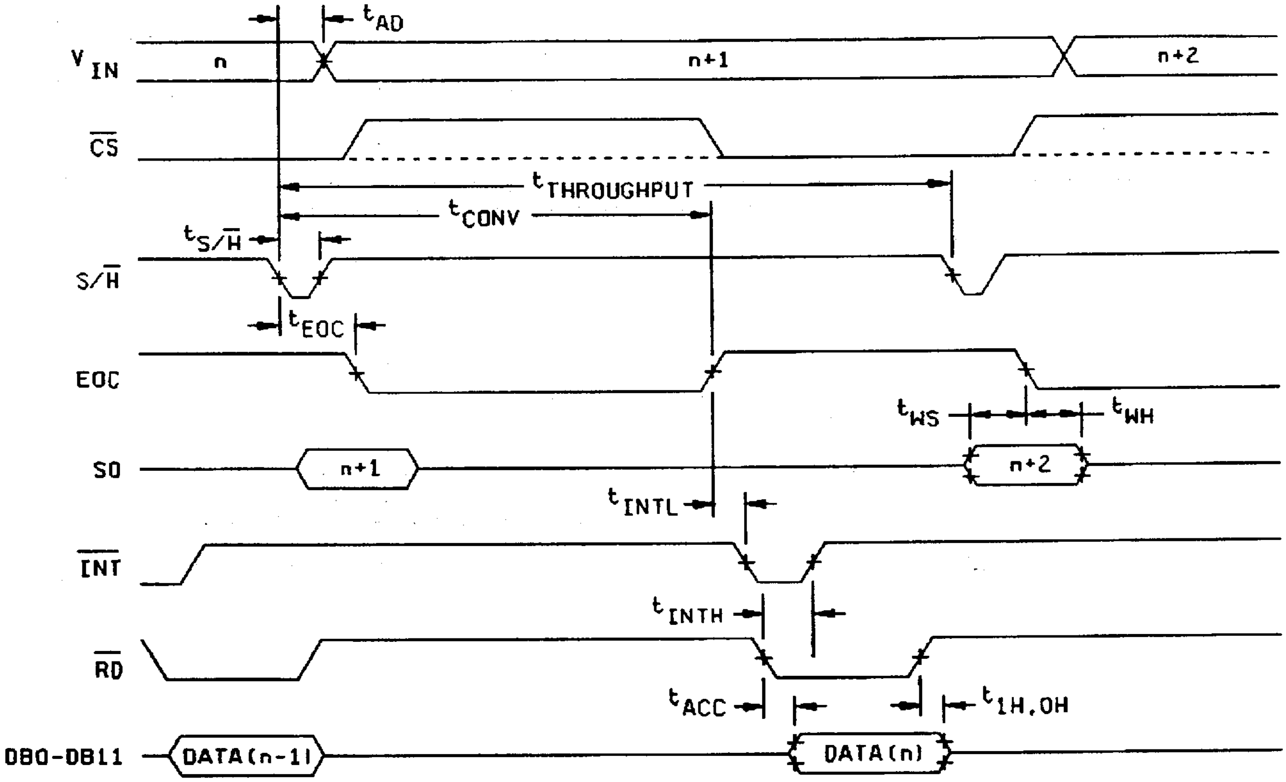
NOTES:

1. Leadframe to be solder dipped 200 microinches/5.08 micrometers minimum, measured at crest of the major flats.
2. Dimension includes the offset of base and lid.

FIGURE 1. Case outline.

Device types	01		
Case outlines	X		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	AGND	23	$\overline{CS}$
2	$V_{REF-(SENSE)}$	24	TEST
3	$V_{REF-(FORCE)}$	25	DV_{CC}
4	$V_{REF}/16$	26	DGND1
5	$V_{REF+(FORCE)}$	27	DGND2
6	$V_{REF+(SENSE)}$	28	NC
7	V_{IN1}	29	$\overline{INT}$
8	NC	30	EOC
9	V_{IN2}	31	DB0
10	NC	32	DB1
11	MUX OUT	33	DB2
12	ADC IN	34	NC
13	AGND	35	DB3
14	AV_{CC}	36	DB4
15	DGND1	37	DB5
16	SO	38	DB6
17	$\overline{PD}$	39	DB7
18	DGND1	40	DB8
19	MODE	41	DB9
20	OE	42	DB10
21	$\overline{RD}$	43	DB11
22	S/$\overline{H}$	44	AV_{CC}

FIGURE 2. Terminal connections.



INTERRUPT INTERFACE TIMING (MODE = 1, OE = 1)

FIGURE 3. Timing diagrams.

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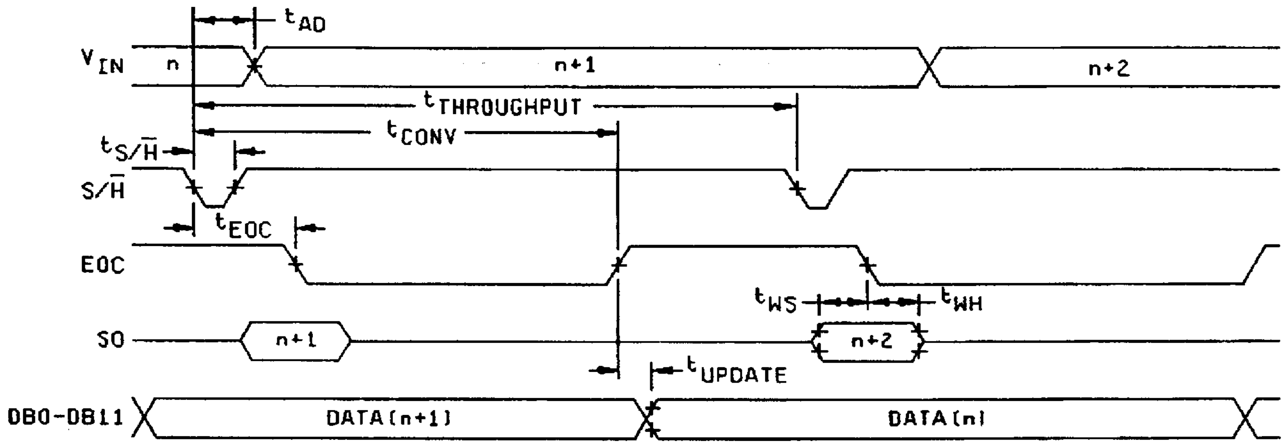
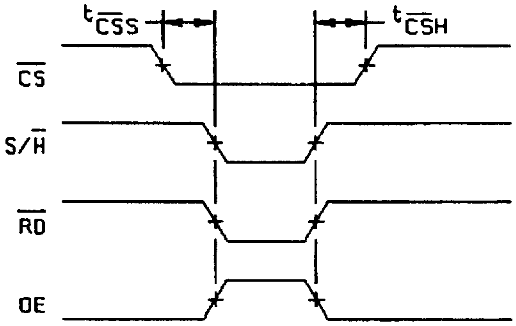


HIGH SPEED INTERFACE TIMING (MODE = 1, OE = 1, $\overline{CS}$ = 0, $\overline{RD}$ = 0)



$\overline{CS}$ SETUP AND HOLD TIMING FOR $S/\overline{H}$, $\overline{RD}$, AND OE

FIGURE 3. Timing diagrams - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/ 9,10,11	1,2,3,4,5,6 1/ 9,10,11	1,2,3,4 1/ 5,6,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,5,6 9,10,11	1,2,3,4,5,6 9,10,11	1,2,3,4,5,6 9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	1	1	1

1/ PDA applies to subgroup 1.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.