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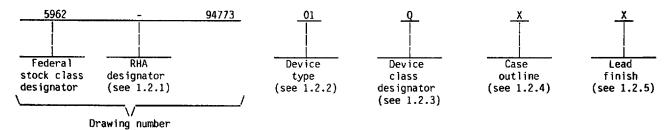
<u>DISTRIBUTION STATEMENT A</u>. Approved for public release; distribution is unlimited.

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1. SCOPE

- 1.1 <u>Scope</u>. This drawing forms a part of a one part one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.
 - 1.2 PIN. The PIN shall be as shown in the following example:



- 1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.
 - 1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	<u>Generic number</u>	<u>Circuit function</u>
01	54F82031	9-bit TTL/BTL address/data transceivers

1.2.3 <u>Device class designator</u>. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class

Device requirements documentation

М

Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883

Q or V

Certification and qualification to MIL-I-38535

1.2.4 <u>Case outline(s)</u>. The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	<u>Terminals</u>	<u>Package style</u>
Х	GDFP1-F48	48	Flat pack

1.2.5 <u>Lead finish</u>. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3	Absolute maximum ratings. 1/2/3/			
	Supply voltage range (v_{CC})		-0.5 V dc to V _{CC} -40 mA to 5 mA -48 mA -200 mA -65°C to +150°C -300°C -500 MIL-STD-1835	dc dc 4/ dc 4/ dc 4/
1.4	Recommended operating conditions. 2/ 3/ 6/			
	Supply voltage range (V_{CC} , BIAS V_{CC} , EG V_{CC}) Low level input voltage range (V_{IL}) (B port) Maximum low level input voltage (V_{IL}) (Except B por High level input voltage range (V_{IH}) (B port) Minimum high level input voltage range (V_{IH})(except Maximum high level output current (I_{OH}) (A port). Maximum low level output current (I_{OL}) (A port). Maximum low level output current (I_{OL}) (B port). Input clamp current (I_{IK})	t)	+4.5 V dc to +5.5 V +0.75 V dc to +1.47 +0.8 V dc +1.62 V dc to 2.3 V +2.0 V dc -3 mA +24 mA +100 mA -18 mA -55°C to +125°C	dc V dc V dc
1.5	Digital logic testing for device classes Q and V.			
	Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)		XX percent <u>7</u> /	
1/ 2/ 3/ 4/ 5/ 6/ 7/	Stresses above the absolute maximum rating may caus maximum levels may degrade performance and affect r Unless otherwise noted, all voltages are referenced. The limits for the parameters specified herein shalt temperature range of -55°C to +125°C. The input negative voltage rating may be exceeded r Power dissipation values are derived using the form specified in 1.4 above, r and r are as specified outputs. Unused or floating pins (input or r) must be held values will be added when they become available.	eliability. I to GND. I apply over the Provided that the Bula Pp = Vcclcc do I not table I here	full specified V _{CC} range input clamp current ratin	and ambient
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2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, bulletin, and handbook</u>. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

MIL-STD-973 - Configuration Management. MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 <u>Non Government publications</u>. The following document(s) for a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (1EEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary Scan Architecture.

(Applications for copies shouldbe addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational sevices.)

2.3 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

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3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.
 - 3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.
 - 3.2.2 <u>Terminal connections</u>. The terminal connections shall be as specified on figure 1.
 - 3.2.3 <u>Iruth table(s)</u>. The truth table(s) shall be as specified on figure 2.
 - 3.2.4 Block diagram. The block diagram shall be as specified on figure 3.
 - 3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.
- 3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.
- 3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.
- 3.5.1 <u>Certification/compliance mark</u>. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.
- 3.6 <u>Certificate of compliance</u>. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change for device class M</u>. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.
- 3.9 <u>Verification and review for device class M</u>. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
- 3.10 <u>Microcircuit group assignment for device class M</u>. Device class M devices covered by this drawing shall be in microcircuit group number 127 (see MIL-I-38535, appendix A).

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- 4. QUALITY ASSURANCE PROVISIONS
- 4.1 <u>Sampling and inspection</u>. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.
- 4.2 <u>Screening</u>. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.
 - 4.2.1 Additional criteria for device class M.
 - a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) $T_A = +125$ °C, minimum.
 - b. Interim and final electrical test parameters shall be as specified in table II herein, except that interim electrical tests prior to burn in are optional at the discretion of the manufacturer for device class M.

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Test and MIL-STD-883	Symbol	Test condition -55°C ≤ T. ≤ +	s <u>2</u> / 125°C	v _{cc}	Group A subgroups	Limits <u>3</u> /		Unit
test method $\underline{1}/$		$-55^{\circ}\text{C} \le \text{T}_{A} \le +$ $+4.5 \text{ V} \le \text{V}_{CC} \le$ unless otherwise s		3229. 0272	Min	Max		
High level output voltage, A port 3006	V _{ОН}	For all inputs affecting output under test VIN = VIH or VIL IOH = -3.0 mA		4.5 V	1, 2, 3	2.5		V
Low level output voltage, A port 3007	V _{OL1}	For all inputs affecting output under test, V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA	4.5 V	1, 2, 3		0.5	٧
Low level output voltage, B port 3007	V _{OL2}		I _{OL} = 80 mA	4.5 V	1, 2, 3	0.7	1.2	V
Output voltage, B port 3007	v _o	V _I (BIAS V _{CC}) = 4.5 V to 5.5 V T _A = 25°C		0.0 V	1	1.62	2.1	٧
Negative input clamp voltage, B port 3022	V _{IK1}	For input under test I _{IN} = -18 mA		4.5 V	1, 2, 3		-1.2	٧
Negative input clamp yoltage, except B port 3022	V _{IK2}	For input under test I _{IN} = -40 mA		4.5 V	1, 2, 3		-0.5	٧
Input current, except B port 3010	I	For input under test V _{IN} = 5.5 V	5.5 V	1, 2, 3		50	μA	
Input current high, except B port 3010	1 1H1	For input under test V _{IN} = 2.7 V		5.5 V	1, 2, 3		50	μA
Input current low, Except B port 3010	1 JL1	For input under test V _{IN} = 0.5 V		5.5 V	1, 2, 3		-50	μА
Input current low, B port 3010	1 1L2	For input under test V _{IN} = 0.75 V		5.5 V	1, 2, 3		-100	μΑ
Output current A port	1 ₉ 95	V ₀ = 0		5.5 V	1, 2, 3	-30	-150	mA
Ou <u>t</u> put current, B port 3011	I ₀₁	$V_{\rm B} = 1V$, $V_{\rm I}$ (BIAS $V_{\rm CC}$) = 4.5 V TO	5.5 V	0.0	1, 2, 3	-30		μA
Ou <u>t</u> put current, B port 3011	I ₀₂	OEB = 0 to 0.8 V		0.0 V to 5.5 V	1, 2, 3		100	μΑ
Ou <u>t</u> put current, B port 3011	I ₀₃	0EB = 0 to 5 V		0.0 V to 2.2 V	1, 2, 3		100	μΑ
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Test and MIL-STD-883	Symbol	Test conditions $2/$ $-55^{\circ}C \le T_{A} \le +125^{\circ}C$	v _{cc}	Group A subgroups	Limit	s <u>3</u> /	Unit
test method <u>1</u> /		$-55^{\circ}\text{C} \le T_{A} \le +125^{\circ}\text{C}$ +4.5 V \le V _{CC} \le +5.5 V unless otherwise specified			Min	Max	
High level <u>o</u> utput current, B port	Іон	V ₀ = 2.1 V	0.0 V to 5.5 V	1, 2, 3		100	μА
Quiescent supply current, A port to B port 3005	I _{CC1}	For all inputs, I ₀ = 0	5.5 V	1, 2, 3		70	mA
Quiescent supply current, B port to A port 3005	I _{CC2}		5.5 V	1, 2, 3		80	
Quiescent supply current, 3005	(BIAS V _{CC})	V _B = 0 to 2 V V _I (BIAS V _{CC}) = 4.5 V to 5.5 V	0.0 V to 4.5 V	1, 2, 3		450	μ
			4.5 V to 5.5 V	1, 2, 3		10	
Input capacitance 3012	CIN	All control inputs VI = VCC or GND See 4.4.1b	5.0 V	4		13	pf
Output capacitance, AO port 3012	C _{OUT}	V _O = V _{CC} or GND See 4.4.1b	5.0 V	4		13	
A/Q capacitance, B port per P1194.0 3012	c _{1/0}	See 4.4.1b	0.0 V to 4.5 V	4		12	pl
			4.5 V to 5.5 V	4		11	
Functional test	<u>6</u> /	V _{IN} = V _{IH} or V _{IL} Verify output V _O	4.5 V	7, 8	L	H	
		See 4.4.1c	5.5 V	7, 8	Ĺ	н	
ropagation delay time, A (thru mode)	t _{PLH1}	$C_L = 30 \text{ pF minimum,}$ $R_1 = 16.5\Omega$	5.0 V	9	1.2	7.0	n
to B 3003		See figure 4	4.5 V and 5.5 V	10, 11	1.0	8.0	
	tPHL1	•	5.0 V	9	1.0	6.7	n:
			4.5 V and 5.5 V	10, 11	0.8	7.8	

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Test and MIL-STD-883	Symbol	Test conditions $2/$ -55°C \leq T _{Δ} \leq +125°C	v _{CC}	Group A subgroups	Limit	Unit	
test method 1/		-55° C ≤ T _A ≤ $+125^{\circ}$ C +4.5 V ≤ V _{CC} ≤ $+5.5$ V unless otherwise specified			Min	Max	
Propagation delay time, A (transparent)	tPLH2	C _L = 30 pF minimum,	5.0 V	9	1.4	7.3	ns
to B 3003		C_L = 30 pF minimum, R_L = 16.5 Ω See figure 4	4.5 V and 5.5 V	10, 11	1.2	8.6	
	t _{PHL2}		5.0 V	9	1.2	7.2	ns
			4.5 V and 5.5 V	10, 11	1.0	8.3	
Propagation del <u>a</u> y	t _{PLH3}		5.0 V	9	1.4	7.7	ns
time, LCA to B 3003	2/2.13		4.5 V and 5.5 V	10, 11	1.0	9.1	
	t _{PHL3}	5.0 V	9	1.6	7.9	ns	
	<u>1</u> /		4.5 V and 5.5 V	10, 11	1.1	9.0	
Propagation delay	t _{PLH4}	$C_L = 50 \text{ pF minimum}$ $R_L = 500\Omega$	5.0 V	9	1.0	7.0	ns
time, LCB to A 3003	2/	R _L = 5000 See figure 4	4.5 V and 5.5 V	10, 11	0.7	7.9	
	tPHL4		5.0 V	9	0.9	6.9	
	1/		4.5 V and 5.5 V	10, 11	0.6	7.4	
Propagation delay	t _{PLH5}	t _{PI H5}	5.0 V	9	0.7	6.4	ns
time, SELI or SELU to A 3003	to A		4.5 V and 5.5 V	10, 11	0.5	7.9	
	tpHL5		5.0 V	9	0.8	6.3	
	<u> 2</u> 5		4.5 V and 5.5 V	10, 11	0.6	7.1	

See footnotes at end of table.

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Test and MIL-STD-883	Symbol	Test conditions $\frac{2}{100}$ -55°C $\leq T_0 \leq +125$ °C	V _{CC}	Group A subgroups	Limits <u>3</u> /		Unit
test method $\underline{1}/$		-55° C ≤ T_A ≤ $+125^{\circ}$ C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified			Min	Max	
Propagation delay time, SEL1 or SEL0	ropagation delay tpLH6		5.0 V	9	1.3	7.8	ns
to B 3003		See figure 4	4.5 V and 5.5 V	10, 11	1.1	9.3	
	t _{PHL6}	1	5.0 V	9	1.1	7.9	
			4.5 V and 5.5 V	10, 11	0.9	9.2	
Propagation delay time.	t _{PLH7}	C _L = 50 pF minimum	5.0 V	9	0.9	6.8	ns
3003	1/	C _L = 50 pF minimum R _L = 500Ω See figure 4	4.5 V and 5.5 V	10, 11	0.7	8.6	
	tPHL7		5.0 V	9	1.1	6.9	1
			4.5 V and 5.5 V	10, 11	0.6	7.6	
Propagation delay time,	t _{PLH8}		5.0 V	9	1.0	7.6	ns
B (transparent) to A 3003			4.5 V and 5.5 V	10, 11	1.0	9.0	
	t _{PHL8}		5.0 V	9	1.4	7.4	
			4.5 V and 5.5 V	10, 11	1.0	8.2	
Propagation_delay_time,	t _{PLH9}	$C_L = 30 \text{ pF minimum}$ $R_1 = 16.5\Omega$	5.0 V	9	1.0	7.3	ns
OEB or OEB to B 3003	11/	R _L = 16.502 See figure 4	4.5 V and 5.5 V	10, 11	0.8	8.4	
	tpHL9		5.0 V	9	1.0	6.9	
			4.5 V and 5.5 V	10, 11	0.6	8.2	

See footnotes at end of table.

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Test and MIL-STD-883 test method <u>1</u> /	Symbol	Test conditions $2/$ $-55^{\circ}C \le I_A \le +125^{\circ}C$ $+4.5 \ V \le V_{CC}^{\circ} \le +5.5 \ V$ unless otherwise specified	V _{CC}	Group A subgroups	Limits <u>3</u> /		Unit
					Min	Max	
Propagation delay time,	t _{P,} ZH1		5.0 V	9	0.4	6.2	ns
to A 3003			4.5 V and 5.5 V	10, 11	0.3	7.3	
	tpZL1		5.0 V	9	0.4	6.1	
	T)		4.5 V and 5.5 V	10, 11	0.3	7.0	
Propagation delay time, output disable, OEA to A 3003	t _{PHZ1}		5.0 V	9	0.3	6.4	ns
			4.5 V and 5.5 V	10, 11	0.2	7.1	
	t _{PLZ1}		5.0 V	9	0.4	6.5	
			4.5 V and 5.5 V	10, 11	0.3	7.2	
Transition time,	t _t	V ₀ = 1.3 V to 1.8 V	5.0 V	9	0.4	4.5	ns
8 outputs			4.5 V and 5.5 V	10, 11	0.4	4.5	
B-port input pulse rejection	t _{PR}		4.5 V and 5.5 V	10, 11	1		ns

See notes at end of table.

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1 2 3 45 6 7	the conditions listed herein. { Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all I _{CC} and △I _{CC} tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated, V _{IN} = GND or V _{IN} ≥ 3.0 V. { For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. { For I/O ports, the limit includes I _{OZH} or I _{OZL} leakage current from the output circuitry. { Not more than one output should be tested at one time, and the duration of the test condition should not exceed one second. { Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances per MIL-STD-883, may be incorporated. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

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STANDARD

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Device type		01 <u>1</u> /			
Case outlines	х				
Terminal number	Terminal symbol	Terminal number	Terminal symbol		
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	OEB OEA DEA VCC VCC A1 GND A2 A3 GND A4 A5 GND A6 A7 GND A8 A9 SEL1 LCB BG VCC LCA BG GND SEL0 TD0	25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48	다. 사항 사항 명원 용권 7 원 6 원 5 원 4 원 3 원 2 원 1 연 5 5 5 5 원 8 명 8 명 8 명 8 명 8 명 8 명 8 명 8 명 8 명 8		

Note

1/ Pins are allocated for the four-wire IEEE 1149.1 (JTAG) test bus, which will be implemented in a future version of this device. Currently, TMS and ICK are not connected and TDI is shorted to TDO.

FIGURE 1. <u>Terminal connections</u>.

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Transceiver function table

	INPUTS	······································	FUNCTION	
0EA	0EB	0EB		
Ł	Н	Ĺ	Ā data to B bus	
Н	L	Х	B data to A bus	
Н	Х	Н		
Н	Н	L	\overline{A} data to B bus, \overline{B} data to A bus	
L	L	Х	Isolation	
Ł	x	H		

Storage mode table

LCA, LCB	RESULT	
0	Transparent	
1	Latches latched	
t	Flip-flops triggered	

Select function table

SEL1	SEL 0	MUX A B	MUX B A
0	0	Latch	Latch
0	1	Thru	Thru
1	0	Flip-flop	Flip-flop
1	1	Flip-flop	Latch

H = High voltage level

L = Low voltage level

X = Irrelevant

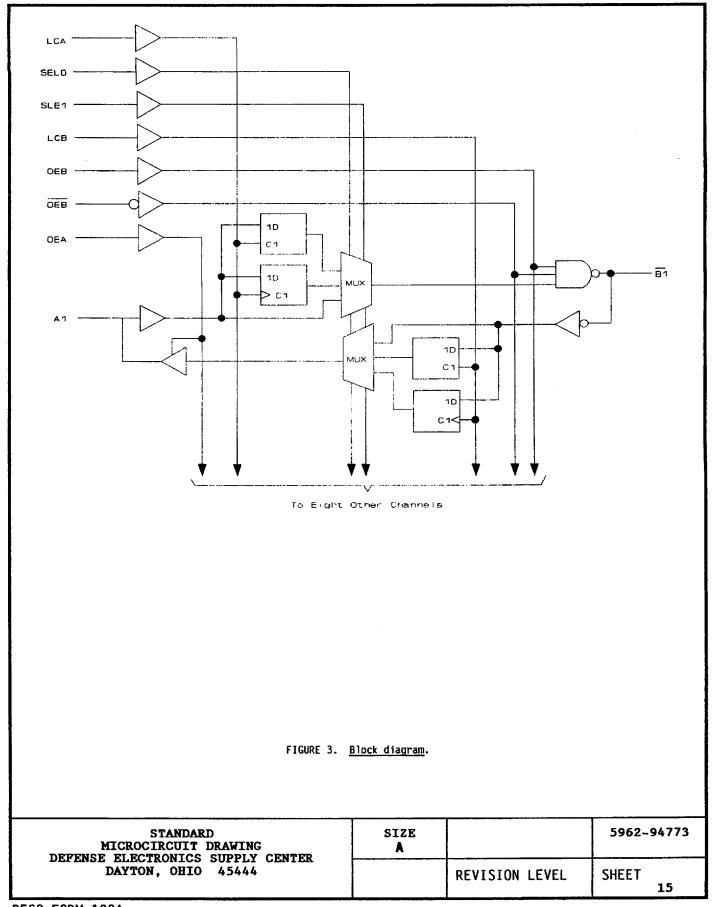
t = Upward transition of clock.

FIGURE 2. <u>Truth tables</u>.

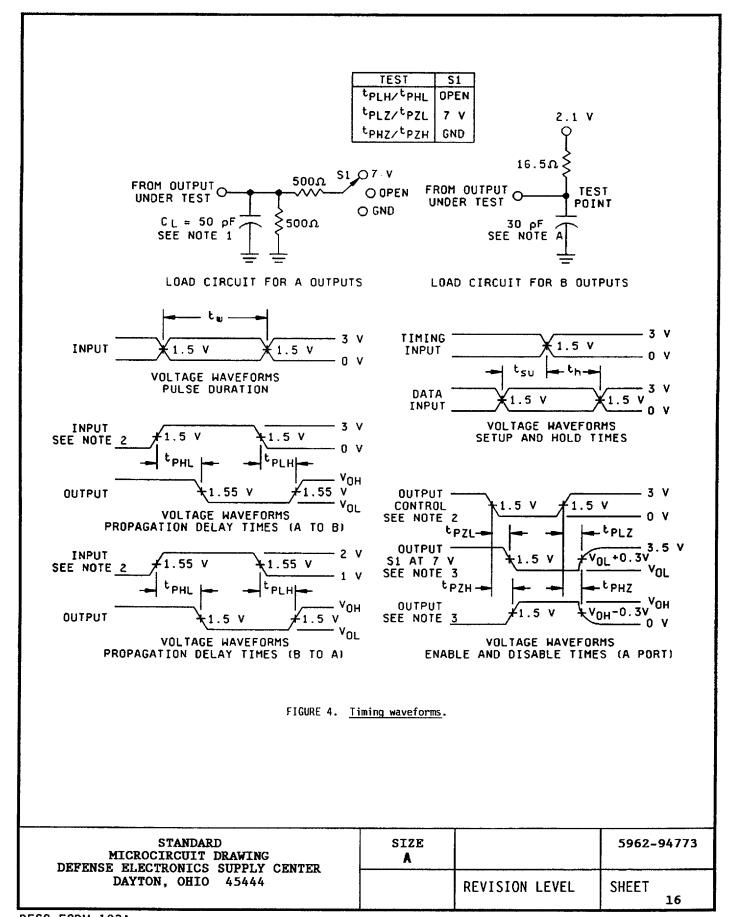
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4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.
- 4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).
- 4.4 <u>Conformance inspection</u>. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. Subgroup 4 (C_{IN} , C_{OUT} , and $C_{I/O}$ measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures. All input and output terminals shall be tested.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth tables. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- 4.4.2 <u>Group C inspection</u>. The group C inspection end-point electrical parameters shall be as specified in table II herein.
 - 4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:
 - a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
 - b. $T_A = +125$ °C, minimum.
 - c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

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TABLE II. <u>Electrical test requirements</u>.

Test requirements	Subgroups (in accordance with MIL-STD-883, IM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	 Device class Q	Device class V
Interim electrical parameters (see 4.2)			
final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/1, 2, 3, 7, 8, 9, 10, 11	<u>2</u> / 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8	1, 2, 3 7, 8	1, 2, 3 7, 8
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3 7, 8	1, 2, 3 7, 8
Group E end-point electrical parameters (see 4.4)			

^{1/} PDA applies to subgroup 1.

- 4.4.3 <u>Group D inspection</u>. The group D inspection end-point electrical parameters shall be as specified in table II herein.
- 4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.
 - c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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 $[\]overline{2}$ / PDA applies to subgroups 1 and 7.

5. PACKAGING

- 5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.6. NOTES
- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
 - 6.1.2 Substitutability. Device class Q devices will replace device class M devices.
- 6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.
- 6.3 <u>Record of users</u>. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.
- 6.4 <u>Comments</u>. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.
- 6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.
- 6.6 One part one part number system. The one part one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIM's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIM. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Orawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

- 6.7.1 Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.
- 6.7.2 <u>Approved sources of supply for device class M</u>. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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