XC1736A/XC1765 Serial Configuration PROM

Product Specification

FEATURES

- One-Time Programmable (OTP) 36,288 x 1 bit and 65,536 x 1 bit serial memories designed to store configuration programs for Programmable Gate Arrays
- Simple interface to Logic Cell™ Arrays (LCA) requires only one user I/O pin
- Daisy chain configuration support for multiple XC2000 or XC3000 LCAs
- Cascadable to support additional configurations or future higher-density arrays
- Military XC1765R screening and quality conformance inspection is patterned after the requirements of MIL-STD-883, methods 5004 and 5005.
- Low-power CMOS EPROM process
- Programmable reset polarity for the XC1765
- Available in the space-efficient 8-pin plastic or ceramic DIP, or in 20-pin surface-mount PLCC package
- PC-based programming supported by the XILINX DS112 and other leading programmer manufacturers

DESCRIPTION

The XC1736A/XC1765 Serial Configuration PROMs (SCP) provide an easy-to-use, cost-effective configuration memory for Xilinx Field Programmable Gate Arrays. Both the XC1736A and the XC1765 are packaged in the economical 8-pin plastic DIP and are also available in the popular 20-pin Plastic Leaded Chip Carrier. The XC1765 is also available in an 8-pin ceramic DIP that supports the military temperature range. The XC17XX family uses a simple serial-access procedure to configure one or more LCA devices. The XC1765 organization (65,536 x 1) supplies enough memory to configure one XC3090 or multiple smaller LCAs. Multiple configurations for a single LCA can also be loaded from the XC17XX family. Using a special feature of the XC1765, the user can select the polarity of the reset function by programming a special EPROM bit.

The XC1736A/XC1765 can be programmed with the PC-based Xilinx XC-DS112 Configuration PROM Programmer or with programmers from other manufacturers. The LCA design file is first compiled into a standard HEX format with the XC-DS501 Development System. It can then be transferred to the programmer through a serial port on the PC.

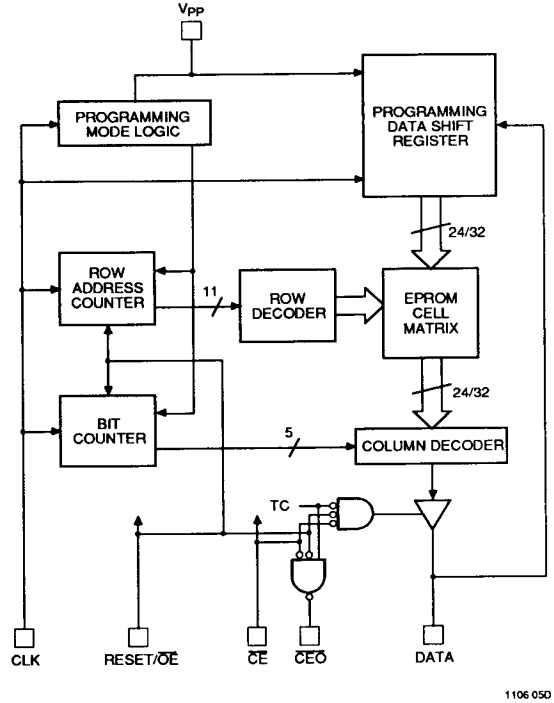
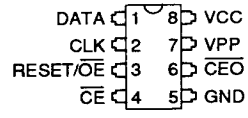
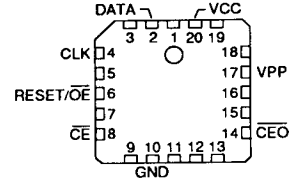


Figure 1. XC1736A/XC1765 Block Diagram



XC1736A/XC1765 8-Pin DIP Pin Assignments



XC1736A/XC1765 20-Pin PLCC Pin Assignments

Table 1. XC1736A/XC1765 Pin Assignments for 8-Pin DIP

PLCC Pin	DIP Pin	Name	I/O	Description
2	1	DATA	O	Three-state DATA output for reading. Input/Output pin for programming.
4	2	CLK	I	Clock input. Used to increment the internal address and bit counters for reading and programming.
6	3	RESET/ $\overline{OE}$	I	Output Enable input. A Low level both the $\overline{CE}$ and RESET/$\overline{OE}$ inputs enables the data output driver. A High level on RESET/$\overline{OE}$ resets both the address and bit counters. In the XC1765, the logic polarity of this input is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. This document describes the pin as RESET/$\overline{OE}$ although the opposite polarity is also possible on the XC1765.
8	4	$\overline{CE}$	I	Chip Enable input. Used for device selection. A Low level on both $\overline{CE}$ and $\overline{OE}$ enables the data output driver. A High level on $\overline{CE}$ disables both the address and bit counters and forces the device into a low power mode.
10	5	GND		Ground pin.
14	6	$\overline{CEO}$	O	Chip Enable Out output. This signal is asserted Low on the clock cycle following the last bit read from the memory. It will stay Low as long as $\overline{CE}$ and $\overline{OE}$ are both Low. It will then follow $\overline{CE}$ until $\overline{OE}$ goes High. Thereafter $\overline{CEO}$ will stay High until the entire PROM is read again and senses the status of RESET polarity.
17	7	V_{PP}		Programming Voltage Supply. Used to enter programming mode (+6 V) and to program the memory (+15 V) Must be connected directly to Vcc for normal Read operation. No overshoot above +15.5 V permitted.
20	8	V_{CC}		+5 V power supply input.

CONTROLLING THE XC1736A/XC1765 SERIAL PROMS

Most connections between the LCA device and the Serial PROM are simple and self-explanatory:

- The DATA output of the XC1736A (or XC1765) drives DIN of the LCA devices.
- The master LCA CCLK output drives the CLK input of the XC1736A/XC1765(s)
- The $\overline{CEO}$ output of any XC1736A/XC1765 can be used to drive the $\overline{CE}$ input of the next XC1736A/XC1765 in a cascade chain of PROMs.
- V_{PP} must be connected to V_{CC}. Leaving V_{PP} open can lead to unreliable, temperature-dependent operation.

There are, however, two different ways to use the inputs $\overline{CE}$ and $\overline{OE}$.

1. The LCA D/$\overline{P}$ or LDC output drives both $\overline{CE}$ and $\overline{OE}$ in parallel. This is the simplest connection, but it fails when a user applies $\overline{RESET}$ during the LCA configuration process. The LCA will abort the configuration and then restart a new configuration, as intended, but the XC1736A/XC1765 does not reset its address counter, since it never saw a High level on its $\overline{OE}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the LCA device is the master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and D/$\overline{P}$ goes High. However, the LCA configuration will be completely wrong, with potential contentions inside the LCA device and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

2. The LCA D/$\overline{P}$ or LDC output drives only the $\overline{CE}$ input of the XC1736A/XC1765, while its $\overline{OE}$ input is driven by the inversion of the LCA $\overline{RESET}$ input. This connection works under all normal circumstances, even when the user aborts a configuration before D/$\overline{P}$ has gone High. The High level on the $\overline{OE}$ input during RESET clears the PROM internal address pointer, so that the reconfiguration starts at the beginning. Most designs have a spare inverter or inverting gate that can be used for this purpose. The XC1765 does not require this inverter since the RESET polarity is programmable, so that it is compatible with the LCA device.

LCA MASTER SERIAL MODE SUMMARY

The I/O and logic functions of the Logic Cell Array and their associated interconnections, are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three LCA mode pins. In Master Mode, the Logic Cell Array automatically loads the configuration program from an external memory. The Serial Configuration PROM has been designed for compatibility with the Master Serial Mode.

Upon power-up or upon reconfiguration, an LCA device will enter Master Serial Mode whenever all three of the LCA mode-select pins are Low (M0=0, M1=0, M2=0). Data are read from the Serial Configuration PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure an LCA. Data from the Serial Configuration PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

Programming the LCA With Counters Reset Upon Completion

Figure 2 shows the connections between an XC3000 LCA device and its SCP. The DATA line from the SCP is connected to the DIN input of the LCA device. CCLK is connected to the CLK input of the SCP. At power-up or upon reconfiguration, the D/$\overline{P}$ signal goes Low (pulled Low by the LCA device at reset, or by external circuitry for reconfiguration), enabling the SCP and its DATA output. During the configuration process, CCLK clocks data out of the SCP on every rising clock edge. At the completion of configuration, the D/$\overline{P}$ signal goes High and resets the internal address counters of the SCP. For XC3000 devices with a late DONE or XC2000 devices, LDC may be used to control $\overline{CE}$.

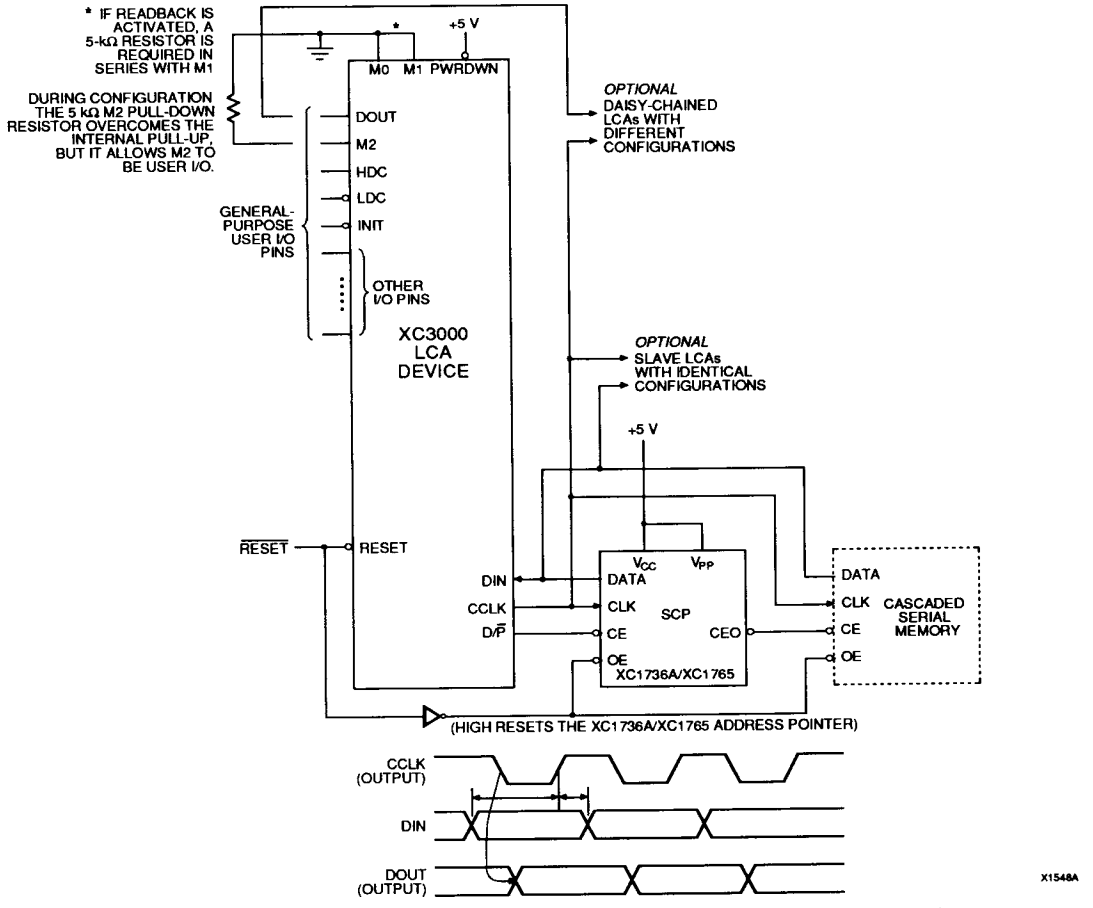


Figure 2. Master Serial Mode. The one-time-programmable XC1736A/XC1765 Serial Configuration PROM supports automatic loading of configuration programs up to 36K/64K bits. Multiple devices can be cascaded to support additional LCAs. An early D/$\overline{P}$ inhibits the PROM data output a CCLK cycle before the LCA I/Os become active.

If the user-programmable, dual-function DIN pin is used only for configuration, it must still be held at a defined level during normal operation. The XC3000 family takes care of this automatically with an on-chip default pull-up resistor. On XC2000-family devices, the user must either configure DIN as an active output, or somehow provide a defined level, e.g., by using an external pull-up resistor, if DIN is configured as an input.

Programming the LCA With Counters Unchanged Upon Completion

When multiple LCA configurations for a single LCA are stored in a Serial Configuration PROM, the $\overline{OE}$ pin should be tied Low as shown in Figure 3. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{OE}$ in is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the LCA with another program, the D/$\overline{P}$ line is pulled Low and configuration begins at the last value of the address counters.

Cascading Serial Configuration PROMs

For multiple LCAs configured as a daisy-chain, or for future LCAs requiring larger configuration memories, cascaded SCPs provide additional memory.

After the last bit from the first SCP is read, the next clock signal to the SCP asserts its $\overline{CEO}$ output Low and disables its DATA line. The second SCP recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 2.

After configuration is complete, the address counters of all cascaded SCPs are reset if $\overline{RESET}$ goes Low forcing the RESET/$\overline{OE}$ on each SCP to go High.

If the address counters are not to be reset upon completion, then the RESET/$\overline{OE}$ inputs can be tied to ground, as shown in Figure 3. To reprogram the LCA device with another program, the D/$\overline{P}$ line goes Low and configuration begins where the address counters had stopped. In this case, avoid contention between DATA and the configured I/O use of DIN.

Extremely large, cascaded memories in some systems may require additional logic if the rippled chip enable is too slow to activate successive SCPs.

STANDBY MODE

The XC17XX enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the SCP consumes less than 0.5 mA of current. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

PROGRAMMING MODE

Figures 4 and 5 show the programming algorithm for the XC1736A/XC1765. Note that programming mode is entered by holding V_{PP} High for at least two clock edges and is exited by removing power from the device or by a Low on both $\overline{CE}$ and $\overline{OE}$.

XC1765 RESET POLARITY

The XC1765 lets the user choose the reset polarity as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. The Xilinx DS112 programmer and its XPP software prompt the user for the desired reset polarity. Any third-party commercial programmer should do the same.

The polarity is programmed into the first four overflow byte locations, 2000H through 2003H. 00000000 in these locations makes the reset active Low, FFFFFFFF in these locations makes the reset active High. The programming of these overflow bytes should be handled transparently by the PROM programmer; it is mentioned here only as additional information.

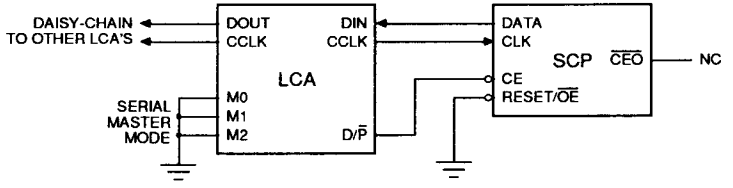


Figure 3. Address Counters Not Reset

Notes: 1. If M2 is tied directly to ground, it should be programmed as an input during operation.
2. If the LCA is reset during configuration, it will abort back to initialization state. D/$\overline{P}$ will not go High, so an external signal is required to reset the 17XX counters.

ABSOLUTE MAXIMUM RATINGS

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{PP}	Supply voltage relative to GND	–0.5 to +15.5	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +125	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

OPERATING CONDITIONS

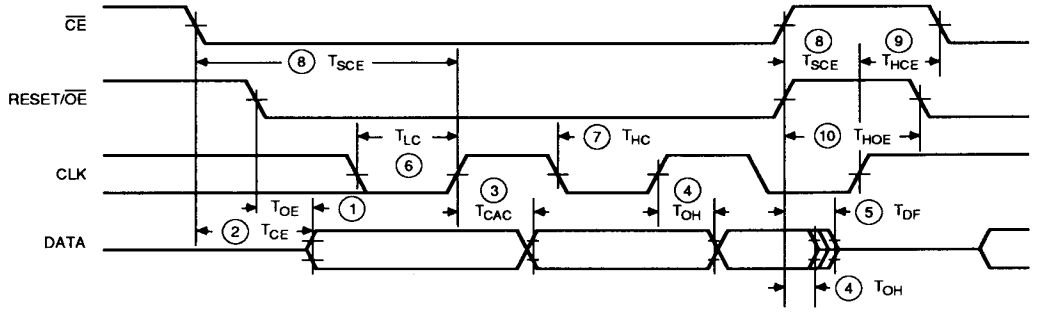
Symbol	Description			Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND	–0°C to +70°C	4.75	5.25	V
	Industrial	Supply voltage relative to GND	–40°C to +85°C	4.5	5.5	V
	Military	Supply voltage relative to GND	–55 °C +125°C	4.5	5.5	V

DC CHARACTERISTICS OVER OPERATING CONDITIONS

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	Vcc	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)	Commercial		0.32	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)	Industrial		0.37	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Military	3.7		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)	Military		0.4	V
I_{CCA}	Supply current, active mode			10	mA
I_{CCS}	Supply current, standby mode			0.5	mA
I_L	Input or output leakage current		–10	10	µA

Note: During normal read operation, V_{PP} ***must*** be connected to V_{CC}.

AC CHARACTERISTICS OVER OPERATING CONDITIONS



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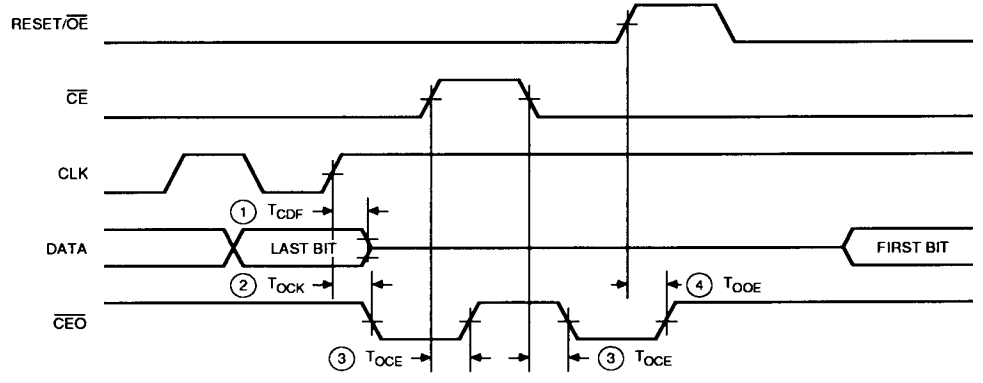
Symbol		Description	Limits Min	Limits Max	Units
1	T_{OE}	$\overline{OE}$ to Data Delay		45	ns
2	T_{CE}	$\overline{CE}$ to Data Delay		60	ns
3	T_{CAC}	CLK to Data Delay		150	ns
4	T_{OH}	Data Hold From $\overline{CE}$, $\overline{OE}$, or CLK	0		ns
5	T_{DF}	$\overline{CE}$ or $\overline{OE}$ to Data Float Delay		50	ns
6	T_{LC}	CLK Low Time[4]	100		ns
7	T_{HC}	CLK High Time	100		ns
8	T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		ns
9	T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)[4]	0		ns
10	T_{HOE}	$\overline{OE}$ High Time (Guarantees Counters Are Reset)	100		ns

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with minimum tester ac load and maximum dc load.
4. Guaranteed by design, not tested.



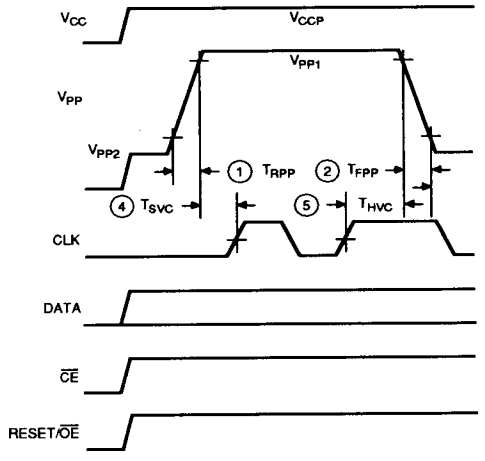
1106 11

Symbol			Limits Min	Limits Max	Units
1	T_{CDF}	CLK to Data Float Delay		50	ns
2	T_{OCK}	CLK to $\overline{CEO}$ Delay		65	ns
3	T_{OCE}	$\overline{CE}$ to $\overline{CEO}$ Delay		45	ns
4	T_{OOE}	RESET/$\overline{OE}$ to $\overline{CEO}$ Delay		40	ns

PROGRAMMING SPECIFICATIONS

The data on pages 2-181, 182, and 183 is not relevant to the use of programmed PROMs and is not required for operating commercially available programming equipment. This information is printed here only as tutorial background information for the interested user.

Any designer of programming equipment will need additional information, available from Xilinx Component Product Marketing. Call (408) 879-5396 or fax (408) 559-7114.



X1746

Enter Programming Mode

DC PROGRAMMING SPECIFICATIONS

Symbol		Description	Limits Min	Limits Max	Units
1	V_{CCP}	Supply voltage during programming	5.25	5.75	V
2	V_{IL}	Low-level input voltage	0.0	0.5	V
3	V_{IH}	High-level input voltage	2.4	V_{CC}	V
4	V_{OL}	Low-level ouptput voltage		0.4	V
5	V_{OH}	High-level output voltage	3.7		V
6	V_{PP1}	Programming voltage*	14.5	15.5	v
7	V_{PP2}	Programming-mode access voltage	5.75	6.25	V
8	I_{PPP}	Supply current in programming mode		60	mA
9	I_L	Input or output leakage current	-10	10	µA
10	V_{CCL}	First pass Low-level supply voltage	4.3	4.5	V
11	V_{CCH}	Second pass High-level supply voltage	5.5	5.7	V

*No overshoot is permitted on this signal. V_{PP} must not be allowed to exceed V_{PP1} max

AC PROGRAMMING SPECIFICATIONS

Symbol		Description	Limits Min	Limits Max	Units
1	T_{RPP}	10% to 90% Rise Time of VPP	50	70	µs
2	T_{FPP}	90% to 10% Fall Time of VPP	50	70	µs
3	T_{PGM}	VPP Programming Pulse Width	0.95	1.05	ms
4	T_{SVC}	Setup of VPP to CLK to Enter Programming Mode	100		ns
5	T_{HVC}	Hold of VPP to CLK to Enter Programming Mode	300		ns

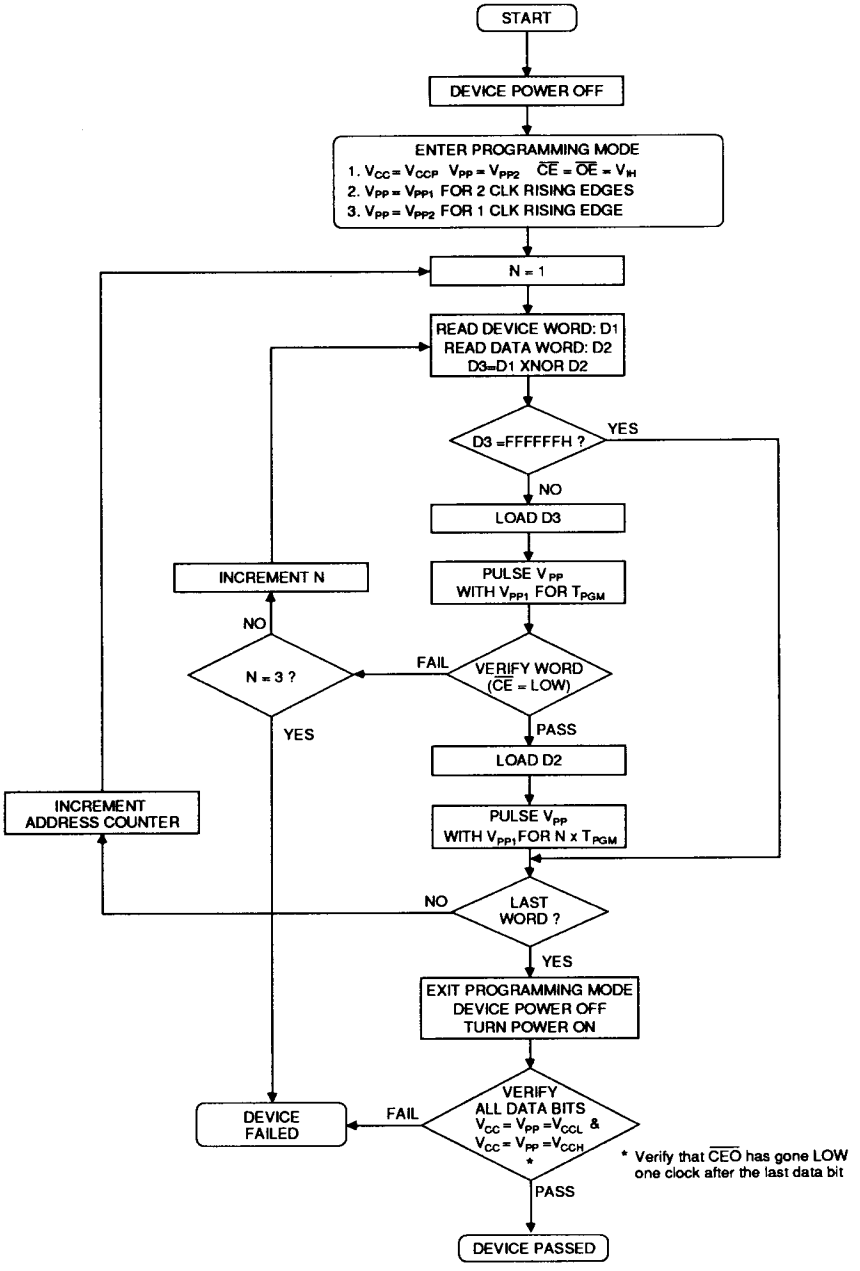


Figure 4. Programming Sequence (XC1736A)

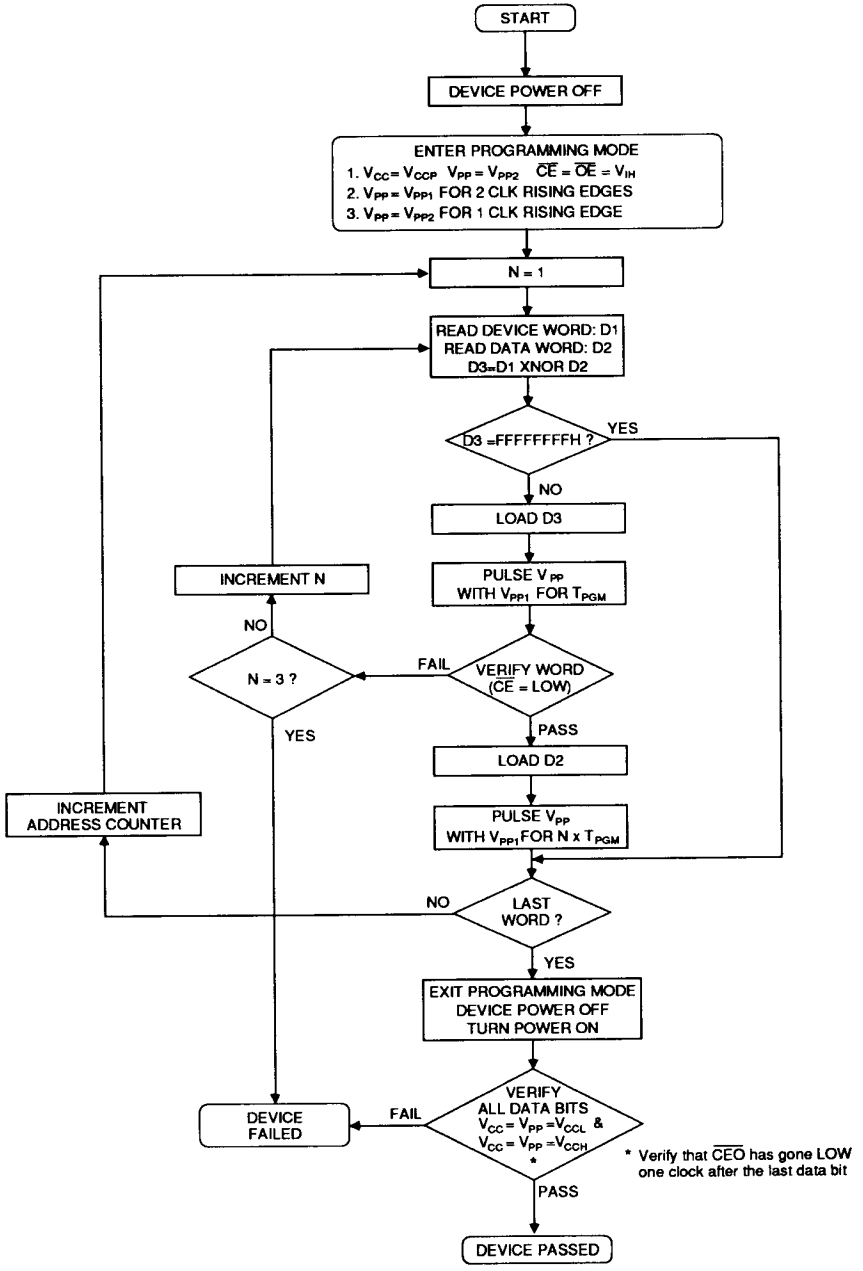


Figure 5. Programming Sequence (XC1765)

SERIAL PROM-PROGRAMMER SUPPORT

Xilinx offers PROM-programmer support for the XC1736A and XC1765 through the DS112 programmer. The latest release of XPP is revision 3.10 which supports the XC1736A and XC1765. The Am1736 is supported by an update to that release: P/N 1060265 for 5-1/4" disk or P/N 1060266 for 3-1/2" disk. Contact Customer Service for details on availability.

Do not program the XC1736A with the DS81 programmer or the XC1736 non "A" algorithm, as this stresses the device causing potential reliability problems. Use the DS112 with the XC1736A algorithm only!

There have been numerous inquiries regarding other vendor support for the serial PROM family (XC1736A and XC1765). Below is the latest list of PROM-programmer manufacturers that offer support for the XC1736A, XC1765, and the Am1736.

Data I/O
(206) 881-6444
Model 29B Unipak 2B V21 XC1736A
V22 XC1765
Model Unisite V3.0 XC1736A
V3.1 XC1765
Model 2900 V1.1 XC1736A
V1.1 XC1765
V1.1 Am1736

Advin Systems
(408) 984-8600
Model SAILOR-PAL/SA
SAILOR-PAL/SB
PILOT 142 143 144 145
Supports XC1736A Am1736 XC1765

Logical Devices
(305) 974-0967
Model ALLPRO
XC1736A
XC1765 V1.51
XC1736 V1.5

Oliver Advanced Engineering
(818) 240-0080
Model OMNI 40 and ONMI 64
XC1736A Rel 2.51Q
XC1765 Rel 2.51Q
Am1736 Rel 2.51Q

Stag Microsystems LTD
UK 707 332-148
US (408) 988-1118
Model System 3000
XC1736A
XC1765

Bytek Corporation
(408) 437-2414
Model 135H-U
XC1736A
XC1765
Am1736

System General
(408) 263-6667
Model SGUP-85A V1.7 XC1736A
V1.7 XC1765

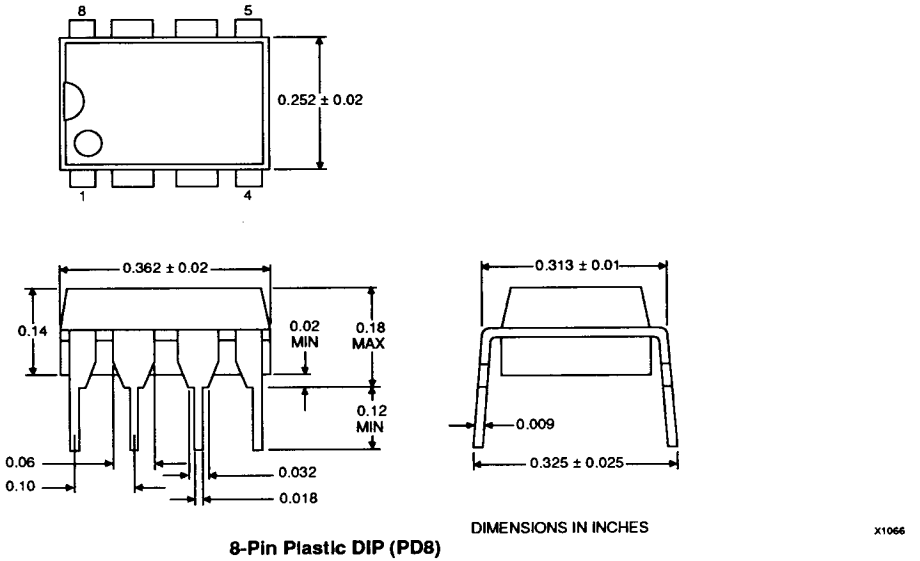
BP Microsystems
(713) 461-9606
Model EP1140 Head 40A
V1.40 XC1736A
V1.40 XC1765
V1.40 Am1736

Link Computer Graphics
(201) 994-6669
Model CLK 3100 V3.1 or greater
XC1736A
XC1765

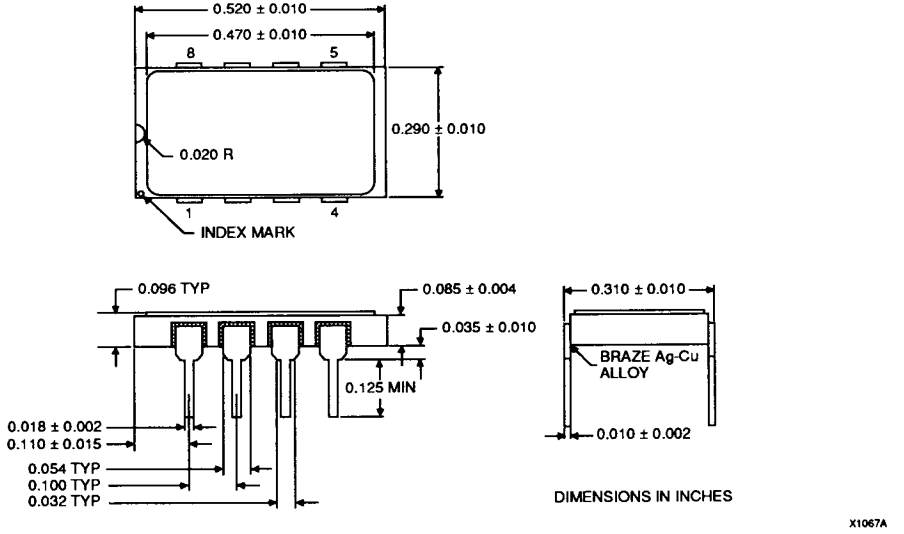
Xeltek
(408) 727-6995
Model Unipro
V2.13 XC1736A
V2.13 XC1765

Pistohl Electronic Tool Company
(408) 255-2422
Model PET 110 PET 120 PET 130
XC1736A
XC1765
Am1736

PHYSICAL DIMENSIONS

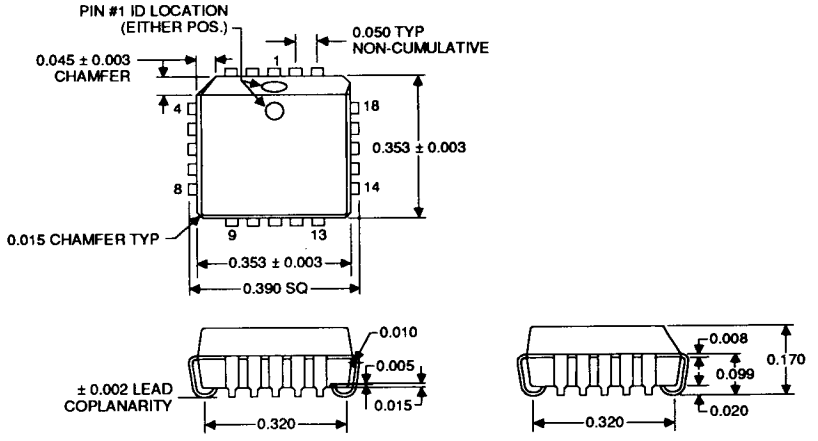


8-Pin Plastic DIP (PD8)

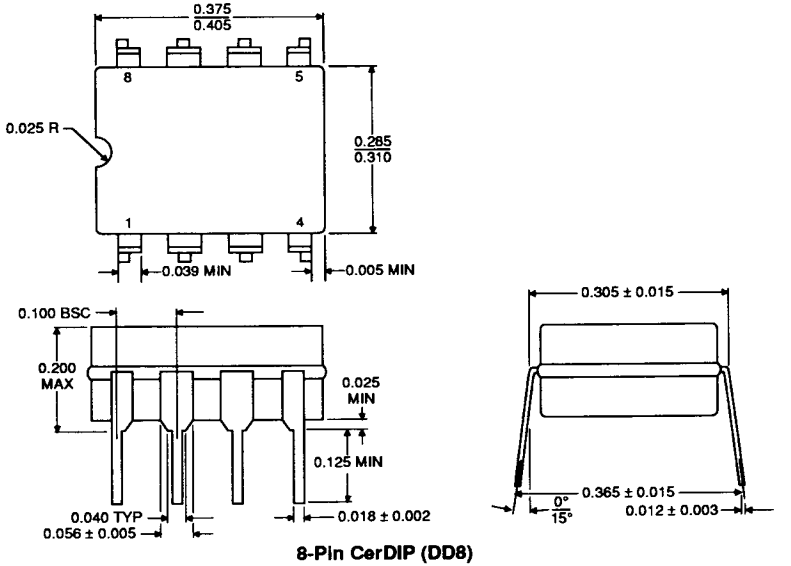


8-Pin Ceramic Sidebrazed DIP (CD8)

PHYSICAL DIMENSIONS (Continued)



20-Pin PLCC (PC20)



8-Pin CerDIP (DD8)

ORDERING INFORMATION AND VALID ORDERING COMBINATIONS

XC17XX - PC20C

DEVICE NUMBER
XC1736A
XC1765

OPERATING RANGE/PROCESSING
C = COMMERCIAL/INDUSTRIAL (-40° TO +85°C)
M = MILITARY (-55° TO +125°)
R = MILITARY (-55° TO +125°C) WITH
MIL-STD-883 LEVEL B EQUIVALENT PROCESSING

PACKAGE TYPE
PC8 = 8-PIN PLASTIC DIP
DD8 = 8-PIN CERDIP
CD8 = 8-PIN CERAMIC SIDE-BRAZED DIP
PC20 = 20-PIN PLASTIC LEADED CHIP CARRIER

X1188

XC1736A-PD8C	XC1765-PD8C
XC1736A-PC20C	XC1765-PC20C
XC1736A-CD8M	XC1765-CD8M
XC1736A-DD8M	XC1765-DD8M
	XC1765-DD8R