MF016-01

SUWA SEIKOSHA

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from M. Chugon

technical manual

SED1500 series

DOT MATRIX LCD DRIVER

- Duty 1/8 – 1/16 LCD Driver
- One-chip LCD Driver (with Built in Display Data RAM)

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SUWA SEIKOSHA CO., LTD.

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1. GENERAL DESCRIPTION

The SED150 Series is a dot matrix LCD driver LSI, developed for not only character display but meeting higher degrees of freedom as in graphic and bit image display. Because the SED150 has a built-in display RAM that serves simultaneously as a refresh memory to store data for all picture elements and a line memory, the SED150 can be coupled to a microcomputer or micro-processor. That part of the display RAM which is not directly used for display can be used as a scratch pad memory for the micro-procesing unit. The SED150 can be interfaced with either a 4-bit or 8-bit micro-processing unit by commands, and particularly, the limited ports of a 4-bit micro-processing unit can be efficiently used.
The SED150 Series has a total of 50 common drivers and segment drivers, and a maximum of 1/16 multiplex drives per chip can be selected by a metal master slice. Because up to 544 different patterns can be driven per chip, the SED150 is suitable to applications involving low-speed, large-capacity display.
The SED150 consumes only a little current because it is operated by low-frequency clocks so that, by combining it with a C MOS micro-processing unit, battery-driven, long-life, handy systems can be built at low cost.

2. FEATURES

2.1 FEATURES

(1) Dot matrix LCD driver capable of bit image and character display.
(2) Directly connectable to 4-bit and 8-bit micro-processing units (advantageous to low-end systems).
- 8-bit/4-bit data transmission modes can be selected as desired.

(3) Display data RAM: 42×2 bytes
672 dots maximum or 16 characters + indicator 32 segments maximum
- Be capable of Read/Write.

(4) Built-in LCD drivers
Common drivers: 16 maximum, 0 minimum
Segment drivers: 42 maximum, 34 minimum
- A wide range of variety within the range of a total of 50 common and segment drivers, selectable by metal master slide, for adaptation to various kinds of LCDs and micro-processing units.

(5) Duty ratio selection
Any duty ratios from 1/8 to 1/16 can be selected. (Metal option)
- 1/16 duty is available in variations capable of common multiple chip composition.

(6) Maximum display capacity
By product specification

Product	Duty	No. of segment drivers	Minimum No. of chips	No. of display dots	No. of characters (per chip)
SED1500	1/8	42	1	336	8 characters × 1 line + 16 seg
SED1501	1/10	40	1	400	
SED1502	1/16	34	1	544	6 characters × 2 lines + 64 seg
SED1503	1/16	42	2	672 × 2	8 characters × 2 lines + 32 seg

* SED1500 can be used for building continuous dot panels of 5 × 7 characters with high dot efficiency. (7 characters per line)

(7) C MOS Si-Gate process

(8) Logic power supply: UM –5V battery (Separate power supply necessary for driving LCD)
- Electrical characteristics are as shown in the specifications. Operation on a UM –3V battery is also possible.
- Inputand output: TTL (LS) compatible (where 5V power is used).

(9) Oscillator circuit built in (CR).

(10) Operating temperature range: –20°C to +75°C

(11) 80-pin plastic flat package.

2.2 SED150 SERIES METAL OPTION GUIDE

(1) The following metal options are available for the SED150 Series to meet the specifications that are frequently required by users.

Optional specifications

1. Liquid crystal drive duty ratio: 1/n (n = 8 to 16)
2. Common output
   Common single chip configuration (for small-capacity display)
   Common multiplechip configuration (for medium- or large-scale display)
3. Type of oscillator
   CR oscillator (Standard specification)
   Crystaloscillator (32.768 kHz)

(2) Optional specifications vs. products

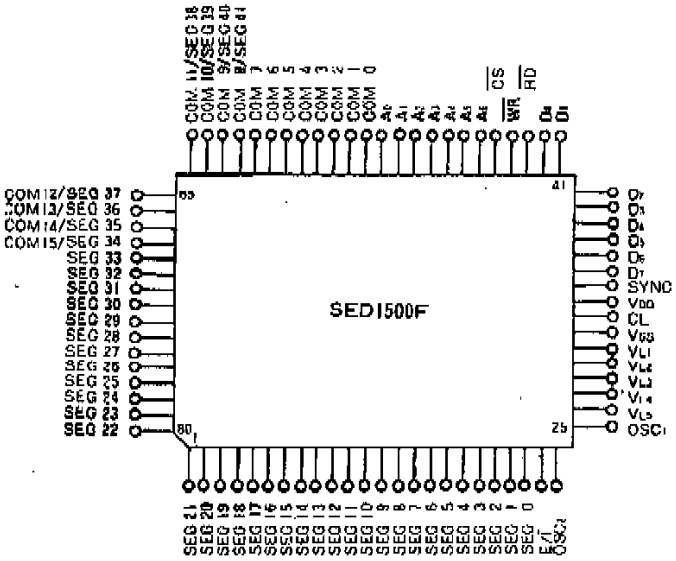
Duty ratio	Common signal chip			Common multiple chip			Crystal oscillator	CR oscillator	
	Product name	No. of common output terminals	No. of segment output terminals	Product name	No. of common output terminals	No. of segment output terminals	Frame frequency	Standard oscillating frequency fosc (Note: 2) MΩ	Initial stage dividing ratio
1/8	SED1500	8	42		4	42	64.0 Hz	32.8 kHz (Rf = 1.4)	1/4
1/9		9	41		5	42	56.9 Hz	36.9 kHz (Rf = 1.2)	1/4
1/10	SED1501	10	40		5	42	68.3 Hz	30.7 kHz (Rf = 1.5)	1/3
1/11		11	39		6	42	62.1 Hz	33.8 kHz (Rf = 1.4)	1/3
1/12		12	38	SED1504	6	42	56.9 Hz	36.9 kHz (Rf = 1.2)	1/3
1/13		13	37		7	42	(78.8 Hz)	26.6 kHz (Rf = 1.8)	1/2
1/14		14	36		7	42	73.1 Hz	28.7 kHz (Rf = 1.6)	1/2
1/15		15	35		8	42	68.3 Hz	30.7 kHz (Rf = 1.5)	1/2
1/16	SED1502	16	34	SED1503	8	42	64.0 Hz	32.8 kHz (Rf = 1.4)	1/2

Note 1: Blanks in the product name columns indicate that product names have not yet been selected.
Note 2: Standard oscillating frequencies apply where a frame frequency of 64 Hz is selected.

3. THEORETICAL CONFIGUARTION AND FUNCTIONS

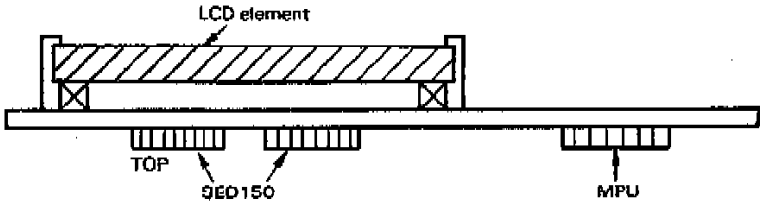
3.1 PIN ARRANGEMENT AND DIMENSIONS

(1) Pin arrangement diagram

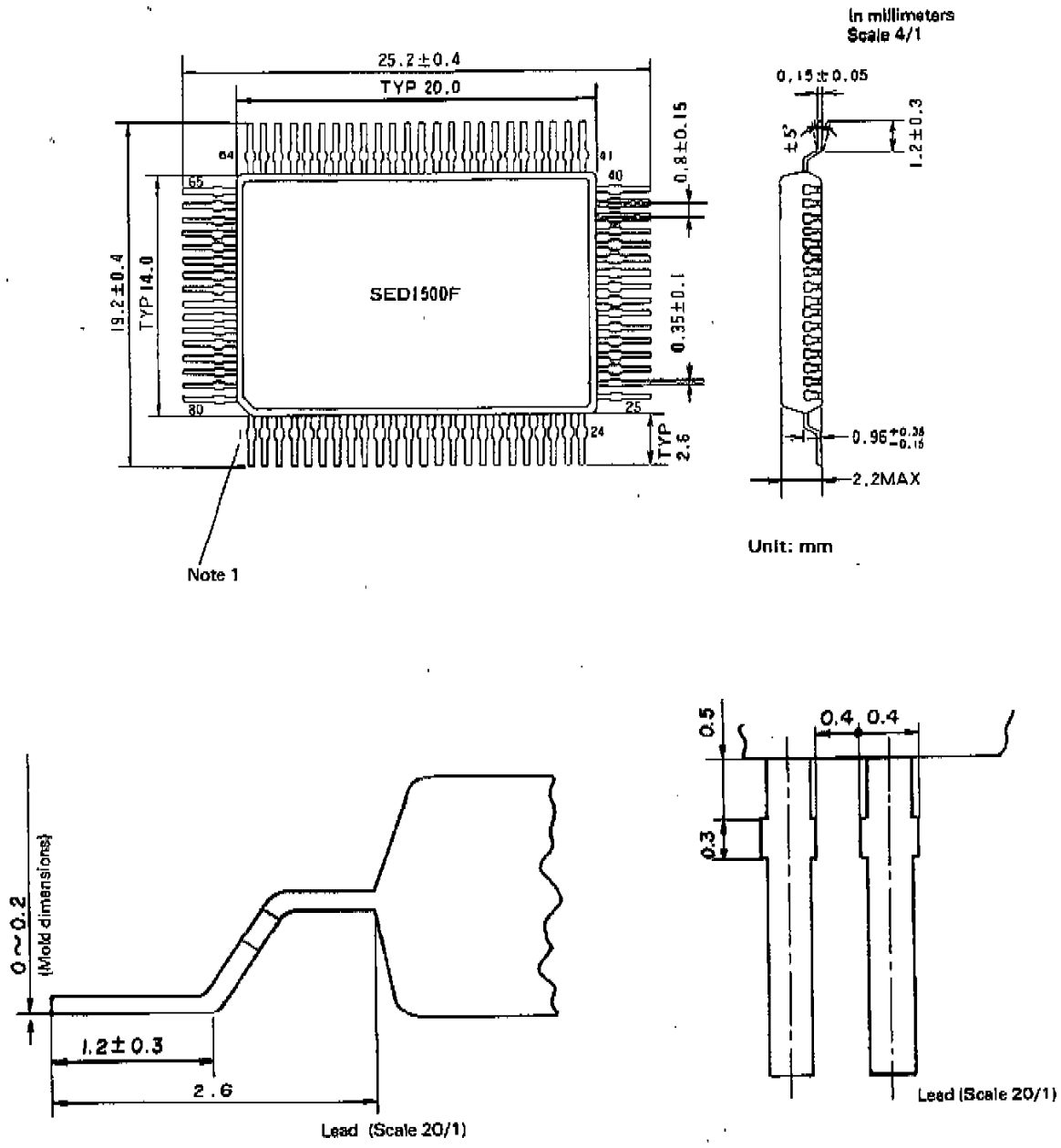


Note: Terminal (Pin No. 61 – No. 68) can be used as either SEG or COM terminal.

(2) Actual example of a display



(3) Dimensional diagram



Note 1: The lead projection from the corner is below the package bottom.

3.2 FUNCTIONS OF TERMINALS

Table of Functions of Terminals

Name of terminal	No. of terminals	Input/output	Connected to	Function
$A_0 \sim A_3$	4	Input	MPU	Address buses for lower 4 bits of DD RAM, command register. Connected to $D_0 \sim D_3$ in case of 1-bus system.
A_4 to A_6	3	Input	MPU	Address buses for upper 3 bits of DD RAM, command register. Connected to $D_4 \sim D_6$ in case of 1 bus system.
D_0 to D_3	4	Input, output	MPU	Tri-state bidirectional data buses for lower 4 lines. Serve as common buses for upper and lower 4 bits in 4-bit transfer mode.
D_4 to D_7	4	Input, output	MPU	Tri-state bidirectional data buses for upper 4 lines. In 4-bit transfer mode, input mode is selected and its data is ignored.
$\overline{RD}$	1	Input	MPU	Read signal $\overline{RD}$ = "L" active
$\overline{WR}$	1	Input	MPU	Write signal $\overline{WR}$ = "L" active
$\overline{CS}$	1	Input	MPU	Chip select signal $\overline{CS}$ = "L" active; $\overline{CS}$ = "H" standby. Bus: High impedance
OSC_1, OSC_2	2			Terminals for connecting internal clock oscillating resistors (or crystal oscillators). OSC_1 is input terminal for operation by external clock.
CL	1	Output	Slave chip	Slave chip driving basic clock to be connected to slave chip OSC_1.
E/$\overline{I}$	1	Input	V_{DD} or V_{SS}	Terminal for selecting master chip/slave chip operation. Slave chip is operated by external clock. Master chip . . . "L" Slave chip . . . "H"
SYNC	1	Input, output	Slave chip	Signal for synchronizing slave chip status with master chip. Input/output terminal for frame signal with duty ratio of 50%. E/$\overline{I}$ = "L" output E/$\overline{I}$ = "H" input
COM_0 to COM_{15}	16 max.	Output	LCD	Common signals. In case of SED1503 slave chip, $COM_0 \sim COM_7$ change to $COM_8 \sim COM_{15}$.
SEG_0 to SEG_{41}	42 max.	Output	LCD	Segment signal. $SEG_{34} \sim SEG_{41}$ change to $COM_{15} \sim COM_8$ depending on models.
VL_1 to VL_5	5		Power supply	LCD driving power supply.
V_{DD}, V_{SS}	2		Power supply	V_{DD} = 0V; V_{SS} = −5V (logic power supply) or V_{DD} = +5V; V_{SS} = 0V
	Total 80			

3.3 BASIC EXTERNAL CONNECTIONS

(1) Power supply

Fig. 3.3-1 is a basic connection diagram showing the basic logic power supply, LCD driving power supply, and oscillator circuits of the SED150 Series. VDD is used in common. The voltage VL5 is adjusted to a level most suitable to the LCD by the temperature compensator circuit. VL5 can be adjusted regardless of VSS.

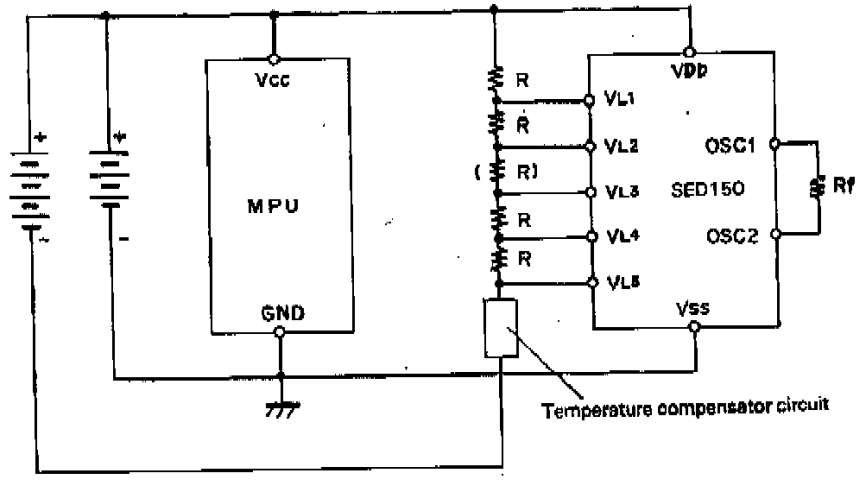
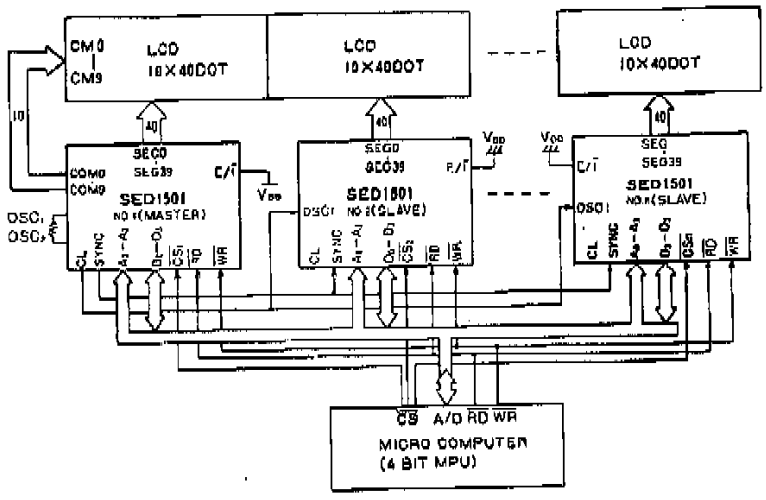


Fig. 3.3-1 Basic Connection Diagram

(2) Examples of LCD system configuration

(a) Example of multi-chip configuration (Example of SED1501; similar configurations available for SED1500, SED1502)

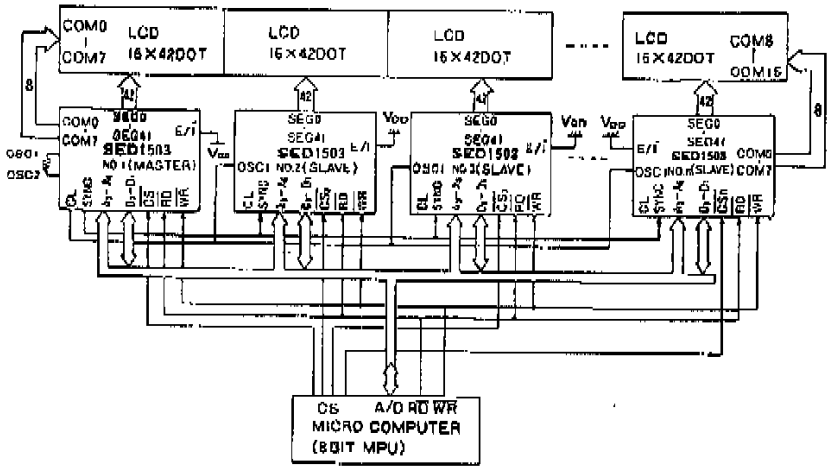
- Number of display dots = 10×40×n; n = 1 to about 10



(b) Example of common multi-chip configuration (SED1503)

- Number of display dots = 16×42×n, 1/16 duty

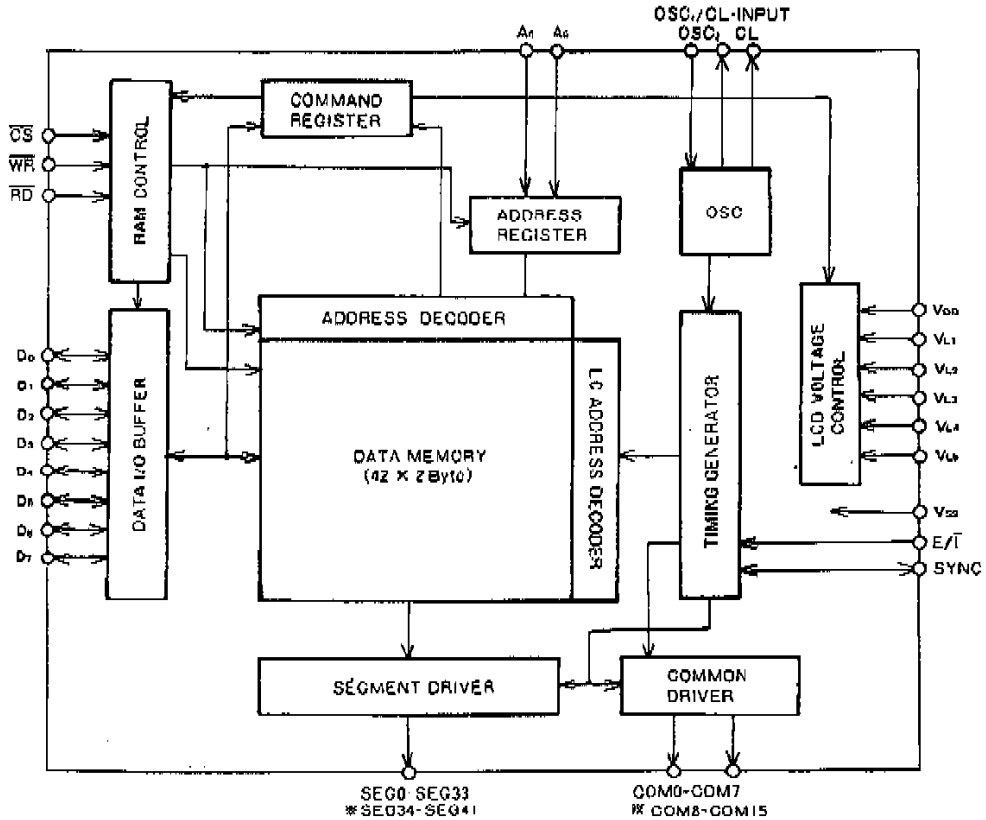
The value of n depends on the load capacity (picture element area) of LCD and the drive capacity of the common driver. In case of normal character display, up to about 10 (n) slaves can be connected.



(3) Power switching on sequence

Switch on or off V_{SS} and V_{L5} simultaneously. When using independent switches, be careful of a latch up which may be rarely induced by a surge voltage.

3.4 BLOCK DIAGRAM



3.5 DESCRIPTION OF EACH BLOCK

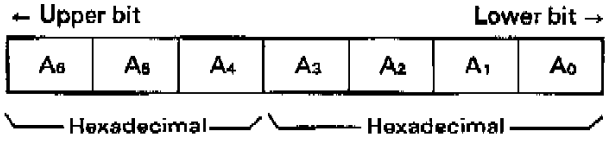
(1) Display data RAM (DD RAM)

The display data RAM is a C MOS static RAM serving as a fresh memory which stores display data for one picture and a line memory. Data "0" and "1" that are written into the DD RAM from data buses DO to D7 are directly displayed on the liquid crystal panel as OFF or ON. Thus, not only characters each composed of 5×7 dots but also other data, such as bit images and a number of segment patterns can be displayed through processing by micro-processing units.

The user area of the display data RAM whichis unused for display is open for use as scratch pad memory for the micro-processing unit. Be careful, however, becuase the user area varies with the number of commons. This is illustrated in Fig. 3.5-1.

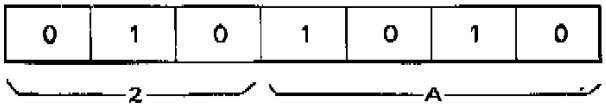
(a) DD RAM address

DD RAM address date is composed of 7 bits, and expressed in hexadecimals.



When expressing address data in hexadecimals, the most significant bit (A7) is expressed by a 0.

Example: DD RAM address 2AH



(b) DD RAM addresses versus positions on LCD element

DD RAM address and dot positions on the LCD panel correspond to each other 1 to 1. In Fig. 3.5-1, for example, the relationship between the hatched dots and DD RAM is as follows.

Position on panel	DD RAM address
Picture element at crosspoint of SEG_{38} and COM_6	Bit of address 26_H and data D_6
Data "1" "0"	ON Off
No display	User area

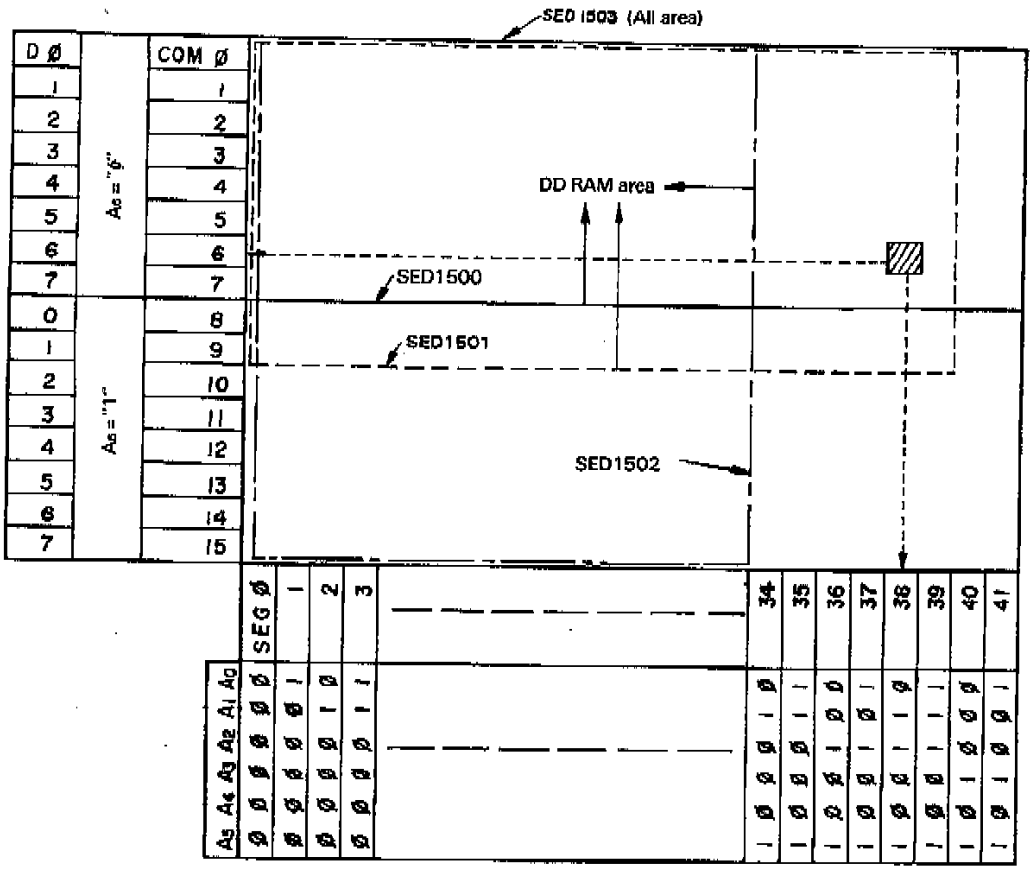


Fig. 3.5-1 Display Data Area of DD RAM

(2) LCD driver

The LCD driver circuit consists of a maximum of 16 common drivers and a maximum of 42 segment drivers as shown in the table below. The circuit outputs a multi-level, two-frame AC drive waveform as shown in Fig.3.5-8. The time for a single frame is TYP 1/64 sec, and a frame signal is output from the SYNC terminal.

Product name	No. of commons	No. of segments	Max. No. of driving dots/chip
SED1500	8	42	336
SED1501	10	40	400
SED1502	16	34	544
SED1503	8	• 42	672

(a) Common multi-chip configuration

The SED1503 drives the largest number of dots per chip because 1/16 duty is achieved by two chips with each chip taking care of 1/8 duty of commons.

In this case, one of the two chips is the master, and the other the slave. That is, the chip for the function select terminal E/I = "L" becomes the master chip and outputs a sync signal.

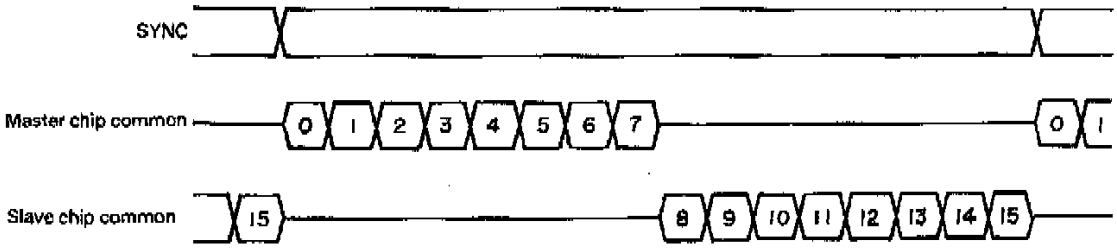


Fig. 3.5-2 Timing Diagram of Common Multi-Chip Configuration

(3) Oscillator circuit

The SED1500 Series has a built-in oscillator circuit with two terminals OSC 1 (IN) and OSC2 (OUT).

(a) Using the built-in oscillator circuit as CR oscillator Connect an oscillation resistor Rf to the oscillator terminals as shown in Fig.3.5-3 so that the sync signal frequency will be 32 Hz (typ).

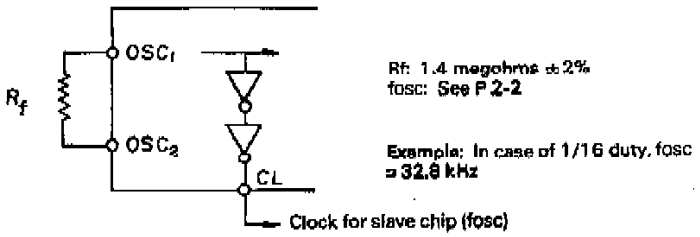


Fig. 3.5-3 CR Oscillator

* OSC 1 and OSC 2 should be wired as short as possible because the oscillating frequency varies with wire capacity.

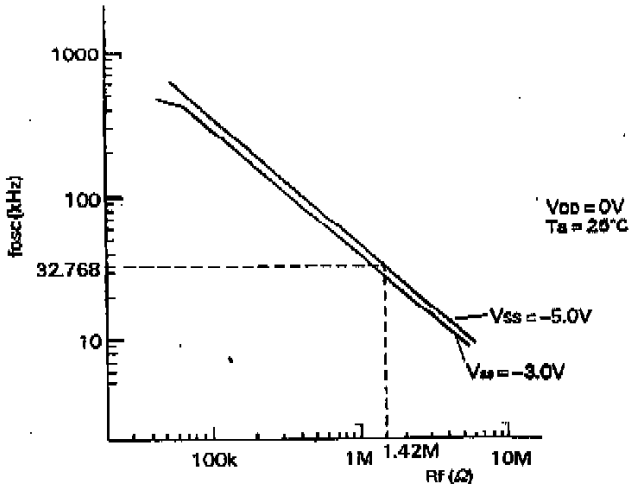
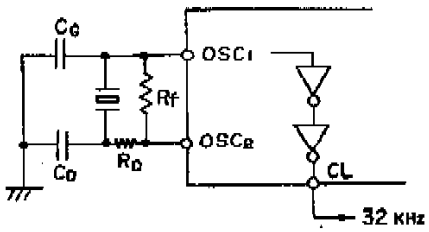


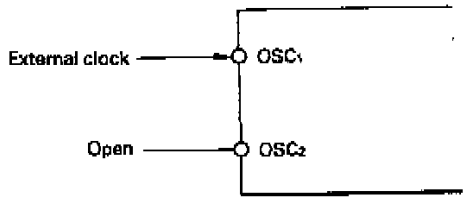
Fig. 3.5-4 Rf vs. Oscillating Frequency

(b) Using the built-in oscillator as crystal oscillator circuit

With the SED150 Series, a 32 kHz crystal oscillator circuit can be composed by the metal master slice corresponding to the LCD driving duty, and the local frequency can be supplied to the outside.



(c) Operation by external clock



* Even when an external clock is input, the clock CL is output from the slave chip.

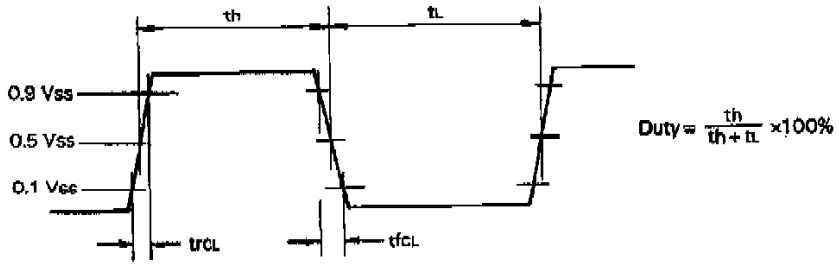


Fig. 3.5-5 External Clock Timing Characteristics

(4) Liquid crystal driving power supply

(a) Voltage diving ratio

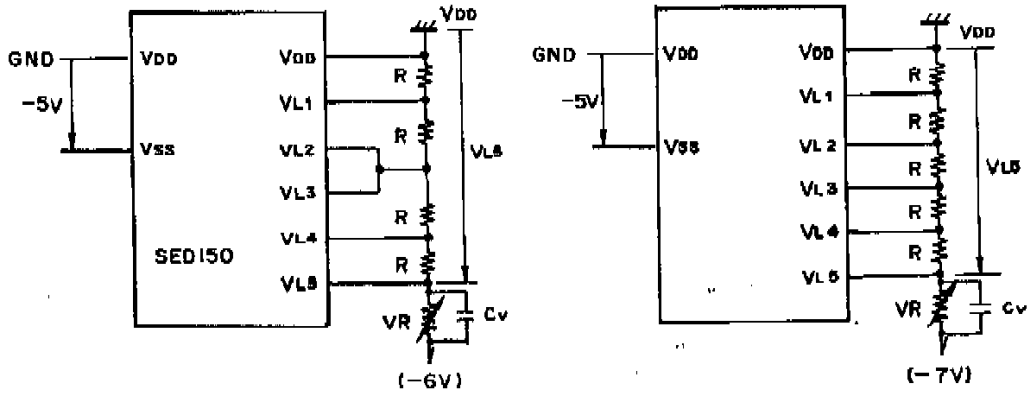
It is necessary for achieving a high level of liquid crystal display to apply various constant voltages of high accuracy in dividing ratio to each of the liquid crystal driving power terminals V_{L1} to V_{L5} as shown in the table below. The voltage dividing ratio must be changed according to the duty ratio.

Duty / Bias / Power	1/8 to (1/11)	(1/12) to 1/16
	1/4	1/5
V_{DD}	GND*1	GND
V_{L1}	1/4 V_{L5}	1/5 V_{L5}
V_{L2}	2/4 V_{L5}	2/5 V_{L5}
V_{L3}		3/5 V_{L5}
V_{L4}	3/4 V_{L5}	4/5 V_{L5}
V_{L5}	V_{L5}	V_{L5}

*1 GND here mens the GND of SED150, and not necessarily the GND of the whole system which includes micro-processing units. In caseof an N MOS micro-processing unit, for example, V_{SS} is connected to the system GND.

(b) Liquid crystal voltage supplying method

The method of supplying the voltages V_{L1} to V_{L5} is illustrated in Fig. 3.3-1 in the paragraph for external connections. The simplest way is to supply them by resistance division. The optimum liquid crystal driving voltage varies with ambient temperature so that it is necessary to add a temperature compensating circuit (variable resistor circuit V_R) to the liquid crystal driving power supply.



(a) 1/4 bias (1/8–1/11 duty) (b) 1/5 bias (1/12–1/16 duty)

Dividing resistance value is selected according to liquid crystal operation margin and power consumption.

(c) Liquid crystal drive waveform distortion compensation

Because the liquid crystal is a capacitive load, a large discharging/charging current flow when a liquid crystal drive waveform changes, causing its distortion. This adversely affects display quality in terms of lowered brightness and a halftone phenomenon. Waveform distortion can be reduced by lowering the dividing resistance value and power impedance, but this increases the current flowing to the dividing resistor and thus curent drain.

The SED150 Series has a power impedance lowering circuit such as shown in Fig. 3.5-6 to compensate for charging/discharging distortion. Thus, a little higher resistance than normal can be selected.

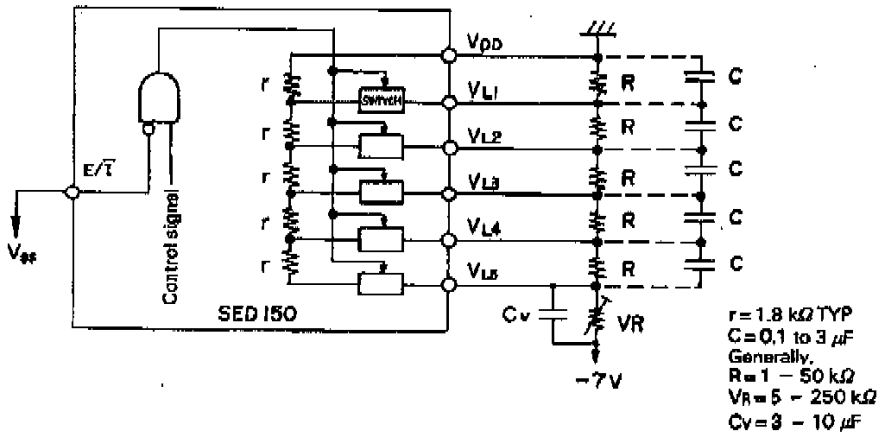


Fig. 3.5-6 Power Impedance Lowering Circuit

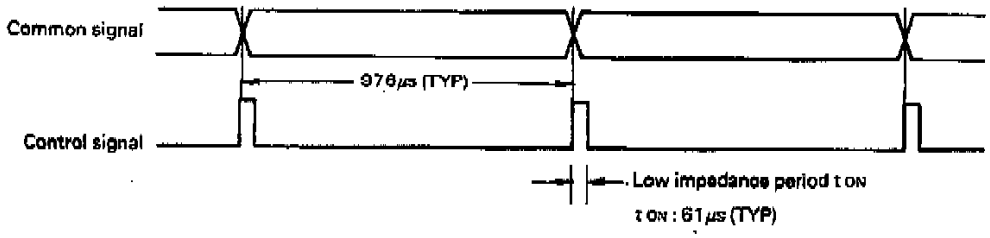


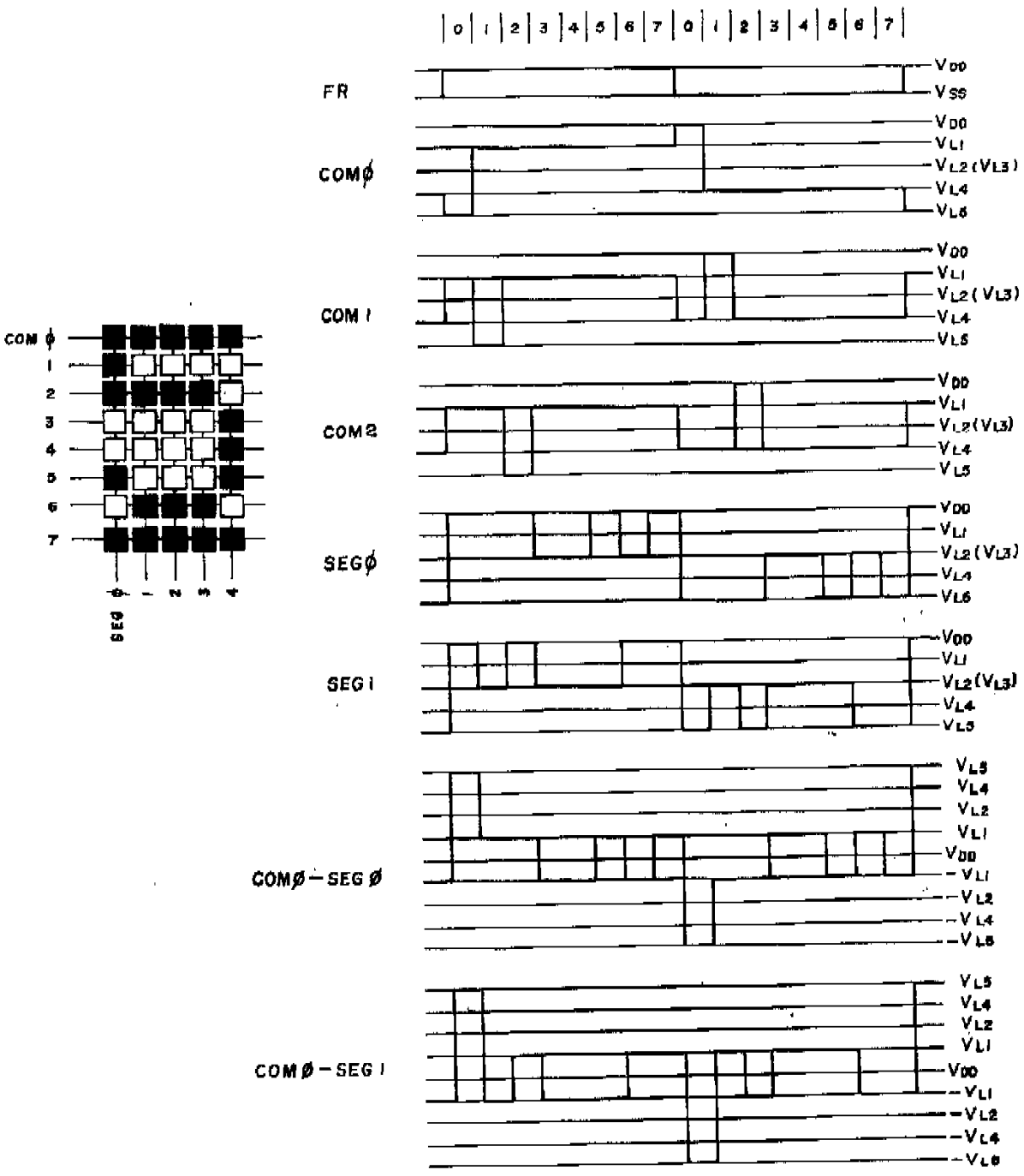
Fig. 3.5-7 Low Impedance Timing (where duty ratio is 1/16, oscillating frequency 32 kHz)

If waveform distortion still remains a problem despite the operation of the low impedance circuit, lower the R and connect a capacitor which is not so large but has a suitable capacitance parallel to the dividing resistor R to effectively solve the problem. Because a resistance cannot be simply selected from tyhe liquid crystal load capacity, it is necessary to experimentally determine one as appropriate to the liquid crystal display element used. In case of using a plurality of SED150, to liquid crystal load can be shared because any of the slave chips can output a common waveform synchronized with the master chip (oscillator circuit operating chip). (See Fig. 3.6-8.)

(5) Liquid crystal drive waveforms

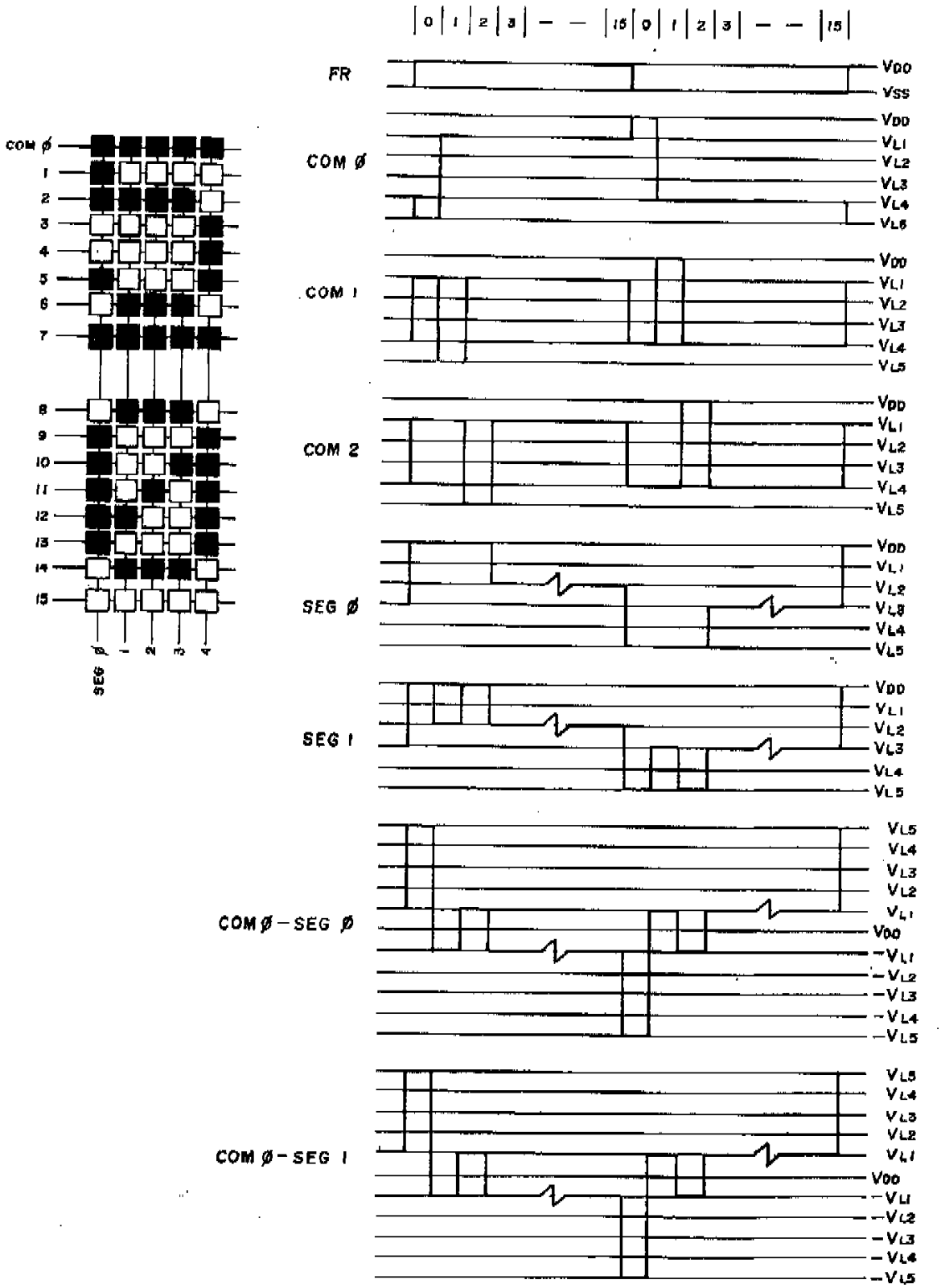
(a) 1/4 bias, 1/8 duty

Figure 3.5-8



(b) 1/5 bias, 1/16 duty

Figure 3.5-9



(6) Timing generator circuit

The timing generator circuit generates all timing pulses required for LCD driving,. That is, the circuit generates a DD RAM read signal and driving signals for common and segment drivers, and synchronizes where two or more chips are used. The operations of the timing generator circuit can be divided into master chip operation and slave chip operation depending on the status of the function and select terminal E/I as shown in Table 3.5-1.

Table 3.5-1

E/I	Operation	SYNC terminal	SED1503 *1
"L"	Operation by local clock (master chip)	Frame signal output (32 Hz)	COM_0 to COM_7 waveform outputs
"H"	Operation by external clock (Slave chip)	Frame signal input	COM_8 to COM_{15} waveform outputs

It takes up to 2 frames (40 ms maximum) for the slave chips to be synchronized with the master chip by a sync signal after swithing power on. The display is automatically blanked becuase display is meaningless during the non-synchronized period. This operation is performed regardless of the status of the command register.

*1 With the SED1500, SED1501, and SED1502, the slave chips output the same common waveform as the master chip.

3.6 INTERFACE WITH MPU

(1) General

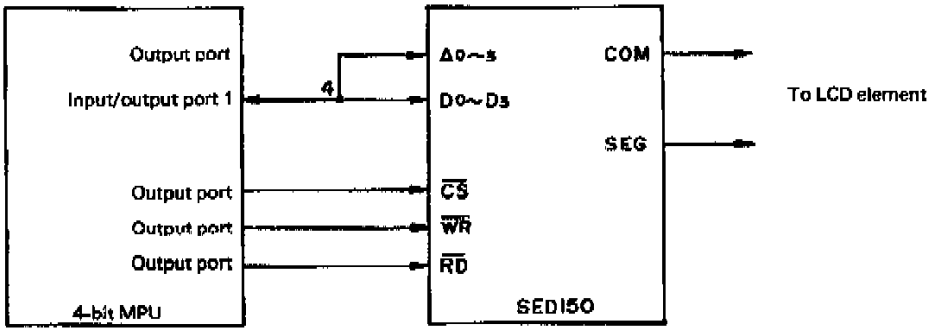
The SED150 Series permits slection of any of the four data tansfer modes shown in the table below by means of commands so that it can be interfaced with both 4- and 8-bit mirco-processing units.

No. of DB bits	No. of AB bits	Bus construction
4	4	DB/AB used in common
4	7	DB, AB independent
8	7	DB/AB used in common
8	7	DB, AB independent

By selecting an appropriate data transfer mode, the SED150 can be connected to the address and data buses of micro-processing units directly or via a peripheral interface (PIA). Examples of direct connection to various kinds of micro-processing units are shown below. In case of an 8-bit machine, micro-processing units may be connected via a normally used interface. It is recommended that the micro-processing units with I/O ports should be connected by this port.

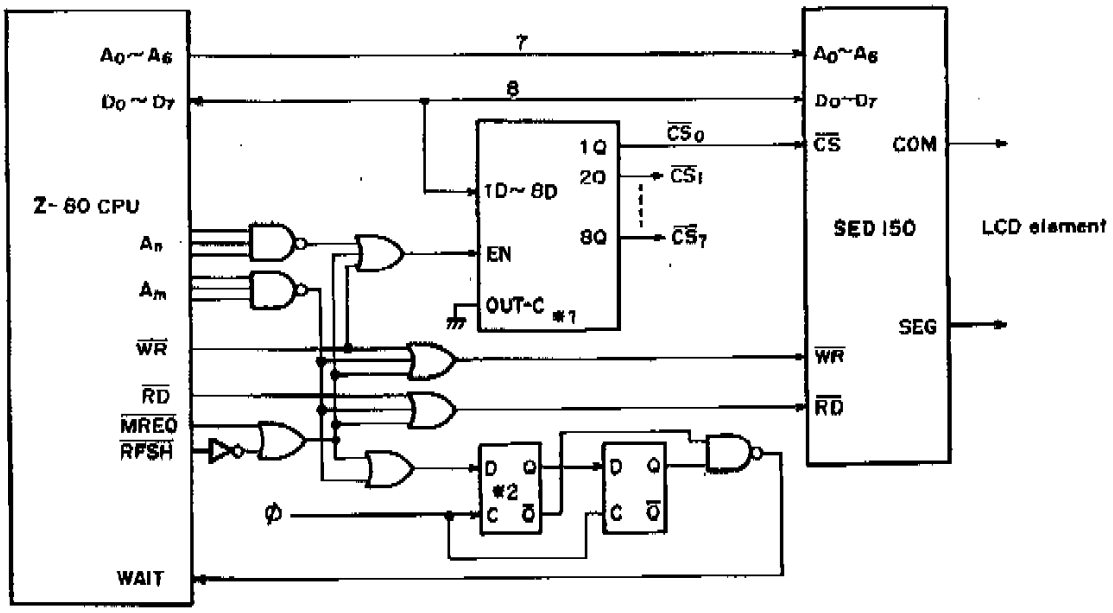
(2) Example of interfacing with a 4-bit MPU

* Various kinds of 4-bit micro-processing units are commercially available so no kinds in particular are specified.



(3) Example of intefacing with an 8-bit MPU

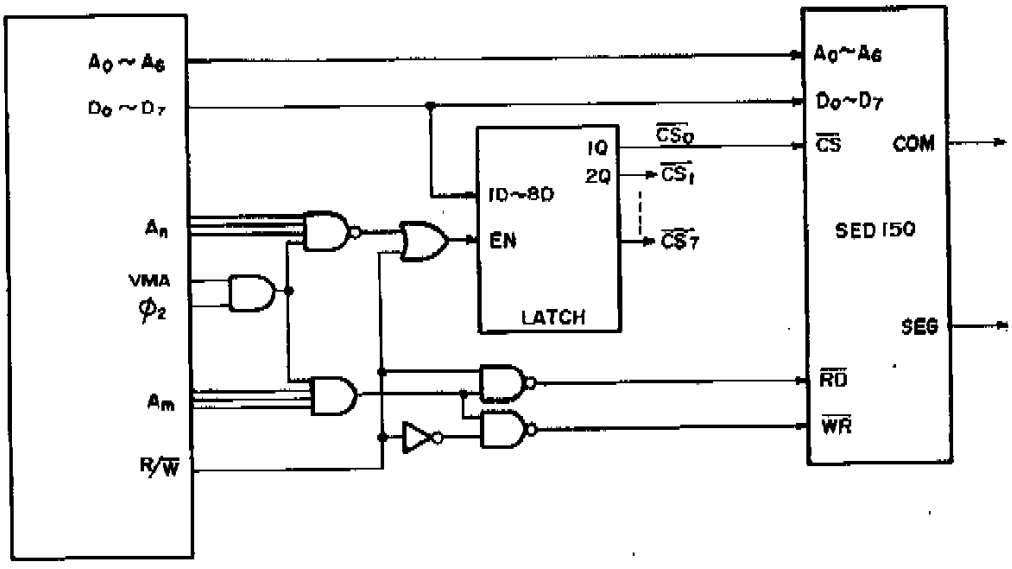
(a) Example: Z-80



* 1: LS374 or (8212, 8255); * 2: LS7474

Timing example: See Fig. 3.6-1 (d)

(b) Example: 6800



Timing example: See Fig. 3.6-1 (d)

(4) Command registers

The SED150 uses 3-bit commands (not code data) for starting internal operations. The commands are as follows.

(1) Bus transfer mode change command: (CR1, CR2)
4/8-bit transfer mode select: CR1
1-bus/2-bus select: CR2

These commands are written exactly in the same way as data is written in the DD RAM. This is, the commands are written in the following addresses of the SED150 via data buses D0 to D2 regardless of the upper or lower status of the 4-bit mode. The data stored in the command registers cannot be read out to the micro-processing units.

Addresses	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
FF$_H$								
BF	1	1	1	1	1	CR_2	CR_1	0
7F								
3F								

Command Register Composition

(a) Bus transfer mode change commands
The following four kinds of but transfer modes are available for the SED150. Transfer modes are designated by code data (CR2, CR1) to be written via data busesD1 and D2.

CR_2	CR_1	Address	Data	Bus construction
0	0	4 bits	4 bits	1 bus (multi)
1	0	7 bits	4 bits	2 buses
0	1	7 bits	8 bits	1 bus (multi)
1	1	7 bits	8 bits	2 buses

(5) Bus higher position/lower position identification

In the 4-bit mode, the SED150 identifies the higher position/lower position of addresses and data by counting the decoded outputs of CR1 and CR2 and control signals $\overline{CS}$, $\overline{RD}$, and $\overline{WE}$.
Addresses and data must be input in the following sequence as shown in Fig. 3.6-1.
Addresses (lower position → higher position) → data (lower position → higher position)

(6) Initializing SED150 by MPU

Because the status of the command registers in the SED150 is unknown after switching power on, it is necessary to initialize the micro-processing units into the desire data transfer mode. To properly initialize, thefollowing four cycles must be executed regardless of the transfer mode of the micro-processing units.

1. Change $\overline{CS}$ from "1" to "0".
2. Write command register address FF (or 3F, 7F, BF) three times consecutively. In case of the 2-bus system, command data are also simultaneously written in from data buses.
3. Write command data (1, 1, 1, 1, 1, CR2, CR1, 0) once.

——→ Command register setting completed

NOTE 1: In case of the 4-bit 1-bus system, the SED150 ignores the upper address bits (A4, A5, A6). But pull them up to address input terminals A4, A5, A6.
NOTE 2: For an initialization example, see Fig. 3.6-2.

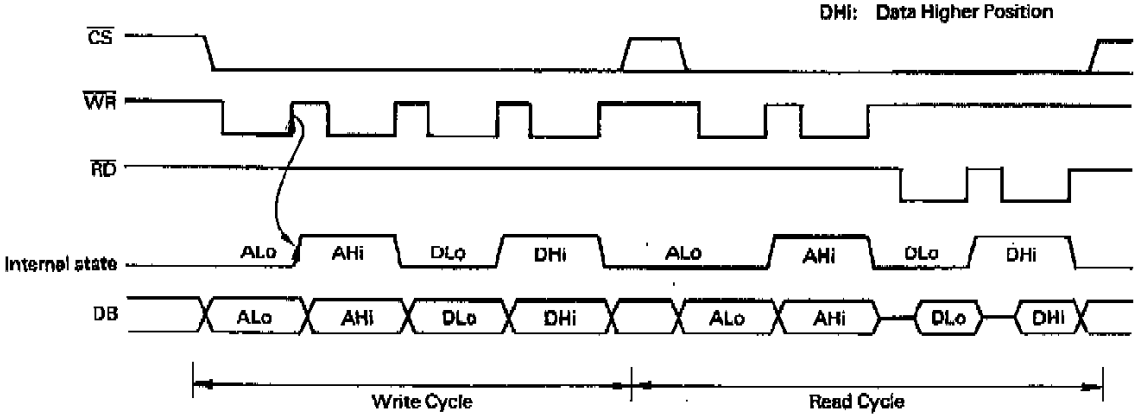
(7) Changing data transfer mode after initialization

The SED150 can be used in a changed data transfer mode even in the process of operation. For example, a change from the 8-bit 2-bus mode to the 4-bit 2-bus mode, or vice versa can be made. In this case, access to the DD RAM immediately after setting commands into the command registers must be made after changing $\overline{CS}$ to high. Unless this step is taken, the contents of the command registers might be destroyed.

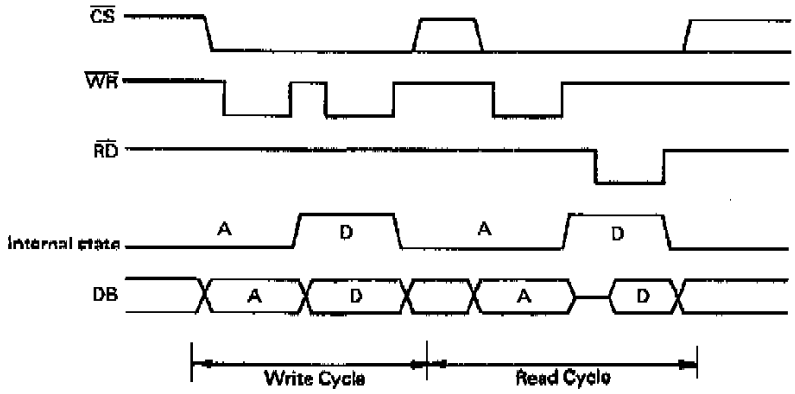
Fig. 3.6-1 Timing Sequence Examples

ALo: Address Lower Position
AHi: Address Higher Position
DLo: Data Lower Position
DHi: Data Higher Position

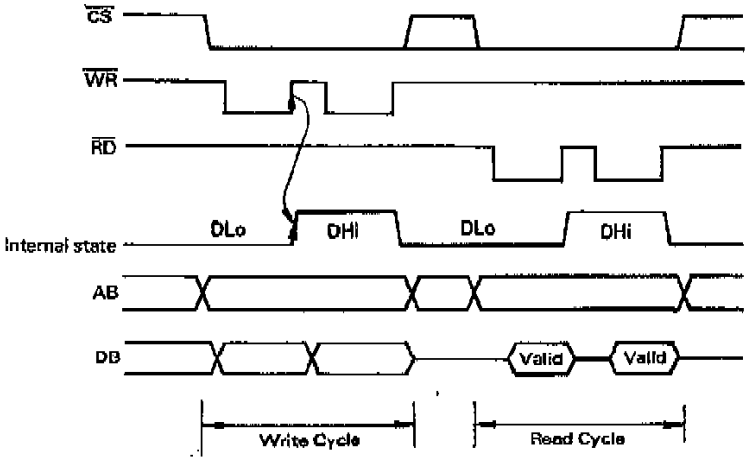
(a) Address 4-bit/data 4-bit 1-bus system



(b) Address 7-bit/data 8-bit 1-but system



(c) Address 7-bit, data 4-bit 2-bus system



(d) Address 7-bit, data 8-bit 2-bus system

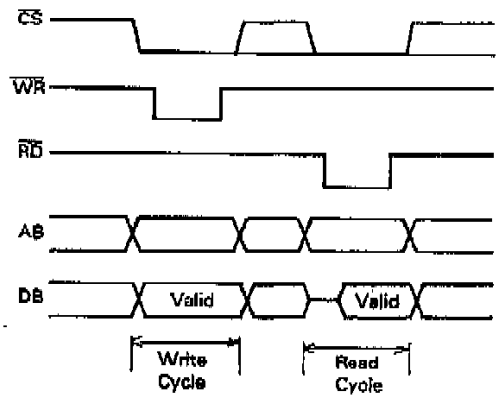
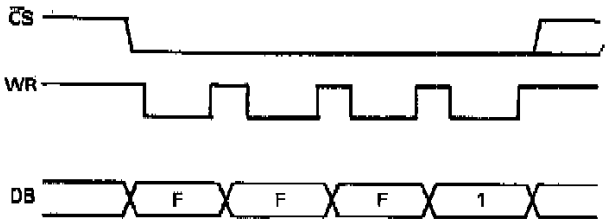


Fig. 3.6-2 Examples of Initialization

(a) 4-bit 1-bus system, Writing command data (1, ø, ø, 0) = 8H



(b) 8-bit 2-bus system, Writing command data (1, 1, 1, 0) = EH

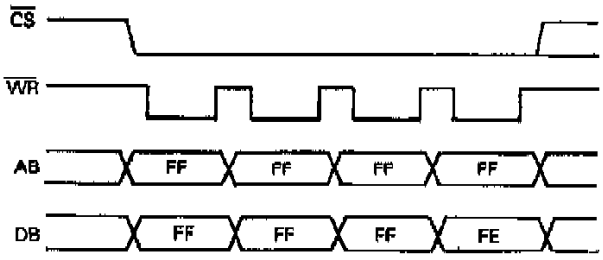
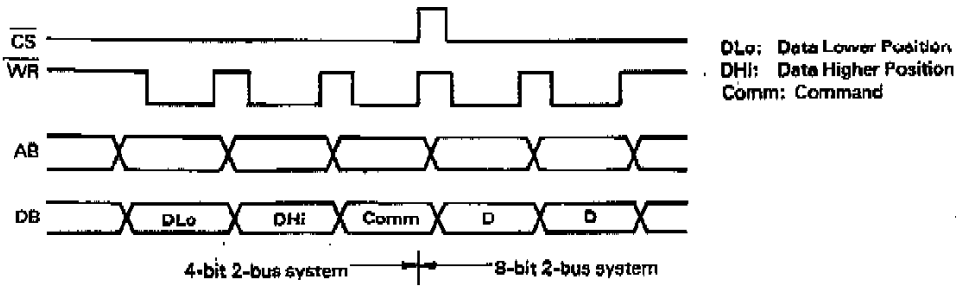


Fig. 3.6-3 Example of Data Transfer Mode Change



(7) DD RAM access vs. liquid crystal display

Access to the DD RAM can be made from the micro-processing unit completely regardless of LCD timing because address selection from the micro-processing unit and address selection from LCD are independent of each other in terms of circuitry.

In case of writing the DD RAM for a long time (more than about 1 mS), such as in writing the DD RAM all over, blank it once by means of a display command, and then write it. The blank signal directly controls the display drivers so that the display can be unconditionally blanked.

(6) Connecting SED150 to LCD panel

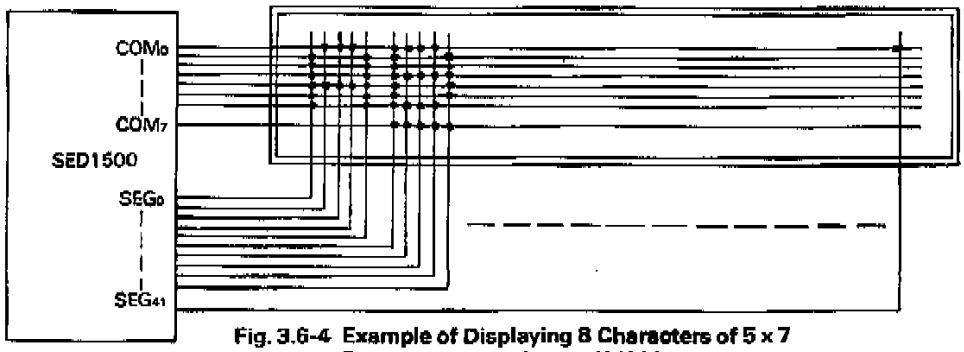
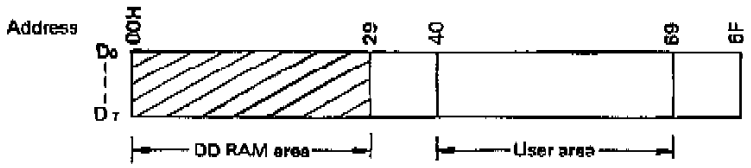


Fig. 3.6-4 Example of Displaying 8 Characters of 5 x 7 Dots x 1 Line + Indicator (1/4 bias, 1/8 duty)



NOTE: Address A7 = "0" is expressed in hexadecimals.
(The same expression is used hereunder.)

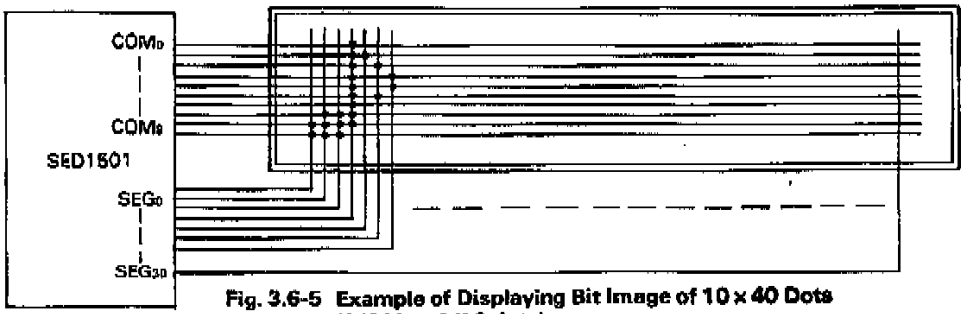
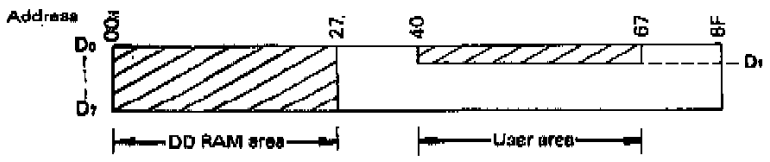


Fig. 3.6-5 Example of Displaying Bit Image of 10 x 40 Dots (1/4 bias, 1/10 duty)



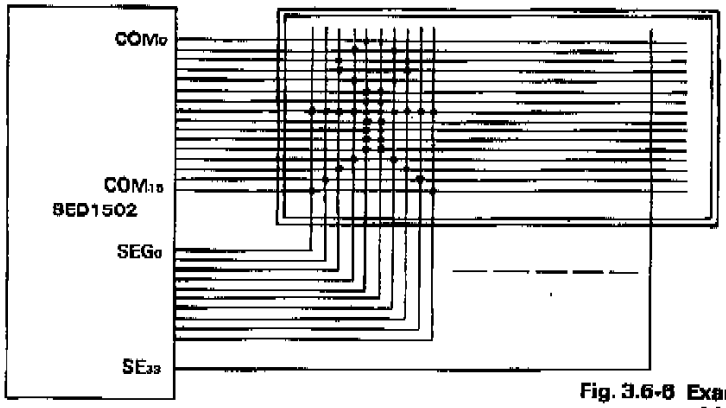
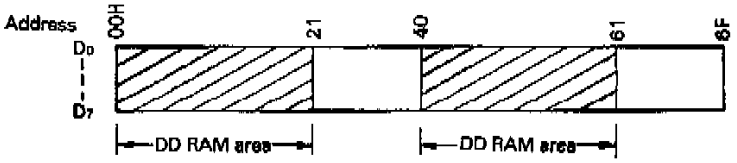


Fig. 3.6-6 Example of Displaying Bit Image of 16 x 34 Dots (1/5 bias, 1/16 duty)



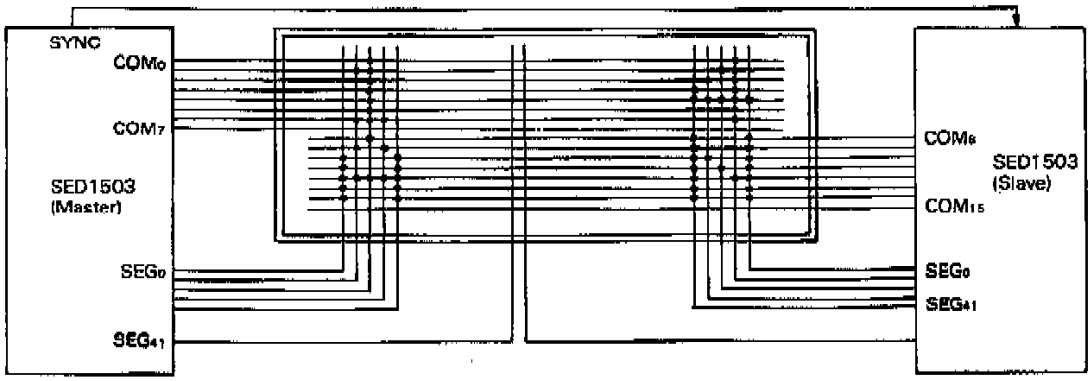
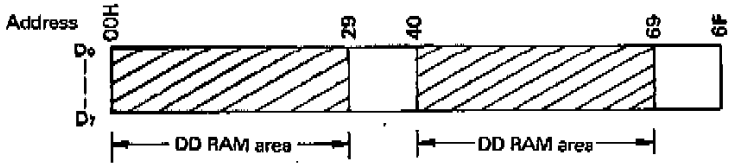
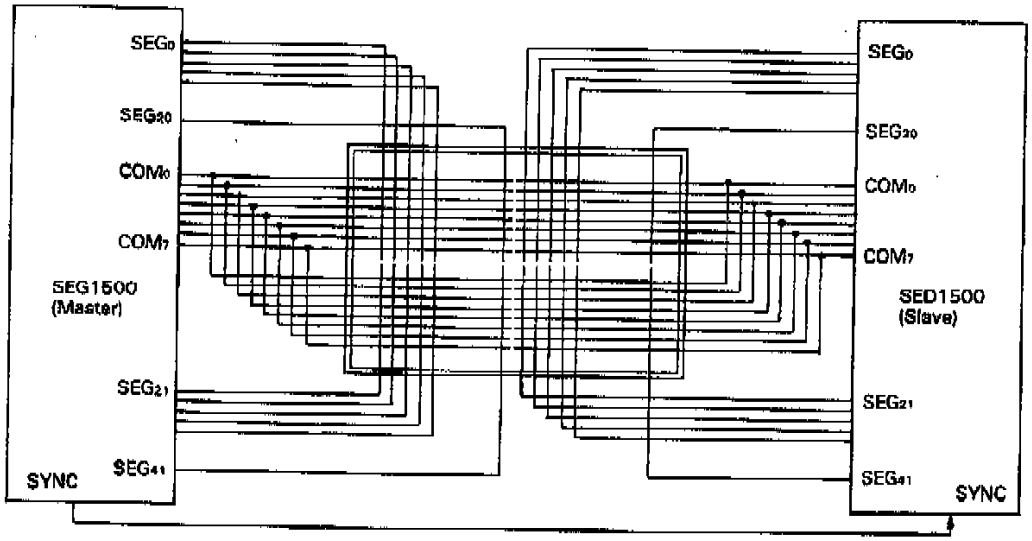


Fig. 3.6-7 Example of Displaying 14 Characters of 5 x 7 Dots x 2 Lines (1/5 bias, 1/16duty, running display possible)



Example of Display where Matrix Arrangement is Changed
(1/4 bias, 1/8 duty) Fig. 3.6-8



4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS (V_{DD} = 0V)

Item	Symbol	Requirements	Unit	Remarks
Source voltage (1)	V_{SS}	V_{DD} −7.0 ~ V_{DD} +0.3	V	
Source voltage (2)	V_{L1} ~ V_{L5}	V_{DD} −13.0 ~ V_{DD} +0.3	V	
Input voltage	V_I	V_{SS} −0.3 ~ V_{DD} +0.3	V	
Operating temperature range	Topr	−20 ~ 75	°C	
Storage temperature range	Tstg	−55 ~ 125	°C	

NOTE 1: Use of the LSI under conditions exceeding the absolute maximum ratings can cause not only faulty operation but permanent destruction. Even if the LSI properly operates for a time under such conditions, its reliability can seriously fall.

NOTE 2: The power supply relationship of $V_{DD} \geq V_{L1} \geq V_{L2} \geq V_{L3} \geq V_{L4} \geq V_{L5}$ must be maintained for driving the liquid crystal display. These voltages are independent of V_{SS}.

4.2 ELECTRICAL CHARACTERISTICS (V_{DD} = 0V, Ta = 25°C)

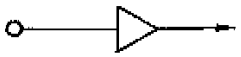
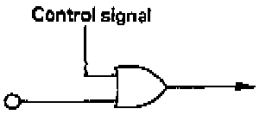
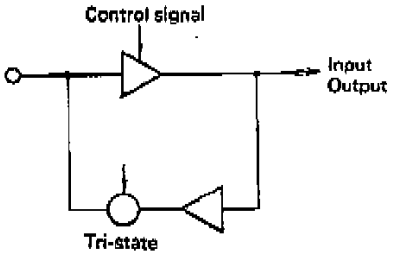
Item		Symbol	Measuring condition	Requirements			Unit	Measuring circuit	Applicable terminal
				Minimum	Typical	Maximum			
Operating voltage (1)		$\|V_{SS}\|$		$\|V_{DD}-3.0\|$	$\|V_{DD}-5.0\|$	$\|V_{DD}-6.0\|$	V		
Operating voltage (2)		$\|V_{L5}\|$		$\|V_{DD}-3.5\|$	$\|V_{DD}-6.0\|$	$\|V_{DD}-10.0\|$	V		
Memory hold voltage		$\|V_{DH}\|$		$\|V_{DD}-2.0\|$		$\|V_{DD}-6.0\|$	V		
TTL	High level input voltage	V_{IHT}		$V_{DD}-2.0$		$V_{DD}+0.3$	V	Fig. 6	$D_0 \sim D_7$, $A_0 \sim A_6$, $\overline{CE}$, RD, WR
TTL	Low level output voltage	V_{ILT}		$V_{SS}-0.3$		$V_{SS}+0.8$	V	Fig. 7	$D_0 \sim D_7$, $A_0 \sim A_6$, $\overline{CE}$, WR
TTL	High level output current (1)	I_{OHT}	$V_{SS}=-4.5V$, $V_{OH}=V_{SS}+2.4V$	-1.0			mA	Fig. 10	$D_0 \sim D_7$
TTL	Low level output current (1)	I_{OLT}	$V_{SS}=-4.5V$, $V_{OL}=V_{SS}+0.4$	2.0			mA	Fig. 11	$D_0 \sim D_7$
CMOS	High level input voltage (2)	V_{IHC}		$V_{DD}-0.6$		$V_{DD}+0.3$	V	Fig. 6	SYNC, OSC_1, E/I
CMOS	Low level input voltage (2)	V_{ILC}		$V_{SS}-0.3$		$V_{SS}+0.6$	V	Fig. 7	SYNC, OSC_1, E/I
CMOS	High level output current (2)	I_{OHC}	$V_{SS}=-4.5V$, $V_{OH}=V_{DD}-0.6V$	-300			μA	Fig. 10	SYNC, CL
CMOS	Low level output current (2)	I_{OLC}	$V_{SS}=-4.5V$, $V_{OL}=V_{SS}-0.6V$	300			μA	Fig. 11	SYNC, CL
CMOS	High level output current (3)	I_{OH3}	$V_{SS}=-4.5V$, $V_{OH}=V_{DD}-0.6V$	-80			μA	Fig. 10	OSC_2
CMOS	Low level output current (3)	I_{OL3}	$V_{SS}=-4.5V$, $V_{OL}=V_{SS}-0.6V$	80			μA	Fig. 11	OSC_2
Input output leak current		I_{IL}	$V_t=V_{DD} \sim V_{SS}$			1.0	μA	Fig. 14	All input terminals
Dynamic current drain (1)		I_{OP1}	$V_{SS}=-5.5V$, $\overline{CS}$ = "H", E/I = "L", $V_{L5}=-10.0V$, Rf = 1.0 MΩ, Output open		60	100	μA	Fig. 14	V_{DD}
Dynamic current drain (2)		I_{OP2}	$V_{SS}=-5.5V$, Cycle time = 1.0 μs, $V_{L5}=-10.0V$, Rf = 1.0 MΩ, Output open		2	5	mA	Fig. 14	V_{DD}
Static current drain		I_{DL}	$V_{SS}=5.5V$, $\overline{CS}$ = OSC_1 = "H", $V_{L5}=-10V$, E/I = "L", Output open			1.0	μA	Fig. 14	V_{DD}
Driver voltage drop	Common terminals: V_{DD} level	V_{C0L}	$V_{L5}=-3.5V$, $V_{SS}=-4.5V$, Terminal load R_L = 40 kΩ/driver			500	mV	Fig. 12	$COM_0 \sim 15$
Driver voltage drop	Common terminals: V_{L1} level	V_{C1H}				100	mV	Fig. 13	$COM_0 \sim 15$
Driver voltage drop	Common terminals: V_{L4} level	V_{C1L}				400	mV	Fig. 12	$COM_0 \sim 15$
Driver voltage drop	Common terminals: V_{L4} level	V_{C4H}				400	mV	Fig. 13	$COM_0 \sim 16$
Driver voltage drop	Common terminals: V_{L4} level	V_{C4L}				100	mV	Fig. 13	$COM_0 \sim 15$
Driver voltage drop	Common terminals: V_{L5} level	V_{C5H}				500	mV	Fig. 13	$COM_0 \sim 15$
Driver voltage drop	Segment terminals: V_{DD} level	V_{S0L}	$V_{L5}=-3.5V$, $V_{SS}=-4.5V$, Terminal load R_L = 40 kΩ/5 drivers			400	mV	Fig. 12	$SEG_0 \sim 41$
Driver voltage drop	Segment terminals: V_{L2} level	V_{S2H}				240	mV	Fig. 13	$SEG_0 \sim 41$
Driver voltage drop	Segment terminals: V_{L3} level	V_{S2L}				240	mV	Fig. 12	$SEG_0 \sim 41$
Driver voltage drop	Segment terminals: V_{L3} level	V_{S3H}				240	mV	Fig. 13	$SEG_0 \sim 41$
Driver voltage drop	Segment terminals: V_{L3} level	V_{S3L}				240	mV	Fig. 13	$SEG_0 \sim 41$
Driver voltage drop	Segment terminals: V_{L5} level	V_{S5H}				400	mV	Fig. 13	$SEG_0 \sim 41$

4.3 OSCILLATION CHARACTERISTICS (CR OSCILLATION) (V_{DD} = 0V, Ta = 25°C)

Item		Symbol	Measuring condition	Requirements			Unit	Measuring circuit	Applicable terminal
				Minimum	Typical	Maximum			
Oscillating frequency		fosc	V_{SS} = −5.0V, Rf = 1.0 MΩ	−16%	45	+16%	kHz		
Oscillation self-start voltage		V_{STA}	Rf = 1.0 MΩ			−2.0	V		
Oscillation stop		V_{STP}	Rf = 1.0 MΩ			−2.0	V		
Frequency deviation (Voltage characteristic)		E_V	$E_V = \frac{f_{osc}(-5.5V) - f_{osc}(-4.5)\,V}{f_{osc}(-5.0V)}$		4	10	%		
Frequency deviation (Temperature characteristic)		E_T	$E_T = \frac{f_{osc}(75°C) - f_{osc}(25°C)}{f_{osc}(75°C)}$		3	10	%		
Ext. Clock Opel.	Input clock frequency	fCL		fo × 0.84	fo	fo × 1.16	kHz		
	Input clock duty	Du		45	50	55	%		
	Clock rise time	trCL				0.3	μs		
	Clock fall time	tfCL				0.3	μs		

* fOSC and fCL are approximately 32.8 kHz regardless of the LCD drive duty ratio. For details, see Item (2) of the SED 1500 Series Metal Option Guide, P2-2.2.
* Crystal oscillation characteristics will be determined by discussion with individual users.

Terminal Construction

Terminal construction	Remarks	Applicable terminal
Fig. 1 Input terminal 		$\overline{CS}$, $E/\overline{A}$, OSC_1
Fig. 2 Input terminal 		$A_0 \sim A_7$, $\overline{WR}$, $\overline{RD}$
Fig. 3 Output terminal 		CL, OSC_2
Fig. 4 Input output terminal 		$D_0 \sim D_7$, SYNC

Measuring Circuit

Fig. 6 Input voltage

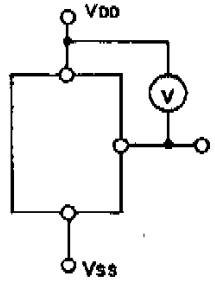


Fig. 7 Input voltage

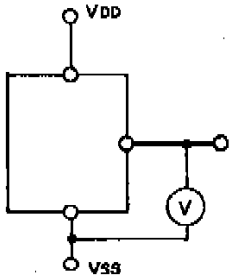


Fig. 8 "L" level input current

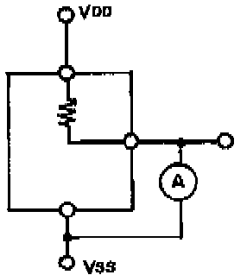


Fig. 9 "H" level input current

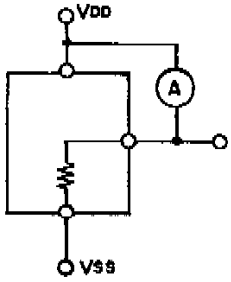


Fig. 10 Input current

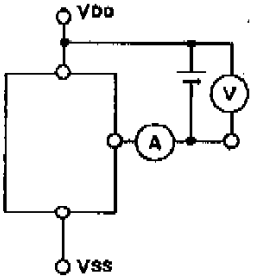


Fig. 11 Output current

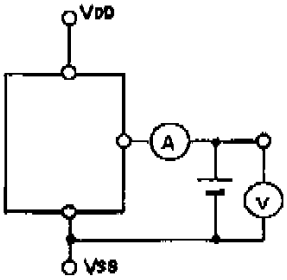


Fig. 12 H-side CL output voltage

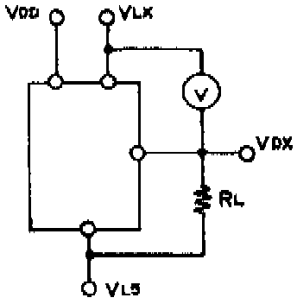


Fig. 13 L-side LC output voltage

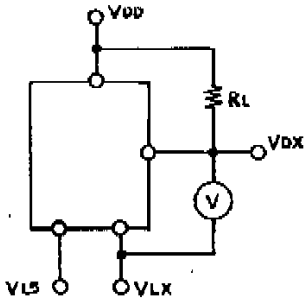
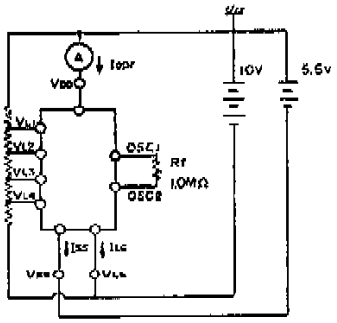


Fig. 14 Current drain



4.4 TIMING CHARACTERISTICS

(a) Read operation

Symbol	Item	Condition	MIN	TYP	MAX	Unit
tRC	Read cycle time		1000			ns
tA1	Access time 1	$V_{IH} = V_{OH} = V_{DD} - 2.0V$			800	ns
tRD	Read input → valid data output time	$V_{IL} = V_{DL} = V_{SS} + 0.8V$			800	ns
tRX	Read input → data output time	C_L = 100 pF + 1 TTL			150	ns
tOTD	Output disable time		30			ns
tOHA	Output hold time	$V_{SS} = -5V \pm 10\%$	20			ns
tAS	Address set pulse width	$T\alpha = -20 \sim +75°C$	200			ns
tAH	Address hold time		100			ns
tPS	Port setup time		200			ns

(b) Write operation

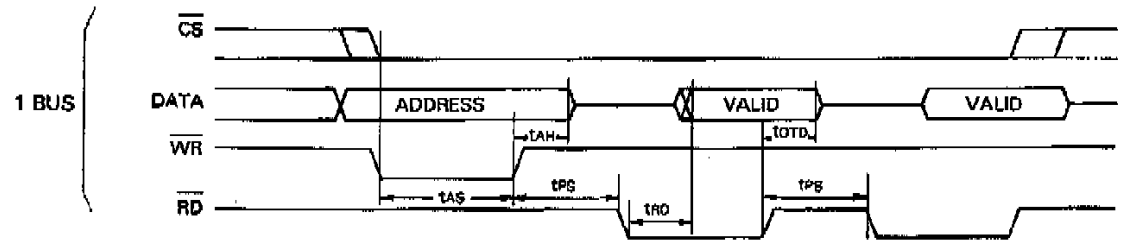
Symbol	Item	Condition	MIN	TYP	MAX	Unit
tWC	Write recovery time		1000			ns
tW	Write time		800			ns
tPS	Port setup time		200			ns
tAW	Address setup time	$V_{IN} = V_{OH} = V_{DD} - 2.0V$	0			ns
tWR	Write recovery time	$V_{IL} = V_{OL} = V_{SS} + 0.8V$	200			ns
tODW	Output disable time	C_L = 100 pF + 1 TTL			0	ns
tDS	Data setup time	$V_{SS} = -5V \pm 10\%$	300			ns
tDH	Data hold time	$T\alpha = -20 \sim +75°C$	100			ns
tAS	Address set pulse width		200			ns
tAH	Address hold time		100			ns

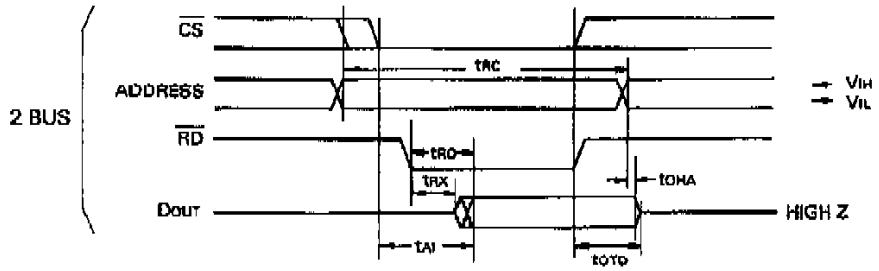
(c) Truth table

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	$A_0 \sim A_3$	$A_4 \sim A_6$	DIN		DOUT		Mode
					$D_0 \sim A_3$	$D_4 \sim D_7$	$D_0 \sim D_3$	$D_4 \sim D_7$	
H	*	*	*	*	*	*	High impedance	High impedance	Standby
L	L	H	Stable	Stable**	High impedance	High impedance	Data output	Data output**	Read cycle
L	H	L	Stable	Stable**	Stable	Stable**	High impedance	High impedance	Write cycle

* "H" or "L" ** High impedance in 4-bit mode

Read Operation





Write Operation