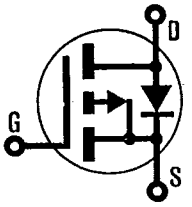
Data Sheet No. PD-9.397B

INTERNATIONAL RECTIFIER IOR

T-43-25

HEXFET® TRANSISTORS IRFG9110

4 P-CHANNEL POWER MOSFETs



IRFG9113

14 LEAD DUAL-IN-LINE QUAD
(CERAMIC SIDE BRAZED PACKAGE)

-100 Volt, 1.3 Ohm, 1.6 Ohm 1.4-Watt HEXFET

The HEXFET® technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry and unique processing of the HEXFET design achieve very low on-state resistance combined with high transconductance and extreme device ruggedness.

The P-Channel HEXFETs are designed for application which require the convenience of reverse polarity operation. They retain all of the features of the more common N-Channel HEXFETs such as voltage control, very fast switching, ease of paralleling, and excellent temperature stability. The P-Channel IRFG9110 device is an approximate electrical complement to the N-Channel IRFG1Z0 HEXFET.

P-Channel HEXFETs are intended for use in power stages where complementary symmetry with N-Channel devices offers circuit simplification; for this the IRFG1Z0 or IRFG110 is the perfect answer. They are also very useful in drive stages because of the circuit versatility offered by the reverse polarity connection. Applications include motor control, audio amplifiers, switched mode converters, control circuits and pulse amplifiers. These packages are well suited for both military and commercial applications.

Features:

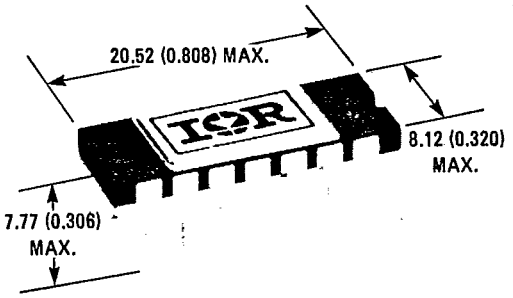
- Hermetically Sealed
- High Reliability
- For Automatic Insertion
- Compact
- Fast Switching
- Low Drive Current
- Easily Paralleled
- Low On-Resistance
- High Input Impedance

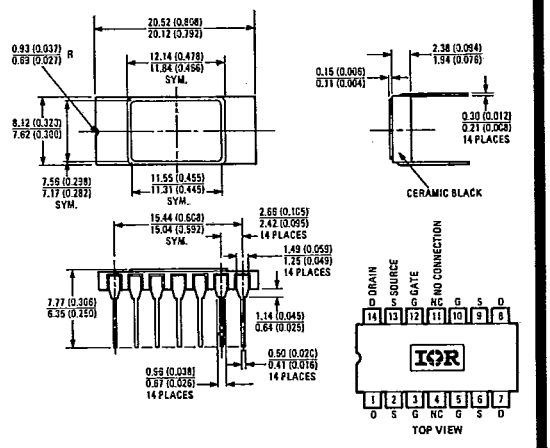
Product Summary

Part Number	V_{DS}	$R_{DS(on)}$	I_D
IRFG9110	-100V	1.4Ω	-0.75A
IRFG9113	-60V	1.8Ω	-0.65A

14-PIN

CASE STYLE AND DIMENSIONS





Conforms to JEDEC Outline MO-036AC
Dimensions in Millimeters and (Inches)

IRFG9110, IRFG9113 Devices

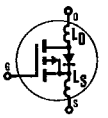
Absolute Maximum Ratings For Each Chip

Parameter		IRFG9110	IRFG9113	Units
V_{DS}	Drain - Source Voltage ①	-100	-60	V
V_{DGR}	Drain - Gate Voltage (R_{GS} = 20 KΩ) ①	-100	-60	V
I_D @ T_A = 25°C	Continuous Drain Current	-0.75	-0.65	A
I_{DM}	Pulsed Drain Current	-3.0	-2.6	A
V_{GS}	Gate - Source Voltage	±20		V
I_{LM}	Inductive Current, Clamped	(See Fig. 14 and 15) L = 100μH -3.0	-2.6	A
T_J T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)		°C

Electrical Characteristics For Each Chip @T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain - Source Breakdown Voltage	IRFG9110	-100	–	–	V	V_{GS} = 0V
		IRFG9113	-60	–	–	V	I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	-2.0	–	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate - Source Leakage Forward	ALL	–	–	-100	nA	V_{GS} = -20V
I_{GSS}	Gate - Source Leakage Reverse	ALL	–	–	100	nA	V_{GS} = 20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	–	-250	μA	V_{DS} = Max. Rating, V_{GS} = 0V
			–	–	-1000	μA	V_{DS} = Max. Rating x 0.8, V_{GS} = 0V, T_C = 125°C
$V_{DS(on)}$	On-State Voltage ②	IRFG9110	–	–	-1.0	V	V_{GS} = -10V, I_D = -0.75
		IRFG9113	–	–	-1.17	V	V_{GS} = -10V, I_D = -0.65A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ②	IRFG9110	–	1.2	1.4	Ω	V_{GS} = -10V, I_D = -0.3A
		IRFG9113	–	1.5	1.8	Ω	
g_{fs}	Forward Transconductance ②	ALL	0.6	0.8	–	S (℧)	V_{DS} > $I_{D(on)}$ x $R_{DS(on)}$ max., I_D = -0.3A
C_{iss}	Input Capacitance	ALL	–	180	250	pF	V_{GS} = 0V, V_{DS} = -25V, f = 1.0 MHz See Fig. 9
C_{oss}	Output Capacitance	ALL	–	85	100	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	–	30	35	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	15	30	ns	V_{DD} = 0.5 BV_{DSS}, I_D = -0.3A, Z_o = 50Ω See Fig. 16 (MOSFET switching times are essentially independent of operating temperature.)
t_r	Rise Time	ALL	–	30	60	ns	
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	20	40	ns	
t_f	Fall Time	ALL	–	20	40	ns	
Q_g	Total Gate Charge (Gate-Source Plus Gate-Drain)	ALL	–	11	–	nC	V_{GS} = -15V, I_D = -2.6A, V_{DS} = 0.8 Max. Rating. See Fig. 17 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs}	Gate-Source Charge	ALL	–	5.7	–	nC	
Q_{gd}	Gate-Drain ("Miller") Charge	ALL	–	5.3	–	nC	
L_D	Internal Drain Inductance	ALL	–	4.0	–	nH	Measure from the drain lead, 2.0mm (0.08 in.) from package to center of die.
L_S	Internal Source Inductance	ALL	–	6.0	–	nH	Measured from the source lead, 2.0mm (0.08 in.) from package to source bonding pad.

Modified MOSFET symbol showing the internal device inductances.



Source-Drain Diode Ratings and Characteristics For Each Chip

I_S	Continuous Source Current (Body Diode)	IRFG9110	–	–	-0.75	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		IRFG9113	–	–	-0.65	A	
I_{SM}	Pulse Source Current (Body Diode)	IRFG9110	–	–	-3.0	A	
		IRFG9113	–	–	-2.6	A	
V_{SD}	Diode Forward Voltage ②	IRFG9110	–	–	-5.5	V	T_A = 25°C, I_S = -0.75A, V_{GS} = 0V
		IRFG9113	–	–	-5.3	V	T_A = 25°C, I_S = -0.65A, V_{GS} = 0V
t_{rr}	Reverse Recovery Time	ALL	–	120	–	ns	T_J = 150°C, I_F = -0.75A, dI_F/dt = 100A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	6.0	–	μC	T_J = 150°C, I_F = -0.75A, dI_F/dt = 100A/μs
t_{on}	Forward Turn-on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

①T_J = 25°C to 150°C. ②Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.

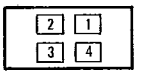
Power Ratings

Test		Single FET	All Four FETs With Equal Power	Units
P_D @ T_A = 25°C	Max. Power Dissipation	1.4	2.5	W
	Linear Derating Factor	11.0	20	mW/°C
R_{th}	Thermal Resistance Junction-to-Ambient	90	50	°C/W
K_{14},K_{23}	Thermal Coupling Factors	0.45	—	%
K_{12},K_{34},K_{13},K_{24}	Thermal Coupling Factors	0.40	—	%

The temperature rise of each device within the package is the result of the power dissipated by the device itself and the power dissipated by the other devices. The power dissipated by the adjacent devices does not have the same effect as the power dissipated within the junction itself. The temperature rise for any particular unit (e.g. (1)) within the package can be calculated with the following expression:

(1) $\Delta T_1 = 90 (P_1 + K_{12} P_2 + K_{13} P_3 + K_{14} P_4)$

where the K_{ij} are the thermal coupling coefficients shown in the Power Ratings Table.



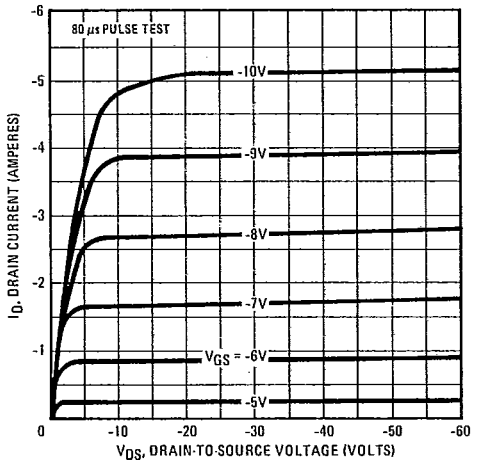


Fig. 1 — Typical Output Characteristics

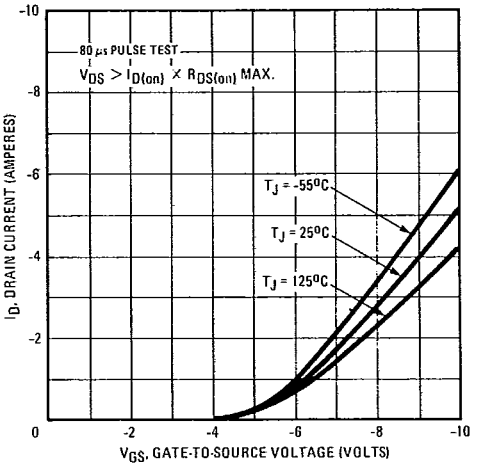


Fig. 2 — Typical Transfer Characteristics

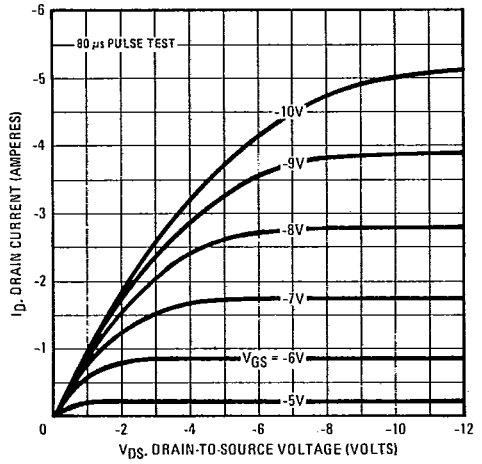


Fig. 3 — Typical Saturation Characteristics

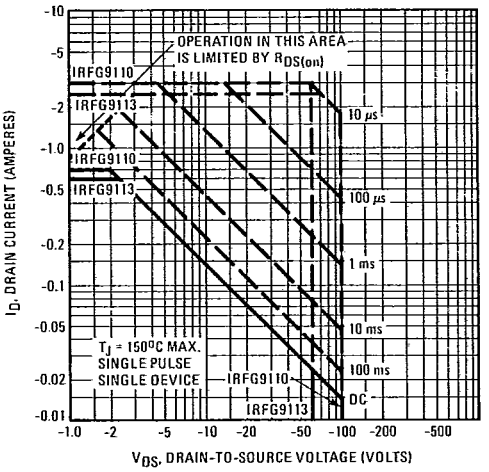


Fig. 4 — Maximum Safe Operating Area

14-PIN

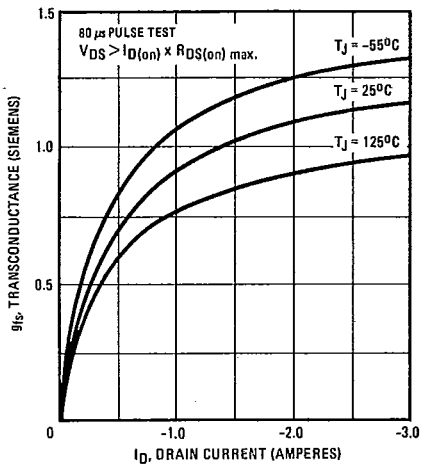


Fig. 5 — Typical Transconductance Vs. Drain Current

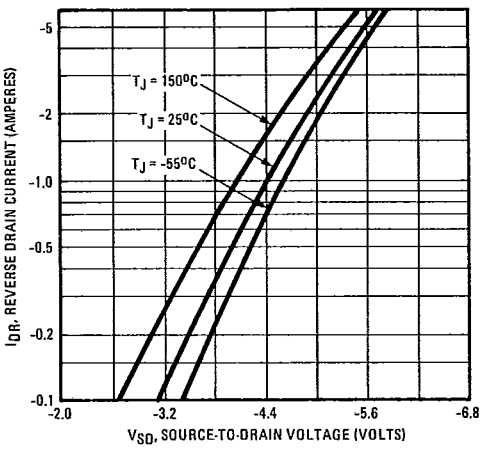


Fig. 6 — Typical Source-Drain Diode Forward Voltage

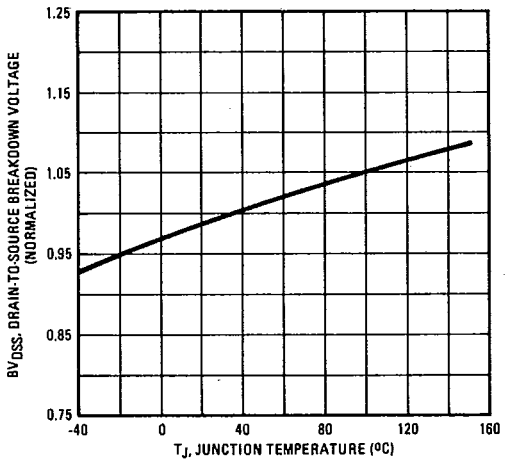


Fig. 7 — Breakdown Voltage Vs. Temperature

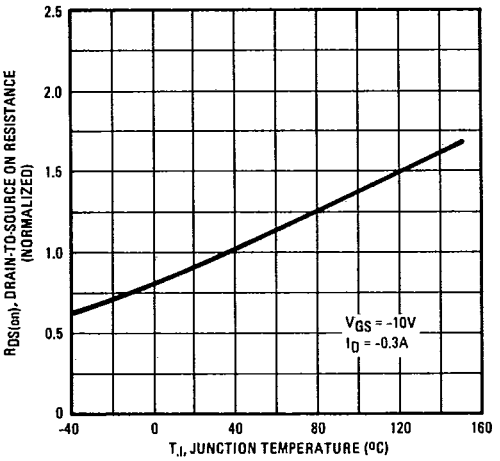


Fig. 8 — Normalized On-Resistance Vs. Temperature

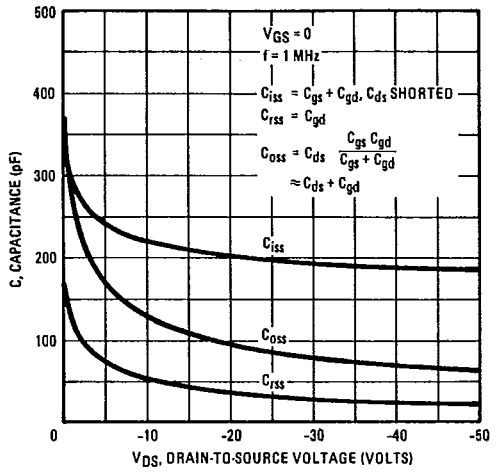


Fig. 9 — Typical Capacitance Vs. Drain-to-Source Voltage

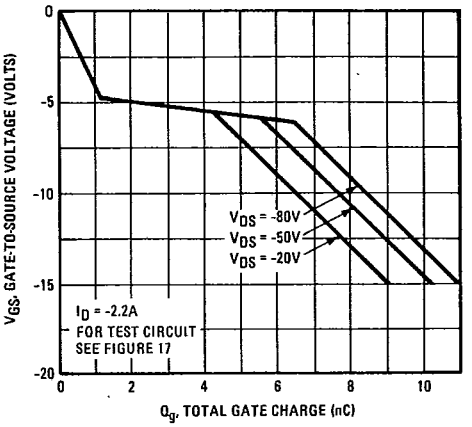


Fig. 10 — Typical Gate Charge Vs. Gate-to-Source Voltage

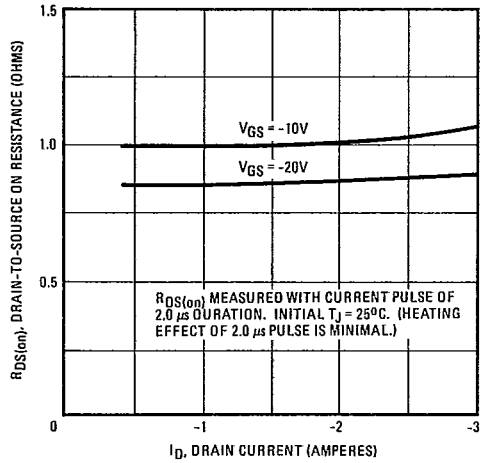


Fig. 11 — Typical On-Resistance Vs. Drain Current

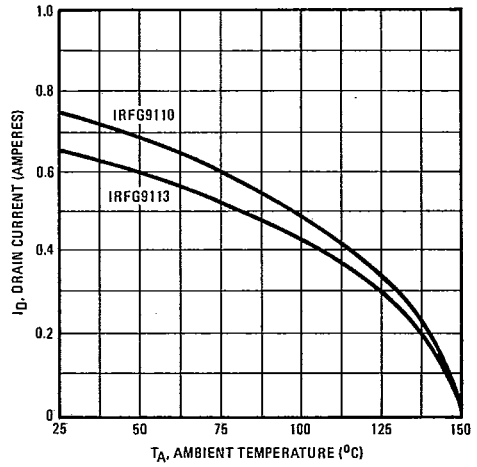


Fig. 12 — Maximum Drain Current Vs. Case Temperature

14-PIN

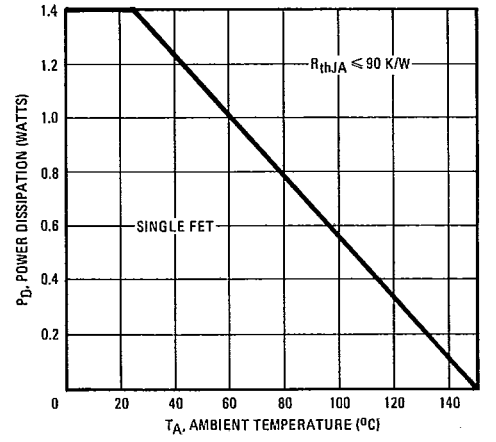


Fig. 13 — Power Vs. Temperature Derating Curve

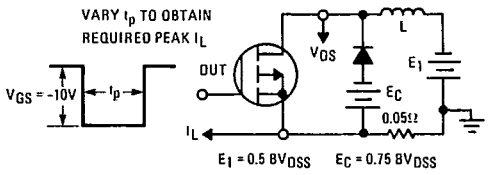


Fig. 14 — Clamped Inductive Test Circuit

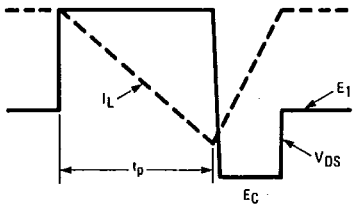
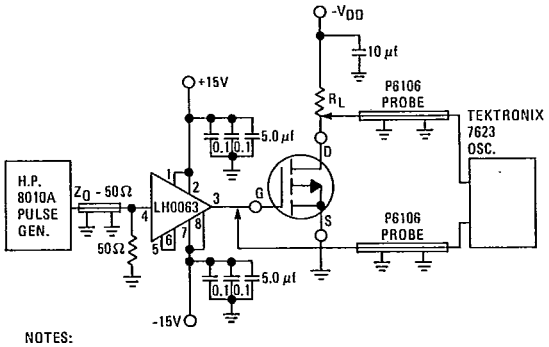
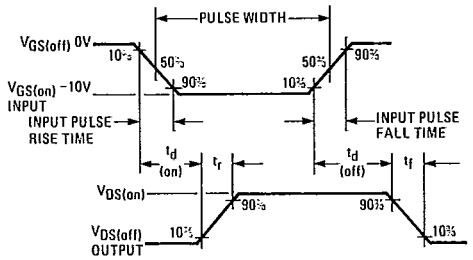


Fig. 15 — Clamped Inductive Waveforms



NOTES:
1. LH0063 CASE GROUNDED.
2. GROUNDED CONNECTIONS COMMON TO GROUND PLANE ON BOARD.
3. PULSE WIDTH=3 μs, PERIOD=1 ms, AMPLITUDE=10V.



NOTES:
WHEN MEASURING RISE TIME, $V_{GS(on)}$ SHALL BE AS SPECIFIED ON THE INPUT WAVEFORM. WHEN MEASURING FALL TIME, $V_{GS(off)}$ SHALL BE SPECIFIED ON THE INPUT WAVEFORM. THE INPUT TRANSITION AND DRAIN VOLTAGE RESPONSE DETECTOR SHALL HAVE RISE AND FALL RESPONSE TIMES SUCH THAT DOUBLING THESE RESPONSES WILL NOT AFFECT THE RESULTS GREATER THAN THE PRECISION OF MEASUREMENT. THE CURRENT SHALL BE SUFFICIENTLY SMALL SO THAT DOUBLING IT DOES NOT AFFECT TESTS RESULTS GREATER THAN THE PRECISION OF MEASUREMENT.

Fig. 16 — Switching Time Test Circuit and Waveform

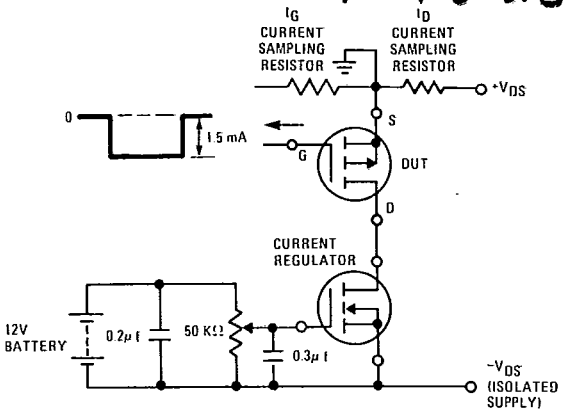


Fig. 17 — Gate Charge Test Circuit