Integrated Device Technology, Inc.

BiCameral™ CacheRAM™ 288K (16K x 9 x 2) FOR RISC CACHES

PRELIMINARY
IDT71B229S

FEATURES:

- Supports the R3000, R3500 and R3001 to 40MHz
- BiCameral organization:
  —Split instruction/data cache support
  —No bank-switching timing contention
- Single address bus
- Single data bus
- Separate write enable and output enable for each bank
- Standard read and write control interface
- Internal address latches
- 32-pin 300 mil SOJ package

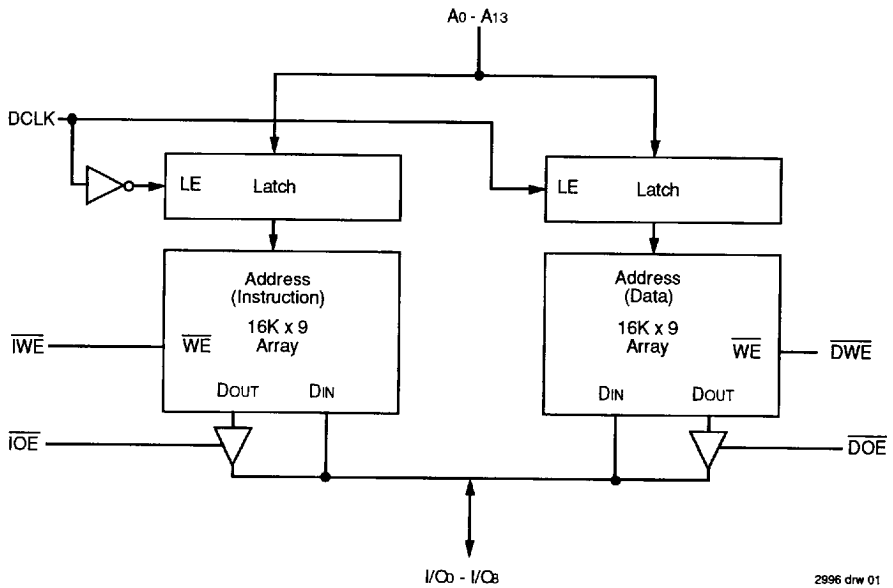
DESCRIPTION:

The IDT71B229 is a BiCameral CacheRAM specifically designed to support the split instruction and data caches of the IDT 79R3000 microprocessor. A complete 128KByte cache for the R3000 or the R3500 can be built with only six to seven IDT71B229s (depending on the main memory size supported by the system), while an R3001 cache can be built with five to six parts. CPU clock frequencies up to 40MHz are supported. The small 300 mil package allows a 128KByte cache to fit in a circuit board area of approximately two square inches.

Internal address latches eliminate the need for external latches. The BiCameral (two bank) organization reduces the number of devices required to support the R3000's split-cache architecture and eliminates contention problems encountered when one RAM bank is being enabled while the other is being disabled. All timing parameters have been optimized to support the complete range of R3000 clock speeds, simplifying R3000 cache design.

Made with BiCMOS, IDT's advanced high-speed process, the IDT71B229 provides dense caches in low board space while consuming minimum power.

FUNCTIONAL BLOCK DIAGRAM



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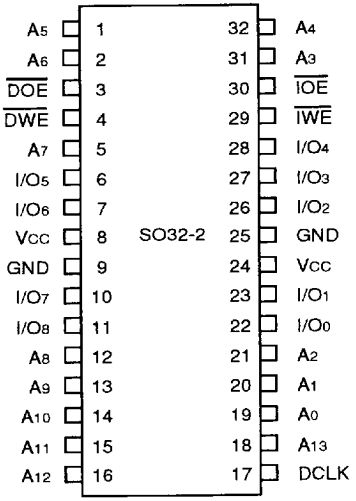
PIN CONFIGURATIONS



SOJ
TOP VIEW

2996 drw 02

TRUTH TABLE 1

$\overline{IOE}$	$\overline{IWE}$	$\overline{DOE}$	$\overline{DWE}$	I/O(0:8)	Function
H	H	L	H	DATA OUT	Read D Bank data
H	H	H	L	DATA IN, HIGH-Z	Write data to D Bank
L	H	H	H	DATA OUT	Read I Bank data
H	L	H	H	DATA IN, HIGH-Z	Write data to I Bank
H	H	H	H	High-Z	No Activity
L	L	X	X	High-Z	Not Allowed
L	X	L	X	High-Z	Not Allowed
L	X	X	L	High-Z	Not Allowed
X	L	L	X	High-Z	Not Allowed
X	L	X	L	High-Z	Not Allowed
X	X	L	L	High-Z	Not Allowed

2996 tbl 01

TRUTH TABLE 2(1)

DCLK	I Address Latch	D Address Latch
L	Transparent	Latched
H	Latched	Transparent

2996 tbl 02

NOTE:
1. L = Low, H = High, X = Don't Care and High-Z = High Impedance

PIN DESCRIPTION

Name	Description
DCLK	DCLK, when high, allows the address inputs to flow through the D bank's address latch. Conversely, the address in the I bank's latch is held during a high input on DCLK. Taking DCLK low freezes data in the D bank's address latch and allows addresses to flow through the I bank's address latch.
$\overline{IOE}$	I Output Enable enables the data outputs from the I bank onto the data input/output pins. $\overline{IOE}$ must not be asserted simultaneously with the $\overline{DOE}$, $\overline{DWE}$ or $\overline{IWE}$ pins.
$\overline{DOE}$	This is an input which enables the data outputs from the D bank onto the data input/output pins. $\overline{DOE}$ must not be asserted simultaneously with the $\overline{IOE}$, $\overline{IWE}$ or $\overline{DWE}$ pins.
$\overline{IWE}$	I Write Enable, when low, gates data from the input/output pins into the RAM at the I bank address indicated by the output of the I bank address latch. Neither $\overline{DOE}$ nor $\overline{IOE}$ should be enabled during a write operation.
$\overline{DWE}$	D Write Enable is an input which is taken low to gate data from the input/output pins onto the RAM at the address being output from the D bank address latch. Neither $\overline{DOE}$ or $\overline{IOE}$ should be asserted during a write operation.
Addr(0:13)	The fourteen address inputs are used to access any of the 16,384 locations in either the D or I bank. When an address latch is in the transparent state, these pins are routed directly to that latch's RAM bank. Taking the latch into its latched state causes that RAM bank to ignore subsequent changes on the address input pins.
I/O0:8	The input/output bus comprises nine signals whose functions are determined by the state of the $\overline{IOE}$, $\overline{IWE}$, $\overline{DOE}$ and $\overline{DWE}$ pins. During Output Enables, data is output upon these pins from the selected RAM bank from an address pointed to by the outputs of that bank's address latch. When either Write Enable is asserted, data can be written from these pins into the selected bank's RAM at the address being output by that bank's address latch. When $\overline{IOE}$, $\overline{IWE}$, $\overline{DOE}$ and $\overline{DWE}$ are all inactive, the input/output pins are floated in a high-impedance state.

2996 tbl 03

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1,2]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	7	pF

NOTES: 2996 tbl 04
1. This parameter is determined by device characterization, but is not production tested.
2. Capacitance is measured between 0V and 3V during switching.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	V_{CC}+0.5	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE: 2996 tbl 05
1. V_{IL} (min.) = –1.5V for pulse width less than 10ns, once per cycle.

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Commercial	Unit
V_{TERM}[2]	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	50	mA

NOTES: 2996 tbl 06
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{IN} must not exceed V_{CC}+0.5V.

DC ELECTRICAL CHARACTERISTICS[1, 2] (V_{CC} = 5.0V ± 5%)

Symbol	Parameter		71B229S12 Com'l.	71B229S16 Com'l.	71B229S22 Com'l.	71B229S28 Com'l	Unit
I_{CC1}	Operating Power Supply Current Outputs Open, V_{CC} = Max., f = 0		145	145	145	145	mA
I_{CC2}	Dynamic Operating Current Outputs Open, V_{CC} = Max., f = f_{MAX}	$\overline{WE} \leq V_{IL}$	250	230	200	190	mA
		$\overline{WE} \geq V_{IH}$	200	190	180	170	mA

2996 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX}=1/t_{CYC}, all Address input pins are cycling at f_{MAX}. For Reads and Writes both ports are cycling at f_{MAX}. f = 0 means no Address inputs change.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	Test Condition	IDT71B229S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2996 tbl 08

ACCESS TIME AND CLOCK FREQUENCY EQUIVALENTS

R3000/1 Clock Frequency	71B229 Access Time
40 MHz	12 ns
33 MHz	16 ns
25 MHz	22 ns
20 MHz	28 ns

2996 tbl 09

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 and 3

2996 tbl 11

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5V ± 5%

2996 tbl 10

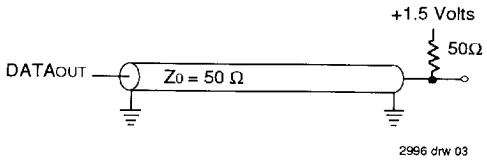
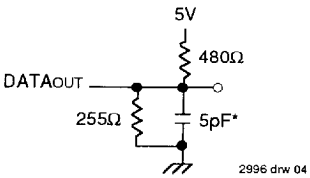


Figure 1. AC Test Load



*Includes scope and jig.

Figure 2. AC Test Load (for tOLZ & tOHZ)

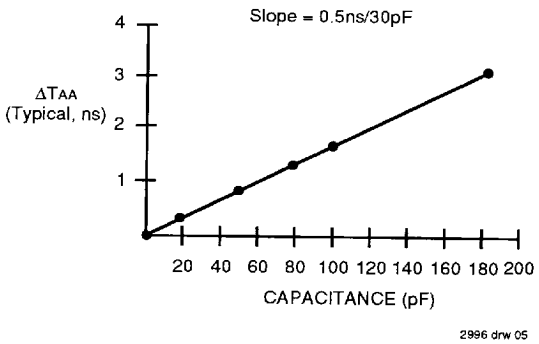


Figure 3. Lumped Capacitive Load, Typical Derating Curve

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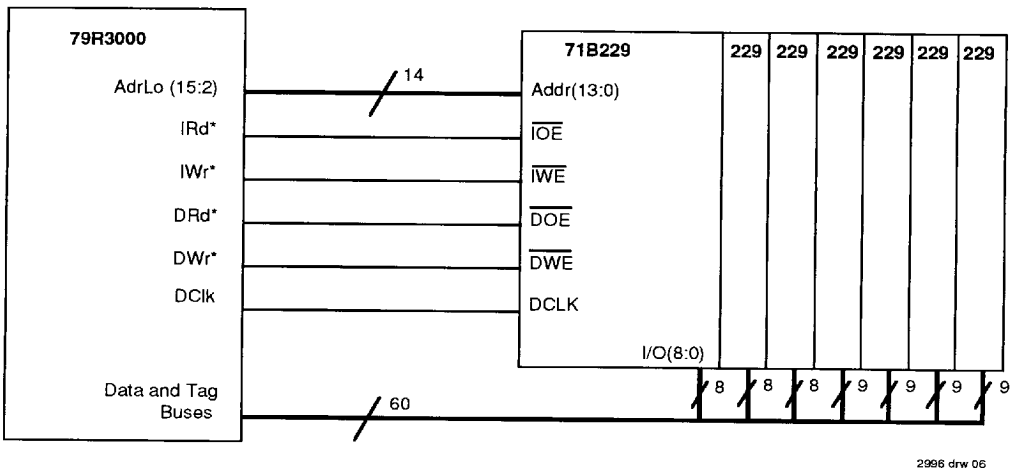


NOTE:
1. Loading of the IRd, IWr, DRd and DWr signals should be split evenly between the pair of R3000 pins dedicated to each of these functions.

Figure 2. Example of Cache Memory System Block Diagram

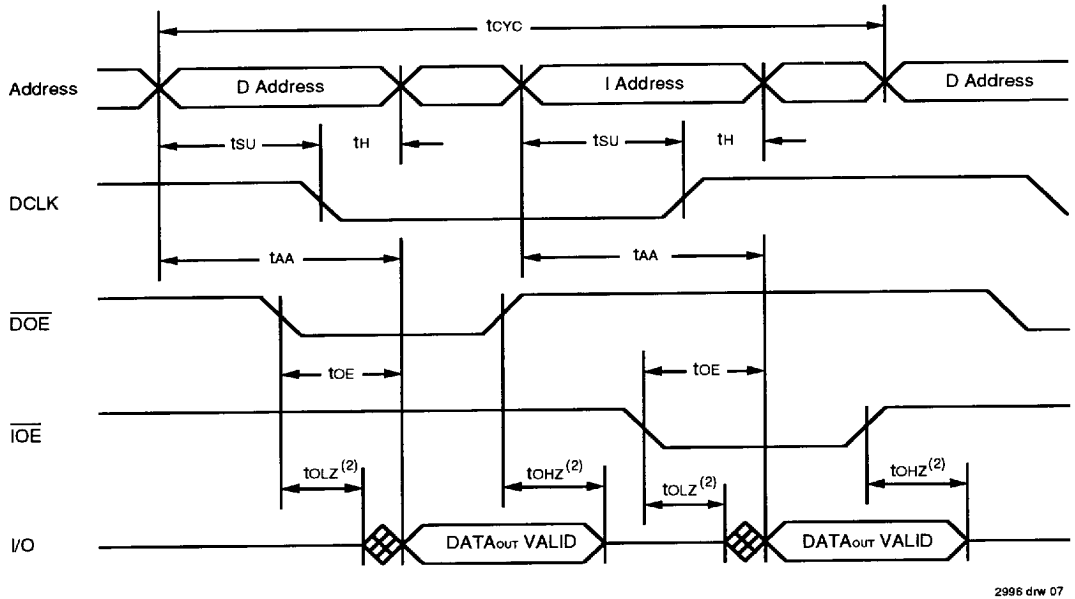
AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 5%)

Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tCYC	Read Cycle Time(1)	25	—	30	—	40	—	50	—	ns
tSU	Address Setup Time	4	—	4	—	5	—	5	—	ns
tH	Address Hold Time	3	—	3	—	4	—	6	—	ns
tAA	Address Access Time	—	12	—	16	—	22	—	28	ns
tOE	Output Enable Time	—	5	—	7	—	10	—	13	ns
tOLZ(2)	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	ns
tOHZ(2)	Output Disable to Output in High-Z	2	5	2	6	2	8	2	10	ns

2996 tbl 12

NOTES:
1. One cycle includes both a D bank read or write and an I bank read or write.
2. This parameter is guaranteed with the AC test load (Figure 2) due to device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLES(1)



2996 drw 07

NOTES:
1. $\overline{DWE}$ and $\overline{IWE}$ must be high during read cycles.
2. The transition is measured ±200mV from steady state.

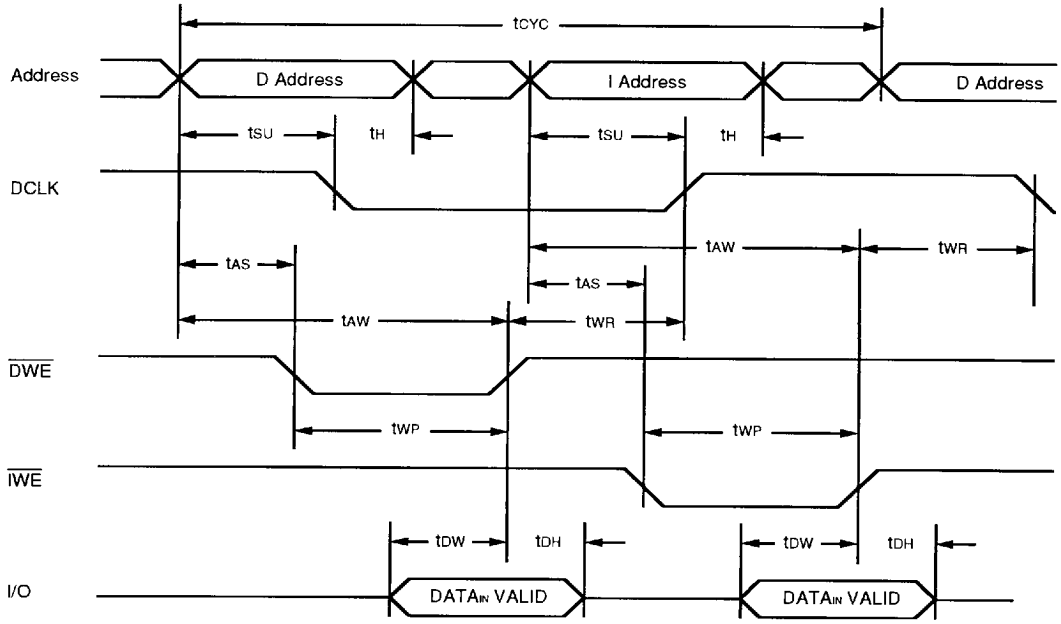
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 5%)

Symbol	Parameter	71B229S12		71B229S16		71B229S22		71B229S28		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
tCYC	Write Cycle Time(1)	25	—	30	—	40	—	50	—	ns
tSU	Address Setup Time	4	—	4	—	5	—	5	—	ns
tH	Address Hold Time	3	—	3	—	4	—	6	—	ns
tAW	Address to End of Write	10	—	13	—	16	—	20	—	ns
tAS	Address to Start of Write	0	—	0	—	0	—	0	—	ns
tWR	Write Recovery Time	–0.5	—	–0.5	—	–0.5	—	–0.5	—	ns
tWP	Write Pulse Width	10	—	13	—	16	—	20	—	ns
tDW	Data to Write Time Overlap	5	—	6	—	7	—	8	—	ns
tDH	Data Hold from Write Time	2	—	2	—	2	—	2	—	ns

NOTE:
1. One cycle includes both a D bank read or write and an I bank read or write.

2996 tbl 13

TIMING WAVEFORM OF WRITE CYCLES(1, 2)



NOTES:
1. $\overline{DOE}$ and $\overline{TOE}$ are HIGH during write cycles.
2. $\overline{DWE}$ must be HIGH or DCLK must be low during all address transitions. Likewise, $\overline{IWE}$ or DCLK must be HIGH during all address transitions.

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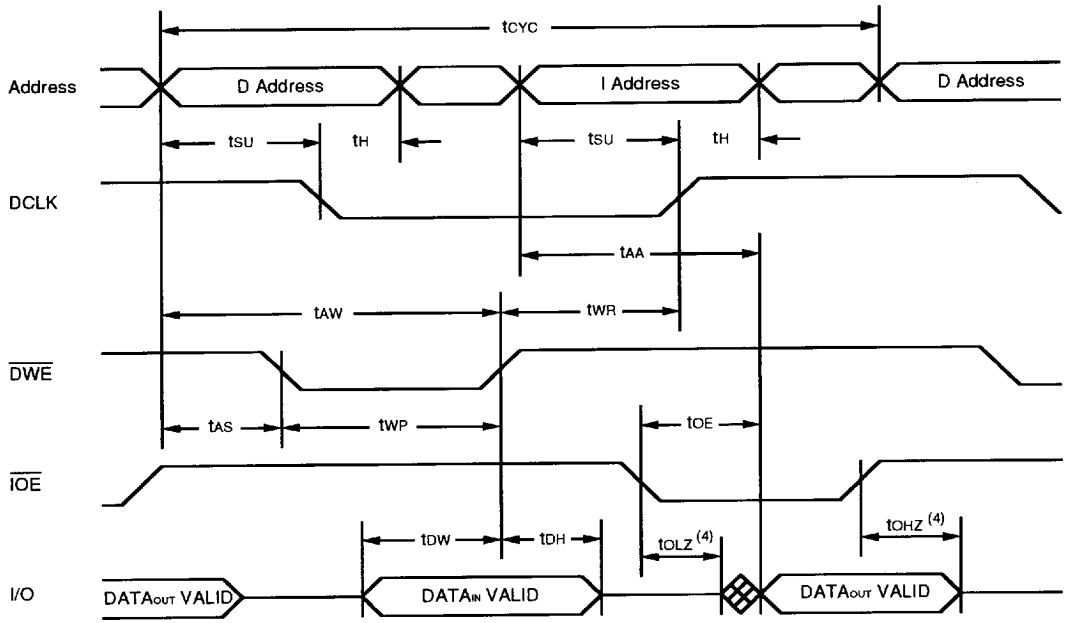
TIMING WAVEFORM OF MIXED READ AND WRITE CYCLES(1, 2, 3)



NOTES:
1. $\overline{DOE}$ and $\overline{IOE}$ are HIGH during write cycles.
2. $\overline{DWE}$ must be HIGH or DCLK must be low during all address transitions. Likewise, $\overline{IWE}$ or DCLK must be HIGH during all address transitions.
3. $\overline{DWE}$ and $\overline{IWE}$ must be HIGH during read cycles.
4. The transition is measured ±200mV from steady state.

ORDERING INFORMATION