HN29W25611 Series

256M AND type Flash Memory
More than 16,057-sector (271,299,072-bit)

HITACHI

ADE-203-995 (Z)
Preliminary, Rev. 0.0
Jan. 8, 1999

Description

The Hitachi HN29W25611 Series is a CMOS Flash Memory with AND type multi-level memory cells. It has fully automatic programming and erase capabilities with a single 3.3 V and 5 V power supply. The functions are controlled by simple external commands. To fit the I/O card applications, the unit of programming and erase is as small as (2048 + 64) bytes. Initial available sectors of HN29W25611 are more than 16,057 (98% of all sector address) and less than 16,384 sectors.

Features

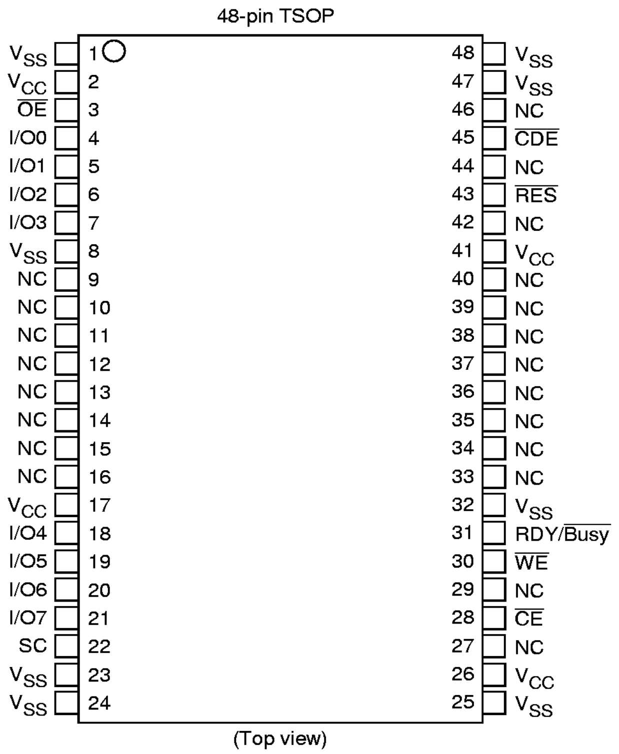
- On-board single power supply (V_{CC}): $V_{CC} = 3.3\ V \pm 0.3\ V$
  $V_{CC} = 5.0\ V \pm 0.5\ V$
- Organization
  - AND Flash Memory: (2048 + 64) bytes × (More than 16,057 sectors)
  - Data register: (2048 + 64) bytes
- Multi-level memory cell
  - 2 bit/per memory cell
- Automatic programming
  - Sector program time: 1.0 ms (typ)
  - System bus free
  - Address, data latch function
  - Internal automatic program verify function
  - Status data polling function
- Automatic erase
  - Single sector erase time: 1.0 ms (typ)
  - System bus free
  - Internal automatic erase verify function
  - Status data polling function

- Erase mode
  - — Single sector erase ((2048 + 64) byte unit)
- Fast serial read access time:
  - — First access time: 50 µs (max)
  - — Serial access time: 50 ns (max)
- Low power dissipation:
  - — I_{CC2} = 50 mA (max) (Read) (V_{CC} = 3.3 V)
  - — I_{CC2} = 70 mA (max) (Read) (V_{CC} = 5 V)
  - — I_{SB2} = 50 µA (max) (Standby) (V_{CC} = 3.3 V)
  - — I_{SB2} = 100 µA (max) (Standby) (V_{CC} = 5 V)
  - — I_{CC3}/I_{CC4} = 40 mA (max) (Erase/Program) (V_{CC} = 3.3 V)
  - — I_{CC3}/I_{CC4} = 60 mA (max) (Erase/Program) (V_{CC} = 5 V)
  - — I_{SB3} = 5 µA (max) (Deep standby) (V_{CC} = 3.3 V)
  - — I_{SB3} = 10 µA (max) (Deep standby) (V_{CC} = 5 V)
- Error correction (more than 1 bit error correction per each sector read) is required for data reliability.

Ordering Information

Type No.	Available sector	Package
HN29W25611T-50	More than 16,057 sectors	12.0 × 18.40 mm^2 0.5 mm pitch 48-pin plastic TSOP I (TFP-48D)

Pin Arrangement

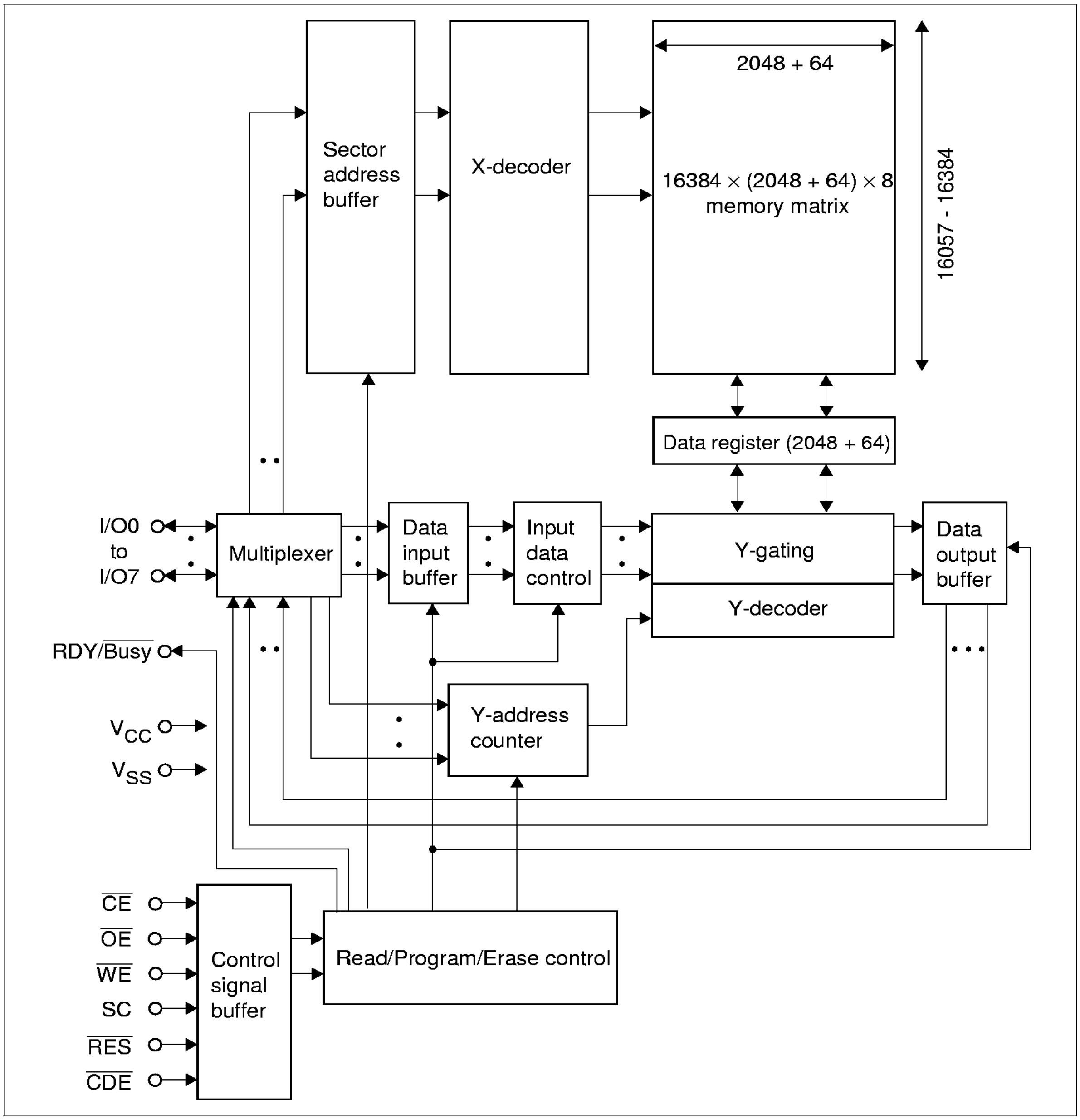


Pin Description

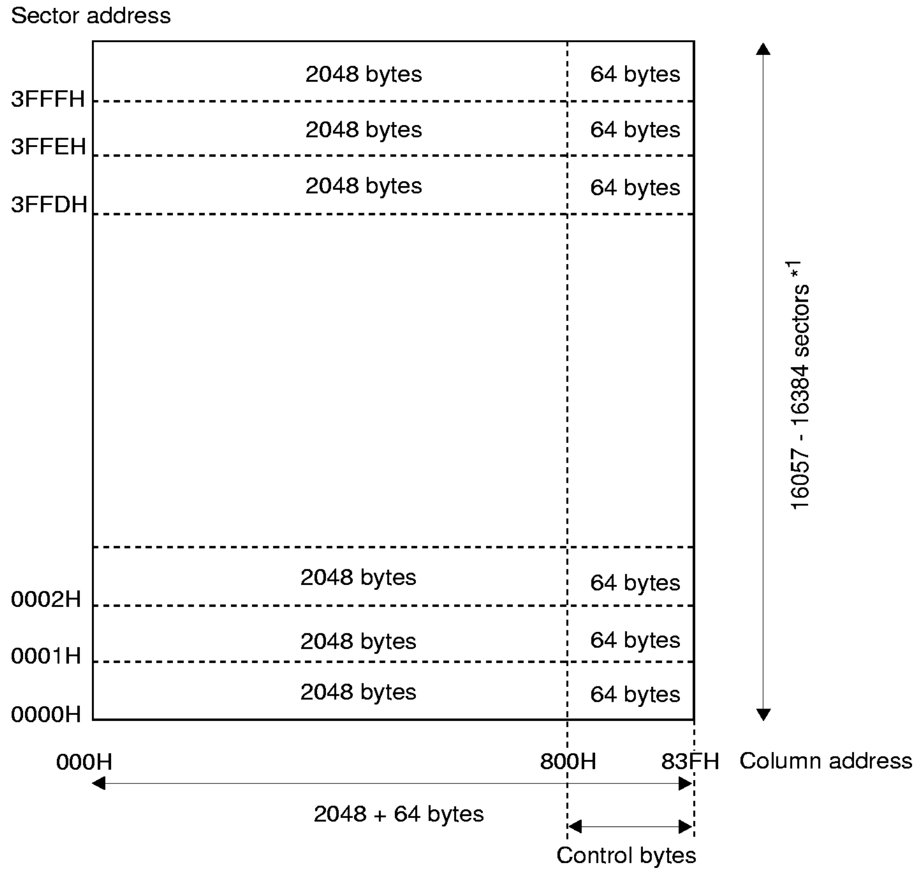
Pin name	Function
I/O0 to I/O7	Input/output
$\overline{\text{CE}}$	Chip enable
$\overline{\text{OE}}$	Output enable
$\overline{\text{WE}}$	Write enable
$\overline{\text{CDE}}$	Command data enable
V_{CC}*1	Power supply
V_{SS}*1	Ground
RDY/$\overline{\text{Busy}}$	Ready/$\overline{\text{Busy}}$
$\overline{\text{RES}}$	Reset
SC	Serial clock
NC	No connection

Note: 1. All V_{CC} and V_{SS} pins should be connected to a common power supply and a ground, respectively.

Block Diagram



Memory Map and Address



Address	Cycles	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7
Sector address	SA (1): First cycle	A0	A1	A2	A3	A4	A5	A6	A7
	SA (2): Second cycle	A8	A9	A10	A11	A12	A13	×[*2]	×
Column address	CA (1): First cycle	A0	A1	A2	A3	A4	A5	A6	A7
	CA (2): Second cycle	A8	A9	A10	A11	×	×	×	×

Notes: 1. Some failed sectors may exist in the device. The failed sectors can be recognized by reading the sector valid data written in a part of the column address 800 to 83F (The specific address is TBD.). The sector valid data must be read and kept outside of the sector before the sector erase. When the sector is programmed, the sector valid data should be written back to the sector.

2. An × means "Don't care". The pin level can be set to either V_{IL} or V_{IH}, referred to DC characteristics.

Pin Function

$\overline{\text{CE}}$: $\overline{\text{CE}}$ is used to select the device. The status returns to the standby at the rising edge of $\overline{\text{CE}}$ in the reading operation. However, the status does not return to the standby at the rising edge of $\overline{\text{CE}}$ in the busy state in programming and erase operation.

$\overline{\text{OE}}$: Memory data and status register data can be read, when $\overline{\text{OE}}$ is V_{IL}.

$\overline{\text{WE}}$: Commands and address are latched at the rising edge of $\overline{\text{WE}}$.

SC: Programming and reading data is latched at the rising edge of SC.

$\overline{\text{RES}}$: $\overline{\text{RES}}$ pin must be kept at the V_{ILR} (V_{SS} ± 0.2 V) level when V_{CC} is turned on and off. In this way, data in the memory is protected against unintentional erase and programming. $\overline{\text{RES}}$ must be kept at the V_{IHR} (V_{CC} ± 0.2 V) level during any operations such as programming, erase and read.

$\overline{\text{CDE}}$: Commands and data are latched when $\overline{\text{CDE}}$ is V_{IL} and address is latched when $\overline{\text{CDE}}$ is V_{IH}.

RDY/$\overline{\text{Busy}}$: The RDY/$\overline{\text{Busy}}$ indicates the program/erase status of the flash memory. The RDY/$\overline{\text{Busy}}$ signal is initially at a high impedance state. It turns to a V_{OL} level after the (40H) command in programming operation or the (B0H) command in erase operation. After the erase or programming operation finishes, the RDY/$\overline{\text{Busy}}$ signal turns back to the high impedance state.

I/O0 to I/O7: The I/O pins are used to input data, address and command, and are used to output memory data and status register data.

Mode Selection

Mode	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	SC	$\overline{\text{RES}}$	$\overline{\text{CDE}}$	RDY/$\overline{\text{Busy}}$*3	I/O0 to I/O7
Deep standby	×*4	×	×	×	V_{ILR}	×	V_{OH}	High-Z
Standby	V_{IH}	×	×	×	V_{IHR}	×	V_{OH}	High-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	×	V_{IHR}	×	V_{OH}	High-Z
Status register read*1	V_{IL}	V_{IL}	V_{IH}	×	V_{IHR}	×	V_{OH}	Status register outputs
Command write*2	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IHR}	V_{IL}	V_{OH}	Din

Notes:
1. Default mode after the power on is the status register read mode (refer to status transition). From I/O0 to I/O7 pins output the status, when $\overline{\text{CE}}$ = V_{IL} and $\overline{\text{OE}}$ = V_{IL} (conventional read operation condition).
2. Refer to the command definition. Data can be read, programmed and erased after commands are written in this mode.
3. The RDY/$\overline{\text{Busy}}$ bus should be pulled up to V_{CC} to maintain the V_{OH} level while the RDY/$\overline{\text{Busy}}$ pin outputs a high impedance.
4. An × means "Don't care". The pin level can be set to either V_{IL} or V_{IH} referred to DC characteristics.

Command Definition*1, 2

Command			Bus cycles	First bus cycle		Second bus cycle		
				Operation mode*3	Data in	Operation mode	Data in	Data out
Read	Serial read (1)	(Without CA)	3	Write	00H	Write	SA (1)*4	
		(With CA)	3 + 2h*6	Write	00H	Write	SA (1)*4	
	Serial read (2)		3	Write	F0H	Write	SA (1)*4	
	Read identifier codes		1	Write	90H	Read		ID*8, 9
	Data recovery read		1	Write	01H	Read		Recovery data
Auto erase	Single sector		4	Write	20H	Write	SA (1)*4	
Auto program	Program (1)	(Without CA*7)	4	Write	10H	Write	SA (1)*4	
		(With CA*7)	4 + 2h*6	Write	10H	Write	SA (1)*4	
	Program (2)*10		4	Write	1FH	Write	SA (1)*4	
	Program (3) (Control bytes)*7		4	Write	0FH	Write	SA (1)*4	
	Program (4)	(WithoutCA*7)	4	Write	11H	Write	SA (1)*4	
		(With CA*7)	4 + 2h*6	Write	11H	Write	SA (1)*4	
Reset			1	Write	FFH			
Clear status register			1	Write	50H			

				Third bus cycle		Fourth bus cycle	
Command			Bus cycles	Operation mode	Data in	Operation mode	Data in
Read	Serial read (1)	(Without CA)	3	Write	SA (2)*4		
		(With CA)	3 + 2h*6	Write	SA (2)*4	Write	CA (1)*5
	Serial read (2)		3	Write	SA (2)*4		
	Read identifier codes		1				
	Data recovery read		1				
Auto erase	Single sector		4	Write	SA (2)*4	Write	B0H*11
Auto program	Program (1)	(Without CA*7)	4	Write	SA (2)*4	Write	40H*11, 12
		(With CA*7)	4 + 2h*6	Write	SA (2)*4	Write	CA (1)
	Program (2)*10		4	Write	SA (2)*4	Write	40H*11, 12
	Program (3)	(Control bytes)*7	4	Write	SA (2)*4	Write	40H*11, 12
	Program (4)	(WithoutCA*7)	4	Write	SA (2)*4	Write	40H*11, 12
		(With CA*7)	4 + 2h*6	Write	SA (2)*4	Write	CA (1)
Reset			1				
Clear status register			1				

Command			Bus cycles	Fifth bus cycle		Sixth bus cycle	
				Operation mode	Data in	Operation mode	Data in
Read	Serial read (1)	(Without CA)	3				
		(With CA)	3 + 2h*6	Write	CA (2)*5		
	Serial read (2)		3				
	Read identifier codes		1				
	Data recovery read		1				
Auto erase	Single sector		4				
Auto program	Program (1)	(Without CA*7)	4				
		(With CA*7)	4 + 2h*6	Write	CA (2)*5	Write	40H*11, 12
	Program (2)*10		4				
	Program (3)	(Control bytes)*7	4				
	Program (4)	(WithoutCA*7)	4				
		(With CA*7)	4 + 2h*6	Write	CA (2)	Write	40H*11, 12
Reset			1				
Clear status register			1				

Notes:
1. Commands and sector address are latched at rising edge of $\overline{\text{WE}}$ pulses. Program data is latched at rising edge of SC pulses.
2. The chip is in the read status register mode when $\overline{\text{RES}}$ is set to V_{IHR} first time after the power up.
3. Refer to the command read and write mode in mode selection.
4. SA (1) = Sector address (A0 to A7), SA (2) = Sector address (A8 to A13).
5. CA (1) = Column address (A0 to A7), CA (2) = Column address (A8 to A11).
   ($0 \leq$ A11 to A0 $\leq$ 83FH)
6. The variable h is the input number of times of set of CA (1) and CA (2) ($1 \leq h \leq 2048 + 64$).
   Set of CA (1) and CA (2) can be input not only one time but free times.
7. By using program (1) and (3), data can additionally be programmed for each sector before erase.
8. ID = Identifier code; Manufacturer code (07H), Device code (99H).
9. The manufacturer identifier code is output when $\overline{\text{CDE}}$ is low and the device identifier code is output when $\overline{\text{CDE}}$ is high.
10. Before program (2) operations, data in the programmed sector must be erased.
11. No commands can be written during auto program and erase (when the RDY/$\overline{\text{Busy}}$ pin outputs a V_{OL}).
12. The fourth or sixth cycle of the auto program comes after the program data input is complete.

Mode Description

Read

Serial Read (1): Memory data D0 to D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 2112. When CA is input, memory data D (m) to D (m + j) in the sector of address SA is sequentially read. Then output data is not valid after the number of the SC pulse exceeds (2112 to m). The mode turns back to the standby mode at any time when $\overline{CE}$ is V_{IH}.

Serial Read (2): Memory data D2048 to D2111 in the sector of address SA is sequentially read. Output data is not valid after the number of the SC pulse exceeds 64. The mode turns back to the standby mode at any time when $\overline{CE}$ is V_{IH}.

Automatic Erase

Single Sector Erase: Memory data D0 to D2111 in the sector of address SA is erased automatically by internal control circuits. After the sector erase starts, the erasure completion can be checked through the RDY/$\overline{\text{Busy}}$ signal and status data polling. All the bits in the sector are "1" after the erase. The sector valid data stored in a part of memory data D2048 to D2111 must be read and kept outside of the sector before the sector erase.

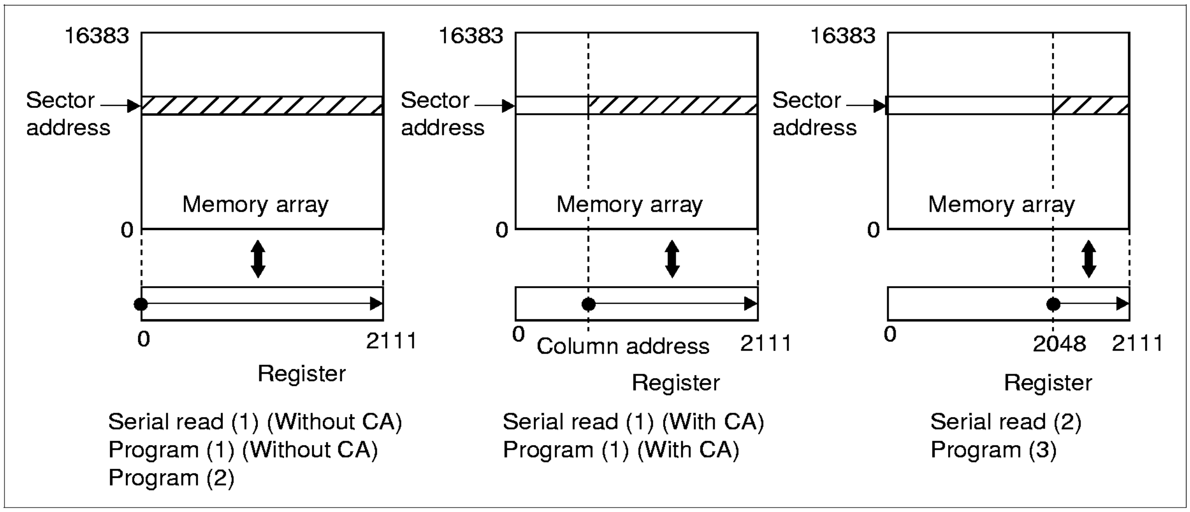
Automatic Program

Program (1): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input, program data PD (m) to PD (m + j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program (1), data can additionally be programmed for each sector before the following erase. When the column is programmed, the data of the column must be [FF]. After the programming starts, the program completion can be checked through the RDY/$\overline{\text{Busy}}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector valid data should be included in the program data PD2048 to PD2111.

Program (2): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. After the programming starts, the program completion can be checked through the RDY/$\overline{\text{Busy}}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed. The sector must be erased before programming. The sector valid data should be included in the program data PD2048 to PD2111.

Program (3): Program data PD2048 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. By using program (3), data can additionally be programmed for each sector before the following erase. When the column is programmed, the data of the column must be [FF]. After the programming starts, the program completion can be checked through the RDY/$\overline{\text{Busy}}$ signal and status data polling. Programmed bits in the sector turn from "1" to "0" when they are programmed.

Program (4): Program data PD0 to PD2111 is programmed into the sector of address SA automatically by internal control circuits. When CA is input, program data PD (m) to PD (m + j) is programmed from CA into the sector of address SA automatically by internal control circuits. By using program (4), data can be rewritten for each sector before the following erase. So the column data before programming operation are either "1" or "0". In this mode, E/W number of times must be counted whenever program (4) execute. After the programming starts, the program completion can be checked through the RDY/$\overline{\text{Busy}}$ signal and status data polling. The sector valid data should be included in the program data PD2048 to PD2111.



Serial read (1) (Without CA)
Program (1) (Without CA)
Program (2)

Serial read (1) (With CA)
Program (1) (With CA)

Serial read (2)
Program (3)

Status Register Read

The status returns to the status register read mode from standby mode, when $\overline{\text{CE}}$ and $\overline{\text{OE}}$ is V_{IL}. In the status register read mode, I/O pins output the same operation status as in the status data polling defined in the function description.

Identifier Read

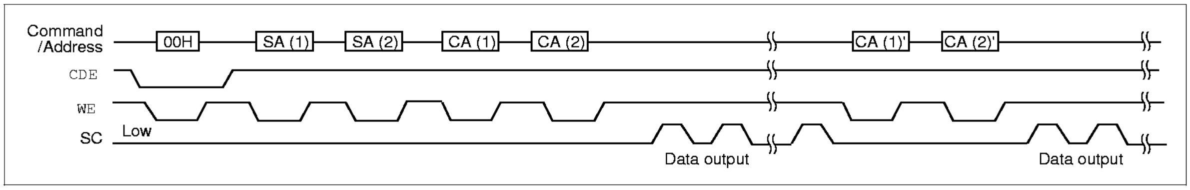
The manufacturer and device identifier code can be read in the identifier read mode. The manufacturer and device identifier code is selected with $\overline{\text{CDE}}$ V_{IL} and V_{IH}, respectively.

Data Recovery Read

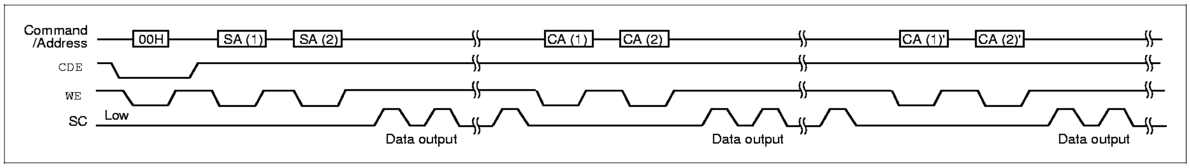
When programming was error, the program data can be read. When additional programming was error, the data compounded of the program data and the origin data in the sector address SA can be read. Output data is not valid after the number of SA pulse exceeds 2112. The mode turns back to the standby mode at any time when $\overline{\text{CE}}$ is V_{IH}.

Command/Address/Data Input Sequence

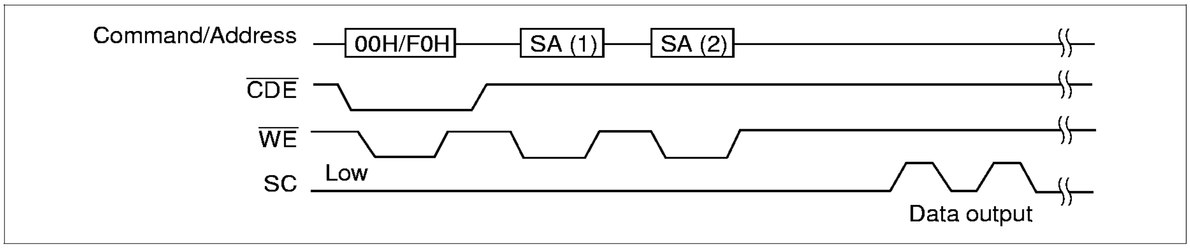
Serial Read (1) (With CA before SC)



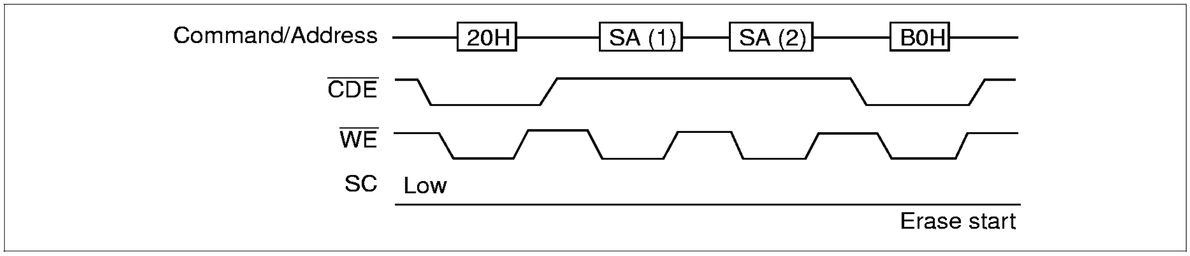
Serial Read (1) (With CA after SC)



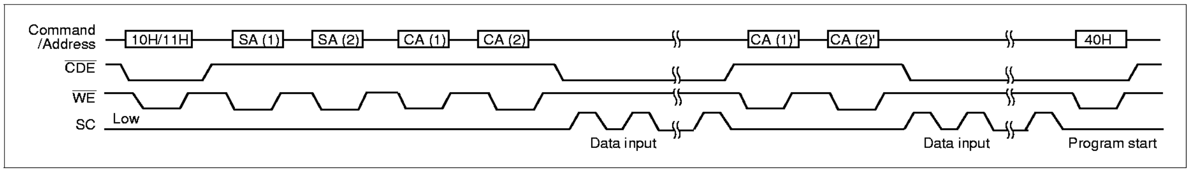
Serial Read (1) (Without CA), (2)



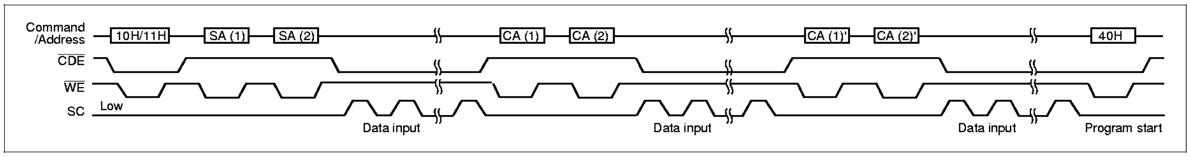
Single Sector Erase



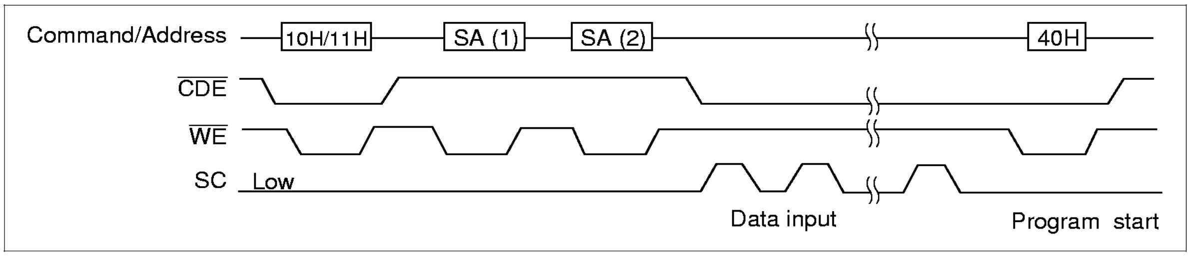
Program (1), (4) (With CA before SC)



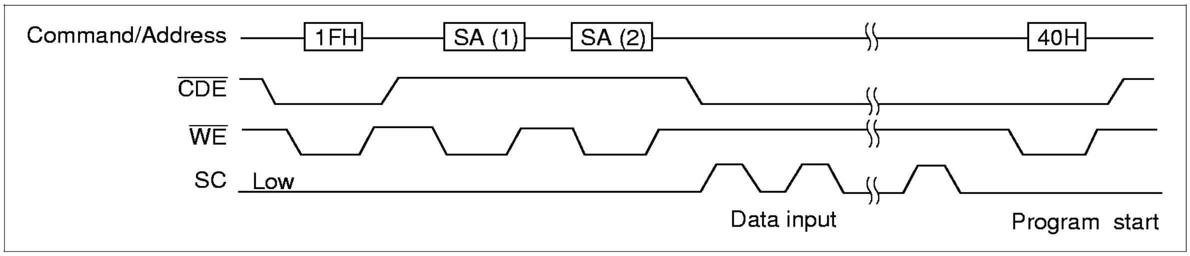
Program (1), (4) (With CA after SC)



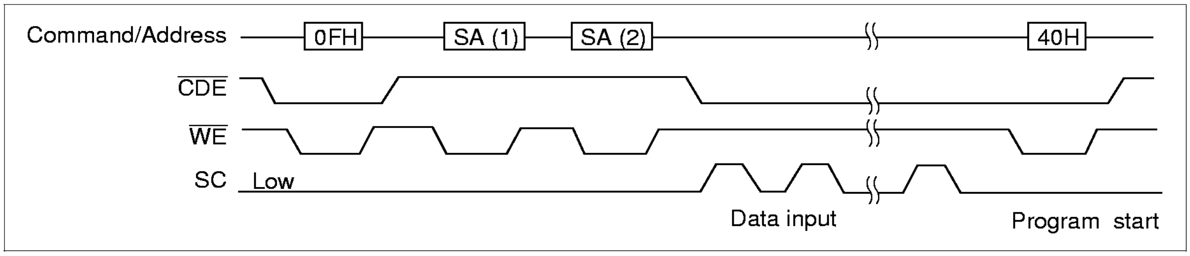
Program (1), (4) (Without CA)



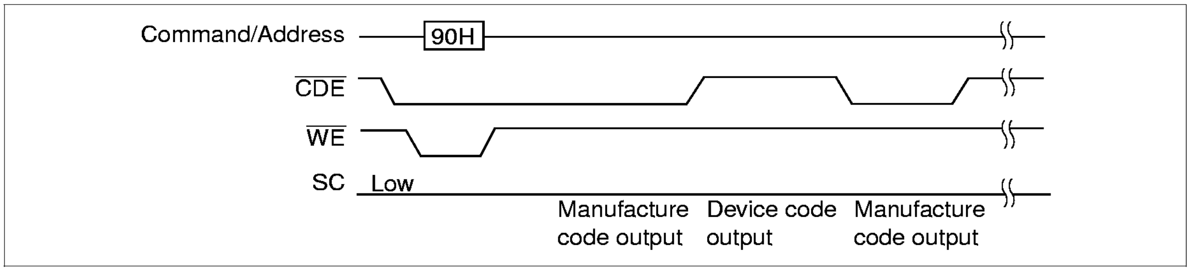
Program (2)



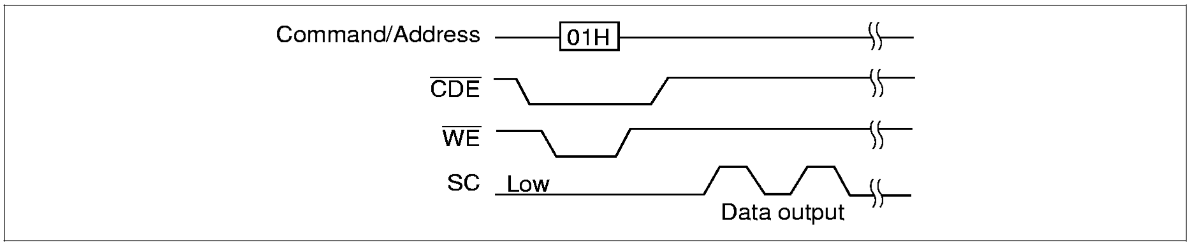
Program (3)



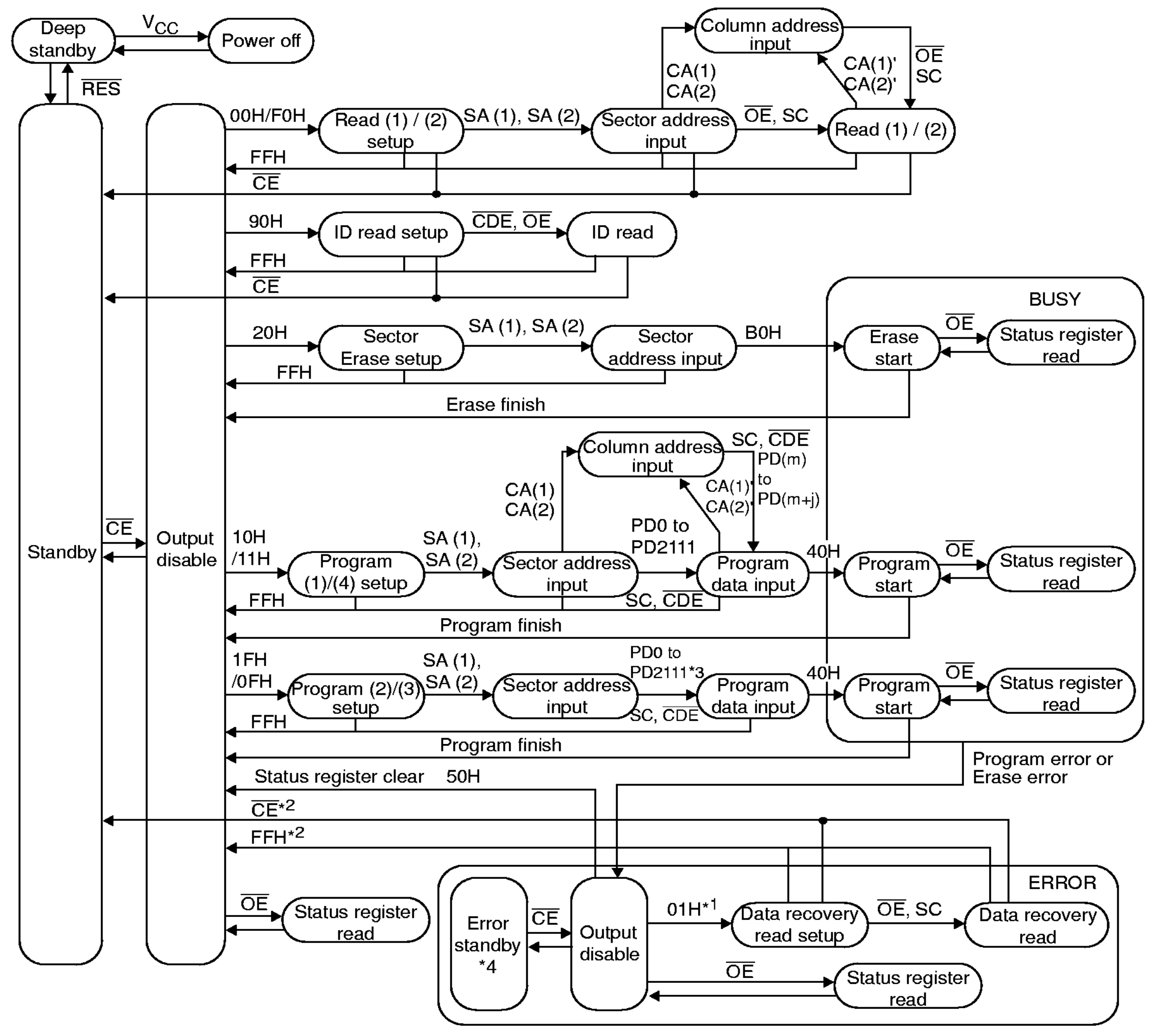
ID Read Mode



Data Recovery Read Mode



Status Transition



Notes: 1. (01H) Data recovery read can be used only for Program (1), (2), (3), (4) errors.
2. When reset is done by CE or FFH, error status flag is cleared.
3. When Program (3) mode, input data is PD2048 to PD2111.
4. When Error standby, I_{CC3} level is current.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
V_{CC} voltage	V_{CC}	–0.6 to +7	V	1
V_{SS} voltage	V_{SS}	0	V	
All input and output voltages	Vin, Vout	–0.6 to +7	V	1, 2
Operating temperature range	Topr	0 to +70	˚C	
Storage temperature range	Tstg	–65 to +125	˚C	3
Storage temperature under bias	Tbias	–10 to +80	˚C	

Notes:
1. Relative to V_{SS}.
2. Vin, Vout = –2.0 V for pulse width ≤ 20 ns.
3. Device storage temperature range before programming.

Capacitance (Ta = 25˚C, f = 1 MHz)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input capacitance	Cin	—	—	6	pF	Vin = 0 V
Output capacitance	Cout	—	—	12	pF	Vout = 0 V

DC Characteristics-1 (V_{CC} = 3.3 V ± 0.3 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = V_{SS} to V_{CC}
Standby V_{CC} current	I_{SB1}	—	0.3	1	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	30	50	µA	$\overline{CE}$ = V_{CC} ± 0.2 V, $\overline{RES}$ = V_{CC} ± 0.2 V
Deep standby V_{CC} current	I_{SB3}	—	1	5	µA	$\overline{RES}$ = V_{SS} ± 0.2 V
Operating V_{CC} current	I_{CC1}	—	20	25	mA	Iout = 0 mA, f = 0.2 MHz
	I_{CC2}	—	30	50	mA	Iout = 0 mA, f = 20 MHz
Operating V_{CC} current (Program)	I_{CC3}	—	20	40	mA	In programming
Operating V_{CC} current (Erase)	I_{CC4}	—	20	40	mA	In erase
Input voltage	V_{IL}	–0.3*[1, 2]	—	0.8	V	
	V_{IH}	2.0	—	V_{CC} + 0.3*[3]	V	
Input voltage ($\overline{RES}$ pin)	V_{ILR}	–0.2	—	0.2	V	
	V_{IHR}	V_{CC} – 0.2	—	V_{CC} + 0.2	V	
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA

Notes: 1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns in the read operation. V_{IL} min = –2.0 V for pulse width ≤ 20 ns in the read operation.

2. V_{IL} min = –0.6 V for pulse width ≤ 20 ns in the erase/data programming operation.

3. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, the operations are not guaranteed.

DC Characteristics-2 (V_{CC} = 5 V ± 0.5 V, Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Input leakage current	I_{LI}	—	—	2	µA	Vin = V_{SS} to V_{CC}
Output leakage current	I_{LO}	—	—	2	µA	Vout = V_{SS} to V_{CC}
Standby V_{CC} current	I_{SB1}	—	0.6	2	mA	$\overline{CE}$ = V_{IH}
	I_{SB2}	—	50	100	µA	$\overline{CE}$ = V_{CC} ± 0.2 V, $\overline{RES}$ = V_{CC} ± 0.2 V
Deep standby V_{CC} current	I_{SB3}	—	2	10	µA	$\overline{RES}$ = V_{SS} ± 0.2 V
Operating V_{CC} current	I_{CC1}	—	30	50	mA	Iout = 0 mA, f = 0.2 MHz
	I_{CC2}	—	50	70	mA	Iout = 0 mA, f = 20 MHz
Operating V_{CC} current (Program)	I_{CC3}	—	30	60	mA	In programming
Operating V_{CC} current (Erase)	I_{CC4}	—	30	60	mA	In erase
Input voltage	V_{IL}	–0.3*[1, 2]	—	0.8	V	
	V_{IH}	2.8	—	V_{CC} + 0.3*[3]	V	
Input voltage ($\overline{RES}$ pin)	V_{ILR}	–0.2	—	0.2	V	
	V_{IHR}	V_{CC} – 0.2	—	V_{CC} + 0.2	V	
Output voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2 mA
	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA

Notes:
1. V_{IL} min = –1.0 V for pulse width ≤ 50 ns in the read operation. V_{IL} min = –2.0 V for pulse width ≤ 20 ns in the read operation.
2. V_{IL} min = –0.6 V for pulse width ≤ 20 ns in the erase/data programming operation.
3. V_{IH} max = V_{CC} + 1.5 V for pulse width ≤ 20 ns. If V_{IH} is over the specified maximum value, the operations are not guaranteed.

AC Characteristics (V_{CC} = 3.3 V ± 0.3 V/V_{CC} = 5 V ± 0.5 V, Ta = 0 to +70˚C)

Test Conditions (V_{CC} = 3.3 V ± 0.3 V)

- Input pulse levels: 0.4 V/2.4 V
- Input pulse levels for $\overline{\text{RES}}$: 0.2 V/V_{CC} – 0.2 V
- Input rise and fall time: ≤ 5 ns
- Output load: 1 TTL gate + 100 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Test Conditions (V_{CC} = 5 V ± 0.5 V)

- Input pulse levels: 0.4 V/2.8 V
- Input pulse levels for $\overline{\text{RES}}$: 0.2 V/V_{CC} – 0.2 V
- Input rise and fall time: ≤ 5 ns
- Output load: 1 TTL gate + 100 pF (Including scope and jig.)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Power on and off, Serial Read Mode

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
Write cycle time	t_{CWC}	120	—	—	ns		
Serial clock cycle time	t_{SCC}	50	—	—	ns		
$\overline{CE}$ setup time	t_{CES}	0	—	—	ns		
$\overline{CE}$ hold time	t_{CEH}	0	—	—	ns		
Write pulse time	t_{WP}	60	—	—	ns	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	
Write pulse high time	t_{WPH}	40	—	—	ns		
Address setup time	t_{AS}	50	—	—	ns		
Address hold time	t_{AH}	10	—	—	ns		
Data setup time	t_{DS}	50	—	—	ns		
Data hold time	t_{DH}	10	—	—	ns		
SC to output delay	t_{SAC}	—	—	50	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$	
$\overline{OE}$ setup time for SC	t_{OES}	0	—	—	ns		
$\overline{OE}$ low to output low-Z	t_{OEL}	0	—	40	ns		
$\overline{OE}$ setup time before read	t_{OEPS}	200	—	—	ns		
$\overline{OE}$ setup time before command write	t_{OEWS}	0	—	—	ns		
SC to output hold	t_{SH}	15	—	—	ns	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$	
$\overline{OE}$ high to output float	t_{DF}	—	—	40	ns	$\overline{CE} = V_{IL}$, $\overline{WE} = V_{IH}$	1
$\overline{WE}$ to SC delay time	t_{WSD}	50	—	—	µs		2
$\overline{RES}$ to $\overline{CE}$ setup time	t_{RP}	1	—	—	ms		
SC to $\overline{OE}$ hold time	t_{SOH}	50	—	—	ns		
SC pulse width	t_{SP}	20	—	—	ns		
SC pulse low time	t_{SPL}	20	—	—	ns		
SC setup time for $\overline{CE}$	t_{SCS}	0	—	—	ns		
$\overline{CDE}$ setup time for $\overline{WE}$	t_{CDS}	0	—	—	ns		
$\overline{CDE}$ hold time for $\overline{WE}$	t_{CDH}	20	—	—	ns		
V_{CC} setup time for $\overline{RES}$	t_{VRS}	1	—	—	µs	$\overline{CE} = V_{IH}$	
$\overline{RES}$ to V_{CC} hold time	t_{VRH}	1	—	—	µs	$\overline{CE} = V_{IH}$	
$\overline{CE}$ setup time for $\overline{RES}$	t_{CESR}	1	—	—	µs		
RDY/$\overline{Busy}$ undefined for V_{CC} off	t_{DFP}	0	—	—	ns		
$\overline{RES}$ high to device ready	t_{BSY}	—	—	1	ms		
$\overline{CE}$ pulse high time	t_{CPH}	200	—	—	ns		
$\overline{CE}$, $\overline{WE}$ setup time for $\overline{RES}$	t_{CWRS}	0	—	—	ns		
$\overline{RES}$ to $\overline{CE}$, $\overline{WE}$ hold time	t_{CWRH}	0	—	—	ns		

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Notes
SC setup for $\overline{WE}$	t_{SW}	50	—	—	ns		
$\overline{CE}$ hold time for $\overline{OE}$	t_{COH}	0	—	—	ns		
SA (2) to CA (2) delay time	t_{SCD}	—	—	30	µs		
RDY/$\overline{Busy}$ setup for SC	t_{RS}	200	—	—	ns		
Time to device busy on read mode	t_{DBR}	—	—	1	µs		
Busy time on reset mode	t_{RBSY}	—	45	—	µs		

Notes: 1. t_{DF} is a time after which the I/O pins become open.

2. t_{WSD} (min) is specified as a reference point only for SC, if t_{WSD} is greater than the specified t_{WSD} (min) limit, then access time is controlled exclusively by t_{SAC}.

Program, Erase and Erase Verify

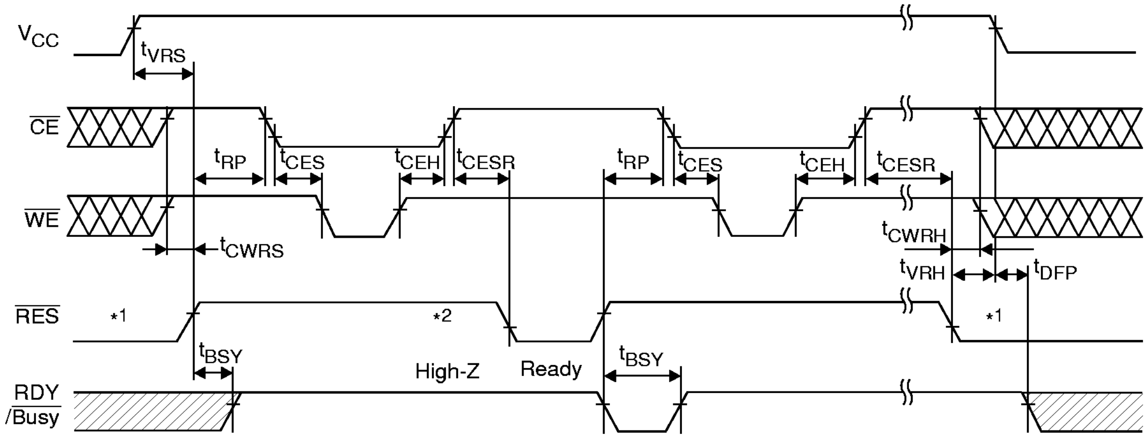
Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Write cycle time	t_{CWC}	120	—	—	ns		
Serial clock cycle time	t_{SCC}	50	—	—	ns		
$\overline{\text{CE}}$ setup time	t_{CES}	0	—	—	ns		
$\overline{\text{CE}}$ hold time	t_{CEH}	0	—	—	ns		
Write pulse time	t_{WP}	60	—	—	ns		
Write pulse high time	t_{WPH}	40	—	—	ns		
Address setup time	t_{AS}	50	—	—	ns		
Address hold time	t_{AH}	10	—	—	ns		
Data setup time	t_{DS}	50	—	—	ns		
Data hold time	t_{DH}	10	—	—	ns		
$\overline{\text{OE}}$ setup time before command write	t_{OEWS}	0	—	—	ns		
$\overline{\text{OE}}$ setup time before status polling	t_{OEPS}	200	—	—	ns		
Time to device busy	t_{DB}	—	—	150	ns		
Time to device busy on read mode	t_{DBR}	—	—	1	µs		
Auto erase time	t_{ASE}	—	1.0	5.0	ms		
Auto program time Program(1), (3)	t_{ASP}	—	1.5	37.0	ms		
Program(2)	t_{ASP}	—	1.0	35.0	ms		
Program(4)	t_{ASP}	—	2.0	40.0	ms		
$\overline{\text{WE}}$ to SC delay time	t_{WSD}	50	—	—	µs		
$\overline{\text{WE}}$ to SC delay time on recovery read mode	t_{WSDR}	2	—	—	µs		
$\overline{\text{CE}}$ pulse high time	t_{CPH}	200	—	—	ns		
SC pulse width	t_{SP}	20	—	—	ns		
SC pulse low time	t_{SPL}	20	—	—	ns		
Data setup time for SC	t_{SDS}	0	—	—	ns		
Data hold time for SC	t_{SDH}	30	—	—	ns	$\overline{\text{CDE}} = V_{IL}$	
SC setup for $\overline{\text{WE}}$	t_{SW}	50	—	—	ns		
SC setup for $\overline{\text{CE}}$	t_{SCS}	0	—	—	ns		
SC hold time for $\overline{\text{WE}}$	t_{SCHW}	20	—	—	ns		
$\overline{\text{CE}}$ to output delay	t_{CE}	—	—	120	ns		

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
$\overline{\text{OE}}$ to output delay	t_{OE}	—	—	60	ns		
$\overline{\text{OE}}$ high to output float	t_{DF}	—	—	40	ns		1
$\overline{\text{RES}}$ to $\overline{\text{WE}}$ setup time	t_{RP}	1	—	—	ms		
$\overline{\text{CDE}}$ setup time for $\overline{\text{WE}}$	t_{CDS}	0	—	—	ns		
$\overline{\text{CDE}}$ hold time for $\overline{\text{WE}}$	t_{CDH}	20	—	—	ns		
$\overline{\text{CDE}}$ setup time for SC	t_{CDSS}	1.5	—	—	µs		
$\overline{\text{CDE}}$ hold time for SC	t_{CDSH}	0	—	—	ns		
Next cycle ready time	t_{RDY}	0	—	—	ns		
$\overline{\text{CDE}}$ to $\overline{\text{OE}}$ hold time	t_{CDOH}	50	—	—	ns		
$\overline{\text{CDE}}$ to output delay	t_{CDAC}	—	—	50	ns		
$\overline{\text{CDE}}$ to output invalid	t_{CDF}	—	—	100	ns		
$\overline{\text{CE}}$ setup time for $\overline{\text{OE}}$	t_{COS}	0	—	—	ns		
$\overline{\text{CE}}$ hold time for $\overline{\text{OE}}$	t_{COH}	0	—	—	ns		
$\overline{\text{CDE}}$ to $\overline{\text{OE}}$ setup time	t_{CDOS}	20	—	—	ns		
$\overline{\text{OE}}$ setup time for SC	t_{OES}	0	—	—	ns		
$\overline{\text{OE}}$ low to output low-Z	t_{OEL}	0	—	—	ns		
SC to output delay	t_{SAC}	—	—	50	ns		
SC to output hold	t_{SH}	15	—	—	ns		
RDY/$\overline{\text{Busy}}$ setup for SC	t_{RS}	200	—	—	ns		
$\overline{\text{CE}}$ hold time for $\overline{\text{WE}}$	t_{CWH}	1.0	—	—	µs		
$\overline{\text{CE}}$ hold time for $\overline{\text{WE}}$ on recovery read mode	t_{CWHR}	2	—	—	µs		
$\overline{\text{WE}}$ hold time for $\overline{\text{WE}}$	t_{WWH}	1	—	—	µs		
Busy time on read mode	t_{RBSY}	—	45	—	µs		

Note: 1. t_{DF} is a time after which the I/O pins become open.

Timing Waveforms

Power on and off Sequence

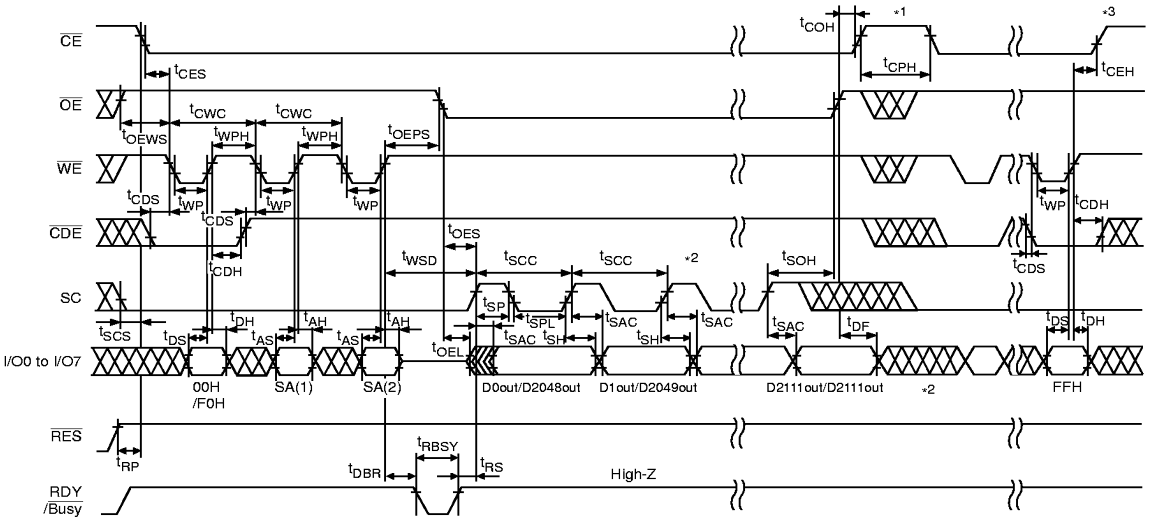


Notes: 1. $\overline{\text{RES}}$ must be kept at the V_{ILR} level referred to DC characteristics at the rising and falling edges of V_{CC} to guarantee data stored in the chip.

2. $\overline{\text{RES}}$ must be kept at the V_{IHR} level referred to DC characteristics while I/O7 outputs the V_{OL} level in the status data polling and RDY/$\overline{\text{Busy}}$ outputs the V_{OL} level.

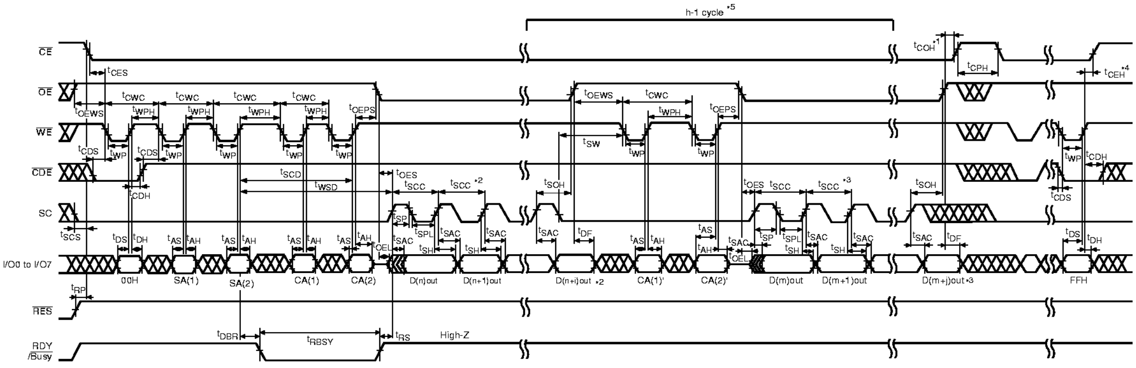
3. ▨ : Undefined

Serial Read (1) (2) Timing Waveform



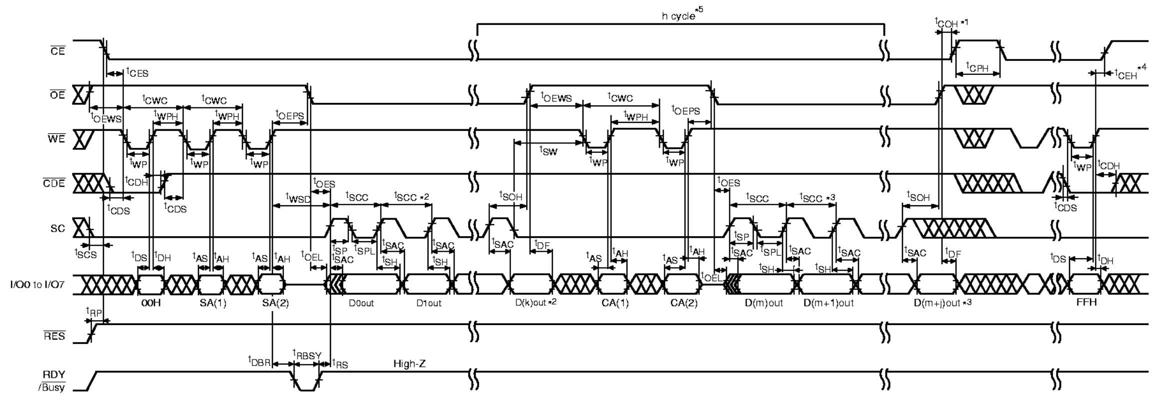
Notes: 1. The status returns to the standby at the rising edge of $\overline{\text{CE}}$.
2. Output data is not valid after the number of the SC pulse exceeds 2112 and 64 in the serial read mode (1)and (2), respectively.
3. After any commands are written, the status can return to the standby after the command FFH is input and $\overline{\text{CE}}$ turns to the V_{IH} level.

Serial Read (1) with CA before SC Timing Waveform



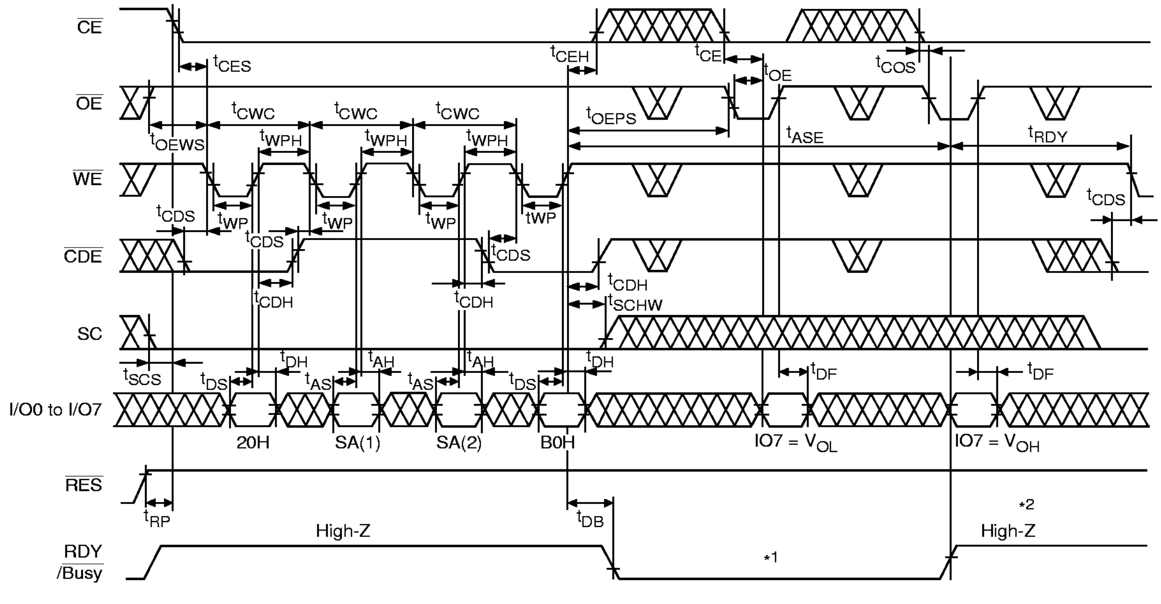
Notes: 1. The status returns to the Standby at the rising edge of $\overline{\text{CE}}$.
2. Output data is not valid after the number of the SC pulse exceeds (2112-n). ($i \le 2111\text{-}n$, $0 \le n \le 2111$)
3. Output data is not valid after the number of the SC pulse exceeds (2112-m). ($j \le 2111\text{-}m$, $0 \le m \le 2111$)
4. After any commands are written, the status can return to the standby after the command FFH is input and $\overline{\text{CE}}$ turns to the V_{IH} level.
5. This interval can be repeated (h-1) cycle. ($1 \le h \le 2048 + 64$)

Serial Read (1) with CA after SC Timing Waveform



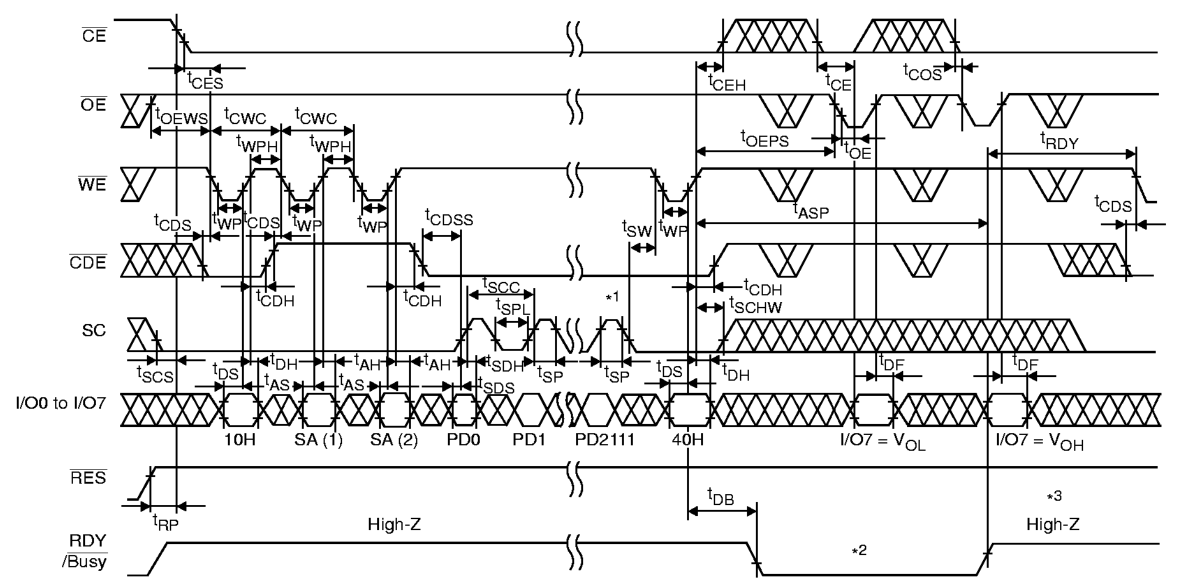
Notes: 1. The status returns to the Standby at the rising edge of $\overline{\text{CE}}$.
2. Output data is not valid after the number of the SC pulse exceeds 2112. $(0 \leq k \leq 2111)$
3. Output data is not valid after the number of the SC pulse exceeds (2112-m). $(j \leq 2111\text{-}m,\ 0 \leq m \leq 2111)$
4. After any commands are written, the status can return to the standby after the command FFH is input and $\overline{\text{CE}}$ turns to the V_{IH} level.
5. This interval can be repeated h cycle. $(1 \leq h \leq 2048 + 64)$

Erase and Status Data Polling Timing Waveform (Sector Erase)



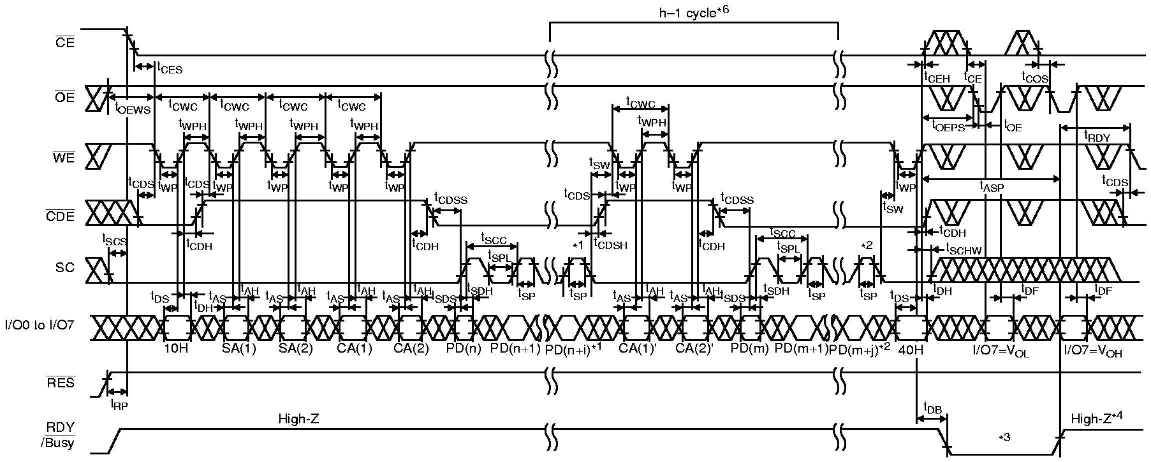
Notes: 1. Any commands,including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ outputs a V_{OL}.
2. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.

Program (1) and Status Data Polling Timing Waveform



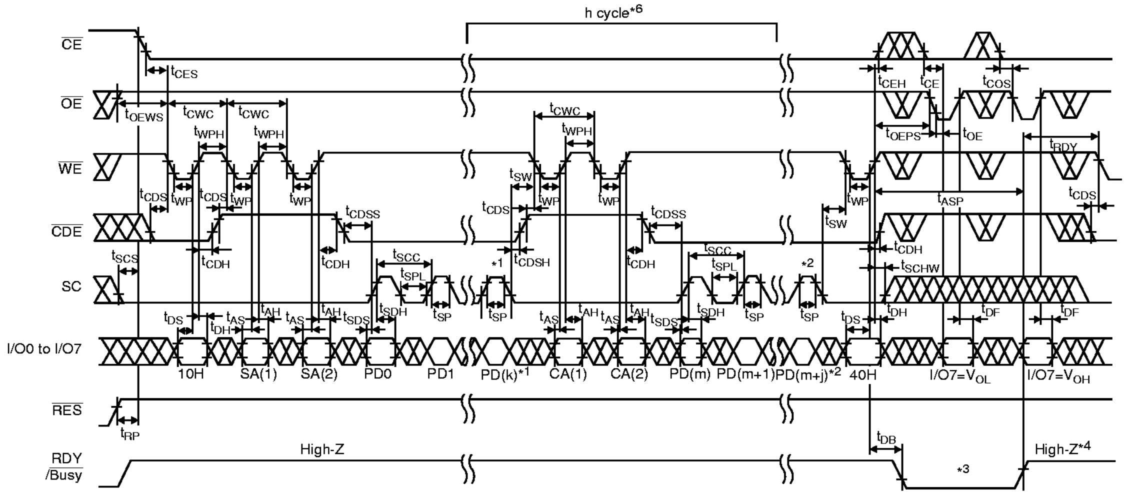
Notes: 1. The programming operation is not guranteed when the number of the SC pulse exceeds 2112.
2. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
3. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
4. By using program (1), data can be programmed additionally for each sector before erase.

Program (1) with CA before SC and Status Data Polling Timing Waveform



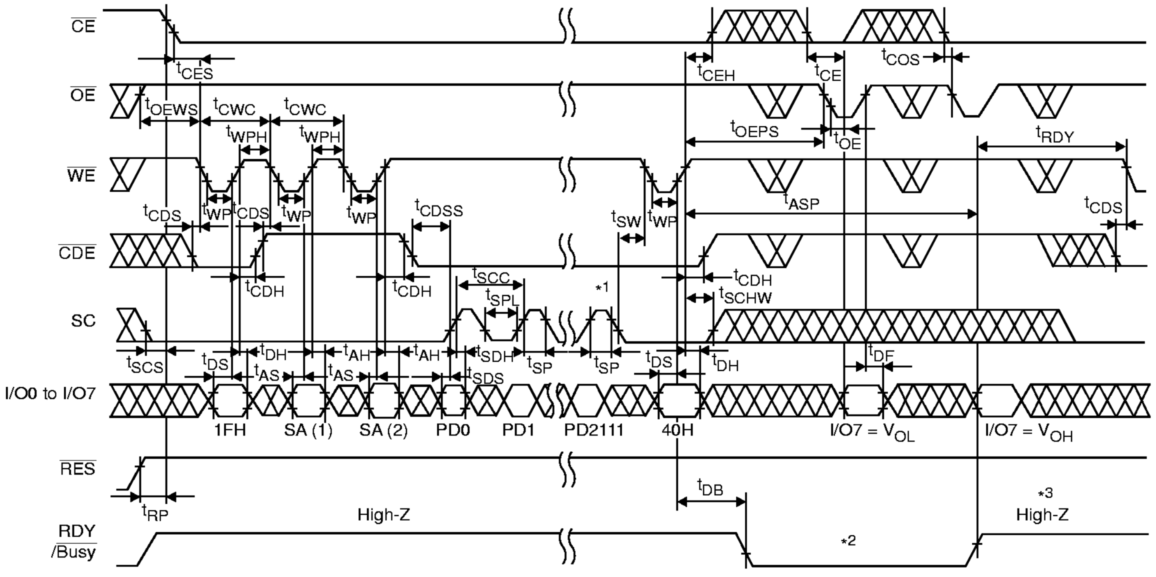
Notes: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112 – n).(i ≤ 2111 – n, 0 ≤ n ≤ 2111)
2. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112 – m).(j ≤ 2111 – m, 0 ≤ m ≤ 2111)
3. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL}.
4. The status returns to the standby status after RDY/Busy returns to High-Z.
5. By using program (1), data can be programmed additionally for each sector before erase.
6. This interval can be repeated (h – 1) cycle.(1 ≤ h ≤ 2048 + 64)

Program (1) with CA after SC and Status Data Polling Timing Waveform



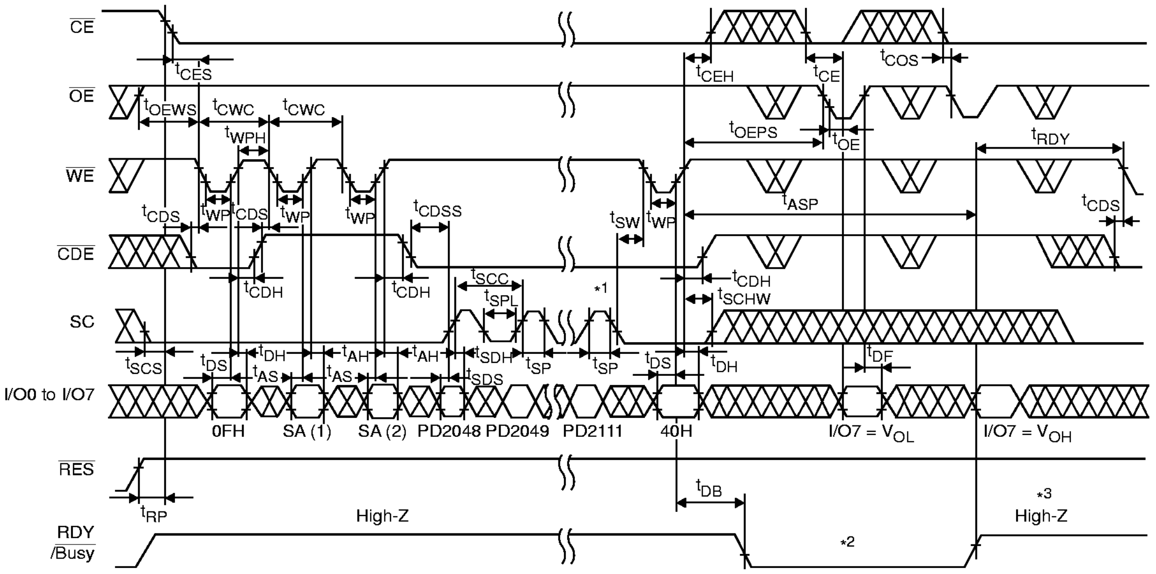
Notes: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.(0 ≤ k ≤ 2111)
2. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112 – m).(j ≤ 2111 – m, 0 ≤ m ≤ 2111)
3. Any commands, including reset command FFH, cannot be input while RDY/Busy is V_{OL}.
4. The status returns to the standby status after RDY/Busy returns to High-Z.
5. By using program (1), data can be programmed additionally for each sector before erase.
6. This interval can be repeated h cycle.(1 ≤ h ≤ 2048 + 64)

Program (2) and Status Data Polling Timing Waveform



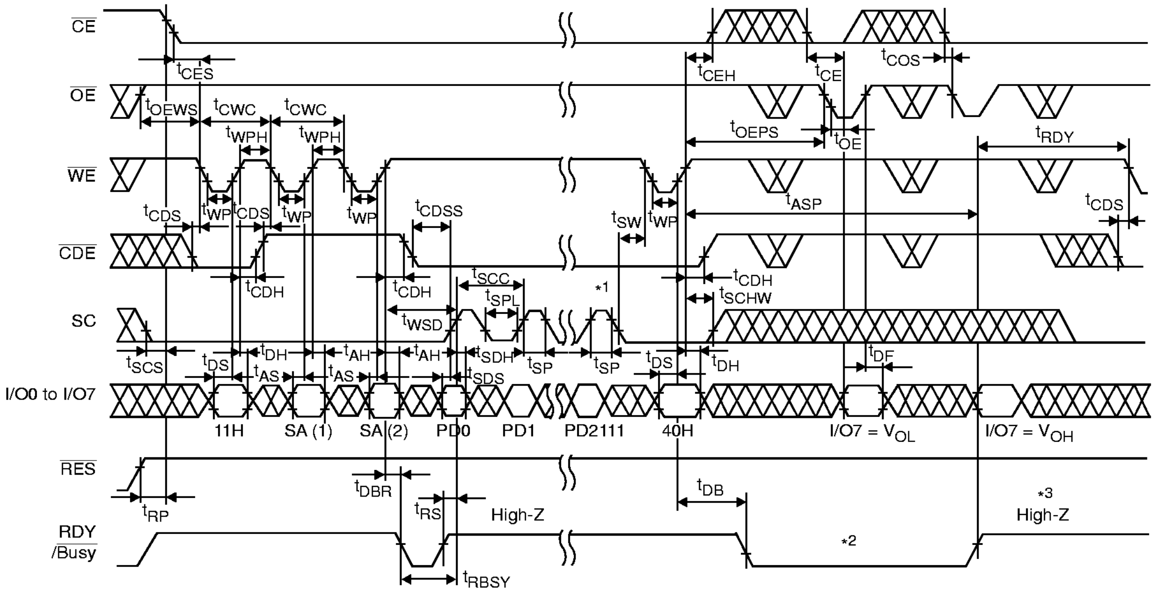
Notes: 1. The programming operation is not guranteed when the number of the SC pulse exceeds 2112.
2. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
3. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
4. By using program (2), the programmed data of each sector must be erased before programming next data.

Program (3) and Status Data Polling Timing Waveform



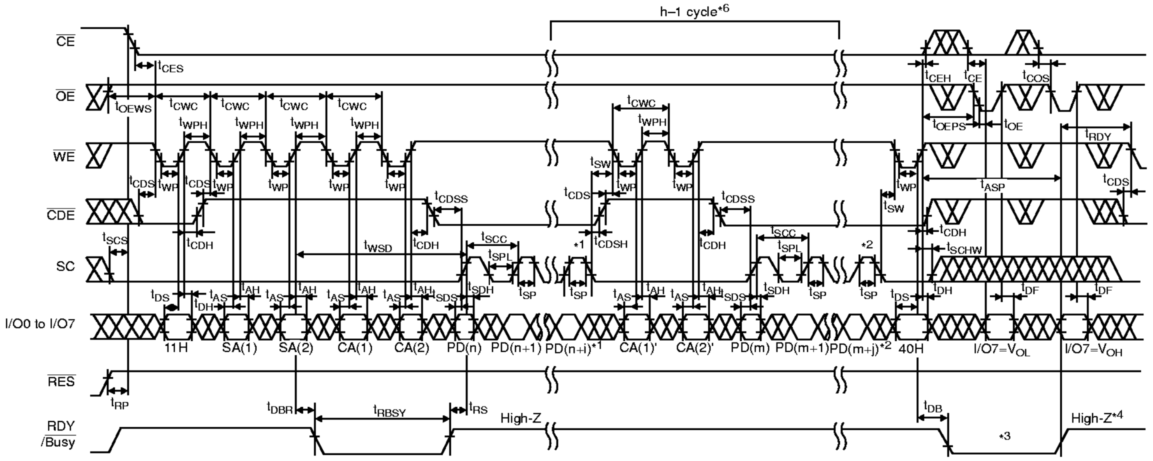
Notes:
1. The programming operation is not guranteed when the number of the SC pulse exceeds 64.
2. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
3. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
4. By using program (3), the data can be programmed additionally for each sector before erase.

Program (4) and Status Data Polling Timing Waveform



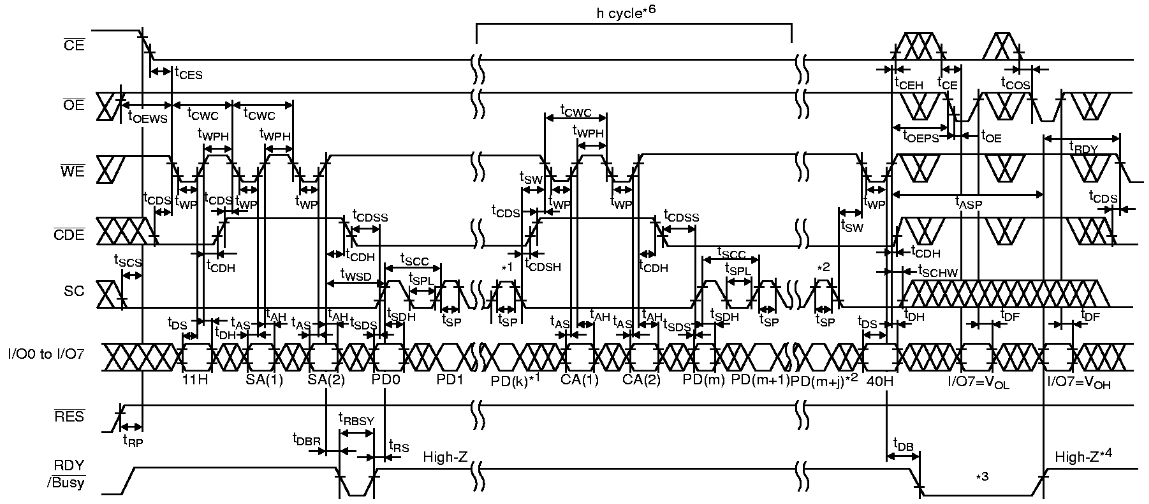
Notes: 1. The programming operation is not guranteed when the number of the SC pulse exceeds 2112.
2. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
3. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
4. By using program (4), data can be rewritten for each sector.

Program (4) with CA before SC and Status Data Polling Timing Waveform



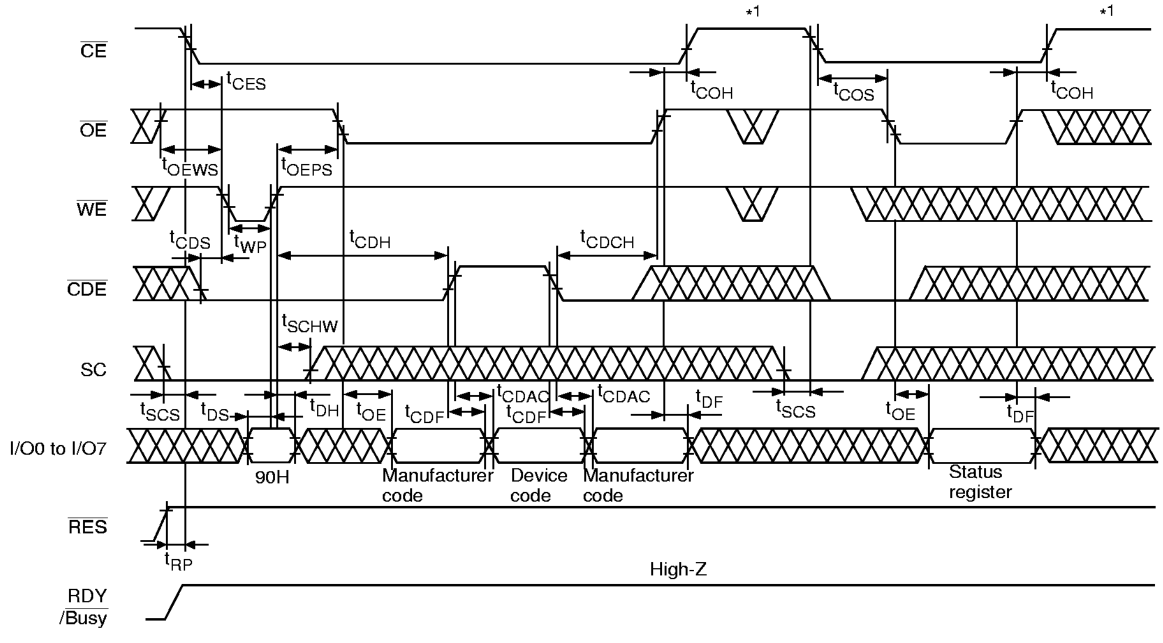
Notes: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112 – n).(i ≤ 2111 – n, 0 ≤ n ≤ 2111)
2. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112 – m).(j ≤ 2111 – m, 0 ≤ m ≤ 2111)
3. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
4. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
5. By using program (4), data can be rewritten for each sector.
6. This interval can be repeated (h – 1) cycle.(1 ≤ h ≤ 2048 + 64)

Program (4) with CA after SC and Status Data Polling Timing Waveform



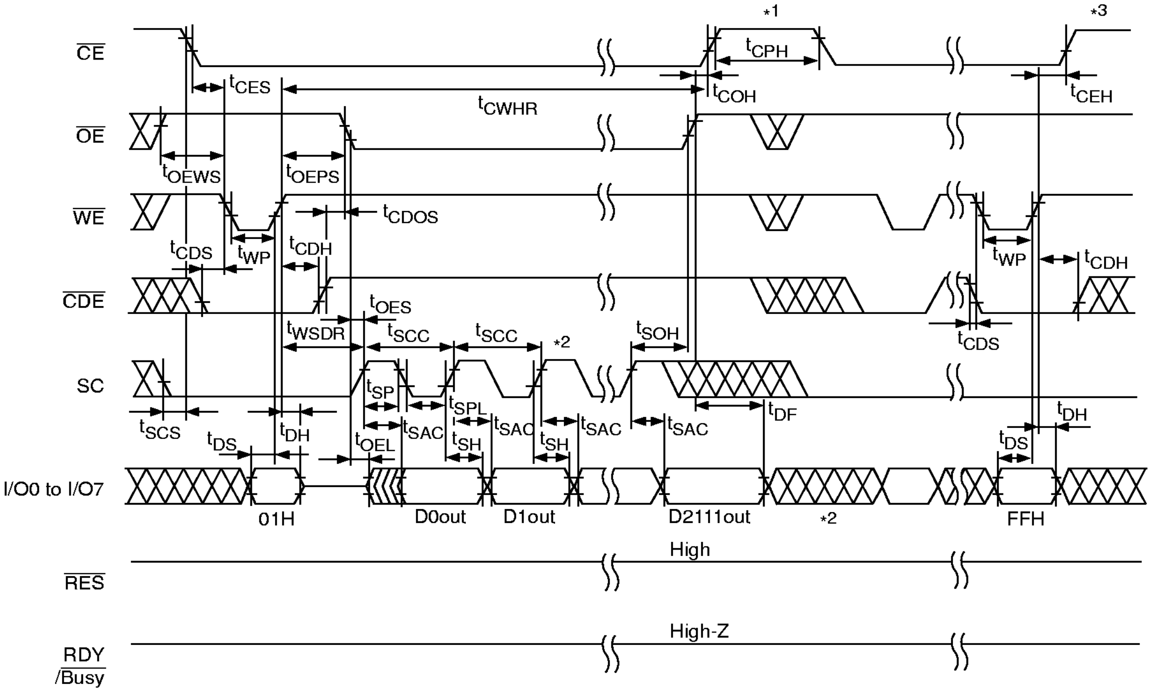
Notes: 1. The programming operation is not guaranteed when the number of the SC pulse exceeds 2112.(0 ≤ k ≤ 2111)
2. The programming operation is not guaranteed when the number of the SC pulse exceeds (2112 – m).(j ≤ 2111 – m, 0 ≤ m ≤ 2111)
3. Any commands, including reset command FFH, cannot be input while RDY/$\overline{\text{Busy}}$ is V_{OL}.
4. The status returns to the standby status after RDY/$\overline{\text{Busy}}$ returns to High-Z.
5. By using program (4), data can be rewritten for each sector.
6. This interval can be repeated h cycle.(1 ≤ h ≤ 2048 + 64)

ID and Status Register Read Timing Waveform



Note: 1. The status returns to the standby at the rising edge of $\overline{CE}$.

Data Recovery Read Timing Waveform

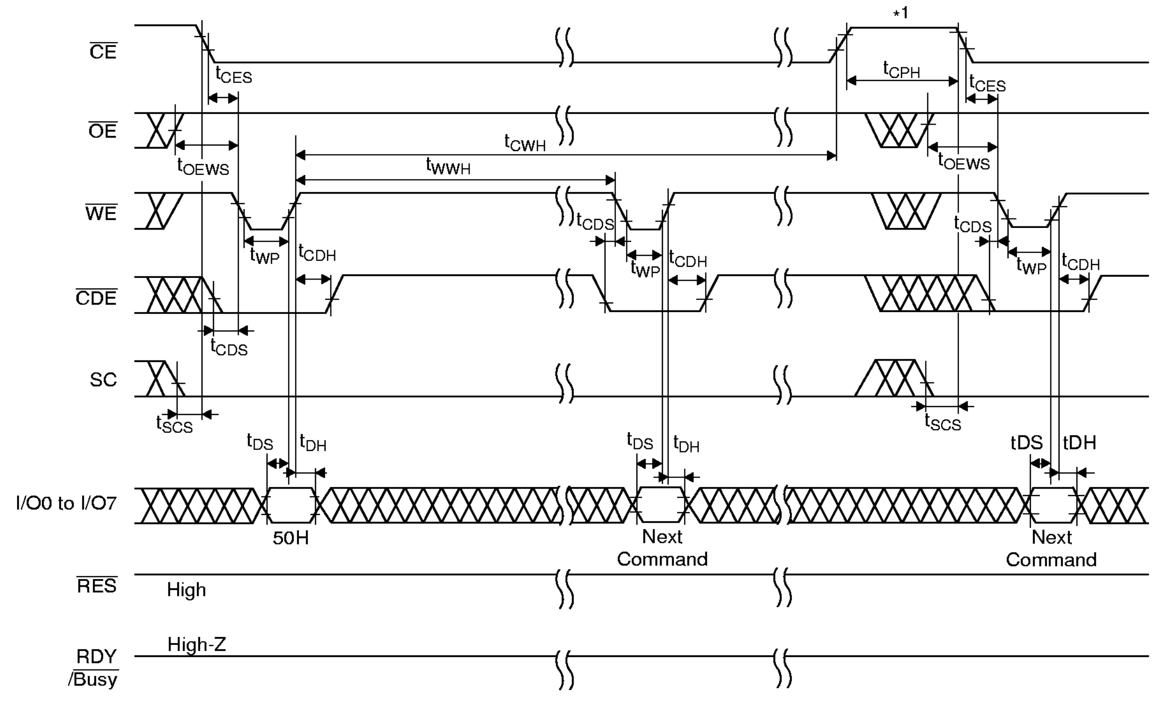


Notes: 1. The status returns to the standby at the rising edge of $\overline{\text{CE}}$.

2. Output data is not valid after the number of the SC pulse exceed 2112 in the recovery data read mode.

3. After any commands are written, the status can turns to the standby after the command FFH is input and $\overline{\text{CE}}$ turns to the V_{IH} level.

Clear Status Register Timing Waveform



Note 1. The status returns to the standby at the rising edge of $\overline{\text{CE}}$.

Function Description

Status Register: The HN29W25611 outputs the operation status data as follows: I/O7 pin outputs a V_{OL} to indicate that the memory is in either erase or program operation. The level of I/O7 pin turns to a V_{OH} when the operation finishes. I/O5 and I/O4 pins output V_{OL}s to indicate that the erase and program operations complete in a finite time, respectively. If these pins output V_{OH}s, it indicates that these operations have timed out. When these pins monitor, I/O7 pin must turn to a V_{OH}. To execute other erase and program operation, the status data must be cleared after a time out occurs. From I/O0 to I/O3 pins are reserved for future use. The pins output V_{OL}s and should be masked out during the status data read mode. The function of the status register is summarized in the following table.

I/O	Flag definition	Definition
I/O7	Ready/$\overline{\text{Busy}}$	V_{OH} = Ready, V_{OL} = Busy
I/O6	Reserved	Outputs a V_{OL} and should be masked out during the status data poling mode.
I/O5	Erase check	V_{OH} = Fail, V_{OL} = Pass
I/O4	Program check	V_{OH} = Fail, V_{OL} = Pass
I/O3	Reserved	Outputs a V_{OL} and should be masked out during the status data poling mode.
I/O2	Reserved	
I/O1	Reserved	
I/O0	Reserved	

Notes

Unusable Sector

Initially, the HN29W25611 contains unusable sectors. Due to the nature of the device architecture, the device can also be screened and tested for partial invalid sectors for selected systems that can utilize the devices.

1. Tested for partial invalid sectors. The usable sectors were programmed the following data.

Column address	820H	821H	822H	823H	824H	825H
Data	1CH	71H	C7H	1CH	71H	C7H

2. No erase and program for the partial invalid sectors by the system.

Item	Min
Usable sectors (initially)	16,057 (98%)

Enable High System Reliability

The device may fail during a program or erase operation due to write or erase cycle. The following architecture will enable high system reliability if a failure occurs.

1. Error in read: Error correction that more than 1 bit error correction per each sector read is required for data reliability.
2. Error in program or erase operation: The device may fail during a program or erase operation due to write or erase cycle. The status register are indicated that the erase and program operation complete in a finite time. When the error happens in sector, try to reprogram the data into another sector. Then, prevent further system access to sector that error happens. Typically, recommended number of a spare sectors are 1.8% within initial usable 16,057 sectors by the each device.
3. Prolongation of Flash memory life: The write/erase endurance is 1×10^5 cycles and the data retention time is more than 10 years under the condition of the error correction.

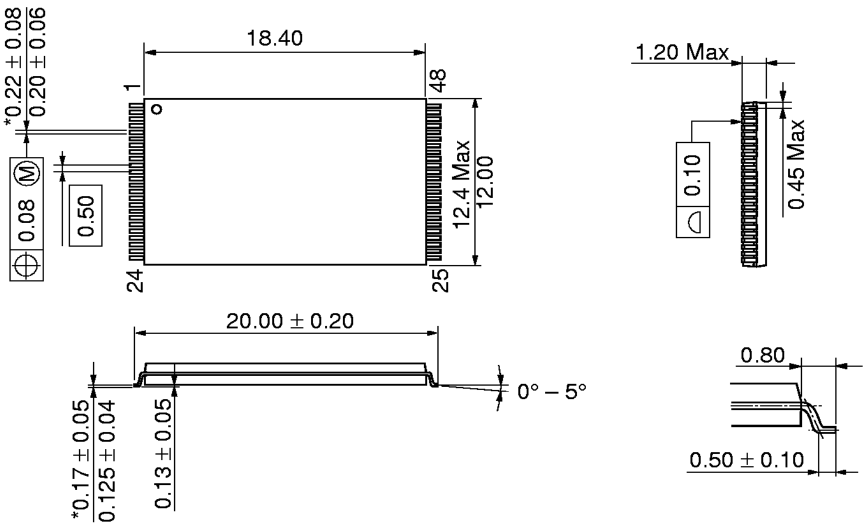
Prohibit the Command except Command Definition

HN29W25611 is prohibited the command except command definition. If the command except command definition is wrote into the device, the data in memory may be damaged by it. No command write except the status transition sequence.

Package Dimensions

HN29W25611T Series (TFP-48D)

Unit: mm



Hitachi Code	TFP-48D
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.26 g

*Dimension including the plating thickness
Base material dimension

Cautions

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