A Cirrus Logic Company

CS7870 CS7875

12-Bit, 100 kHz, Sampling A/D Converters

Features

- Monolithic CMOS A/D Converter
  - 2 µs Track/Hold Amplifier
  - 8 µs A/D Converter
  - 3 V Voltage Reference
  - Internal Clock
  - Parallel, Serial and Byte Outputs
- 12-Bit ADC and Reference Accuracy
  - Linearity: 0.5 LSB
  - SNR: 73 dB
- Input Ranges
  - ±3 V for CS7870
  - 0 to +5 V for CS7875
- Low Power: 75 mW

General Description

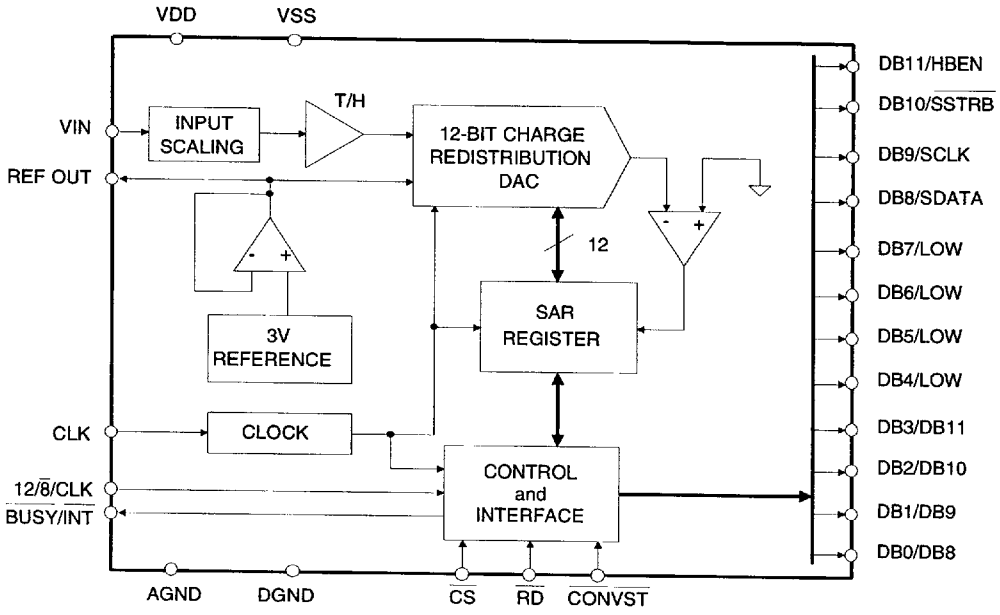
The CS7870 and CS7875 are complete monolithic CMOS analog-to-digital converters providing 100kHz throughput. The capacitive DAC has been calibrated at the factory to ensure 12-bit performance.

The CS7870/CS7875 have a high speed digital interface with three-state data outputs and standard control inputs allowing easy interfacing to common microprocessors and digital signal processors. Conversion results are available in either 12-bit parallel, two 8-bit bytes, or serial data.

The CS7870/CS7875 are available in a 24-pin, 0.3" plastic dual-in-line package (PDIP), and a 28-pin PLCC package.

The CS7870/CS7875 are pin compatible replacements for the AD7870/7875 with equal or better performance.

ORDERING INFORMATION: Page 23



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ANALOG CHARACTERISTICS (V_{DD} = +5V±5%; V_{SS} = -5V±5%; AGND = DGND = 0V; CLK = 2.5 MHz, unless otherwise specified. T_A = T_{MIN} to T_{MAX})

Parameter*		Symbol	CS7870-K Min	CS7870-K Typ	CS7870-K Max	CS7875-K Min	CS7875-K Typ	CS7875-K Max	Units
Specified Temperature Range	(Note 1)			0 to +70			0 to +70		°C
Dynamic Performance	***(Note 2)***								
Signal-to-Noise-and-Distortion	(Note 3)	SINAD	70	72.6	-	70	71.8	-	dB
Signal-to-Noise Ratio		SNR	70	72.8	-	70	72	-	dB
Total Harmonic Distortion	(Note 4)	THD	-80	-85	-	-75	-77	-	dB
Spurious-Free-Dynamic-Range	(Note 4)	SFDR	-80	-85	-	-75	-78	-	dBc
Intermodulation Distortion	(Note 5)	IMD							
Second Order Terms			-80	-88	-	-75	-78	-	dBc
Third Order Terms			-80	-88	-	-75	-88	-	dBc
Accuracy									
Integral Non-Linearity		INL	-	0.5	1.0	-	0.7	2.0	LSB
Differential Non-Linearity		DNL	-	0.5	1.0	-	0.5	1.0	LSB
No Missing Codes		NMC		Guaranteed			Guaranteed		
Unipolar Offset Error	(CS7875)	VOS_U				-	1.0	3.0	LSB
Bipolar Zero Error	(CS7870)	VOS_B	-	0.5	1.0				LSB
Positive Full Scale Error	(Note 6)	FSE_P	-	2.0	5.0	-	5.0	10.0	LSB
Bipolar Negative Full Scale Error (CS7870)	(Note 6)	FSE_N	-	2.0	5.0				LSB
Analog Input									
Input Voltage Range		V_{IN}	-3	-	+3	0	-	+5	V
Input Current			-	-	500	-	-	500	µA
Aperture Delay		t_{apd}	-	25	-	-	25	-	ns
Aperture Jitter		t_{apj}		100	-	-	100	-	ps

Notes:
1. All parameters guaranteed by design, test, and/or characterization.
2. V_{IN} = ±3Vpp for CS7870, and 0V to +5V for CS7875.
3. V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 100kHz. Typically 71.5dB for 10kHz<V_{IN}<50kHz.
4. V_{IN} = 10kHz Sine Wave, f_{SAMPLE} = 100kHz. Typically -80dBc for 0<V_{IN}<50kHz.
5. fa = 9kHz, fb = 9.8kHz, f_{SAMPLE} = 100kHz.
6. Measured with respect to internal reference and includes bipolar offset error.

* Parameter definitions are given at the end of this datasheet prior to the package outline information.

ANALOG CHARACTERISTICS (Continued)

Parameter	Symbol	CS7870-K Min	CS7870-K Typ	CS7870-K Max	CS7875-K Min	CS7875-K Typ	CS7875-K Max	Units
Specified Temperature Rnage			0 to +70			0 to +70		°C
Reference Output								
Output Voltage	V_R	2.99	-	3.01	2.99	-	3.01	V
REF OUT Tempco		-	-	60	-	-	60	ppm/°C
Load Regulation (Note 7)	$\Delta V_R/\Delta I$	-	0.6	1	-	0.6	1	mV
Output Noise Voltage	eN	-	100	-	-	100	-	μV_{rms}
Output Current Drive Source Current	I_{SOURCE}	-	500	-	-	500	-	µA
Sink Current	I_{SINK}	-	500	-	-	500	-	µA
Conversion & Throughput								
Conversion Time	t_{conv}							
External Clock (CLKIN = 2.5 MHz)		-	-	8	-	-	8	µs
Internal Clock		7	-	9	7	-	9	µs
Acquisition Time	t_{acq}	-	-	2	-	-	2	µs
Throughput	f_{tp}	100	-	-	100	-	-	kHz
Power Supplies								
Positive Supply Current @ + 5.0V	I_{DD}	-	9	11	-	9	11	mA
Negative Supply Current @ -5.0V	I_{SS}	-	6	8	-	6	8	mA
Power Dissipation	PD	-	75	95	-	75	95	mW

Notes: 7. Reference Load Current Change (0-500 µA). Reference Load should not be changed during conversion.

LSB	%FS	ppm FS	mV
0.25	0.0061	61	0.37
0.50	0.0122	122	0.73
1.00	0.0244	244	1.46
2.00	0.0488	488	2.92
4.00	0.0976	976	5.86

CS7870 Unit Conversion Factors: (V_{IN} = ±3V)

LSB	%FS	ppm FS	mV
0.25	0.0061	61	0.31
0.50	0.0122	122	0.61
1.00	0.0244	244	1.22
2.00	0.0488	488	2.44
4.00	0.0976	976	4.88

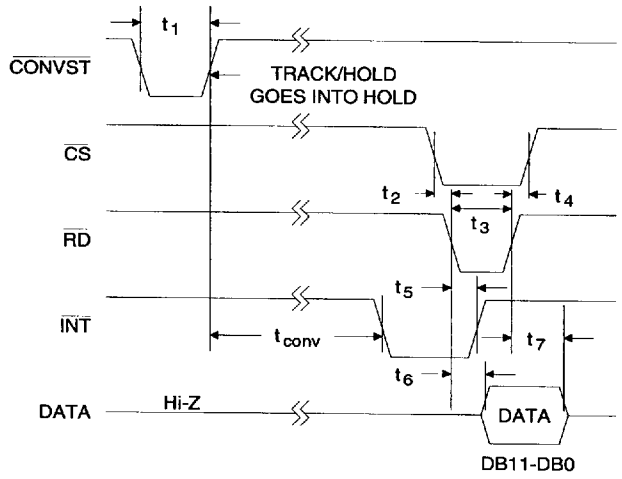
CS7875 Unit Conversion Factors: (V_{IN} = 0 to 5V)

SWITCHING CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}; V_{DD} = +5V±5%, V_{SS} = -5V±5%; AGND = DGND = 0V, (Note 8))

Parameter		Symbol	CS7870-K Min	CS7870-K Typ	CS7870-K Max	CS7875-K Min	CS7875-K Typ	CS7875-K Max	Units
Specified Temperature Range				0 to +70			0 to +70		°C
CLKIN	Period	t_{clk}	370	-	-	370	-	-	ns
CLKIN	Low Time	t_{clkl}	0.4	-	0.6	0.4	-	0.6	MCC*
	High Time	t_{clkh}	0.4	-	0.6	0.4	-	0.6	MCC*
			160	-	-	160	-	-	ns
Rise Times	Any Digital Input	t_{rise}	-	-	20	-	-	20	ns
	Any Digital Output	t_{rise}	-	20	-	-	20	-	ns
Fall Times	Any Digital Input	t_{fall}	-	-	20	-	-	20	ns
	Any Digital Output	t_{fall}	-	20	-	-	20	-	ns
Mode 1 Timing									
Conversion Time		t_{conv}	-	-	20	-	-	20	MCC*
CONVST Pulse Width		t_1	95	-	-	95	-	-	ns
CS to RD Setup Time		t_2	0	-	-	0	-	-	ns
RD Pulse Width		t_3	60	-	-	60	-	-	ns
CS to RD Hold Time		t_4	0	-	-	0	-	-	ns
RD to INT Delay		t_5	-	-	70	-	-	70	ns
Data Access Time after RD	(Note 9)	t_6	-	-	57	-	-	57	ns
Output Float Delay RD Rising to Hi-Z	(Note 10)	t_7	5	-	95	5	-	95	ns
HBEN to RD Setup Time		t_8	95	-	-	95	-	-	ns
RD Inactive to HBEN Hold Time		t_9	0	-	-	0	-	-	ns
Serial Clock Timing									
SSTRB Falling Time to SCLK Falling	(Note 11)	t_{10}	100	-	-	100	-	-	ns
Serial Clock	Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
	Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SCLK rising to Valid Data	(Note 12)	t_{12}	-	-	135	-	-	135	ns
SCLK rising to SSTRB		t_{13}	20	-	100	20	-	100	ns
Bus relinquish time after SCLK		t_{14}	10	-	100	10	-	100	ns

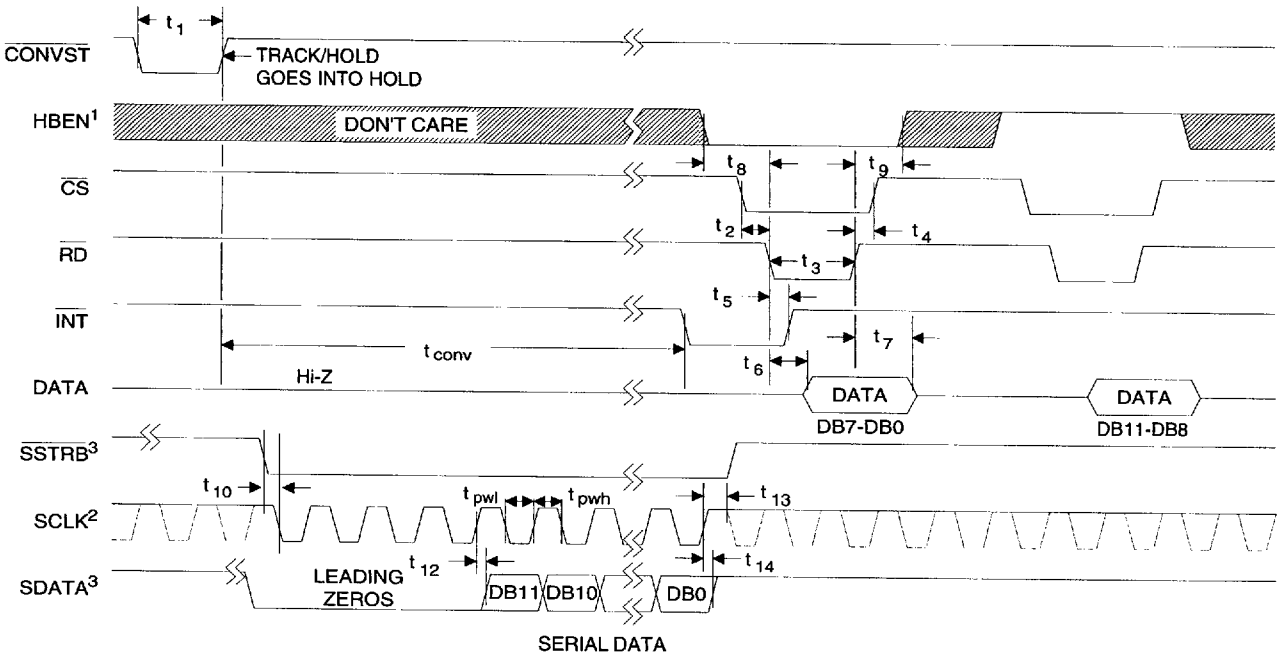
*MCC = Master Clock Cycles, 1 MCC = t_{clk}

Notes:
8. All input signals are specified with $t_{rise} = t_{fall}$ = 5ns (10% to 90% of 5V) and timed from a voltage level of 1.6V.
9. Measured with the load circuits of Figure 5 and defined as the time required for an output to cross 0.8V or 2.4V.
10. Defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 6.
11. t_{10} = MCC/2 - 25ns. t_{10} = 175ns for t_{clk} = 400ns.
12. CL = 35pF. SDATA will drive higher capacitive loads but this will add to t_{12}.



Note: 12/8/CLK = +5V.

Figure 1. Mode 1 Timing Diagram, 12-Bit Parallel Read



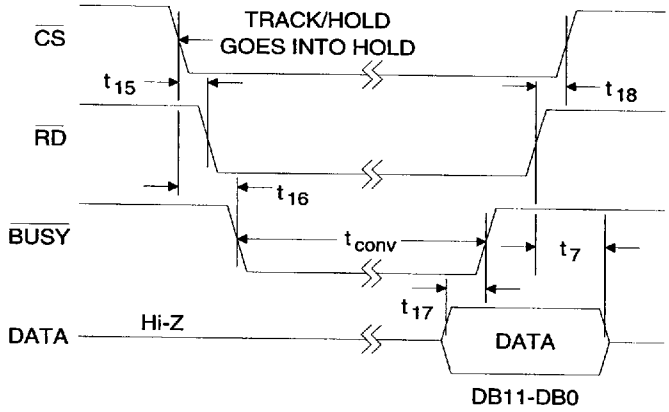
Notes:
1. Times t_2, t_3, t_4, t_8, and t_9 are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when 12/8/CLK = -5V
   Noncontinuous when 12/8/CLK = 0V
   External 2kΩ pull-up resistor.
3. External 4.7kΩ pull-up resistor.

Figure 2. Mode 1 Timing Diagram, Byte or Serial Read

SWITCHING CHARACTERISTICS (Continued)

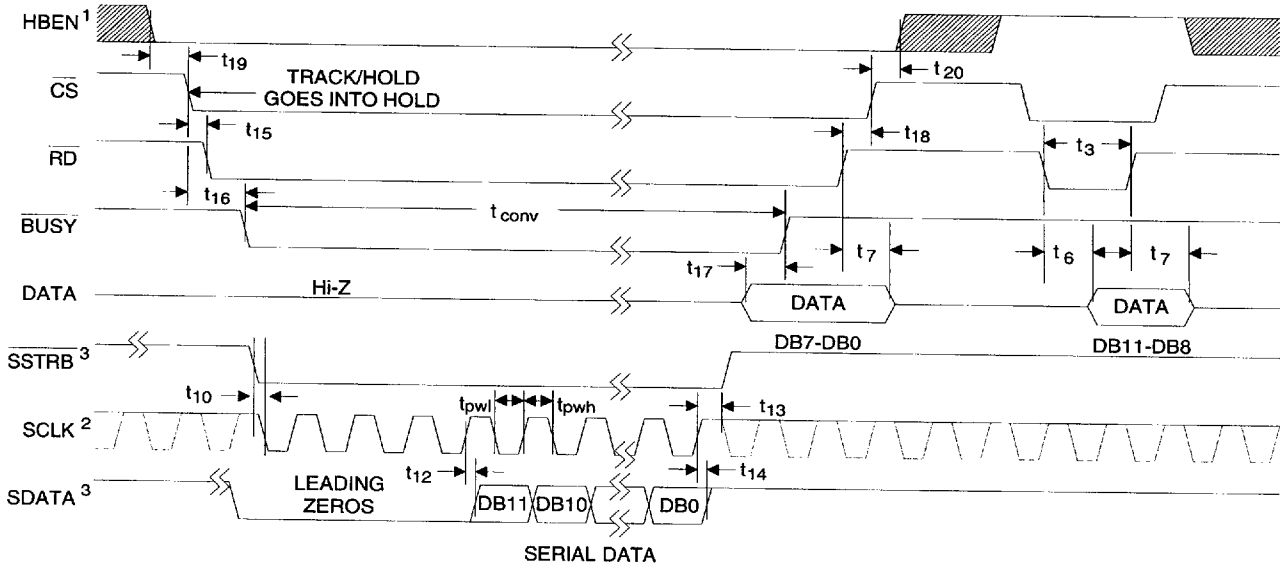
Parameter	Symbol	CS7870-K Min	CS7870-K Typ	CS7870-K Max	CS7875-K Min	CS7875-K Typ	CS7875-K Max	Units
Specified Temperature Range			0 to +70			0 to +70		°C
Mode 2 Timing								
Conversion Time	t_{conv}	-	-	25	-	-	25	MCC*
CS to RD Setup Time	t_{15}	60	-	-	60	-	-	ns
CS to Busy Delay	t_{16}	-	-	120	-	-	120	ns
Data Setup Time	t_{17}	200	-	-	200	-	-	ns
CS to RD Hold Time	t_{18}	0	-	-	0	-	-	ns
Output Float Delay RD Rising to Hi-Z(Note 10)	t_7	5	-	95	5	-	95	ns
HBEN to CS Setup Time	t_{19}	0	-	-	0	-	-	ns
HBEN to CS Hold Time	t_{20}	0	-	-	0	-	-	ns
RD Pulse Width	t_3	60	-	-	60	-	-	ns
Data Access Time after RD (Note 9)	t_6	-	-	57	-	-	57	ns
Serial Clock Timing								
Serial Clock Pulse Width High	t_{pwh}	0.4	-	0.6	0.4	-	0.6	MCC*
Pulse Width Low	t_{pwl}	0.4	-	0.6	0.4	-	0.6	MCC*
SSTRB Falling to SCLK Falling (Note 11)	t_{10}	100	-	-	100	-	-	ns
SCLK rising to Valid Data (Note 12)	t_{12}	-	-	135	-	-	135	ns
SCLK rising to SSTRB	t_{13}	20	-	100	20	-	100	ns
Bus relinquish time after SCLK	t_{14}	10	-	100	10	-	100	ns

*MCC = Master Clock Cycles, 1 MCC = t_{clk}



Note: 12/$\overline{8}$/CLK = +5V.

Figure 3. Mode 2 Timing Diagram, 12-Bit Parallel Read



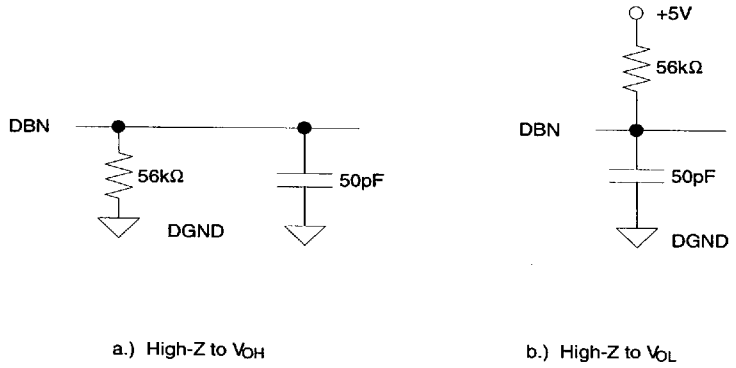
Notes:
1. Times t_{15}, t_{18}, t_{19}, and t_{20} are the same for a high byte read as for a low byte read.
2. Continuous SCLK (Dashed line) when 12/$\overline{8}$/CLK = -5V
   Noncontinuous when 12/$\overline{8}$/CLK = 0V
   External 2kΩ pull-up resistor.
3. External 4.7kΩ pull-up resistor.

Figure 4. Mode 2 Timing Diagram, Byte or Serial Read

DIGITAL CHARACTERISTICS (T_A = T_{MIN} to T_{MAX}: V_{DD} = 5V±5%; V_{SS} = -5V±5%)

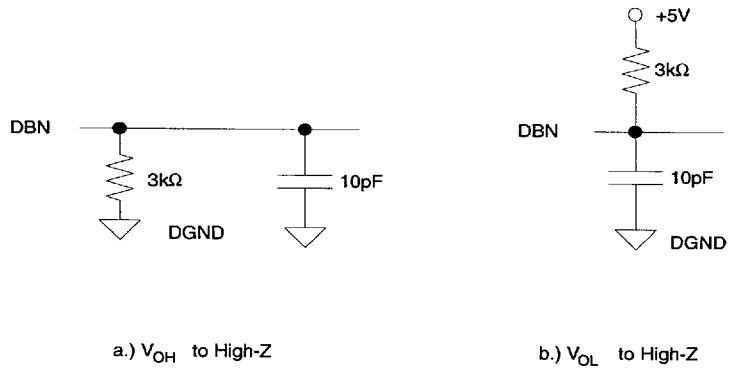
Parameter	Symbol	Min	Typ	Max	Units
Logic Inputs					
High-Level Input Voltage	V_{IH}	3.3	-	-	V
Low-Level Input Voltage	V_{IL}	-	-	0.8	V
Input Leakage Current	I_{in}	-	-	10	µA
Input Capacitance	C_{in}	-	-	10	pF
Logic Outputs					
High-Level Output Voltage (Note 13)	V_{OH}	4.0	-	-	V
Low-Level Output Voltage (Note 14)	V_{OL}	-	-	0.4	V
DB11-DB0 Floating State Leakage Current	I_{OZ}	-	-	25	µA
DB11-DB0 Output Capacitance	C_{out}	-	-	15	pF

Notes: 13. I_{SOURCE} = -40 µA
14. I_{SINK} = 1.6 mA



a.) High-Z to V_{OH} b.) High-Z to V_{OL}

Figure 5. Load Circuits for Access Time



a.) V_{OH} to High-Z b.) V_{OL} to High-Z

Figure 6. Load Circuits for Output Float Delay

RECOMMENDED OPERATING CONDITIONS (AGND, DGND = 0V. All voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
Positive Analog Supply		VA+	4.75	5.0	5.25	V
Negative Analog Supply		VA-	-4.75	-5.0	-5.25	V
Analog Input Voltage	CS7870	V_{IN}	-3	-	+3	V
	CS7875	V_{IN}	0	-	+5	V
12/8/CLK Input Voltage Range			VA-, 0V, VA+			V
CLKIN Input Voltage Range			0	-	VA+	V
Other Digital Input Voltage Ranges			0	-	VA+	V
AGND to DGND Voltage Differential			-	-	10	mV
Eternal Clock Frequency			-	2.5	-	MHz

ABSOLUTE MAXIMUM RATINGS (AGND = 0V, All voltages with respect to ground)

Parameter		Symbol	Min	Typ	Max	Units
Positive Analog Supply		VA+	-0.3	-	6.0	V
Negative Analog Supply		VA-	0.3	-	-6.0	V
Analog Input Voltage		V_{IN}	(VA-)-0.3	-	(VA+)+0.3	
12/8/CLK Input Voltage Range			(VA-)-0.3	-	(VA+)+0.3	V
CLKIN Input Voltage Range			(VA-)-0.3	-	(VA+)+0.3	V
Other Digital Input Voltage Ranges			-0.3	-	(VA+)+0.3	V
REF OUT Current			-	-	10	mA
Sustained Digital Output Current			-	-	5	mA
AGND to DGND Voltage Differential			-	-	100	mV
Operating Temperature Range	CS7870/75-KP/KL		0	-	+70	°C
Storage Temperature Range			-65	-	+150	°C
Lead Solder Temperature			-	-	+300	°C

* WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

NOTE: Temperatures specified define ambient conditions in free-air during test and do not refer to the junction temperature of the device.

GENERAL DESCRIPTION

The CS7870 and CS7875 are complete 12-bit 100 kSPS sampling ADCs, utilizing a successive approximation architecture. Factory calibration ensures 12-bit conversion accuracy over industrial and military temperature ranges. The CS7870 analog input range is ±3 V (0 V to +5 V for the CS7875), with the output data provided in parallel, byte or serial formats. The internal capacitor array DAC acts as an inherent sample-and-hold, and forms the heart of the CS7870/CS7875. The on-chip +3 V reference is available at the REFOUT pin. An on-board 2.5 MHz clock oscillator is also available.

OPERATIONAL OVERVIEW

Track-and-Hold Operation

Track-and-hold operation within the CS7870/CS7875 is transparent to the user. The capacitor array DAC acts as the hold capacitor. During tracking mode all elements of the capacitor array DAC are switched to the analog input for charging. The load capacitance of the entire array during tracking mode is typically 5 pF. The input bandwidth of the track-and-hold is typically 2 MHz. The ADC goes into hold mode on the rising edge of $\overline{\text{CONVST}}$.

Capacitor Array DAC Calibration

To achieve 12-bit accuracy from the capacitor array DAC, the CS7870/CS7875 uses a novel calibration scheme. Each bit capacitor consists of several capacitors that are trimmed to optimize the overall bit weighting with an internal resolution of 14-bits, resulting in nearly ideal differential and integral linearity.

The calibration coefficients for the capacitive bit weights are stored in an on-chip EEPROM during the factory calibration. When the converter is subsequently powered-up these coefficients are applied to the capacitor array DAC. With the DAC calibration provided automatically on power-up, it is unnecessary to calibrate the DAC before using the converter. Additionally, the low temperature coefficient of the capacitor array easily maintains 12-bit accuracy over the full temperature range without recalibration.

Reference Operation

The reference voltage is available at the REF OUT pin and is capable of sourcing 500 mA to peripheral devices. This pin should normally be left open. If used, it can be directly decoupled to AGND with up to 50 pF of capacitance, or through a 200 W resistor to a +10 mF tantalum capacitor. The reference voltage is calibrated on power-up, with full accuracy achieved after 1.1 sec.

Analog Input

The CS7870 provides a ±3 V analog input voltage range (0 V to +5 V for the CS7875). The equivalent analog input circuit is illustrated in Figure 7 (shown in track mode). During hold mode the input impedance to the device is typically 10 MΩ, and the various elements of the capacitor array DAC are connected to either AGND or VREF. In switching back from hold mode to track mode, some elements in the capacitor array must be charged by the analog input. For the CS7870, the worst case charging current occurs when the analog input changes from +3V to -3V (+5V to 0V for the CS7875).

To ensure that the capacitor array DAC has settled to within 0.25 LSB during the allowed acquisition time, the source resistance should be less than 4 kΩ.

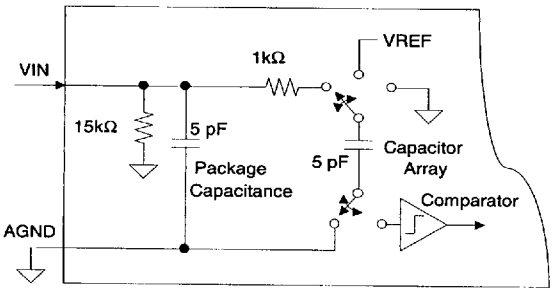


Figure 7. Analog Input Model (Track Mode).

Output Coding

The digital output coding ...

CS7870 Input	2's Complement Output		
+3V	0111	1111	1111
0V	0000	0000	0000
-3V	1000	0000	0000

CS7875 Input	Binary Output		
+5V	1111	1111	1111
+2.5V	0111	1111	1111
0V	0000	0000	0000

High-Speed System Clock

The CS7870/CS7875 employs a high-speed clock (typically 2.5 MHz) to control internal operations. This high-speed clock can be generated internally with the on-board oscillator, or it can be supplied from an external CMOS source. Connecting a CMOS clock signal to the CLKIN pin allows the converter to operate from an external clock. Alternatively, connecting the CLKIN pin to VA- activates the internal clock oscillator.

External Clock.....CLKIN = External Clock Source
Internal Clock ... CLKIN = VA-

Digital Output Formats

The CS7870/CS7875 provides three digital output formats. These include 12-bit parallel, two 8-bit bytes, and serial modes. The output data format is controlled by the level applied to the 12/$\overline{8}$/CLK pin.

Figure 8 shows the schematic for the CS7870/CS7875 in 12-bit parallel mode. The twelve bits of data are output simultaneously on DB11/(MSB) through DB0 (LSB)..

12/$\overline{8}$/CLK	Digital Outputs
+VA	12-Bit Parallel
GND	Byte; Serial w/Non-Continuous SCLK
-VA	Byte; Serial /Continuous SCLK

In byte mode, two 8-bit read operations (four leading zeros with 4 data bits ... plus 8 more data bits) are required to collect the data as shown in Figure 9. In byte mode, the DB11/HBEN pin defers to the HBEN function, selecting the high or low byte of data to be read from the ADC. The lower eight bits of data are placed on the data bus when HBEN is held low. To access the four MSBs of data, HBEN must be held high. The 4 MSBs of the 12-bit data word are right justified with zeros in the upper nibble of the high byte.

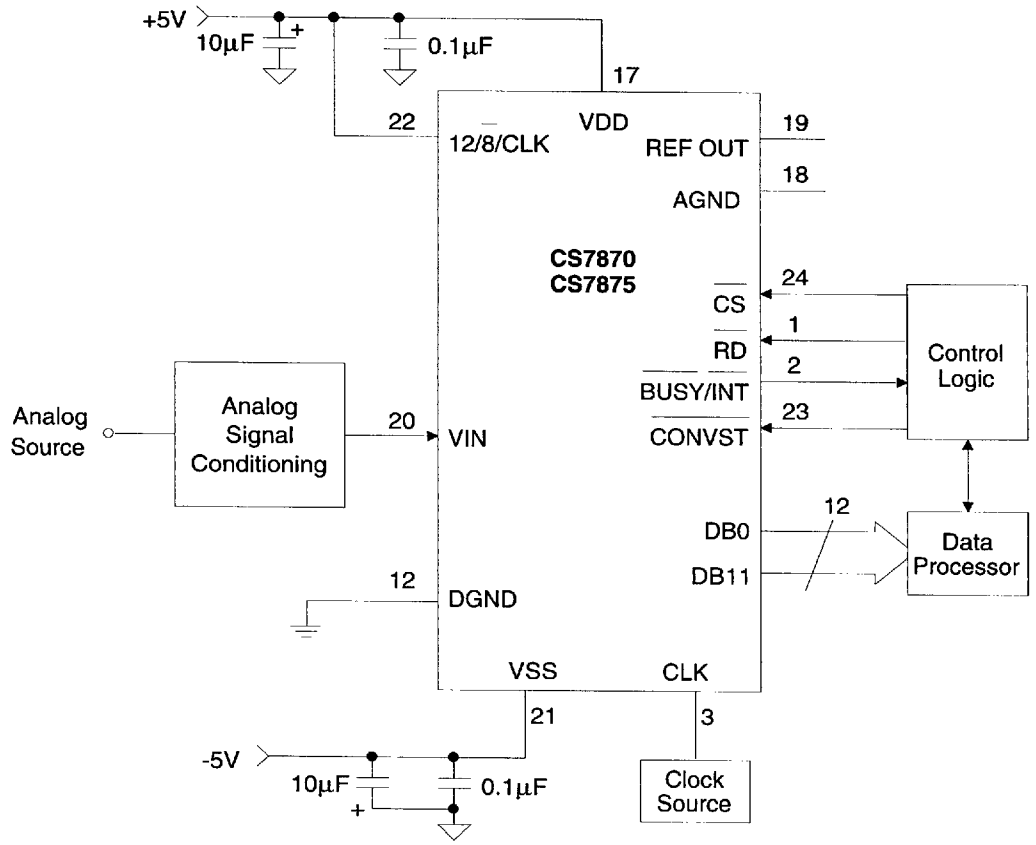


Figure 8. System Connection Diagram: Parallel Data Format

In serial mode, DB8/SDATA, DB9/SCLK and DB10/$\overline{SSTRB}$ defer to their serial functions. The serial strobe pin $\overline{SSTRB}$ provides a framing signal for serial data. Serial data is available at the SDATA pin when $\overline{SSTRB}$ falls low. $\overline{SSTRB}$ falls low within three clock cycles of $\overline{CONVST}$. A total of sixteen bits (four leading zeros and twelve data bits starting with the MSB) are clocked out on the SDATA pin on the rising edge of SCLK. The data bits become valid no more than t_{12} after the rising edge of SCLK. $\overline{SSTRB}$ goes low during data transmission and automatically returns high when the LSB has been clocked out on the SDATA line. Serial data operation is identical for MODE 1 and MODE 2 timing control (see next two sections). For serial operation, 0V on the 12/$\overline{8}$/CLK pin causes the serial clock to run only when data is being clocked out of the device; SCLK goes high after data transmission is completed. If the 12/$\overline{8}$/CLK is connected to -VA, the SCLK output will run continuously, independent of data transmission.

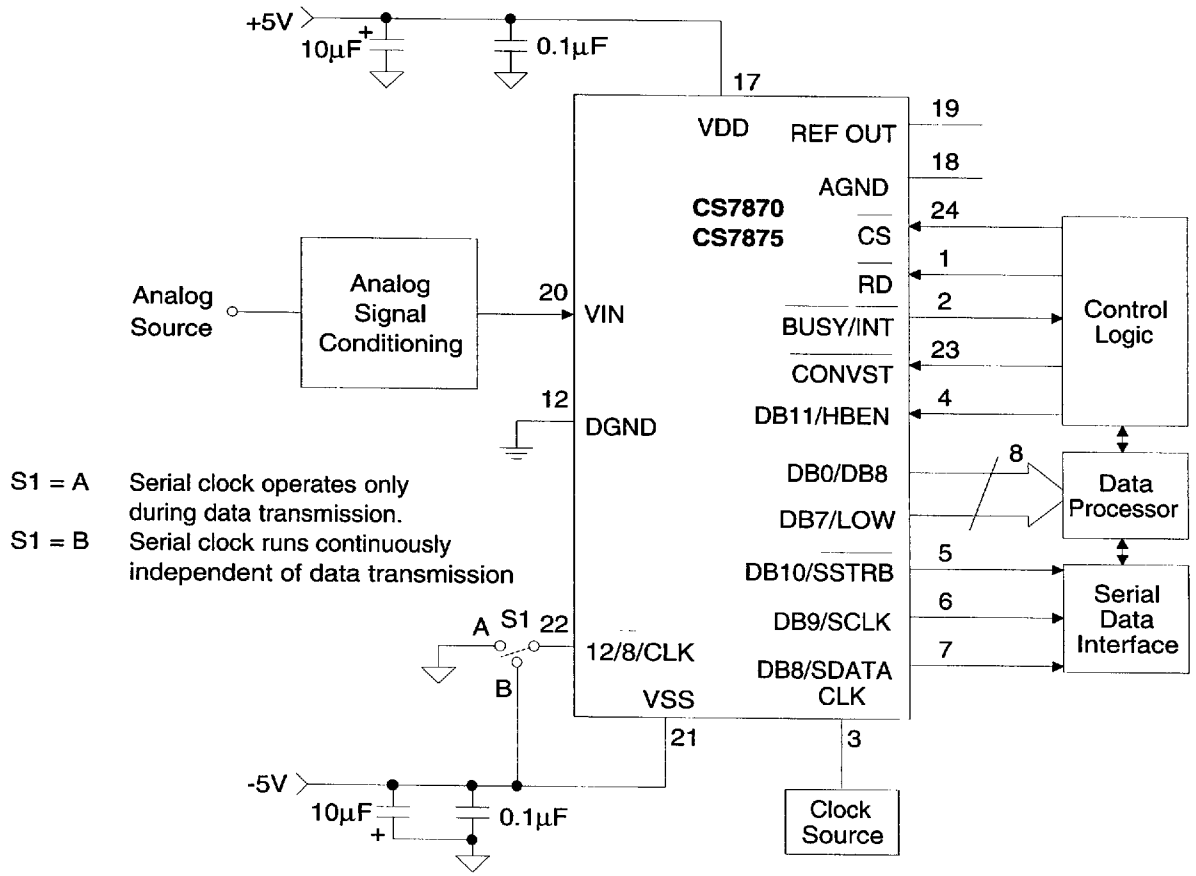


Figure 9. System Connection Diagram: Serial and Byte Data format

MODE 1 Operation

The $\overline{\text{CONVST}}$ signal is used to put the device into hold mode and initiate a conversion. At the end of conversion the device returns to it's tracking mode. MODE 1 timing is primarily used in DSP type applications where precise control of $\overline{\text{CONVST}}$ timing is required.

Conversion begins on the rising edge of $\overline{\text{CONVST}}$ provided that $\overline{\text{CS}}$ is high. The BUSY/$\overline{\text{INT}}$ line performs the $\overline{\text{INT}}$ function and can be used to interrupt the microprocessor. $\overline{\text{INT}}$ is normally high and goes low at the end of conversion. The ADC begins to acquire the analog input when $\overline{\text{INT}}$ goes low. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC, and also resets $\overline{\text{INT}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low for the ADC to operate correctly in this mode. Data cannot be read during a conversion cycle because the output data latches are disabled while a conversion is in progress.

MODE 1 - 12-Bit Parallel Read

Figure 10 shows the MODE 1 timing diagram for 12-bit parallel operation (12/$\overline{8}$/CLK = +VA). A data read operation performed at the end of conversion will read all twelve bits of data at the same time.

MODE 1 - Byte Read

Figure 11 shows the MODE 1 timing diagram for byte operation. At the end of conversion when INT goes low, either the low byte or the high byte of data can be read, depending on the status of HBEN. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{INT}}$ high.

MODE 1 - Serial Read

The MODE 1 timing diagram for serial operation is shown in Figure 12. Conversion begins on the falling edge of $\overline{\text{CONVST}}$, and data is clocked out on SDATA immediately upon the falling edge of $\overline{\text{SSTRB}}$. The data is output as four leading zeroes followed by the twelve data bits with the MSB first. The first zero should be latched into the external receiving circuitry on the first falling edge of SCLK after $\overline{\text{SSTRB}}$ goes low. A total of sixteen falling SCLK edges will latch all sixteen bits of output data. $\overline{\text{SSTRB}}$ automatically returns high after the last bit of data has been clocked out of the device.

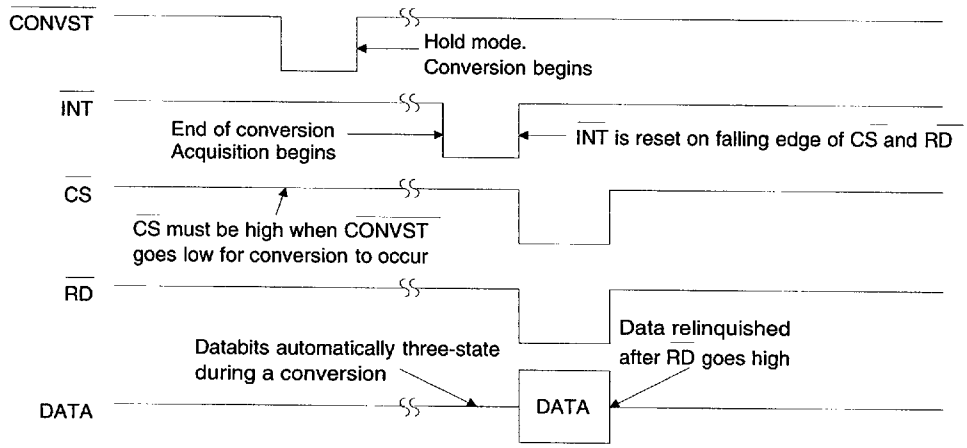
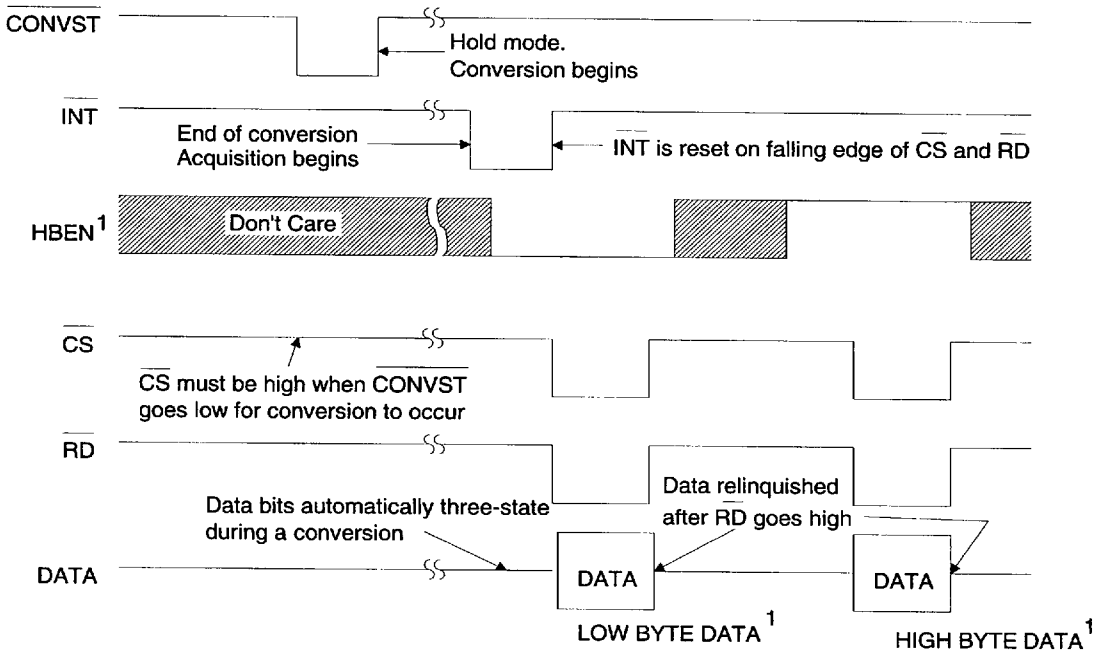


Figure 10. Mode 1 Timing Diagram, 12-bit Parallel Read



Note: 1. In the above diagram HBEN is exercised to read the low byte first (DB7-DB0) and then the high byte (DB11-DB8). To change the order in which the bytes are read, simply invert the HBEN signal shown above.

Figure 11. Mode 1 Timing Diagram, Byte Read

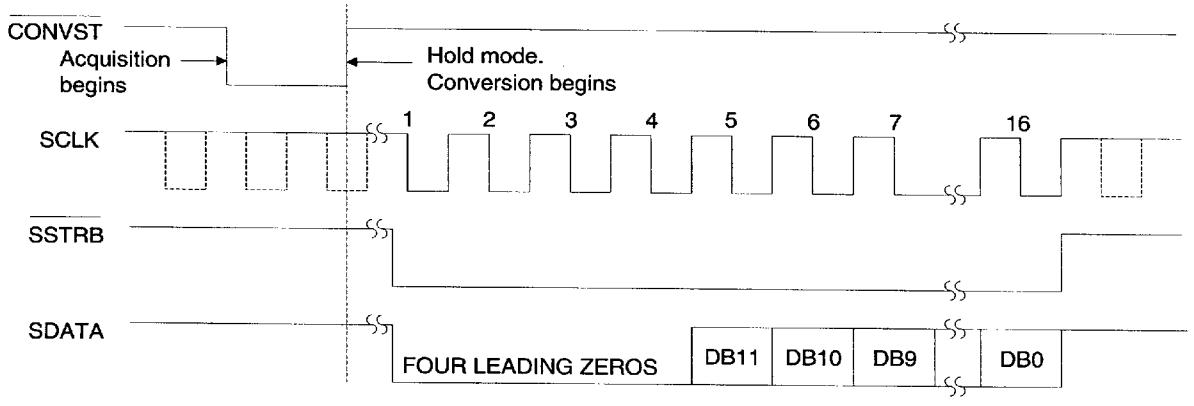


Figure 12. Mode 1 Timing Diagram - Serial Read

MODE 2 Operation

Mode 2 operation allows the ADC conversion to be initiated by a read operation from a µC. The $\overline{BUSY}$ signal can be used in this mode to halt µC operations by placing the µC in a WAIT state until the conversion is complete. This avoids having to handling interrupts and timing delays , assuring that the conversion cycle is complete before any attempted data read.

In this mode, $\overline{CONVST}$ must be held permanently low. Bringing $\overline{CS}$ low (while $\overline{HBEN}$ is low) puts the device into hold mode and initiates a conversion. The $\overline{BUSY}/\overline{INT}$ pin defers to the $\overline{BUSY}$ function such that $\overline{BUSY}$ goes low at the start of conversion and returns high at the end of conversion.

MODE 2 - 12-Bit Parallel Read

The MODE 2 timing diagrams for the parallel data output format are shown in Figure 13. This mode of operation forces the µC into a WAIT state until the conversion has been completed. It removes the risk of inadvertently reading invalid data before the conversion cycle has been completed.

MODE 2 - Byte Read

Figure 14 shows the timing diagram for byte operation in MODE 2. Since $\overline{HBEN}$ must be low to initiate a conversion, the lower byte of data will be accessed first during the two-byte read operation. This is followed by a second byte read operation (with $\overline{HBEN}$ high) to complete the data transfer.

MODE 2 - Serial Read

The timing diagram for MODE 2 serial operation is shown in Figure 15. The device goes into hold mode on the falling edge of $\overline{CS}$ and conversion begins when $\overline{BUSY}$ goes low. The data is clocked out similarly as for MODE 1 serial operation. Upon clocking of the final data bit $\overline{BUSY}$ returns high indicating end of conversion.

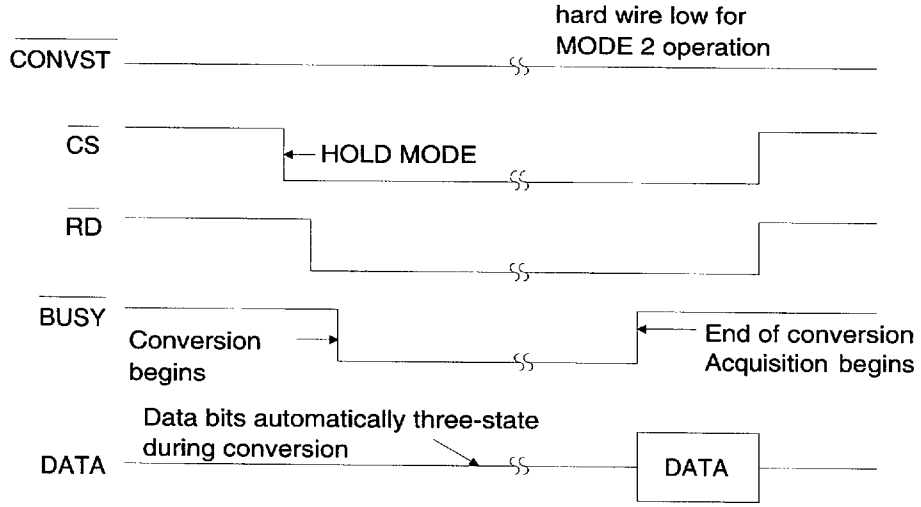


Figure 13 Mode 2 Timing Diagram, 12-bit Parallel Read

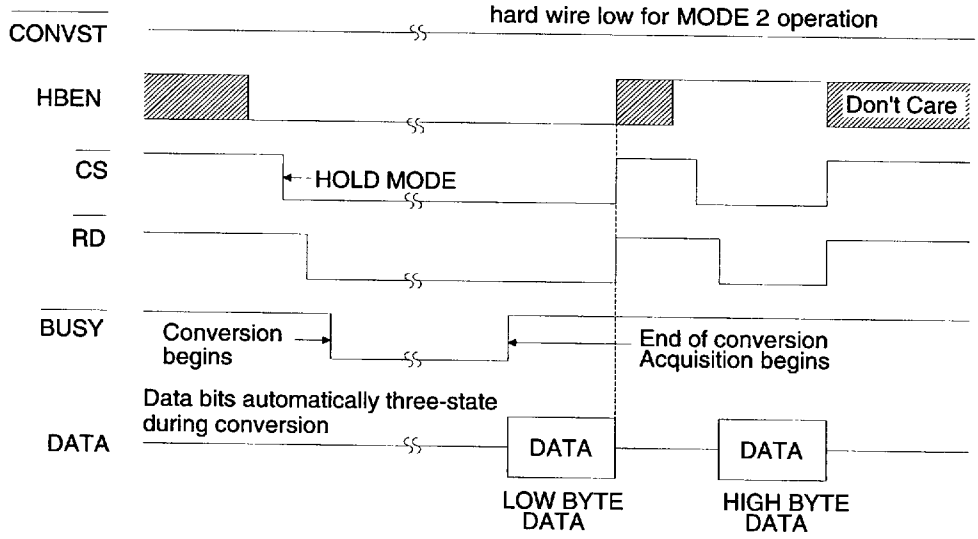


Figure 14. Mode 2 Timing Diagram, 12-bit Byte Read

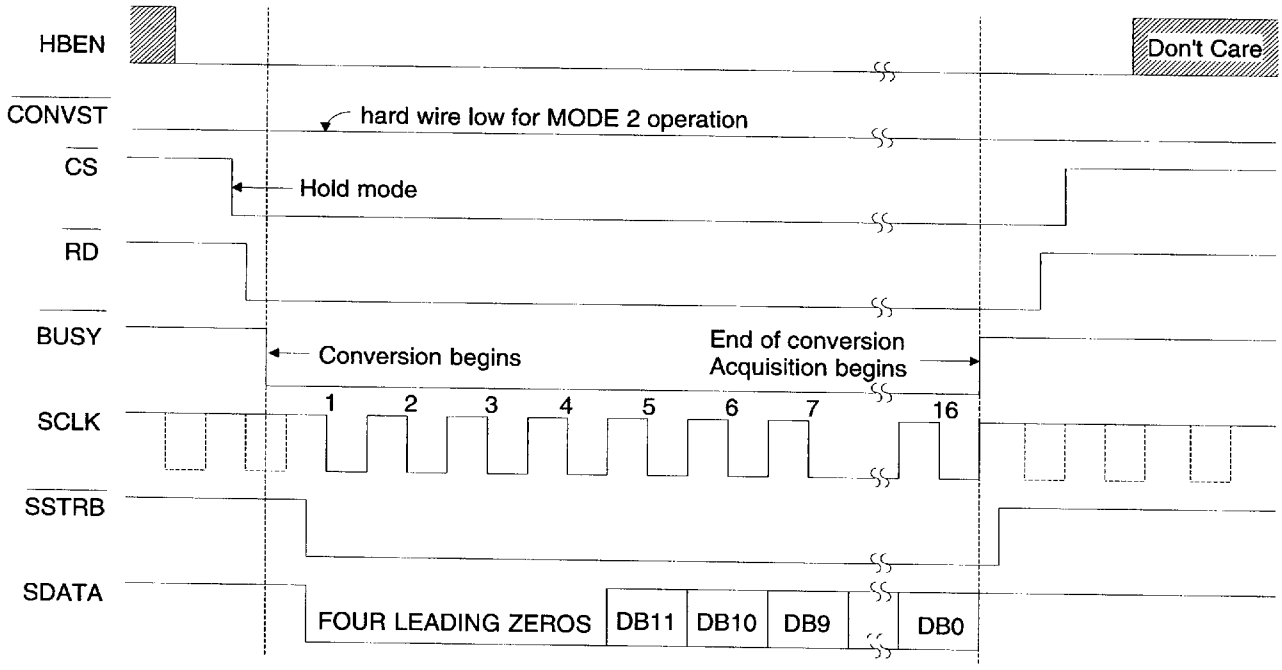


Figure 15. Mode 2 Timing Diagram, Serial Read

STAND-ALONE OPERATION

The CS7870/CS7875 supports stand-alone conversion when used in MODE 2 parallel interface operation as shown in Figure 16. Conversion is initiated by pulse to the $\overline{CS}$ input of the ADC. The duration of the pulse must be longer than the ADC conversion time. The $\overline{BUSY}$ output drives the $\overline{RD}$ input and data is latched on the rising edge of $\overline{BUSY}$ to an external latch.

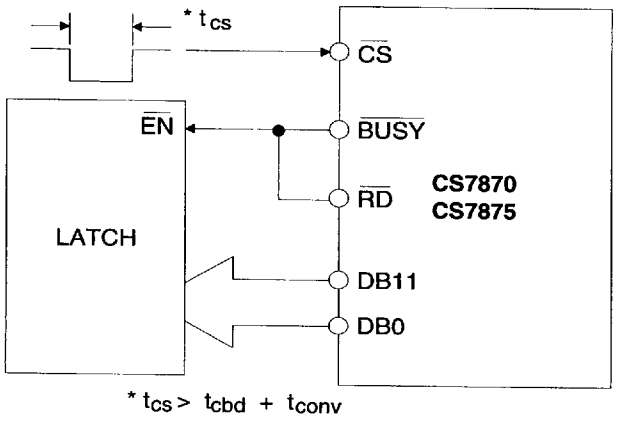


Figure 16. Stand-Alone Operation

Power Supplies, AGND, and DGND

Figure 8 illustrates the recommended power supply decoupling scheme with a 0.1µF ceramic and a +10µF tantalum capacitor for both the VA+ and the VA- pins. The capacitors should be located as close as practical to the supply pins. AGND is the power supply current return, and is also the preferred ground reference for the decoupling capacitors.

Typically a low-impedance ground plane is used around and under the ADC, with connections to both AGND and DGND. If a split ground is used, DGND is the ground reference for any digital circuits that follow the CS7870/CS7875. When split grounds are used, the AGND to DGND voltage differential should be kept below ±10mV for best operation.

Special Note: The CS7870/7875 employ on-chip memory to store power-up reset calibration data. If the power supply voltage is dropped below 3 V, it is possible that this memory may lose the current calibration data. The ADC's can be reset by switching power off and then back on, to initiate the power-on reset sequence.

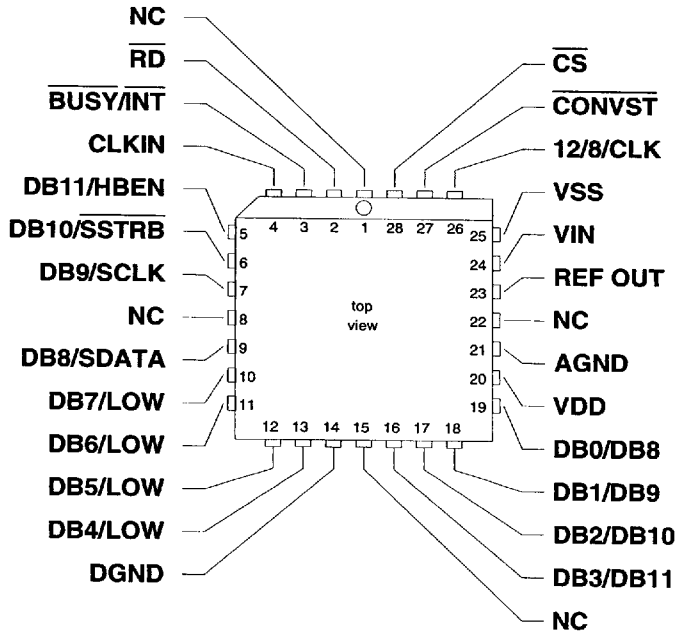
Layout considerations

The CS7870/CS7875 is a high-speed component which requires adherence to standard high-frequency printed circuit board layout techniques to maintain optimum performance. These include proper supply decoupling, minimum length circuit traces, and physical separation of digital and analog components and circuit traces. See the CDB7870/75 evaluation board data sheet for more details.

PIN DESCRIPTIONS

READ	**$\overline{RD}$**	1	24	**$\overline{CS}$**	CHIP SELECT
BUSY/INTERRUPT	**$\overline{BUSY/INT}$**	2	23	**$\overline{CONVST}$**	CONVERT START
CLOCK INPUT	**CLKIN**	3	22	**12/$\overline{8}$/CLK**	DATA OUTPUT FORMAT
DB11/HIGH BYTE ENABLE	**DB11/HBEN**	4	21	**V_{SS}**	NEGATIVE ANALOG SUPPLY
DB10/SERIAL STROBE	**DB10/$\overline{SSTRB}$**	5	20	**V_{IN}**	ANALOG INPUT
DB9/SERIAL CLOCK	**DB9/SCLK**	6	19	**REF OUT**	VOLTAGE REF OUT
DB8/SERIAL DATA	**DB8/SDATA**	7	18	**AGND**	ANALOG GROUND
DATA OUT	**DB7/LOW**	8	17	**V_{DD}**	POSITIVE ANALOG SUPPLY
DATA OUT	**DB6/LOW**	9	16	**DB0/DB8**	DATA OUT
DATA OUT	**DB5/LOW**	10	15	**DB1/DB9**	DATA OUT
DATA OUT	**DB4/LOW**	11	14	**DB2/DB10**	DATA OUT
DIGITAL GROUND	**DGND**	12	13	**DB3/DB11**	DATA OUT

24-Pin Plastic



28-Pin PLCC

Power Supply Connections

V_{DD} – Positive Supply, PIN 17.
+5V±5%.

V_{SS} – Negative Supply, PIN 21.
-5V±5%.

DGND – Digital Ground, PIN 12.
Ground reference for digital circuitry.

AGND – Analog Ground, PIN 18.
Ground reference for track-and-hold, reference and DAC.

Oscillator

CLK – Clock Input, PIN 3.
An external 2.5MHz (CMOS compatible) clock is applied at this pin. Connecting this pin to V_{SS} enables the internal clock oscillator.

Digital Inputs

CS – Chip Select, PIN 24.
Active low logic input. The device is selected when this input is active. With $\overline{CONVST}$ tied low, a new conversion is initiated when $\overline{CS}$ goes low.

RD – Read, PIN 1.
Active low logic input. This input is used in conjunction with $\overline{CS}$ low to enable the data outputs.

12/$\overline{8}$/CLK – Output Mode Selection, PIN 22.
Defines the output data format and serial clock format. With 12/$\overline{8}$/CLK at +5V, the output data format is 12-bit parallel only. With 12/$\overline{8}$/CLK at 0V, either byte or serial data is available and SCLK is not continuous. With 12/$\overline{8}$/CLK at -5V, byte or serial data is again available but SCLK is now continuous.

CONVST – Convert Start, PIN 23.
A low to high transition on this input puts the track-and-hold into its hold mode and starts conversion. This input is asynchronous to the CLK and independent of $\overline{CS}$ and $\overline{RD}$.

Digital Outputs

BUSY/$\overline{INT}$ – Busy/Interrupt, PIN 2.
Active low logic output indicating converter status. See timing diagrams.

DB11/HBEN – Data Bit 11/High Byte Enable, PIN 4.

The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB11 output. When byte data is selected, this pin becomes the HBEN logic input. HBEN is used for 8-bit bus interfacing. When HBEN is low, DB7/LOW to DB0/DB8 become DB7 to DB0. With HBEN high, DB7/LOW to DB0/DB8 are used for the upper byte of data (see Table 1).

DB10/$\overline{\text{SSTRB}}$ – Data Bit 10/Serial Strobe, PIN 5.

The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB10 output. $\overline{\text{SSTRB}}$ provides a strobe or framing pulse for serial data.

DB9/SCLK – Data Bit 9/Serial Clock, PIN 6.

The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB9 output. SCLK is the gated serial clock output derived from the internal or external ADC clock. If 12/$\overline{8}$/CLK is at -5V, then SCLK runs continuously. If 12/$\overline{8}$/CLK is at 0V, then SCLK goes high after serial transmission is complete.

DB8/SDATA – Data Bit 8/Serial Data, PIN 7.

The function of this pin is dependent on the state of the 12/$\overline{8}$/CLK input. When 12-bit parallel data is selected, this pin provides the DB8 output. SDATA is used with SCLK and $\overline{\text{SSTRB}}$ for serial data transfer. Serial data is valid on the falling edge of SCLK while $\overline{\text{SSTRB}}$ is low.

DB7/LOW, DB6/LOW, DB5/LOW, DB4/LOW – Three-state data outputs, PINS 8, 9, 10, 11.

The outputs of these pins are controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB7-DB4. With 12/$\overline{8}$/CLK low or -5V, their function is controlled by HBEN (see Table 1).

DB3/DB11, DB2/DB10, DB1/DB9, DB0/DB8 – Three-state data outputs, PINS 13, 14, 15, 16.

The outputs of these pins are controlled by $\overline{\text{CS}}$ and $\overline{\text{RD}}$. Their function depends on the 12/$\overline{8}$/CLK and HBEN inputs. With 12/$\overline{8}$/CLK high, they are always DB3-DB0. With 12/$\overline{8}$/CLK low or -5V, their function is controlled by HBEN (see Table 1).

HBEN	DB7/LOW	DB6/LOW	DB5/LOW	DB4/LOW	DB3/DB11	DB2/DB10	DB1/DB9	DB0/DB8
HIGH	LOW	LOW	LOW	LOW	DB11/(MSB)	DB10	DB9	DB8
LOW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0/(LSB)

Table 1. Output Data for Byte Interfacing

Analog Output

REF OUT - Voltage Reference Output, PIN 19.

The internal +3V reference is provided at this pin. The external load capability is 500µA. This pin should be left open. If used, it can be directly decoupled to AGND with up to 50pF, or through a 200Ω resistor to a +10µF tantalum and 0.1µF ceramic capacitors. REF OUT settling time is approximately 1.1 sec.

Analog Input

V_{IN} - Analog Input, PIN 20.

The analog input range for the CS7870 is ±3V, ... 0V to +5V for the CS7875.

Ordering Information

Model	Temp (°C)	Tempco (ppm/°C)	SINAD (dB)	INL (LSB)	Package
V_{IN} Range = ±3V					
CS7870-KP	0 to +70	60	72	0.5	24-pin 0.3" PDIP
CS7870-KL	0 to +70	60	72	0.5	28-pin PLCC
V_{IN} Range = 0V to +5V					
CS7875-KP	0 to +70	60	72	0.5	24-pin 0.3" PDIP
CS7875-KL	0 to +70	60	72	0.5	28-pin PLCC

Cross Reference List

Crystal Semiconductor	Analog Devices
V_{IN} = ±3V	
CS7870-KP	AD7870JN, AD7870KN
CS7870-KL	AD7870JP, AD7870KP
V_{IN} = 0V to +5V	
CS7875-KP	AD7875KN
CS7875-KL	AD7875KP

PARAMETER DEFINITIONS

REF OUT Tempco

REF OUT Tempco is the worst case slope that is calculated from the change in reference value at +25°C to the value at T_{MIN} or T_{MAX}

i.e. REF OUT Tempco = (V_{ref} @ 25°C - V_{ref} @ T_{MAX})/(T_{MAX} - 25°C) or

REF OUT Tempco = (V_{ref} @ 25°C - V_{ref} @ T_{MIN})/(25°C - T_{MIN}).

Differential Linearity

The deviation of a code's width from ideal. Units in LSBs.

Integral Non-Linearity Error - INL

The deviation of a code from a straight line passing through the endpoints of the transfer function after zero- and full-scale errors have been accounted for. "Zero-scale" is a point 1/2 LSB below the first code transition and "full-scale" is a point 1/2 LSB beyond the code transition to all ones. The deviation is measured from the middle of each particular code.

Full-Scale Error - FSE_P

The deviation of the last code transition from the ideal (VREF-3/2 LSB's). Units in LSB's.

Unipolar Offset (CS7875) - V_{UP}

The deviation of the first code transition from the ideal (1/2 LSB above AGND). Units in LSB's.

Bipolar Offset (CS7870) - V_{BP}

The deviation of the mid-scale transition (011...111 to 100...000) from the ideal (1/2 LSB below AGND). Units in LSB's.

Bipolar Negative Full-Scale Error (CS7870) - FSE_N

The deviation of the first code transition from the ideal. The ideal is defined as lying on a straight line which passes through the final and mid-scale code transitions. Units in LSB's.

Spurious-Free-Dynamic-Range - SFDR

The ratio of the rms value of the signal, to the rms value of the next largest spectral component (excepting dc). This component is often an aliased harmonic when the signal frequency is a significant proportion of the sampling rate. Units dBc (decibels relative to the carrier).

Total Harmonic Distortion - THD

The ratio of the rms sum of the significant harmonics (2^{nd} thru 5^{th}), to the rms value of the signal. Units in decibels.

Signal-to-Noise Ratio (s/n) - SNR

The ratio of the rms value of the signal, to the rms sum of all other spectral components below the Nyquist rate (excepting dc and distortion terms). Expressed in decibels

Signal-to-Noise-and-Distortion (s/[n+d]) - SINAD

The ratio of the rms value of the signal, to the rms sum of all other spectral components below the Nyquist rate (excepting dc), including distortion components. Expressed in decibels

Intermodulation Distortion - IMD

The ratio of the rms value of the larger of two test frequencies, which are each 6dB down from full-scale, to the rms value of the largest 2^{nd} and 3^{rd} order intermodulation components. Units in decibels relative to carrier.

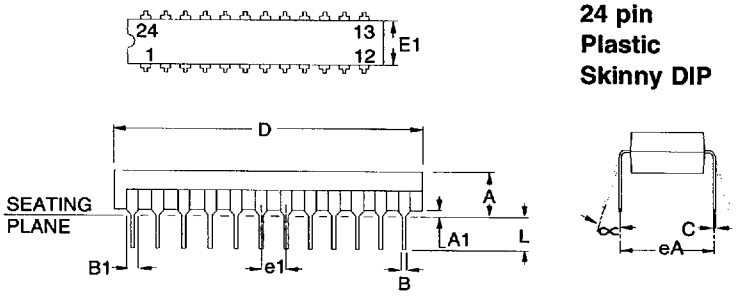
Aperture Delay Time - t_{apd}

The time required after $\overline{\text{CONVST}}$ goes high for the sampling switch to open fully. Effectively a sampling delay which can be nulled by advancing the sampling signal. Units in nanoseconds.

Aperture Jitter - t_{apj}

The range of variation in the aperture time. Effectively the "sampling window" which ultimately dictates the maximum input signal slew rate acceptable for a given accuracy. Units in picoseconds.

PACKAGE DIMENSIONS

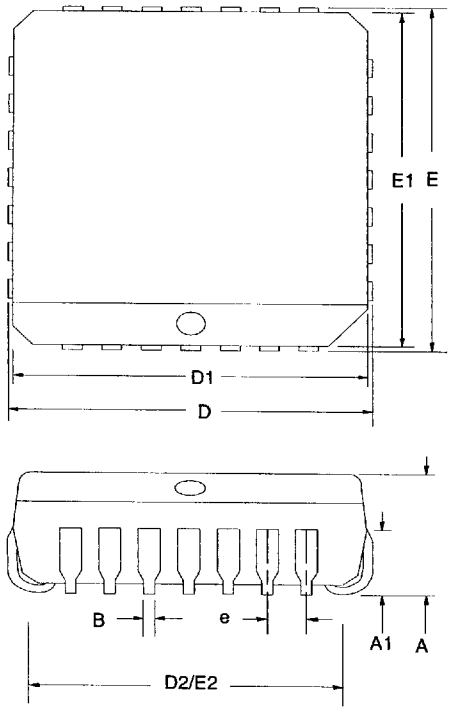


24 pin Plastic Skinny DIP

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	3.94	4.32	4.57	0.155	0.170	0.180
A1	0.51	0.76	1.02	0.020	0.030	0.040
B	0.36	0.46	0.56	0.014	0.018	0.022
B1	1.02	1.27	1.65	0.040	0.050	0.065
C	0.20	0.25	0.38	0.008	0.010	0.015
D	31.37	31.75	32.13	1.235	1.250	1.265
E1	6.10	6.35	6.60	0.240	0.250	0.260
e1	2.41	2.54	2.67	0.095	0.100	0.105
eA	7.62	-	8.25	0.300	-	0.325
L	3.18	-	3.81	0.125	-	0.150
∝	0°	-	15°	0°	-	15°

NOTES:

1. POSITIONAL TOLERANCE OF LEADS SHALL BE WITHIN 0.25mm (0.010") AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION eA TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION E1 DOES NOT INCLUDE MOLD FLASH.



28-pin PLCC

DIM	28					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	4.20	4.45	4.57	0.165	0.175	0.180
A1	2.29	2.79	3.04	0.090	0.110	0.120
B	0.33	0.41	0.53	0.013	0.016	0.021
D/E	12.32	12.45	12.57	0.485	0.490	0.495
D1/E1	11.43	11.51	11.58	0.450	0.453	0.456
D2/E2	9.91	10.41	10.92	0.390	0.410	0.430
e	1.19	1.27	1.35	0.047	0.050	0.053

A Cirrus Logic Company

CDB7870 CDB7875

Evaluation Board for CS7870 & CS7875

Features

- Throughput rates up to 100kHz.
- Operation with on-board or off-board clocks.
- Buffered serial data, 12-bit parallel word, or two 8-bit bytes
- Digital and Analog Patch Areas
- CS7870 ±3V input
  CS7875 0V to +5V input

General Description

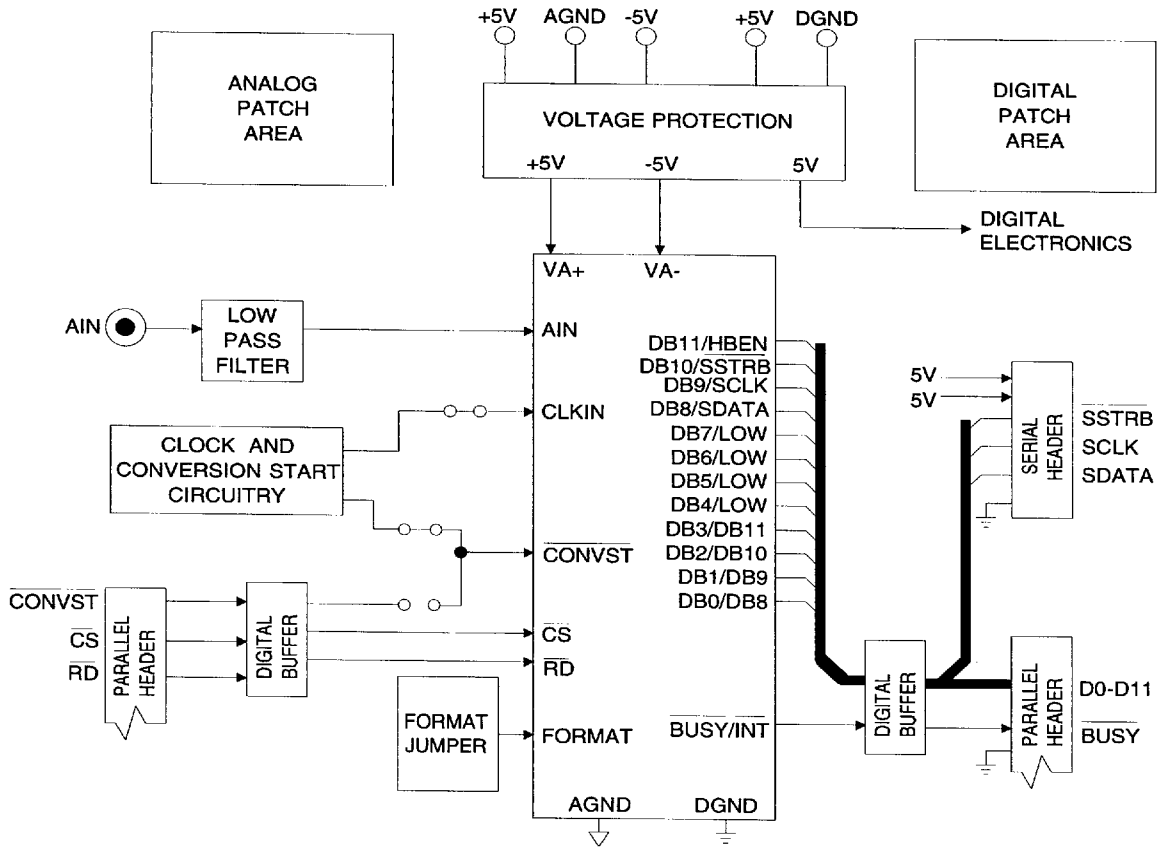
The CDB7870/5 Evaluation Boards allow fast evaluation of the CS7870 & CS7875 12-bit, 100kHz, sampling A/D Converters.

The board provides a convenient platform for easy circuit development and evaluation. A versatile tool that can simplify design and reduce the design cycle resulting in a quicker time to market.

Analog input is via a BNC connector. Buffered digital outputs are available from the ADC in serial, 12-bit parallel word, or two 8-bit bytes formats.

ORDERING INFORMATION

CDB7870 Evaluation Board with CS7870-BP Installed
CDB7875 Evaluation Board with CS7875-BP Installed



Crystal Semiconductor Corporation
P.O. Box 17847, Austin, TX 78760
(512) 445 7222 FAX: (512) 445 7581

Introduction

The CDB7870 and CDB7875 evaluation boards provide a tool for testing and designing with the CS7870/5 series of A/D Converters. The boards are configured for operation from ±5V analog and +5V digital power supplies. A BNC connector is provided for the analog input signal. An on-board jumper selects the output data and serial clock formats. Parallel and serial connectors provide an interface to the digital logic.

Power Supplies

Figure 1 shows the power supply arrangements. ±5V is required to operate the ADC and analog portion of the board. Zener diodes are provided for over-voltage protection. A separate +5V digital supply is required for the digital logic. At least one individual decoupling capacitor is provided for each IC.

Analog Input Circuit

The analog input signal is brought on the evaluation board via the BNC connector J8. Diodes D1 and D2 provide protection against over voltage. R4 and C13 make a low pass filter, whose corner frequency is 80 kHz. Notice that no external trim components are required. R6 is a 10 kΩ terminating resister which provides a load for the signal source. R6 can be changed to match the analog input source impedance if required. The footprint is large enough to accommodate a 50 Ω, 0.5 W resistor.

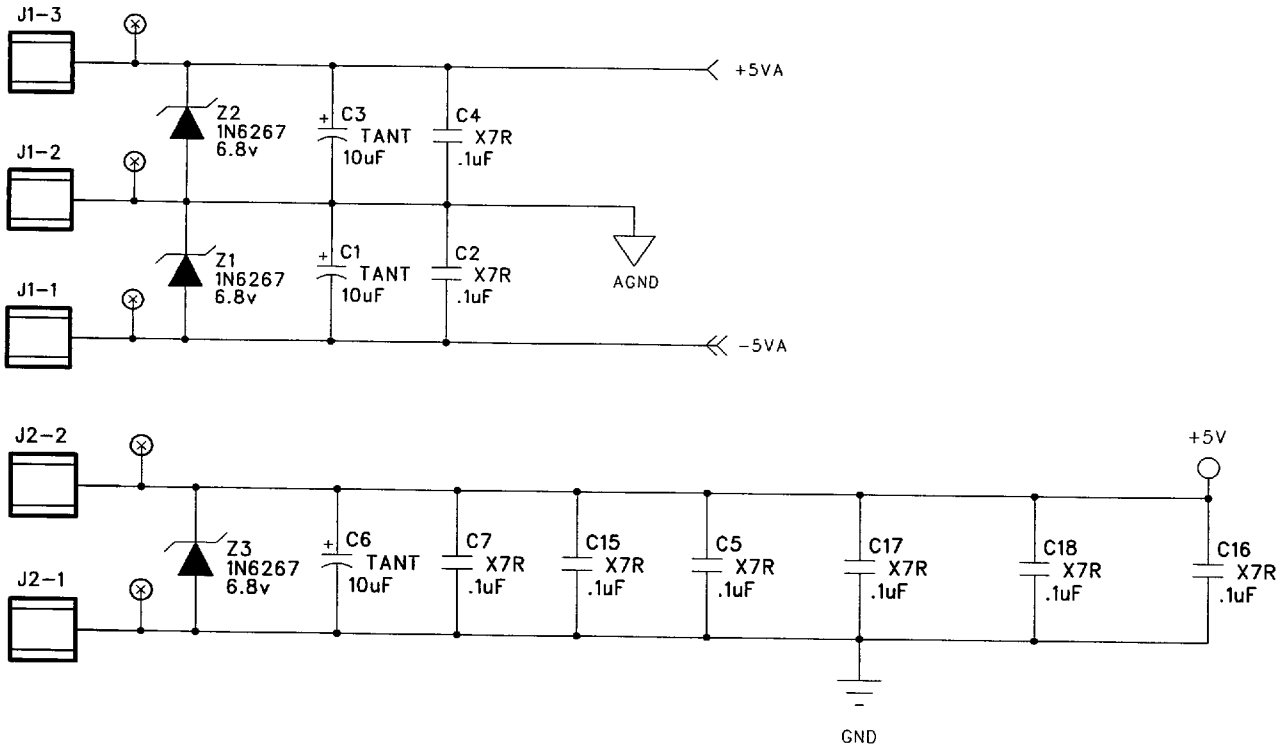


Figure 1. Power Supplies

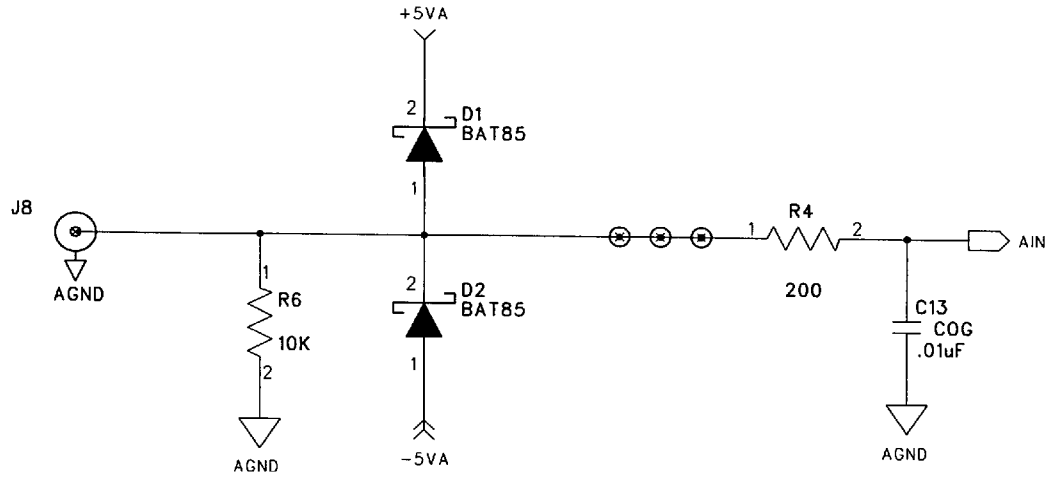


Figure 2. Analog Input Circuit

Clock and Conversion

Figure 3 shows the on-board clock and conversion control circuitry. The evaluation board is designed to run off the on-board 2.5MHz oscillator (U4). The ADC can also operate from an internal clock oscillator, by connecting the CLKIN pin to -5VA. Test points are provided to easily implement the internal oscillator.

The $\overline{\text{CONVST}}$ signal on the evaluation board is derived from the on-board 2.5MHz clock oscillator. The 2.5MHz is divided by 25, providing a 100 kHz signal. External signals can be used by breaking the $\overline{\text{CONVST}}$ jumper at the test points and attaching the external signal at pin 6 of connector J4.

Digital Output Data

The CS7870/5 ADCs support three digital output data formats. These include 12-bit parallel, 8-bit byte, and serial interface formats. Several of the ADC output pins have dual roles or modes of operation (see the CS7870/5 data sheets). The position of the "FORMAT" jumper determines which output format is active, with all three formats available through the 40-pin header J4. Serial output data is also available through the 10-pin header J3.

12-Bit Parallel Operation

Selecting the "+" position for the "FORMAT" jumper places the board in 12-bit parallel mode. All parallel output signals are buffered by U1 and U3, and are available on header J4 (Figure 4). The rising edge of the $\overline{\text{BUSY}}$ signal, available on pin-40 of J4, can be used to latch the 12-bit parallel data into subsequent digital circuitry.

8-Bit Byte Operation

Selecting the "0" or the "-" position for the "FORMAT" jumper places the board in 8-bit byte mode. The data is available on D0 to D7 of header J4 in two separate read operations. The lower byte is read with HBEN low. The four more significant bits are read with HBEN high. The high byte word includes four leading zeros (D4 to D7) to fill out the remaining four significant bits from the ADC. All byte output signals are buffered by U1 and U3.

Serial Operation

Selecting the "0" or the "-" position for the "FORMAT" jumper also places the board in serial mode. In the "-" position, the serial clock SCLK operates continuously; in the "0" jumper position, the serial clock SCLK is active only when the ADC is outputting serial data. The rising edge of SCLK can be used to latch serial data into subsequent circuitry. The serial data and control lines are available on J3, and the DATA8 (SDATA), DATA9(SCLK), and DATA10 ($\overline{\text{SSTRB}}$) lines of J4. All serial output signals are buffered by U1.

Convert Start Operation

MODE 1 Operation

The $\overline{\text{CONVST}}$ signal is used to put the ADC into hold mode and initiate a conversion. At the end of the conversion, the ADC returns to its tracking mode. Conversion begins on the rising edge of the $\overline{\text{CONVST}}$, provided that $\overline{\text{CS}}$ is high (note that external pull-up resistors on $\overline{\text{CS}}$ and $\overline{\text{RD}}$ default both to logic high if no external logic signal is present for these pins on the J4 header). The $\overline{\text{BUSY}}$ line on J4, which goes low when the output data becomes available, can be used as a microprocessor interrupt. Bringing $\overline{\text{CS}}$ and $\overline{\text{RD}}$ low allows data to be read from the ADC and also resets $\overline{\text{BUSY}}$ high. $\overline{\text{CONVST}}$ must be high when $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are brought low in this mode. Data cannot be read during the conversion cycle because the ADC output latches are disabled during this process.

FORMAT JUMPER	
+	12-bit parallel mode
0	8-bit byte or serial (16 bit SCLK)
-	8-bit byte or serial (continuous SCLK)

MODE 2 Operation

In this mode, $\overline{\text{CONVST}}$ is held permanently low (Break $\overline{\text{CONVST}}$ jumper at the test points and add jumper between $\overline{\text{CONST\_BUF}}$ and $\overline{\text{CONVST}}$. Ground the $\overline{\text{HOLD}}$ signal J4-6). Bringing $\overline{\text{CS}}$ low (while HBEN is low) through the J4 header, puts the ADC into hold mode and initiates a conversion. The $\overline{\text{BUSY}}$ line on J4 goes low at the start of the conversion and returns high at the end of conversion.

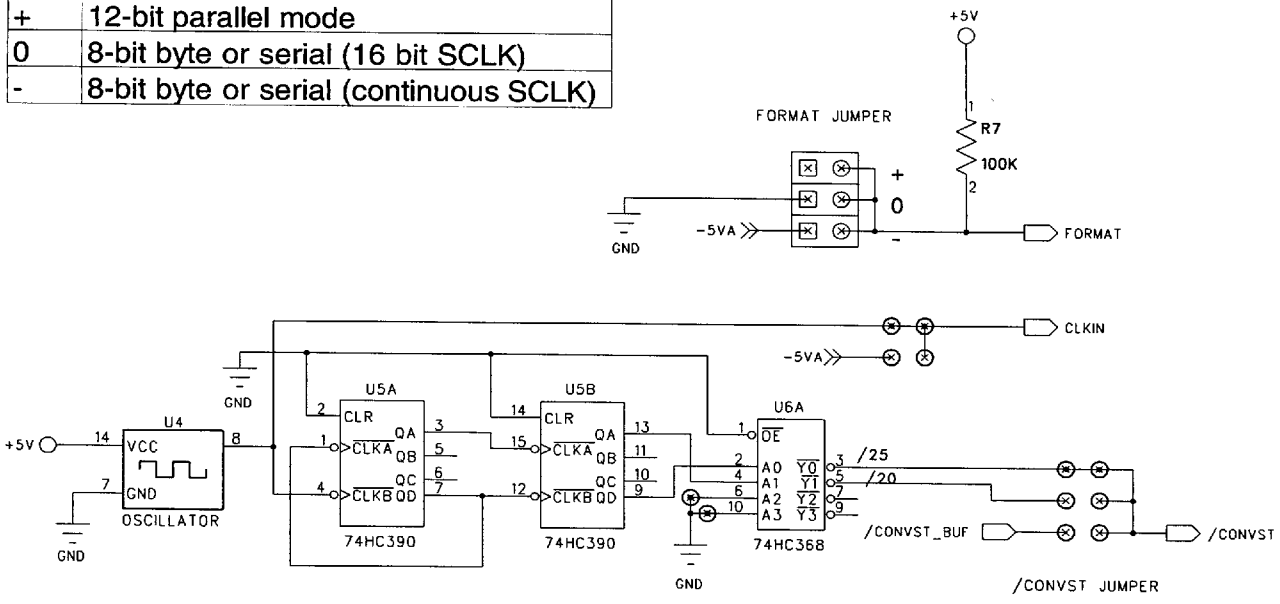


Figure 3. Clock and Convert Start Circuitry

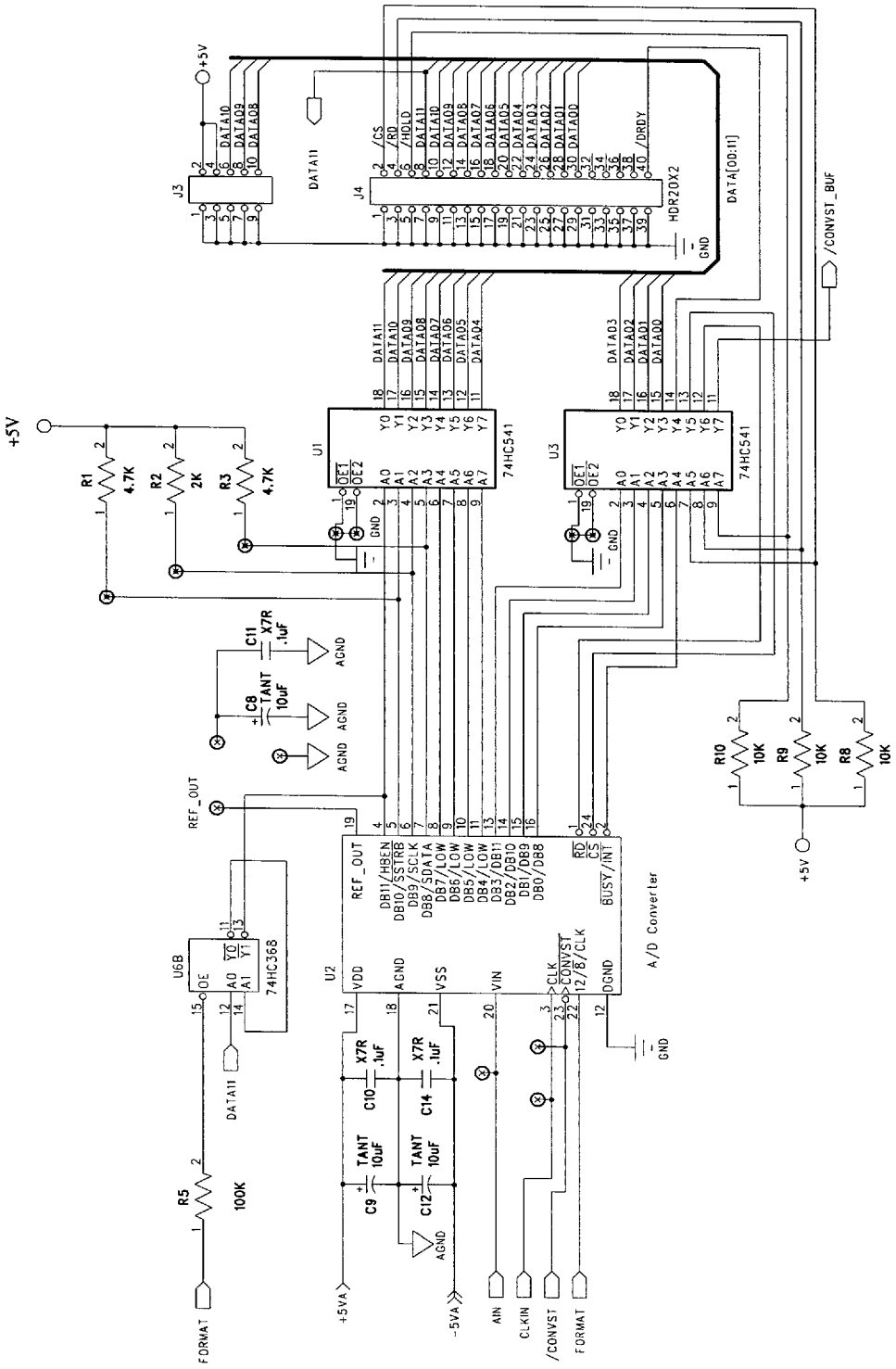


Figure 4. ADC Connections and Digital Output

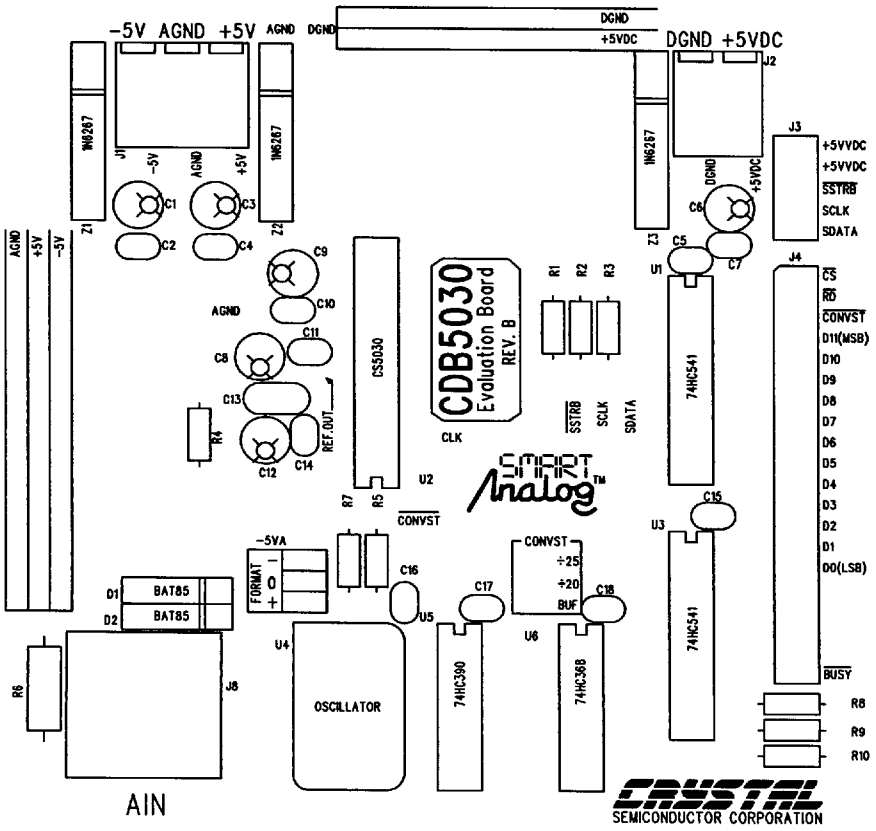


Figure 5. CDB7870/CDB7875 Component Layout

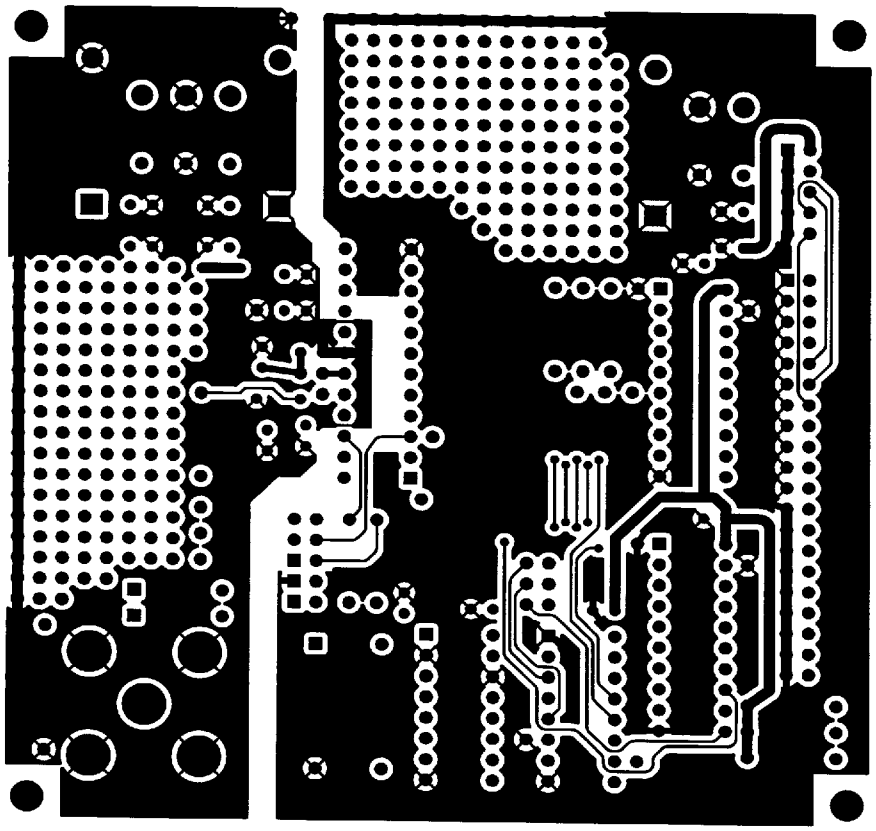


Figure 6. Top Ground Plane Layer (NOT TO SCALE)

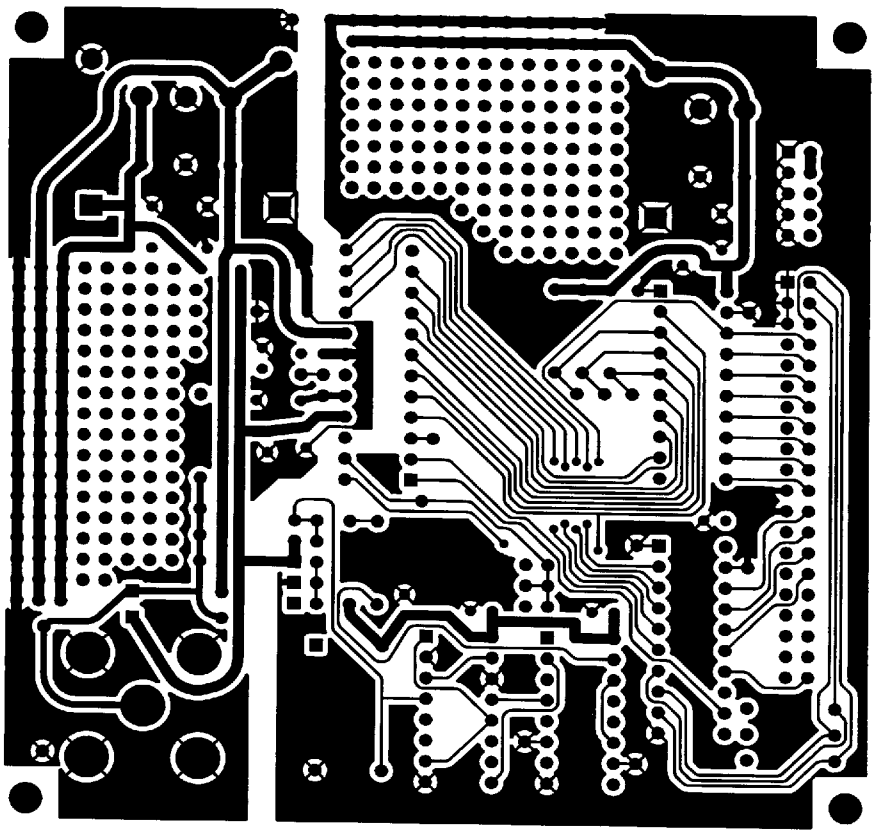


Figure 7. Bottom Trace Layer (NOT TO SCALE)