

Structure Silicon Monolithic Integrated Circuit

Product Series 5ch Sensorless System Motor Driver for MD

Type BD6603KVT

Features • Operates at low power supply voltage (2.3V min.)

• Power DMOS output with low ON resistance (0.8 $\Omega$  typ.)

· Incorporates a charge pump circuit for VG boost

· 3-phase full-wave sensorless driving system for spindle

• 4ch, 2-value control H-bridges for sled/focus/tracking/head up/down

2ch half-bridges for spindle/sled VM power supply

# OAbsolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
Power supply voltage for control circuit	VCC	7	V
Power supply voltage for driver block	VM	7	V
Power supply voltage for pre-driver block	VG	15	V
Input voltage	VIN	0~VCC	V
Output current	Iomax	*500	mA
Power dissipation	Pd	**1250	mW
Operating temperature range	Topr	-25~+75	$^{\circ}$
Storage temperature range	Tstg	-55~+150	$^{\circ}$
Junction temperature	Tjmax	+150	$^{\circ}$

<sup>\*</sup>Must not exceed Pd or ASO, Tjmax=150°C.

# OOperating conditions (Ta=-25~+75°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit
Power supply voltage	VCC	2.3	3.0	6.5	V
	VM	_	_	6.5	V
	VG	VM+3	9	14	V
Pulse input frequency	fin	_	_	200	kHz

<sup>\* \*</sup> Reduced by 10.0mW/°C over Ta=25°C, when mounted on a glass epoxy board (70mm×70mm×1.6mm).



## OElectrical characteristics

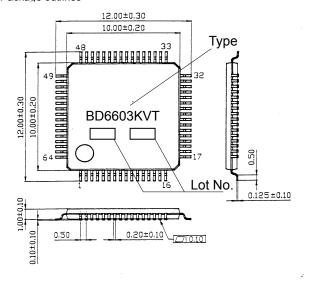
(Unless otherwise specified, Ta=25 $^{\circ}$ C, VCC=3V, VM=2.5V, fin=176kHz)

Demonstra	Limit			11-4	0 1111		
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions	
0: "	ICC	_	5.6	8.0	mA	at operation in all blocks	
Circuit current	IST	_	16	50	μA	at standby in all blocks	
Output ON resistance	RON	_	0.8	1.2	Ω	upper and lower ON resistance in total VG=10V	
$\sim$ Boost circuit $\sim$							
0	VG1	7.5	8.9	10.0	V	each input L	
Output voltage	VG2	6.0	7.3	9.5	V	at operation in all blocks	
$\sim$ Oscillation circuit $\sim$							
Self propelled oscillating frequency	fOSC	125	250	400	kHz		
External clock synchronous range	fSYNC	_	_	500	kHz	input from EXTCLK pin	
$\sim$ Spindle (3-phase full-wave sensorl	ess driver) b	ock $\sim$					
Position detection comparator offset	VCO	-10	_	+10	mV		
Detection comparator input range	VCD	0	_	VCC-1.0	V		
CST charge current	ICTO	-0.9	-2.1	-3.3	μA	CST=1V	
CST discharge current	ICTI	2.0	3.6	5.3	mA	CST=1V	
CSL charge current	ICLO	-4.0	-8.0	-12	μA	CSL=VCC-0.4V	
CSL discharge current	ICLI	2.0	5.5	5.3	μA	CSL=VCC-0.4V	
Brake comparator input current	IBR	_	_	2.0	μA	BRK=VCC	
Brake comparator input offset	VBO	-15	_	+15	mV		
Brake comparator input range	VBD	0	_	VCC-1.5	V		
FG output L voltage	VOLF	_	0.2	0.3	V	Io=500μA	
~Sled, focus, tracking, head up/down, PWM power supply (H-bridge, half-bridge driver) block~							
Logic H level input voltage	VINH	VCC-0.4	_	_	V		
Logic L level input voltage	VINL	_	_	0.4	V		
Logic H level input current	IINH1	_		1	μA	VIN=3V	
	IINH2	_	350	600	μΑ	VIN=3V EXTCLK pin	
Logic L level input current	IINL	-1	_	_	μΑ	VIN=0V	
Output propagation delay time	TRISE	_	0.2	1	µsec		
	TFALL	_	0.1	0.7	µsec		
Minimum input pulse width	tmin	200	_	_	nsec	output pulse width 2/3tmin or more	

<sup>⊚</sup>This product is not designed for protection against radioactive rays.

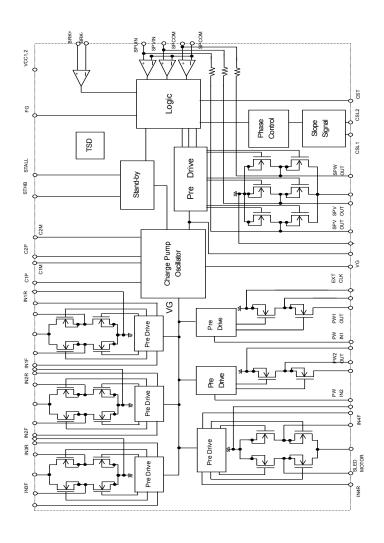


# OPackage outlines



TQFP64V outlines (Unit: mm)

# OBlock diagram



## OPin No./Pin name

	1	
Pin name	NO.	Pin name
PWIN2	33	CSL1
IN1F	34	FG
IN1R	35	IN4R
IN2F	36	IN4F
IN2R	37	IN3R
H1PG2	38	IN3F
H1ROUT	39	H4PG1
H1VM	40	H4FOUT
H1FOUT	41	H4VM
H1PG1	42	H4ROUT
H2PG2	43	H4PG2
H2ROUT	44	H3PG1
H2VM	45	H3FOUT
H2FOUT	46	H3VM
H2PG1	47	H3ROUT
BRK-	48	H3PG2
BRK+	49	VG
SPUIN	50	C2M
SPVIN	51	C2P
SPWIN	52	C1M
SPCOM	53	C1P
SGND	54	EXTCLK
ASGND	55	STHB
SPPG2	56	STALL
SPUOUT	57	VCC1
SPVM2	58	VCC2
SPVOUT	59	PW2VM
SPPG1	60	PW2OUT
SPWOUT	61	PWPG
SPVM1	62	PW10UT
CST	63	PW1VM
CSL2	64	PWIN1
	PWIN2 IN1F IN1R IN2F IN2R H1PG2 H1ROUT H1VM H1FOUT H1PG1 H2PG2 H2ROUT H2VM H2FOUT H2VM H2FOUT H2PG1 BRK- BRK- SPUIN SPVIN SPVIN SPVIN SPUIN SPCOM SGND ASGND ASGND SPPG2 SPUOUT SPVM2 SPVOUT SPPG1 SPWM1 CST	PWIN2 33 IN1F 34 IN1F 34 IN1R 35 IN2F 36 IN2R 37 H1PG2 38 H1ROUT 39 H1VM 40 H1FOUT 41 H1PG1 42 H2PG2 43 H2ROUT 44 H2VM 45 H2FOUT 46 H2PG1 47 BRK- 48 BRK- 49 SPUIN 50 SPVIN 51 SPWIN 52 SPCOM 53 SGND 54 ASGND 55 SPPG2 56 SPUOUT 57 SPVM2 58 SPVOUT 59 SPPG1 60 SPWOUT 61 SPVM1 62 CST 63



#### ONotes on the use

#### (1) Absolute maximum ratings

If the input voltage or the operating temperature range exceeds absolute maximum ratings, IC may be damaged. No destruction mode (e.g., short-circuiting or open) can be specified in that case. If such special mode as will exceed absolute maximum ratings is assumed, take the physical safety measures, such as a fuse.

## (2) Power supply lines

The regenerated current by BEMF of the motor will return. Therefore, take measures, such as the insertion of a capacitor between the power supply and GND as the pass of the regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may loose some capacitance at low temperatures.

#### (3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

#### (4) Design for heat

Use the design for heat that allows for a sufficient margin in light of the power dissipation (Pd) in actual using conditions.

## (5) Operation in strong magnetic field

Use caution when using the IC in the strong magnetic field as doing so may cause the IC to malfunction.

#### (6) ASO

When using the IC, make settings so that the output transistors for the motor will not be used under conditions in excess of the absolute maximum ratings and ASO.

#### (7) Thermal shutdown circuit

This IC incorporates thermal shutdown circuit(TSD circuit).

When the chip temperature becomes the one shown in below, TSD circuit operates and makes the coil output to motor open. It is designed to shut the IC off from runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed

TSD ON temperature[°C] (typ.)	Hysteresis emperature [°C] (typ.)
175	20

## (8) Ground wiring pattern

When having both small signal and large current GND, it is recommended to isolate the two GND patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause voltage variations of the small signal GND. Be careful not to change the GND wiring pattern of any external parts, either.

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