FINAL

T-75-37-05

Advanced Micro Devices

Am7968/Am7969

TAXIchip™ Integrated Circuits (Transparent Asynchronous Xmitter-Receiver Interface)

DISTINCTIVE CHARACTERISTICS

- **Parallel TTL bus Interface**
  - Eight Data and four Command Pins
  - or nine Data and three Command Pins
  - or ten Data and two Command Pins
- **Transparent synchronous serial link**
  - +5 V ECL Serial I/O
  - AC or DC coupled
  - NRZI 4B/5B, 5B/6B encoding/decoding
- **Drive coaxial cable or twisted pair directly**
- **Easy interface with fiber optic data links**
- **32–140 Mbps (4–17.5 Mbytes/sec) data throughput**
- **Asynchronous input using STRB/ACK**
- **Automatic MUX/DEMUX of Data and Command**
- **Complete on-chip PLL, Crystal Oscillator**
- **Single +5 V supply operation**
- **28-pin PLCC or DIP or LCC**

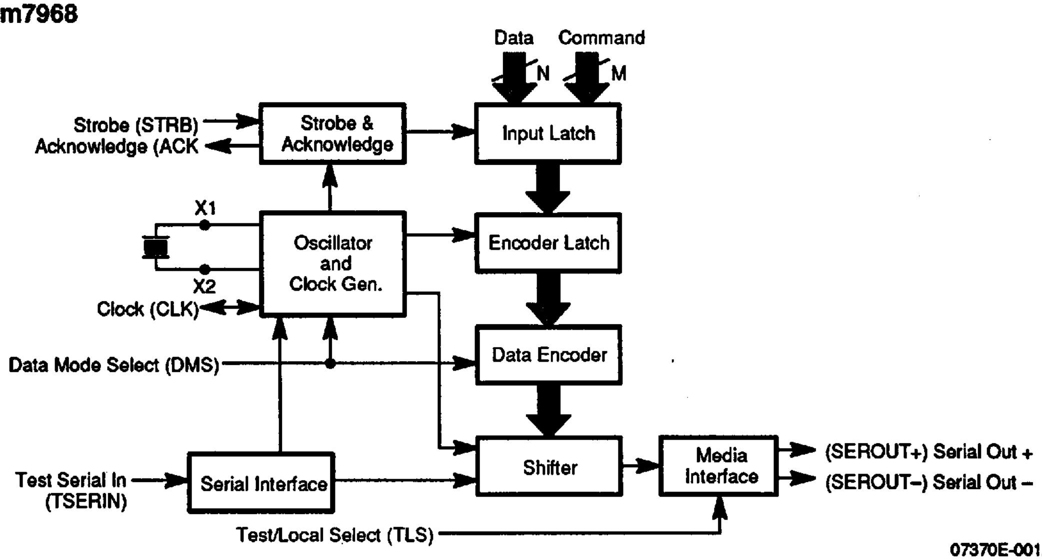
GENERAL DESCRIPTION

The Am7968 TAXIchip Transmitter and Am7969 TAXIchip Receiver Chipset is a general-purpose interface for very high-speed (4–17.5 Mbytes/sec, 40–175 Mbaud serially) point-to-point communications over coaxial or fiber-optic media. The TAXIchip set emulates a pseudo-parallel register. They load data into one side and output it on the other, except in this case, the "other" side is separated by a long serial link.

The speed of a TAXIchip system is adjustable over a range of frequencies, with parallel bus transfer rates of 4 Mbytes/sec at the low end, and up to 17.5 Mbytes/sec at the high end. The flexible bus interface scheme of the TAXIchip set accepts bytes that are either 8, 9, or 10 bits wide. Byte transfers can be Data or Command signaling.

BLOCK DIAGRAM

Am7968



07370E-001A

Note:

N can be 8, 9, or 10 bits; total of N + M = 12.

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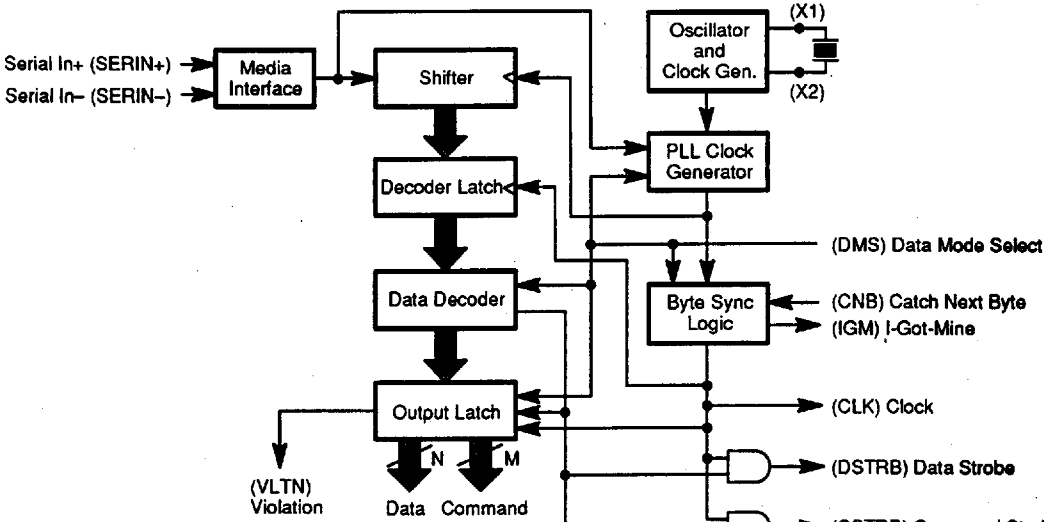
Issue Date: October 1992

BLOCK DIAGRAM (Continued)
Am7969

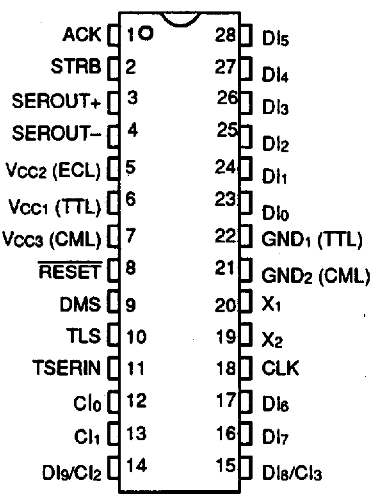


Note:
N can be 8, 9, or 10 bits Total of N + M = 12

07370E-002A

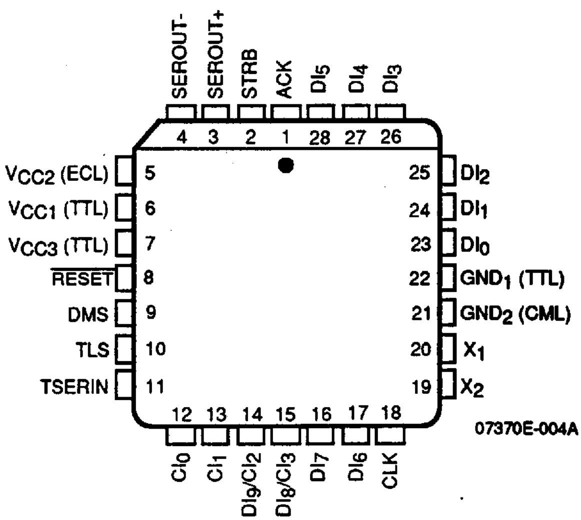
CONNECTION DIAGRAMS
Top View
Am7968

DIPs



07370E-003A

LCC/PLCC



07370E-004A

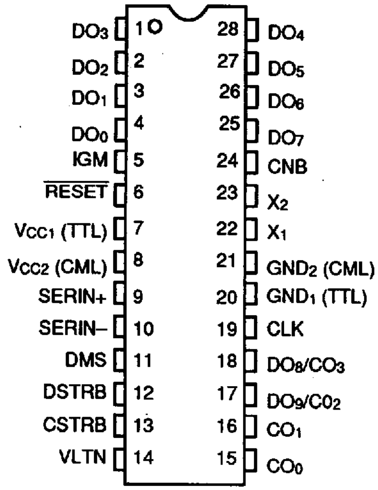
Note:
Pin 1 is marked for orientation.

CONNECTION DIAGRAMS (Continued)

Top View

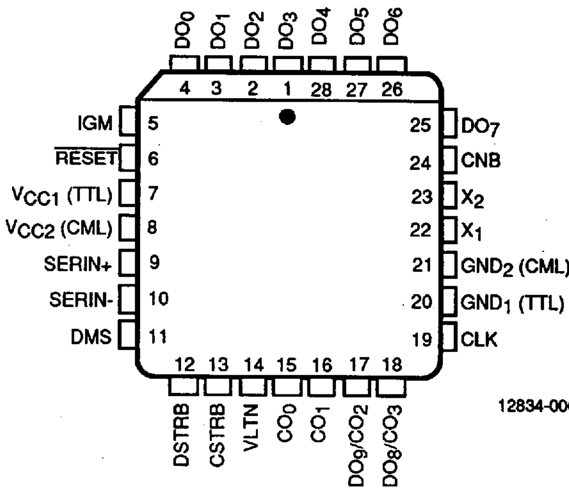
Am7969

DIPs



12834-005A

LCC/PLCC

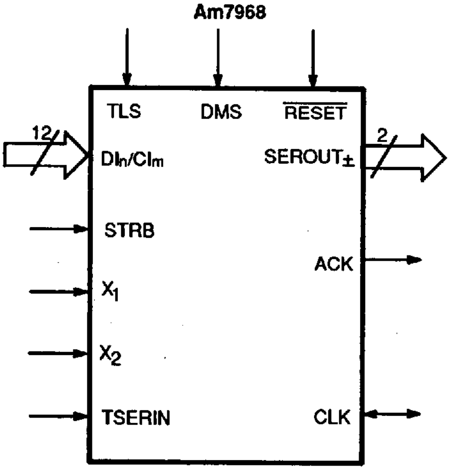


12834-006A

Note:
Pin 1 is marked for orientation.

LOGIC SYMBOLS

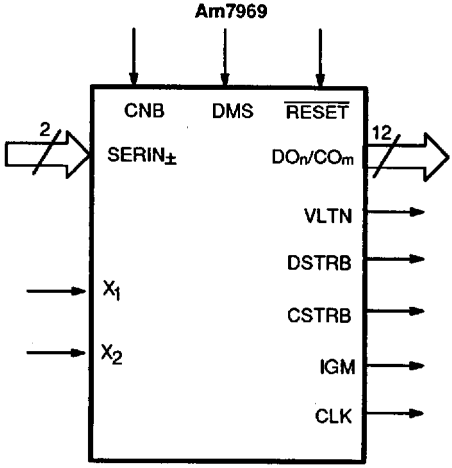
Am7968



12834-007A

Vcc = Power Supply (3)
GND = Ground (2)

Am7969



12834-008A

Vcc = Power Supply (2)
GND = Ground (2)

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The ordering number (Valid Combination) is formed by a combination of:

AM7968
AM7969 **–125** **D** **C**

TEMPERATURE RANGE
C = Commerical (0 to +70°C)

PACKAGE TYPE
P = 28-Pin Plastic DIP (PD 028)
D = 28-Pin Ceramic DIP (CD 028)
J = 28-Pin Plastic Leaded Chip Carrier (PL 028)

SPEED OPTION
–125 = Max. Serial Encoded Transmission Rate is 125 MHz
–175 = Max. Serial Encoded Transmission Rate is 175 MHz

DEVICE NUMBER/DESCRIPTION
Am7968 TAXIchip Transmitter
Am7969 TAXIchip Receiver

Valid Combinations	
AM7968-125	PC, DC, JC
AM7969-125	
AM7968-175	PC, DC, JC
AM7969-175	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

CPL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. CPL (Controlled Products List) products are compliant with MIL-STD-883C requirements with exceptions for Vcc or operating temperature. The order number (Valid Combination) is formed by a combination of:

AM7968 / AM7969 -125 V /L K C

C = Controlled Product List

TEMPERATURE RANGE
K = –30°C to 125°C
M = –55°C to 125°C

PACKAGE TYPE
D = 28-Pin Ceramic DIP (CD 028)
L = 28-Pin Ceramic Leadless Chip Carrier (CL 028)

Vcc RANGE
Blank = 4.5 V to 5.5 V
V = 4.75 V to 5.5 V

SPEED OPTION
–125 = Max. Serial Encoded Transmission Rate is 125 MHz

DEVICE NUMBER/DESCRIPTION
Am7968 – TAXIchip Transmitter (Local Mode only)
Am7969 – TAXIchip Receiver (Local Mode only)

Valid Combinations	
AM7968-125	/LKC, /DKC
AM7969-125	
AM7968-125 V	/LMC, /DMC
AM7969-125 V	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, or to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

Am7968 TAXIchip Transmitter

$DI_0 - DI_7$

Parallel Data In (TTL Inputs)

These eight inputs accept parallel data from the host system, to be latched, encoded and transmitted.

DI_8/CI_3

Parallel Data (8) In or Command (3) In (TTL Input)

DI_8/CI_3 input is either Data or Command, depending upon the state of *DMS*.

DI_9/CI_2

Parallel Data (9) In or Command (2) In (TTL Input)

DI_9/CI_2 input is either Data or Command, depending upon the state of *DMS*.

$CI_0 - CI_1$

Parallel Command In (TTL Inputs)

These two inputs accept parallel command information from the host system. If one or more command bits are logic "1", the command bit pattern is latched, encoded, and transmitted in place of any pattern on the Data inputs.

STRB

Input Strobe Signal (TTL Input)

A rising edge on the *STRB* input causes the Data *($DI_0 - DI_9$)* or the Command *($CI_0 - CI_3$)* inputs to be latched into the Am7968 Transmitter. The *STRB* signal is normally taken LOW after *ACK* has risen.

ACK

Input-Strobe Acknowledge (TTL Output)

ACK High signifies that the Am7968 is ready to accept new Data and Command. The timing of *ACK's* response to *STRB* depends on the condition of the Input Latch (in given CLK cycle).

If the Input Latch is empty, data is immediately stored and *ACK* closely follows *STRB*. If the Input Latch contains previously stored data when *STRB* is asserted, *ACK* is delayed until the next falling edge of *CLK*. Note that for *ACK* to rise *STRB* must maintain HIGH for both of the above conditions.

SEROUT+, SEROUT–

Differential Serial Data Out (Differential Open Emitter ECL Outputs)

These differential ECL outputs generate data at ECL voltage levels referenced to +5.0 V. When connected to appropriated pull down resistors, they are capable of driving 50-Ω terminated lines, either directly or through isolating capacitors.

X_1, X_2

Crystal Oscillator Inputs (Inputs)

The two crystal input pins connect to an internal parallel mode oscillator which operates at the fundamental frequency of the external crystal. The byte rate matches the crystal frequency. During normal operation, the byte rate is set by the crystal frequency.

Alternatively, *X_1* can be driven by an external TTL frequency source. In multiple TAXI systems this external source could be another Am7968's *CLK* output.

DMS

Data Mode Select (Input)

Data Mode Select input determines the Data pattern width. When it is wired to GND, the Am7968 Transmitter will assume Data to be eight bits wide, with four bits of Command. When it is wired to V_{CC}, the Am7968 Transmitter will assume Data to be nine bits wide, with three bits of Command. If *DMS* is left floating (or terminated to 1/2 V_{CC}), the Am7968 will assume Data to be ten bits wide, with two bits of Command.

TLS

Test/Local Select (Input)

TLS input determines the mode of operation. When *TLS* is wired to GND, the Am7968 Transmitter assumes a Local mode connection to the media. It will output NRZI encoded data, and will enable its *CLK* output driver. The *TLS* pin should always be grounded during normal operation.

When *TLS* is wired to V_{CC} (Test Mode 1),the serial data is NRZ, *CLK* becomes an input, and ACK timing is modified. This mode is only used for Automatic Test Equipment (ATE) testing at full speed.

When this input is left unconnected, it floats to an intermediate level which puts the Am7968 Transmitter into its Test Mode 2. In Test Mode 2, the internal clock multiplier is switched out, and the internal logic is clocked directly from the *CLK* pin. Test Mode 2 is included to ease Automatic Test Equipment (A.T.E.) testing by making the internal logic of the Transmitter synchronous to the external clock instead of the internal PLL.

CLK
Clock (TTL I/O)

CLK is an I/O pin that supplies the byte-rate clock reference to drive all internal logic. When *TLS* is connected to ground (Local mode), *CLK* is enabled as a free-running (byte-rate) clock output which runs at the Crystal Oscillator frequency; this output can be used to drive the X_1 input of TAXIchip Receivers or other system logic. In Test mode *CLK* becomes an input. In Test Mode 1 *CLK* is a Byte rate input and in Test Mode 2 it is a Bit rate input.

$\overline{\text{RESET}}$
PLL RESET (Input)

This pin is normally left open, but can be momentarily grounded to force the internal PLL to reactivate lock. This allows for correction in the unlikely occurrence of PLL lockup on application of power.

$\overline{\text{RESET}}$ has an internal pull-up resistor which causes it to float high when left unconnected (50 K ohm nominal).

TSERIN
Test Serial Input (Pseudo ECL Input)

This pin is left unconnected in Local Mode operation. TSERIN can be used to input serial data patterns into the Shifter in Test Mode 1 operation.

V_{CC1}, V_{CC2}, V_{CC3}
Power Supply

V_{CC1}, V_{CC2}, and V_{CC3} are +5.0 volt nominal power supply pins. V_{CC1} powers TTL I/O, V_{CC2} powers ECL and V_{CC3} powers internal Logic and Analog circuitry.

GND_1, GND_2
Ground Pins

GND_1 is a TTL I/O Ground and GND_2 is an internal Logic and Analog Ground.

Am7969 TAXIchip Receiver

$DO_0 - DO_7$

Parallel Data Out (TTL Outputs)

These eight outputs reflect the most recent Data received by the Am7969 Receiver.

DO_8/CO_3

Parallel Data (8) Out or Command (3) Out (TTL Output)

DO_8/CO_3 output will be either a Data or Command bit, depending upon the state of *DMS*.

DO_9/CO_2

Parallel Data (9) Out or Command (2) Out (TTL Output)

DO_9/CO_2 output will be either a Data or Command bit, depending upon the state of *DMS*.

$CO_0 - CO_1$

Parallel Command Out (TTL Output)

These two outputs reflect the most recent Command data received by the Am7969 Receiver.

DSTRB

Output Data Strobe (TTL Output)

The rising edge of this output signals the presence of new Data on the *$DO_0 - DO_9$* lines. Data is valid just before the rising edge of *DSTRB*.

CSTRB

Command Data Strobe (TTL Output)

The rising edge of this output signals the presence of new Command data on the *$CO_0 - CO_3$* lines. Command bits are valid just before the rising edge of *CSTRB*.

VLTN

Violation (TTL Output)

The rising edge of this output indicates that a transmission error has been detected. It changes state at the same time *DO_i* or *CO_i* change and will be followed by either *DSTRB* or *CSTRB*. This pin goes LOW when the next valid byte is decoded.

IGM

I-Got-Mine (TTL Output)

This pin signals cascaded Am7969 Receivers that their upstream neighbor has captured its assigned data byte. *IGM* falls at the mid-byte when the first half of a sync byte is detected in the Shifter. It rises at mid-byte when it detects a non-sync pattern. During Local mode operation the *IGM* signal is undefined.

CLK

Clock (TTL Output)

This is a free-running clock output which runs at the byte rate, and is synchronous with the serial input. It falls at the time that the Decoder Latch is loaded from the Shifter, and rises at mid-byte. The *CLK* output of the Receiver is not suitable as a frequency source for another TAXI Transmitter or Receiver. It is intended to be used by the host system as a clock synchronous with the received data.

CNB

Catch Next Byte Input (TTL Input)

If this input is connected to the *CLK* output, the Receiver will be in the Local mode, and each received byte will be captured, decoded and latched to the outputs.

If the *CNB* input is HIGH, it allows the Am7969 Receiver to capture the first byte after a sync. The Am7969 Receiver will wait for another sync before latching the data out, and capturing another. If *CNB* is toggled LOW, it will react as if it had decoded a sync byte.

In Cascade mode, *CNB* input is typically connected to an upstream Am7969's *IGM* output. The first Am7969 Receiver in line will have its *CNB* input connected to V_{CC}.

SERIN+, SERIN–

Differential Serial Data In (ECL Inputs)

Data is shifted serially into the Shifter. The *SERIN+* and *SERIN–* differential ECL inputs accept ECL voltage swings, which are referenced to +5.0 V. When *SERIN–* is grounded, the Am7969 is put into Test Mode; *SERIN+* becomes a single-ended ECL input, the PLL clock generator is bypassed, and *X_1* determines the bit rate (rather than the byte rate). Both pins have internal pull down resistors which cause unterminated inputs to stay low.

X_1, X_2

Crystal Oscillator Inputs (Inputs)

These two crystal input pins connect to an internal parallel/mode oscillator which oscillates at the fundamental frequency external crystal. During normal operation, the byte rate is set by the crystal frequency. Alternatively, *X_1* can be driven by an external frequency source. In multiple TAXI systems, this external source could be a TAXI Transmitter's *CLK* output or an external TTL frequency source.

DMS

Data Mode Select (Input)

DMS selects the Data pattern width. When it is wired to GND, the Am7969 Receiver will assume Data to be eight bits wide, with four bits of Command. When it is wired to V_{CC} the Am7969 Receiver will assume Data to be nine bits wide, with three bits of Command. If *DMS* is left floating (or terminated to 1/2 V_{CC}), the Am7969 Receiver will assume Data to be ten bits wide, with two bits of Command.

$\overline{\text{RESET}}$

PLL RESET (Input)

This pin is normally left open, but can be momentarily grounded to force the internal PLL to reactivate lock. This allows for correction in the unlikely occurance of PLL Lockup on application of power.

$\overline{\text{RESET}}$ has an internal pull-up resistor (50 K nominal) which causes it to float high when left unconnected.

V_{CC1}, V_{CC2}

Power Supply

V_{CC1} and V_{CC2} are +5.0 volt nominal power supply pins. V_{CC1} powers TTL I/O, and V_{CC2} powers internal Logic and Analog circuitry.

GND_1, GND_2

Ground

GND_1 is a TTL I/O Ground, GND_2 is an internal Logic and Analog Ground.

FUNCTIONAL DESCRIPTION

System Configuration

The TAXIchip system provides a means of connecting parallel data systems over a serial link (Figure 2). In LOCAL Mode (normal operation mode) each TX/RX pair is connected over a serial link which can be a Fiber Optic or Copper Media (Figure 3).

The Am7968 Transmitter accepts inputs from a sending host system using a simple *STRB/ACK* handshake. Parallel bits are saved by the Am7968's input latch on the rising edge of a *STRB* input. The input latch can be updated on every *CLK* cycle; if it still contains previously stored data when a second *STRB* pulse arrives, Data is stored in the input latch, and the second *ACK* response is delayed until the next *CLK* cycle.

The inputs to an Am7968 Transmitter can be either Data or Command and may originate from two different parts of the host system. A byte cycle may contain Data or Command, but not both. Data represents the normal data channel message traffic between host systems. Commands can come from a communication control section of the host system. Commands occur at a relatively infrequent rate but have priority over Data. Examples include communication specific commands such as REQUEST-TO-SEND or CLEAR-TO-SEND; or application specific commands such as MESSAGE-ADDRESS-FOLLOWS, MESSAGE-TYPE-FOLLOWS, INITIALIZE YOUR SYSTEM, ERROR, RETRANSMIT, HALT, etc.

The Am7968 Transmitter switches between Data and Command by examining Command input patterns. All 0s on Command input pins cause information on the Am7968's Data input pins to be latched into the device on the rising edge of *STRB*. All other Command patterns cause a Command symbol to be sent in response to an input strobe. The pattern on the Data inputs is ignored when a Command symbol is sent. In either case, if there is no *STRB* before the next byte boundary, a Sync symbol will be transmitted. The sync pattern maintains link synchronization and provides an adequate signal transition density to keep the Receiver Phase-Locked-Loop (PLL) circuits in lock. It was chosen for its unique pattern which never occurs in any Data or Command messages. This feature allows Sync to be used to establish byte boundaries.

The Sync pattern utilized by TAXIchip set keeps the automatic gain control (AGC) fiber-optic transceiver circuits in their normal range because the pattern has zero DC offset.

The Am7969 Receiver detects the difference between Data and Command patterns and routes each to the proper Output Latch. When a new Data pattern enters the output latch, *DSTRB* is pulsed and Command information remains unchanged. If a Command pattern is sent to the output latch or if Sync is received, *CSTRB* is pulsed and Data outputs remain in their previous state. Reception of a Sync pattern clears the Command outputs to all 0's, since Sync is a legal command.

Noise-induced bit errors can distort transmitted bit patterns. The Am7969 Receiver logic detects most noise-induced transmission errors. Invalid bit patterns are recognized and indicated by the assertion of the violation (*VLTN*) output pin. This signal rises to a logic "1" state at the same time that Data or Command outputs change and remains HIGH until a valid pattern is detected by the Data Decoder. The error detection method used in the Receiver cannot identify bit errors which transform one valid Command or Data pattern to another. Fault-sensitive systems should use additional error checking mechanisms to guarantee message integrity.

Am7968 Transmitter

The Transmitter accepts messages from its parallel input pins (Command or Data). Once latched into an Am7968, a parallel message is encoded, serialized, and shifted out to the serial link. The idle time between transmitted bytes (evident by lack of STRB) is filled with Sync bytes.

Am7969 Receiver

Receivers accept differential signals on the *SERIN+/SERIN–* input pins. This information, previously encoded by an Am7968 Transmitter, is loaded into a decoder.

When serial patterns are received, they are decoded and routed to the appropriate outputs. If the received message is a Command, it is stored in the output latch, appears at the Command output pins, and *CSTRB* is pulsed; Data output pins continue holding the last Data byte and *DSTRB* stays inactive. If a Data message follows the reception of a Command, Command output pins continue holding the previous Command byte and *CSTRB* stays inactive. The command outputs will retain their states until another Command signal is received (Sync is considered to be a valid command which, when decoded, sets Command outputs to "0" and issues a resulting *CSTRB*).

Byte Width

The TAXIchip set has twelve parallel interface pins which are designated to carry either Command or Data bits. The Data Mode Select (*DMS*) pin on each chip can be set to select one of three modes of operation: eight Data and four Command bits, nine Data and three Command, or ten Data and two Command. This allows the system designer to select the byte-width which best suits system needs.

Am7968 Encoder/Am7969 Decoder

To guarantee that the Am7969's PLL can stay locked onto an incoming bit stream, the data encoding scheme must provide an adequate number of transitions in each data pattern. This implies a limit on the maximum time allowed between transitions. The TAXIchip set encoding scheme is based on the ANSI X3T9.5 (FDDI) committee's 4-bit/5-bit (4B/5B) code.

An ANSI X3T9.5 system used an 8-bit parallel data pattern. This pattern is divided into two 4-bit nibbles which are each encoded into a 5-bit symbol. Of the thirty-two patterns possible with these five bits, sixteen are chosen to represent the sixteen input Data patterns. Some of the others are used as Command symbols. Those remaining represent invalid patterns that fail either the run-length test or DC balance tests.

Transmitters in 8-bit mode use two 4B/5B encoders to encode eight Data bits into a 10-bit pattern. In 9-bit mode, Transmitters use one 5B/6B encoder and one 4B/5B encoder to code nine Data bits into an 11-bit pattern. In 10-bit mode, two 5B/6B encoders are used to change ten bits of Data into a 12-bit pattern (see Tables 1 and 2 for encoding patterns).

The Am7968 Transmitter further encodes all symbols using NRZI (Non Return to Zero, Invert on Ones). NRZI represents a "1" by a transition and a "0" by the lack of transition. In this system a "1" can be a HIGH-to-LOW or LOW-to-HIGH transition. This combination of 4B/5B and NRZI encoding ensures at least two transitions per symbol and permits a maximum of three consecutive non-transition bit times. The Am7969 then uses the same method to decode incoming symbols so that the whole encoding/decoding process is transparent to the user.

Most Serially transmitted data patterns with this code will have the same average amount of HIGH and LOW times. This near DC balance minimizes pattern-sensitive decoding errors which are caused by jitter in AC-coupled systems.

Operational Modes

In normal operational mode, a single Transmitter/Receiver pair is used to transfer 8, 9, or 10 bits of parallel Data over a private serial link. (On the Am7968, the *TLS* pin is tied to ground and *TSERIN* is left unconnected). On the Am7969, *CNB* must be connected to the CLK output. The Am7969 Receiver continuously deserializes the incoming bit stream, decodes the resulting patterns, and saves parallel data at its output latches (see Figure 3).

Local mode provides a fast and efficient parallel throughout because data can be transferred on every clock cycle. On the other hand, it is not necessary for the host to match the byte rate set by the Transmitter's crystal oscillator; the Am7968 automatically sends a Sync pattern during each clock cycle in which no new Data or Command messages are being transmitted.

Cascade Mode (for –125 only)

For very wide parallel buses, TAXI Receiver's (commercial temperature parts only) can be Cascaded. The Am7969 Receivers all have their *SERIN+* and *SERIN–* pins connected to the media (or an optical data link). *IGM* of each Am7969 is connected to *CNB* of its downstream neighbor or is left unconnected on the Receiver farthest downstream. *CNB* of the first Receiver is tied HIGH, making this device the only Receiver in the chain that can act on the first non-Sync pattern in a message (see below).

Each TAXIchip Receiver monitors the serial link and a special acknowledgment scheme is used to direct symbols into each of the Am7969s. When a Catch-Next-Byte (*CNB*) input is HIGH, the Receiver will capture the next non-Sync symbol from the serial link. At this point, the device forces its I-Got-Mine (*IGM*) pin HIGH to tell the downstream Receiver to capture the next symbol. The Receiver then waits for the Sync symbol or for its *CNB* to be set LOW before transferring the message to its output latch. *IGM* is forced LOW whenever a Sync byte is detected or when *CNB* goes LOW. This *IGM-CNB* exchange continues down the chain until the last Receiver captures its respective byte. The next byte to appear on the serial link will be a Sync symbol which is detected by all of the cascaded Am7969s. On the following Clock cycle their messages are transferred to the output latch of each device and sent to the receiving host. *IGM* pins on all Receivers are also set LOW when the first half of the Sync symbol is detected.

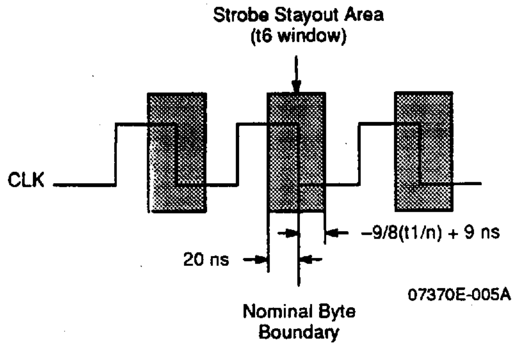
Asynchronous Operation

Inputs to the Am7968 Transmitter Input Latch can be asynchronous to its internal clock. Data *STRB* will latch data into the Am7968 Transmitter and an internal clock will transfer the data to the Encoder Latch at the first byte boundary. Data can be entered at any rate less than the maximum transfer rate without regard to actual byte boundaries. As data rates approach the TAXI BYTE RATE, care must be taken to insure that the 2 BYTE FIFO inside TAXI Transmitter is not over filled. *STRB/ACK* handshake will assure that every byte is transferred correctly. At higher byte rates, where delays and setup/hold times make the *STRB/ACK* handshake impractical, *STRB* should be synchronized with *CLK*.

Synchronous Operation

The Transmitter may be strobed synchronous by tying the strobe to the input clock. When doing this a provision should be make to inhibit the strobe periodically to ensure proper byte alignment. In the absence of a strobe, Syncs will be transmitted on the serial link which will allow the receiver to re-align the byte boundaries. In addition it is essential that the delay between the falling edge of the internal byte clock (CLK) and the rising edge of strobe does not violate t_{BB} specification shown in the SWITCHING CHARACTERISTICS Section.

The internal byte clock controls the flow of data from the input register through the shift register. The falling edge of the internal byte clock delineates the end of one byte from the start of the next. Due to various tolerances in the PLL, the period of the internal byte clock may vary slightly. This effect may cause a shift in the location of the byte boundary with respect to the falling edge of the clock. This variation may move the byte boundary and therefore creates a window during which the part should not be strobed. This window called the t_6 window, is shown in the Figure below. If the part is strobed during the t_6 window data will not be lost however, a sync may be added and the transmitter latency will be increased by one byte time.



Sync Acquisition

In case of errors which cause Am7969 Receivers to lose byte/symbol sync, and on power-up, internal logic detects this loss-re-acquisition of sync and modifies the *CLK* output. *CLK* output is actually a buffered version of the signal which controls Data transfers inside the Am7969 Receiver on byte boundaries. Byte boundaries move when the Am7969 Receiver loses, and re-acquires sync. To protect slave systems (which may use this output as a clock synchronous with the incoming data) from having clocks which are too narrow, the output logic will stretch an output pulse when the pulse would have been less than a byte-time long. The data being processed just prior to this re-acquisition of sync will be lost. The Sync symbol, and all subsequent data will be processed correctly.

TAXI User Test Modes

TLS input can be used to force the Am7968 Transmitter into either of the two Test modes. If *TLS* is open or terminated to approximately Vcc/2 (Test Mode 2), the internal VCO is switched out and everything is clocked directly from the *CLK* input. The serial output data rate will be at the CLK bit rate and not at 10X, 11X, or 12X, as is the case in normal operation. Test Mode 2 will allow testing of the logic in the Latches, Encoder, and Shifter without having to first stabilize the PLL clock multiplier. In Test Mode 1 (*TLS* wired to Vcc), the PLL is enabled and the chip operates normally, except that the output is an NRZ stream (CLK is an input & ACK function is slightly modified). This will allow testing of all functions at full rate without needing to perform match loop tests to accommodate the data inversion characteristics of NRZI.

Differential *SERIN+/SERIN–* inputs can be used to force the Am7969 Receiver into its Test mode. This will allow testing of the logic in the Latches, Decoder, and Shifter without having to first stabilize the the PLL. If *SERIN–* is tied to ground, the internal Vco is switched out and X_1 becomes the internal bit rate clock. The serial data rate will be at the CLK bit rate, not at 10X, 11X, or 12X, as is the case in normal operation. In this mode, *SERIN+* becomes a single-ended serial data input with nominal 100K ECL threshold voltages (Referenced to +5 volts).

These Test Mode switches make the parts determinate, synchronous systems, instead of statistical, asynchronous ones. An automatic test system will be able to clock each part through the functional test patterns at any rate or sequence that is convenient. After the logic has been verified, the part can be put back into the normal mode, and the PLL functions verified knowing that the rest of the chip is functional.

Oscillator

The Am7968 and Am7969 contain an inverting amplifier intended to form the basis of a parallel mode oscillator. The design of this oscillator considered several factors related to its application.

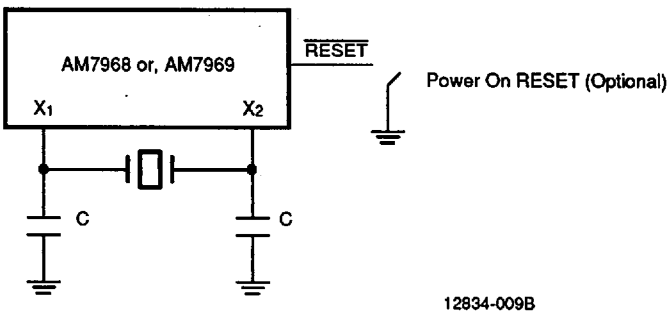
The first consideration is the desired frequency accuracy. This may be subdivided into several areas. An oscillator is considered stable if it is insensitive to variations in temperature and supply voltage, and if it is unaffected by individual component changes and aging. The design of the TAXIchip set is such that the degree to which these goals are met is determined primarily by the choice of external components. Various types of crystal are available and the manufacturers' literature should be consulted to determine the appropriate type. For good temperature stability, zero temperature coefficient capacitors should be used (Type NPO).

The mechanism by which a crystal resonates is electromechanical. This resonance occurs at a fundamental frequency (1st harmonic) and at all odd harmonics of this frequency (even harmonic resonance is not mechanically possible). Unless otherwise constrained, crystal oscillators operate at their fundamental frequencies.

A typical crystal specification for use in this circuit is:

Fundamental Frequency	3.3–17.5 MHz ± 0.1%
Resonance: Mode	Parallel
Load Capacitor (Correlation)	30 pF
Operating Temperature Range	0 to 70°C
Temperature Stability	±100 ppm
Drive Level (Correlation)	2 mW
Effective Series Resistance	25 Ω (max)
Holder Type	Low profile
Aging for 10 years	±10 ppm

It is good practice to ground the case of the crystal to eliminate stray pick-up and keep all connections as short as possible.



C* = 220 pF for 4.0–12.5 MHz crystal, 150 pF for a 12.5–17.5 MHz Crystal.
*C determined by crystal specifications and trace capacities. Values shown are typical.

Figure 1. Connections for 4.0–17.5 MHz

Table 1. TAXIchip Encoder Patterns

4B/5B Encoder Scheme			5B/6B Encoder Scheme		
HEX Data	4-Bit Binary Data	5-Bit Encoded Symbol	HEX Data	5-Bit Binary Data*	6-Bit Encoded Symbol
0	0000	11110	00	00000	110110
1	0001	01001	01	00001	010001
2	0010	10100	02	00010	100100
3	0011	10101	03	00011	100101
4	0100	01010	04	00100	010010
5	0101	01011	05	00101	010011
6	0110	01110	06	00110	010110
7	0111	01111	07	00111	010111
8	1000	10010	08	01000	100010
9	1001	10011	09	01001	110001
A	1010	10110	0A	01010	110111
B	1011	10111	0B	01011	100111
C	1100	11010	0C	01100	110010
D	1101	11011	0D	01101	110011
E	1110	11100	0E	01110	110100
F	1111	11101	0F	01111	110101
			10	10000	111110
			11	10001	011001
			12	10010	101001
			13	10011	101101
			14	10100	011010
			15	10101	011011
			16	10110	011110
			17	10111	011111
			18	11000	101010
			19	11001	101011
			1A	11010	101110
			1B	11011	101111
			1C	11100	111010
			1D	11101	111011
			1E	11110	111100
			1F	11111	111101

*** Note:**

HEX data is parallel input data which is represented by the 4- or 5-bit binary data listed in the column to the immediate right of HEX data. Binary bits are listed from left to right in the following order.

8-Bit Mode: D_7, D_6, D_5, D_4, (4-Bit Binary), and D_3, D_2, D_1, D_0, (4-Bit Binary)

9-Bit Mode: D_8, D_7, D_6, D_5, D_4, (5-Bit Binary), and D_3, D_2, D_1, D_0, (4-Bit Binary)

10-Bit Mode: D_8, D_7, D_6, D_5, D_4, (5-Bit Binary), and D9,D_3, D_2, D_1, D_0, (5-Bit Binary)

Serial bits are shifted out with the most significant bit of the most significant nibble coming out first.

Table 2. TAXIchip Command Symbols

Am7968 Transmitter				Am7969 Receiver	
Command Input				**Command Output**	
HEX	**Binary**	**Encoded Symbol**	**Mnemonic**	**HEX**	**Binary**
8-Bit Mode					
0	0000	XXXXX XXXXX	Data	No Change (Note 2)	No Change (Note 2)
No STRB (Note 1)	No STRB (Note 1)	11000 10001	JK (8-bit Sync)	0	0000
1	0001	11111 11111	I I	1	0001
2	0010	01101 01101	TT	2	0010
3	0011	01101 11001	TS	3	0011
4	0100	11111 00100	I H	4	0100
5	0101	01101 00111	TR	5	0101
6	0110	11001 00111	SR	6	0110
7	0111	11001 11001	SS	7	0111
8 (Note 3)	1000	00100 00100	HH	8	1000
9	1001	00100 11111	HI	9	1001
A (Note 3)	1010	00100 00000	HQ	A	1010
B	1011	00111 00111	RR	B	1011
C	1100	00111 11001	RS	C	1100
D (Note 3)	1101	00000 00100	QH	D	1101
E (Note 3)	1110	00000 11111	Q I	E	1110
F (Note 3)	1111	00000 00000	QQ	F	1111
9-Bit Mode					
0	000	XXXXXX XXXXX	Data	No Change (Note 2)	No Change (Note 2)
No STRB (Note 1)	No STRB (Note 1)	011000 10001	LK (9-bit Sync)	0	000
1	001	111111 11111	I ' I	1	001
2	010	011101 01101	T ' T	2	010
3	011	011101 11001	T'S	3	011
4	100	111111 00100	I' H	4	100
5	101	011101 00111	T'R	5	101
6	110	111001 00111	S'R	6	110
7	111	111001 11001	S'S	7	111
10-Bit Mode					
0	00	XXXXXX XXXXXX	Data	No Change (Note 2)	No Change (Note 2)
No STRB (Note 1)	No STRB (Note 1)	011000 100011	LM (10-bit Sync)	0	00
1	01	111111 111111	I ' I '	1	01
2	10	011101 011101	T ' T '	2	10
3	11	011101 111001	T ' S '	3	11

Notes:

1. Command pattern Sync cannot be explicitly sent by Am7968 Transmitter with any combination of inputs and STRB, but is used to pad between user data.
2. A strobe with all 0s on the Command input lines will cause Data to be sent. See Table 1.
3. While these Commands are legal data and will not disrupt normal operation if used occasionally, they may cause data errors if grouped into recurrent fields. Normal PLL operation cannot be guaranteed if one or more of these commands is continuously repeated.

Am7968 Transmitter Functional Block Description

(Refer to page 1)

Crystal Oscillator/Clock Generator

The serial link speed is derived from a master frequency source (byte rate). This source can either be the built-in Crystal Oscillator, or a clock signal applied through the X_1 pin. This signal is buffered and sent to the *CLK* output when Am7968 Transmitter is in Local mode.

CLK (input is multiplied by ten (8-bit mode), eleven (9-bit mode), or twelve (10-bit mode), using the internal PLL to create the bit rate.

The working frequency can be varied between 3.3 MHz and 17.5 MHz. The crystal frequency required to achieve the maximum 175 Mbaud on the serial link, and the resultant usable data transfer rate will be:

Mode	Crystal Frequency	Am7968-125 Input and Am7969-125 Maximum Parallel Throughput	Internal Divide Ratio
8-Bit	12.50 MHz	80 ns/pattern (100 Mbit/sec)	125/10
9-Bit	11.36 MHz	88 ns/pattern (102 Mbit/sec)	125/11
10-Bit	10.42 MHz	96 ns/pattern (104 Mbit/sec)	125/12
Mode	**Crystal Frequency**	**Am7968-175 Input and Am7969-175 Maximum Parallel Throughput**	**Internal Divide Ratio**
8-Bit	17.50 MHz	57.1 ns/pattern (140 Mbit/sec)	175/10
9-Bit	15.90 MHz	62.8 ns/pattern (143 Mbit/sec)	175/11
10-Bit	14.58 MHz	68.5 ns/pattern (145 Mbit/sec)	175/12

Input Latch

The Am7968's Input Latch accommodates asynchronous strobing of Data and Command by being divided into two stages.

If *STRB* is asserted when both stages are empty, Data or Command bits are transferred directly to the second stage of the Input Latch and *ACK* rises shortly after *STRB*. This pattern is now ready to move to the Encoder Latch at the next falling edge of *CLK*.

An input pattern is strobed into the first stage of the Input Latch only when the second stage is BUSY (contains previously stored data). The Transmitter will be BUSY when *STRB* is asserted a second time in a given *CLK* cycle. Contents of the first stage are not protected from subsequent *STRBs* within the same *CLK* cycle. At the falling edge of *CLK*, previously stored data is transferred from the second stage to the Encoder Latch and the new data is clocked into the second stage of the Input Latch. If in Local mode, *ACK* will rise at this time.

Encoder Latch

Input to the Encoder Latch is clocked by an internal signal which is synchronous with the shifted byte being sent on the serial link. Whenever a new input pattern is strobed into the Input Latch, the data is transferred to the Encoder Latch at the next opportunity.

Data Encoder

Encodes twelve data inputs (8, 9, 10 Data bits or 4, 3, 2 Command inputs) into 10, 11, or 12 bits. The Command data inputs control the transmitted symbol. If all Command inputs are LOW, the symbol for the Data bits will be sent. If Command inputs have any other pattern then the symbol representing that Command will be transmitted.

Shifter

The Shifter is parallel-loaded from the Encoder at the first available byte boundary, and then shifted until the next byte boundary. The Shifter is being serially loaded at all times. As data is being shifted out of the Transmitter, the shifter fills from the LSB. If parallel data is available at the end of the byte, it is parallel-loaded into the Shifter and begins shifting out during the next clock cycle. Otherwise, the serially loaded data fills the next byte. The serial data which loads into the Shifter is generated by an internal state machine which generates a repeating Sync pattern.

Media Interface

The Media Interface is differential ECL, referenced to +5 V. It is capable of driving lines terminated with 50 Ω to (Vcc - 2.0) volts.

Am7969 Receiver Functional Block Description

(Refer to page 1)

Crystal Oscillator/Clock Generator

The data recovery PLL in the Am7969 must be supplied with a reference frequency at the expected byte rate of the data to be recovered. The source of this frequency can either be the built-in Crystal Oscillator, or an external clock signal applied through the X_1 pin. The reference frequency source is then multiplied by ten (8-bit mode), eleven (9-bit mode) or twelve (10-bit mode) using an internal PLL.

Media Interface

SERIN+, SERIN– inputs are to be driven by differential ECL voltages, referenced to +5 V. Serial data at these inputs will serve as the reference for PLL tracking.

PLL Clock Generator

A PLL Clock recovery loop follows the incoming data and allows the encoded clock and data stream to be decoded into a separated clock and data pattern. It uses the crystal oscillator and clock generator to predict the expected frequency of data and will track jittered data with a characteristically small offset frequency.

Shifter

The Shifter is serially loaded from the Media Interface, using the bit clock generated by PLL.

Byte Sync Logic

The incoming data stream is a continuous stream of data bits, without any significant signal which denotes byte boundaries. This logic will continuously monitor the data stream, and upon discovering the reserved code used for Am7969 Receiver Sync, will initialize a synchronous counter which counts bits, and indicates byte boundaries.

The logic signal that times data transfers from the Shifter to the Decoder Latch is buffered and sent to the *CLK* output. *CLK* output from the Receiver is not suitable as a frequency source for another TAXI Transmitter or Receiver. It is intended to be used by the host system as a clock synchronous with the received data. This output is synchronous with the byte boundary and is synchronous with the Receiver's internal byte clock.

Byte Sync Logic is responsible for generating the internal strobe signals for Parallel Output Latches. It also generates the *IGM* (I-Got-Mine) signal in Test mode when the first byte after a Sync symbol is transferred.

Parallel outputs are made on a byte boundary, after *CNB* falls, or when Sync is detected.

The I-Got-Mine (*IGM*) signal will fall when the first half of a Sync is detected in the Shifter or when *CNB* goes LOW. It will remain LOW until the first half of a non-Sync byte is detected in the Shifter, whereupon it will rise (assuming that the *CNB* input is HIGH). A continuous stream of normal data or command bytes will cause *IGM* to go HIGH and remain HIGH. A continuous stream of Sync's will cause *IGM* to stay LOW. *IGM* will go HIGH during the byte before data appears at the output. This feature could be used to generate an early warning of incoming data.

Decoder Latch

Data is loaded from the Shifter to this latch at each symbol/byte boundary. It serves as the input to the Data Decoder.

Data Decoder

Decodes ten, eleven, or twelve data inputs into twelve outputs. In 8-bit mode, data is decoded into either an 8-bit Data pattern or a 4-bit Command pattern. In 9-bit mode, data is decoded into either a 9-bit Data pattern or a 3-bit Command pattern. In 10-bit mode, data is decoded into either a 10-bit Data pattern or a 2-bit Command pattern.

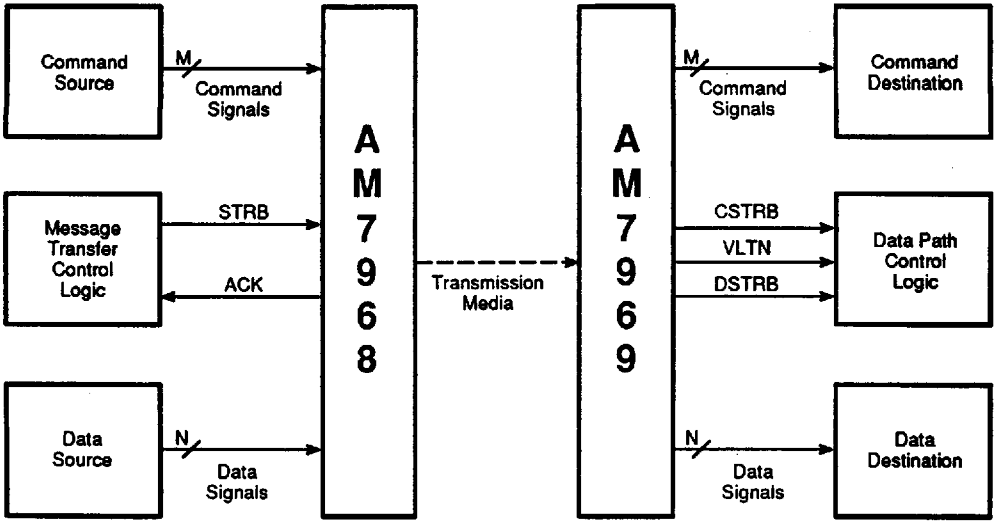
The decoder separates Data symbols from Command symbols, and causes the appropriate strobe output to be asserted.

Parallel Output Latch

Output Latch will be clocked by the byte clock, and will reflect the most recent data on the link. Any Data pattern will be latched to the Data outputs and will not affect the status of the Command outputs. Likewise, any Command pattern will be latched to the Command outputs without affecting the state of the Data outputs.

Any data transfer, either Data or Command will be synchronous with an appropriate output strobe. However, there will be *CSTRBs* when there is no active data on the link, since Sync is a valid Command code.

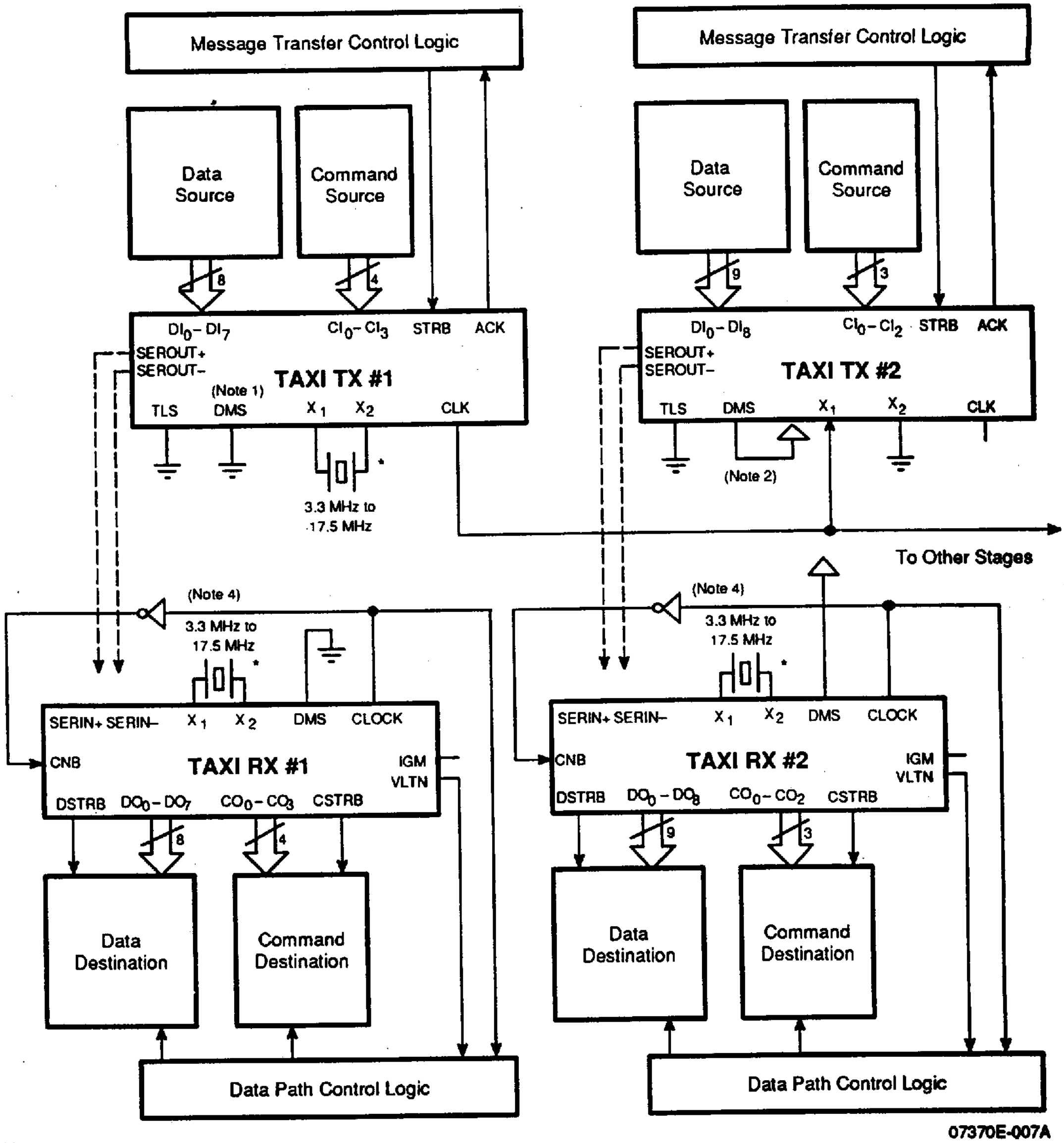
Any pattern which does not decode to a valid Command or Data pattern is flagged as a violation. The output of the decoder during these violations is indeterminate and will result in either a *CSTRB* or *DSTRB* output when the indeterminate pattern is transferred to the output latch.



Note:

N can be 8, 9, or 10 bits of parallel data; total of N + M = 12.

Figure 2. TAXIchip System Block Diagram



Notes:

1. DMS = GND = 8 Bit Mode   TLS = GND = Local Mode   Pin 11 = Don't Connect = Local Mode
2. DMS = V_{CC} = 9 Bit Mode   TLS = GND = Local Mode   Pin 11 = Don't Connect = Local Mode
3. Two 8-bit local mode systems in parallel will result in an effective data rate of 200 Mbps.
4. Use inverter for operation above 140 MHz only.

*Alternatively, the X_1 inputs may be driven by external TTL frequency sources.

Figure 3. TAXIchip System in Local Mode

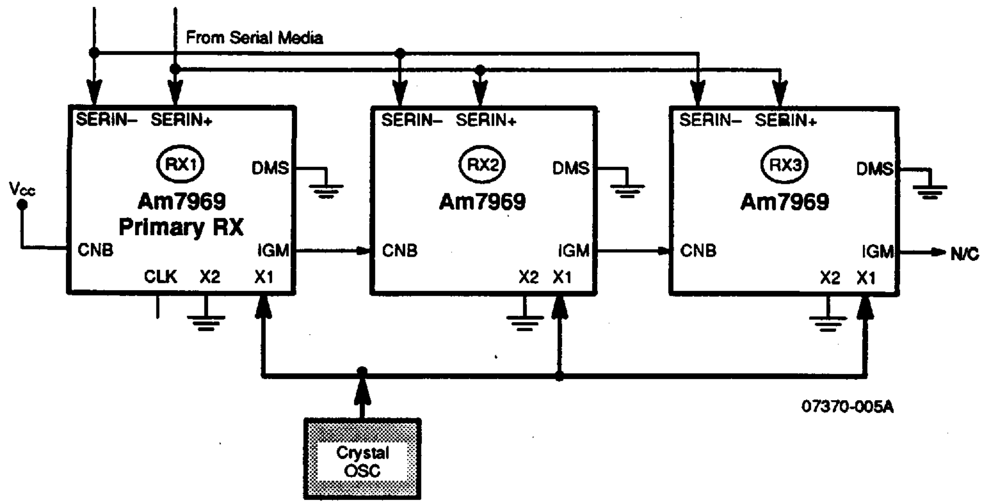


Figure 4. Cascaded Receiver Clock Connections (Commercial –125 only)

Am7968/Am7969-125

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Ambient Temperature Under Bias	–55 to +125°C
Supply Voltage to Ground Potential Continuous	–0.5 to +7.0 V
DC Voltage Applied to Outputs	–0.5 V to V_{CC} Max.
DC Input Voltage	–0.5 to +5.5 V
DC Output Current	±100 mA
DC Input Current	–30 to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_A)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Am7968-125 TAXIchip Transmitter

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
Bus Interface Signals: DI_0–DI_7, DI_8/CI_3, DI_9/CI_2, CI_0–CI_1, STRB, ACK, CLK						
V_{OH1}	Output HIGH Voltage ACK	V_{CC} = Min., I_{OH} = –1 mA, V_{IN} = 0 or 3 V		2.4		V
V_{OH2}	Output HIGH Voltage CLK	V_{CC} = Min., I_{OH} = –3 mA, V_{IN} = 0 or 3 V		2.4		V
V_{OL}	Output LOW Voltage ACK, CLK	V_{CC} = Min., I_{OL} = 8 mA, V_{IN} = 0 or 3 V			0.45	V
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 9)		2.0		V
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 9)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min. I_{IN} = –18 mA			–1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			–400	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50	µA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V	All Inputs Except CLK		50	µA
			CLK Input		150	µA
I_{SC}	Output Short Circuit Current ACK, CLK	(Note 4)		–15	–85	mA
Serial Interface Signals: SEROUT+, SEROUT–						
V_{OH}	Output HIGH Voltage	V_{CC} = Min. ECL Load		V_{CC} –1.025	V_{CC} –0.88	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. ECL Load		V_{CC} –1.81	V_{CC} –1.62	V
Miscellaneous Signals: X_1, V_{CC1}, V_{CC2}, V_{CC3}						
V_{IHX}	Input HIGH Voltage X_1			2.0		V
V_{ILX}	Input LOW Voltage X_1				0.8	V
I_{ILX}	Input LOW Current X_1	V_{IN} = 0.45 V			–900	µA
I_{IHX}	Input HIGH Current X_1	V_{IN} = 2.4 V			+600	µA
I_{CC}	Supply Current	SEROUT = ECL Load, DMS = 0, V_{CC1} = V_{CC2} = V_{CC3} = Max.	Pin V_{CC1} (TTL)		20	mA
			Pin V_{CC2} (ECL)		45	mA
			Pin V_{CC3} (CML)		200	mA

*See notes following end of Switching Characteristics tables.

Am7969-125 TAXIchip Receiver

Parameter Symbol	Parameter Description	Test Conditions (Note 1)	Min.	Max.	Unit
Bus Interface Signals: DO_0–DO_7, DO_8/CO_3, DO_9/CO_2, CO_0–CO_1, DSTRB, CSTRB, IGM, CLK, CNB, VLTN					
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1 mA V_{IN} = 0 or 3 V	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA V_{IN} = 0 or 3 V		0.45	V
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 9)	2.0		V
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 9)		0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA		–1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V		–400	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V		50	µA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V		50	µA
I_{SC}	Output Short Circuit Current (Note 4)		–15	–85	mA
Serial Interface Signals: SERIN+, SERIN–					
V_{IHS}	Input HIGH Voltage SERIN+	(Notes 9, 21)	V_{CC} –1.165	V_{CC} –0.88	V
V_{ILS}	Input LOW Voltage SERIN+	(Notes 9, 21)	V_{CC} –1.81	V_{CC} –1.475	V
V_{THT}	Test Mode Threshold SERIN–	V_{CC} = Max.		0.25	V
V_{DIF}	Differential Input Voltage		0.3	1.1	V
V_{ICM}	Input Common Mode Voltage	(Note 6)	3.05	V_{CC} –0.55	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{CC} –1.81 V	0.5		µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} –0.88 V		220	µA
Miscellaneous Signals: X_1, V_{CC1}, V_{CC2}					
V_{IHX}	Input HIGH Threshold X_1		2.0		V
V_{ILX}	Input LOW Threshold X_1			0.8	V
I_{ILX}	Input LOW Current X_1	V_{IN} = 0.45 V		–900	µA
I_{IHX}	Input HIGH Current X_1	V_{IN} = 2.4 V		+600	µA
I_{CC}	Supply Current	V_{CC1} = V_{CC2} = Max. — Pin V_{CC1} (TTL)		50	mA
		DMS = 0 V — Pin V_{CC2} (CML)	20	300	mA

SWITCHING CHARACTERISTICS (Note 20)

Am7968-125 TAXIchip Transmitter (Notes 10, 13, 22)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
Bus Interface Signals: DI_0–DI_7, DI_8/CI_3, DI_9/CI_2, CI_0–CI_1, STRB, ACK, CLK						
1	t_P	CLK Period		8n	25n	ns
2	t_{PW}	CLK Pulse Width HIGH		30		ns
3	t_{PW}	CLK Pulse Width LOW		30		ns
4	t_{PW}	STRB Pulse Width HIGH (Note 7)		15		ns
5	t_{PW}	STRB Pulse Width LOW		15		ns
6	t_{BB}	Internal Byte Boundary to CLK↓ (Note 11)		$\frac{-9t_1}{8n}+9$	20	ns
9	t_S	Data–STRB Setup Time		5		ns
10	t_H	Data–STRB Hold Time		15		ns
11	t_H	ACK↑ to STRB↓ Hold (Note 8)	TTL Output Load	0		ns
12	t_H	ACK↓ to STRB↑ Hold	TTL Output Load	0		ns
13	t_{PD}	STRB↑ to ACK↑ (Note 18)	TTL Output Load		40	ns
14	t_{PD}	STRB↓ to ACK↓	TTL Output Load		23	ns
15	t_{PD}	CLK↓ to ACK↑ (Note 18)	TTL Output Load		$\frac{3t_1}{n}+33$	ns
Serial Interface Signals: SEROUT+, SEROUT– (Note 2)						
22	$t_{SK}^{\dagger}$	SEROUT± Skew	ECL Output Load	–200	+200	ps
23	$t_R^{\dagger}$	SEROUT± Output Rise Time	ECL Output Load	.45	2	ns
24	$t_F^{\dagger}$	SEROUT± Output Fall Time	ECL Output Load	.45	2	ns
26	$t_{PW}^{\dagger}$	SEROUT ± Pulse Width LOW	ECL Output Load	$\frac{t_1}{n}-5\%$	$\frac{t_1}{n}+5\%$	ns
27	$t_{PW}^{\dagger}$	SEROUT ± Pulse Width HIGH	ECL Output Load	$\frac{t_1}{n}-5\%$	$\frac{t_1}{n}+5\%$	ns
Miscellaneous Signals: X_1 (Note 15)						
29	t_{PW}	X_1 Pulse Width HIGH (Note 12)	TTL Output Load on CLK	35		ns
30	t_{PW}	X_1Pulse Width LOW (Note 12)	TTL Output Load on CLK	35		ns
32	t_{PD}	X_1↑ to CLK↑	TTL Load		32	ns
33	t_{PD}	X_1↓ to CLK↓	TTL Load		32	ns

Am7969-125 TAXIchip Receiver (Notes 13, 14, 22)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Bus Interface Signals:		**DO0–DO7,DO8/CO3,DO9/CO2,CO0–CO1,DSTRB,CSTRB, IGM,CLK,CNB,VLTN**				
35	t_P	CLK Period (Note 24)		8n	25n	ns
36	t_{PD}	Data Valid to STRB↑ Delay	TTL Output Load	$\frac{2t_{35}}{n}$		ns
37	t_{PD}	CLK↓ to STRB↑	TTL Output Load		$\frac{2t_{35}}{n}+15$	ns
38	t_{PD}	CLK↑ to STRB↓	TTL Output Load	$\frac{t_{35}}{n}-7$		ns
38a	t_{PD}	STRB↑ to CLK↑ (Note 23)	TTL Output Load	$\frac{3t_{35}}{n}-14$		ns
39	t_{PD}	CLK↓ to Data Valid Delay	TTL Output Load		$-\left(\frac{t_{35}}{n}\right)+23$	ns
40	t_{PW}	STRB Pulse Width HIGH	TTL Output Load	$\frac{5t_{35}}{2n}$	$\frac{5t_{35}}{n}$	ns
41	t_{PW}	CLK Pulse Width HIGH	TTL Output Load	$\frac{5t_{35}}{n}-15$		ns
42	t_{PW}	CLK Pulse Width LOW	TTL Output Load	$\frac{5t_{35}}{n}-15$		ns
43	t_{PD}	SERIN to CLK↓ Delay	TTL Output Load	$\frac{t_{35}}{2n}+17$	$\frac{2t_{35}}{n}+26$	ns
44	t_{PD}	CLK↑ to IGM↓	TTL Output Load		$\frac{2t_{35}}{n}+7$	ns
45	t_{PD}	CLK↑ to IGM↑	TTL Output Load		$\frac{2t_{35}}{n}+10$	ns
46	t_{PD}	CNB↓ to IGM↓	TTL Output Load		20	ns
47	t_S	CNB↑ to CLK↑ Setup Time (Note 5)		$-\left(\frac{2t_{35}}{n}-32\right)$		ns
47A	t_S	CNB↓ to CLK↑ Setup Time (Note 19)		$-\left(\frac{t_{35}}{n}-31\right)$		ns
48	t_H	CNB↓ to CLK↑ Hold		$\frac{2t_{35}}{n}+5$		ns
49	t_{PW}	CNB Pulse Width LOW		$\frac{2t_{35}}{n}$		ns
Serial Interface Signals:		**SERIN+, SERIN–**				
57	t_J†	SERIN± Peak to Peak Input Jitter Tolerance (Note 16)			5	ns
Miscellaneous Signals:		**X_1 (Note 15)**				
60	t_{PW}	X_1 Pulse Width HIGH		35		ns
61	t_{PW}	X_1 Pulse Width LOW		35		ns

Am7968/Am7969-175
ABSOLUTE MAXIMUM RATINGS

StorageTemperature	–65 to + 50°C
Ambient Temperature Under Bias	–55 to +125°C
Supply Voltage to Ground Potential Continuous	–0.5 to +7.0 V
DC Voltage Applied to Outputs	–0.5 V to V_{CC} Max.
DC Input Voltage	–0.5 to +5.5 V
DC Output Current	+100 mA
DC Input Current	–30 to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Temperature (T_C)	0 to +70°C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Am7968-175 TAXIchip Transmitter

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
Bus Interface Signals: DI_0–DI_7, DI_8/CI_3, DI_9/CI_2, CI_0–CI_1, STRB, ACK, CLK						
V_{OH1}	Output HIGH Voltage ACK	V_{CC} = Min., I_{OH} = –1 mA V_{IN} = 0 or 3 V		2.4		V
V_{OH2}	Output HIGH Voltage CLK	V_{CC} = Min., I_{OH} = –3 mA V_{IN} = 0 or 3 V		2.4		V
V_{OL}	Output LOW Voltage ACK, CLK	V_{CC} = Min., I_{OL} = 8 mA V_{IN} = 0 or 3 V			0.45	V
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 9)		2.0		V
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 9)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min. I_{IN} = –18 mA			–1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			–400	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50	µA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V	All Inputs Except CLK		50	µA
			CLK Input		150	µA
I_{SC}	Output Short Circuit Current ACK, CLK	(Note 4)		–15	–85	mA
Serial Interface Signals: SEROUT+, SEROUT–						
V_{OH}	Output HIGH Voltage	V_{CC} = Min. ECL Load		V_{CC} –1.025	V_{CC} –0.88	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. ECL Load		V_{CC} –1.81	V_{CC} –1.62	V
Miscellaneous Signals: X_1, V_{CC1}, V_{CC2}, V_{CC3}						
V_{IHX}	Input HIGH Voltage X_1			2.0		V
V_{ILX}	Input LOW Voltage X_1				0.8	V
I_{ILX}	Input LOW Current X_1	V_{IN} = 0.45 V			–900	µA
I_{IHX}	Input HIGH Current X_1	V_{IN} = 2.4 V			+600	µA
I_{CC}	Supply Current	SEROUT = ECL Load, DMS = 0 V_{CC1} = V_{CC2} = V_{CC3} = Max.	Pin V_{CC1} (TTL)		20	mA
			Pin V_{CC2} (ECL)		45	mA
			Pin V_{CC3} (CML)		200	mA

*See notes following end of Switching Characteristics tables.

Am7969-175 TAXIchip Receiver

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
Bus Interface Signals: DO_0–DO_7, DO_8/CO_3, DO_9/CO_2, CO_0–CO_1, DSTRB, CSTRB, IGM, CLK, CNB, VLTN						
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1 mA V_{IN} = 0 or 3 V		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA V_{IN} = 0 or 3 V			0.45	V
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 9)		2.0		V
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 9)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			–400	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50	μA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V			50	μA
I_{SC}	Output Short Circuit Current (Note 4)			–15	–85	mA
Serial Interface Signals: SERIN+, SERIN–						
V_{IHS}	Input HIGH Voltage SERIN+	(Notes 9, 21)		V_{CC} –1.165	V_{CC} –0.88	V
V_{ILS}	Input LOW Voltage SERIN+	(Notes 9, 21)		V_{CC} –1.81	V_{CC} –1.475	V
V_{THT}	Test Mode Threshold SERIN–	V_{CC} = Max.			0.25	V
V_{DIF}	Differential Input Voltage			0.3	1.1	V
V_{ICM}	Input Common Mode Voltage	(Note 6)		3.05	V_{CC} –0.55	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{CC} –1.81 V		0.5		μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} –0.88 V			220	μA
Miscellaneous Signals: X_1, V_{CC1}, V_{CC2}						
V_{IHX}	Input HIGH Threshold X_1			2.0		V
V_{ILX}	Input LOW Threshold X_1				0.8	V
I_{ILX}	Input LOW Current X_1	V_{IN} = 0.45 V			–900	μA
I_{IHX}	Input HIGH Current X_1	V_{IN} = 2.4 V			+600	μA
I_{CC}	Supply Current	V_{CC1} = V_{CC2} = Max.	Pin V_{CC1} (TTL)		50	mA
		DMS = 0 V	Pin V_{CC2} (CML)		300	mA

SWITCHING CHARACTERISTICS (Note 20)

Am7968-175 TAXIchip Transmitter (Notes 10, 13, 22)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
Bus Interface Signals: DI_0–DI_7, DI_8/CI_3, DI_9/CI_2, CI_0–CI_1, STRB, ACK, CLK						
1	t_P	CLK Period		5.7 n	8 n	ns
2	t_{PW}	CLK Pulse Width HIGH		20		ns
3	t_{PW}	CLK Pulse Width LOW		20		ns
4	t_{PW}	STRB Pulse Width HIGH (Note 7)		15		ns
5	t_{PW}	STRB Pulse Width LOW		15		ns
6	t_{BB}	Internal Byte Boundary to CLK↓ (Note 11)		$\frac{-9t_1}{8n}+9$	20	ns
9	t_S	Data–STRB Setup Time		5		ns
10	t_H	Data–STRB Hold Time		15		ns
11	t_H	ACK↑ to STRB↓ Hold (Note 8)	TTL Output Load	0		ns
12	t_H	ACK↓ to STRB↑ Hold	TTL Output Load	0		ns
13	t_{PD}	STRB↑ to ACK↑ (Note 18)	TTL Output Load		40	ns
14	t_{PD}	STRB↓ to ACK↓	TTL Output Load		23	ns
15	t_{PD}	CLK↓ to ACK↑ (Note 18)	TTL Output Load		$\frac{3t_1}{n}+33$	ns
Serial Interface Signals: SEROUT+, SEROUT– (Note 2)						
22	$t_{SK}^{\dagger}$	SEROUT± Skew	ECL Output Load	–200	+200	ps
23	$t_R^{\dagger}$	SEROUT± Output Rise Time	ECL Output Load	.45	2	ns
24	$t_F^{\dagger}$	SEROUT± Output Fall Time	ECL Output Load	.45	2	ns
26	$t_{PW}^{\dagger}$	SEROUT ± Pulse Width LOW	ECL Output Load	$\frac{t_1}{n}-5\%$	$\frac{t_1}{n}+5\%$	ns
27	$t_{PW}^{\dagger}$	SEROUT ± Pulse Width HIGH	ECL Output Load	$\frac{t_1}{n}-5\%$	$\frac{t_1}{n}+5\%$	ns
Miscellaneous Signals: X_1 (Note 15)						
29	t_{PW}	X_1 Pulse Width HIGH (Note 12)	TTL Output Load on CLK	24		ns
30	t_{PW}	X_1 Pulse Width LOW (Note 12)	TTL Output Load on CLK	24		ns
32	t_{PD}	X_1↑ to CLK↑	TTL Load		32	ns
33	t_{PD}	X_1↓ to CLK↓	TTL Load		32	ns

Am7969-175 TAXIchip Receiver (Notes 13, 14, 22)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Bus Interface Signals: DO0–DO7, DO8/CO3, DO9/CO2, CO0–CO1, DSTRB, CSTRB, IGM, CLK, CNB, VLTN						
35	t_P	CLK Period (Note 24)		5.7 n	8 n	ns
36	t_{PD}	Data Valid to STRB↑ Delay	TTL Output Load	$\frac{2t_{35}}{n} - 2$		ns
37	t_{PD}	CLK↓ to STRB↑	TTL Output Load		$\frac{2t_{35}}{n} + 15$	ns
38	t_{PD}	CLK↑ to STRB↓	TTL Output Load	$\frac{t_{35}}{n} - 5$		ns
38a	t_{PD}	STRB↑ to CLK↑ (Note 23)	TTL Output Load	$\frac{3t_{35}}{n} - 10$		ns
39	t_{PD}	CLK↓ to Data Valid Delay	TTL Output Load		$-\left(\frac{t_{35}}{n}\right) + 23$	ns
40	t_{PW}	STRB Pulse Width HIGH	TTL Output Load	$\frac{5t_{35}}{2n}$	$\frac{5t_{35}}{n}$	ns
41	t_{PW}	CLK Pulse Width HIGH	TTL Output Load	$\frac{5t_{35}}{n} - 7$		ns
42	t_{PW}	CLK Pulse Width LOW	TTL Output Load	$\frac{5t_{35}}{n} - 4$		ns
43	t_{PD}	SERIN to CLK↓ Delay	TTL Output Load	$\frac{t_{35}}{2n} + 17$	$\frac{2t_{35}}{n} + 26$	ns
47A	t_S	CNB↓ to CLK↑ Setup Time (Note 19)		$-\left(\frac{t_{35}}{n} - 31\right)$		ns
47B	t_S	CNB↑ to CLK↓ Setup Time		29		ns
48	t_H	CNB↓ to CLK↑ Hold		$\frac{2t_{35}}{n} - 3$		ns
49	t_{PW}	CNB Pulse Width LOW		$\frac{2t_{35}}{n}$		ns
Serial Interface Signals: SERIN+, SERIN–						
57	$t_J^{\dagger}$	SERIN± Peak to Peak Input Jitter Tolerance (Note 16)			2	ns
Miscellaneous Signals: X_1 (Note 15)						
60	t_{PW}	X_1 Pulse Width HIGH		21		ns
61	t_{PW}	X_1 Pulse Width LOW		21		ns

Am7968/Am7969-125 MILITARY

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65 to +150°C
Ambient Temperature Under Bias	–55 to +125°C
Supply Voltage to Ground Potential Continuous	–0.5 to +7.0 V
DC Voltage Applied to Outputs	–0.5 V to V_{CC} Max.
DC Input Voltage	–0.5 to +5.5 V
DC Output Current	±100 mA
DC Input Current	–30 to +5.0 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Military (CPL) Devices

Am7968-125 V/LMC	
Am7968-125 V/DMC	
Am7969-125 V/LMC	
Am7969-125 V/DMC	
Temperature (T_C)	–55 to +125° C
Supply Voltage (V_{CC})	+4.75 to +5.5 V
Am7968-125/LKC	
Am7968-125/DKC	
Am7969-125/LKC	
Am7969-125/DKC	
Temperature (T_C)	–30 to +125° C
Supply Voltage (V_{CC})	+4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified (for CPL Products Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Am7968-125 Military TAXIchip Transmitter

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
Bus Interface Signals: DI_0–DI_7, DI_8/CI_3, DI_9/CI_2, CI_0–CI_1, STRB, ACK, CLK						
V_{OH1}	Output HIGH Voltage ACK	V_{CC} = Min., I_{OH} = –1 mA V_{IN} = 0 or 3 V		2.4		V
V_{OH2}	Output HIGH Voltage CLK	V_{CC} = Min., I_{OH} = –1 mA V_{IN} = 0 or 3 V		2.4		V
V_{OL}	Output LOW Voltage ACK, CLK	V_{CC} = Min., I_{OL} = 8 mA V_{IN} = 0 or 3 V			0.45	V
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 9)	T_C = –30 to +125°C	2.0		V
			T_C = –55 to +125°C	2.1		V
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 9)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min. I_{IN} = –18 mA			–1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			–400	µA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50	µA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V	All Inputs Except CLK		50	µA
			CLK Input		150	µA
I_{SC}	Output Short Circuit Current ACK, CLK	(Note 4)		–15	–85	mA
Serial Interface Signals: SEROUT+, SEROUT–						
V_{OH}	Output HIGH Voltage	V_{CC} = Min. ECL Load		V_{CC} –1.165	V_{CC} –0.88	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. ECL Load		V_{CC} –1.81	V_{CC} –1.62	V
Miscellaneous Signals: X_1, V_{CC1}, V_{CC2}, V_{CC3}						
V_{IHX}	Input HIGH Voltage X_1	V_{CC} = Max. (Note 9)	T_C = –30 to +125°C	2.0		V
			T_C = –55 to +125°C	2.1		V
V_{ILX}	Input LOW Voltage X_1				0.8	V
I_{ILX}	Input LOW Current X_1	V_{IN} = 0.45 V			–900	µA
I_{IHX}	Input HIGH Current X_1	V_{IN} = 2.4 V			+600	µA
I_{CC}	Supply Current	SEROUT = ECL Load, DMS = 0 V_{CC1} = V_{CC2} = V_{CC3} = Max.	Pin V_{CC1} (TTL)		30	mA
			Pin V_{CC2} (ECL)		45	mA
			Pin V_{CC3} (CML)		215	mA

*See notes following end of Switching Characteristics tables.

Am7969-125 Military TAXIchip Receiver

Parameter Symbol	Parameter Description	Test Conditions (Note 1)		Min.	Max.	Unit
Bus Interface Signals: DO_0–DO_7, DO_8/CO_3, DO_9/CO_2, CO_0–CO_1, DSTRB, CSTRB, IGM, CLK, CNB, VLTN						
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1 mA V_{IN} = 0 or 3 V		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA V_{IN} = 0 or 3 V			0.45	V
V_{IH}	Input HIGH Voltage	V_{CC} = Max. (Note 9)		2.0		V
V_{IL}	Input LOW Voltage	V_{CC} = Max. (Note 9)			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min., I_{IN} = –18 mA			–1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.4 V			–400	μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7 V			50	μA
I_I	Input Leakage Current	V_{CC} = Max., V_{IN} = 5.5 V			50	μA
I_{SC}	Output Short Circuit Current (Note 4)			–15	–85	mA
Serial Interface Signals: SERIN+, SERIN–						
V_{IHS}	Input HIGH Voltage SERIN+	(Notes 9, 21)		V_{CC} –1.165	V_{CC} –0.88	V
V_{ILS}	Input LOW Voltage SERIN+	(Notes 9, 21)		V_{CC} –1.81	V_{CC} –1.475	V
V_{THT}	Test Mode Threshold SERIN–	V_{CC} = Max.			0.25	V
V_{DIF}	Differential Input Voltage			0.3	1.1	V
V_{ICM}	Input Common Mode Voltage	(Note 6)		3.05	V_{CC} –0.55	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = V_{CC} –1.81 V		0.5		μA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC} –0.88 V			220	μA
Miscellaneous Signals: X_1, V_{CC1}, V_{CC2}						
V_{IHX}	Input HIGH Threshold X_1			2.0		V
V_{ILX}	Input LOW Threshold X_1				0.8	V
I_{ILX}	Input LOW Current X_1	V_{IN} = 0.45 V			–900	μA
I_{IHX}	Input HIGH Current X_1	V_{IN} = 2.4 V			+600	μA
I_{CC}	Supply Current	V_{CC1} = V_{CC2} = Max.	Pin V_{CC1} (TTL)		55	mA
		DMS = 0 V	Pin V_{CC2} (CML)		335	mA

SWITCHING CHARACTERISTICS over operating range unless otherwise specified (Note 20) (for CPL Products Group A, Subgroups 9, 10, and 11 are tested unless otherwise noted)

Am7968-125 Military TAXIchip Transmitter (Notes 10, 13, 22)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
Bus Interface Signals: DI_0–DI_7, DI_8/CI_3, DI_9/CI_2, CI_0–CI_1, STRB, ACK, CLK						
1	t_P	CLK Period		8 n	25 n	ns
2	t_{PW}	CLK Pulse Width HIGH		25		ns
3	t_{PW}	CLK Pulse Width LOW		25		ns
4	t_{PW}	STRB Pulse Width HIGH (Note 7)		20		ns
5	t_{PW}	STRB Pulse Width LOW		20		ns
6	t_{BB}	Internal Byte Boundary to CLK↓ (Note 11)		$\frac{-9t_1}{8n}+3$	25	ns
9	t_S	Data–STRB Setup Time		10		ns
10	t_H	Data–STRB Hold Time		15		ns
11	t_H	ACK↑ to STRB↓ Hold (Note 8)	TTL Output Load	0		ns
12	t_H	ACK↓ to STRB↑ Hold	TTL Output Load	0		ns
13	t_{PD}	STRB↑ to ACK↑ (Note 18)	TTL Output Load		45	ns
14	t_{PD}	STRB↓ to ACK↓	TTL Output Load		25	ns
15	t_{PD}	CLK↓ to ACK↑ (Note 18)	TTL Output Load		$\frac{3t_1}{n}+43$	ns
Miscellaneous Signals: X_1 (Note 15)						
29	t_{PW}	X_1 Pulse Width HIGH (Note 12)	TTL Output Load on CLK	35		ns
30	t_{PW}	X_1 Pulse Width LOW (Note 12)	TTL Output Load on CLK	35		ns
32	t_{PD}	X_1↑ to CLK↑	TTL Load		32	ns
33	t_{PD}	X_1↓ to CLK↓	TTL Load		32	ns

Am7969-125 Military TAXIchip Receiver (Notes 13, 14, 22)

No.	Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Bus Interface Signals: DO0–DO7, DO8/CO3, DO9/CO2, CO0–CO1, DSTRB, CSTRB, IGM, CLK, CNB, VLTN						
35	t_P	CLK Period (Note 24)		8 n	25 n	ns
36	t_{PD}	Data Valid to STRB↑ Delay	TTL Output Load	$\frac{2t_{35}}{n}$		ns
37	t_{PD}	CLK↓ to STRB↑	TTL Output Load		$\frac{2t_{35}}{n}+15$	ns
38	t_{PD}	CLK↑ to STRB↓	TTL Output Load	$\frac{t_{35}}{n}-7$		ns
38a	t_{PD}	STRB↑ to CLK↑ (Note 23)	TTL Output Load	$\frac{3t_{35}}{n}-14$		ns
39	t_{PD}	CLK↓ to Data Valid Delay	TTL Output Load		$-\left(\frac{t_{35}}{n}\right)+23$	ns
40	t_{PW}	STRB Pulse Width HIGH	TTL Output Load	$\frac{5t_{35}}{2n}$	$\frac{5t_{35}}{n}$	ns
41	t_{PW}	CLK Pulse Width HIGH	TTL Output Load	$\frac{5t_{35}}{n}-15$		ns
42	t_{PW}	CLK Pulse Width LOW	TTL Output Load	$\frac{5t_{35}}{2n}-15$		ns
43	t_{PD}	SERIN to CLK↓ Delay	TTL Output Load	$\frac{t_{35}}{2n}+17$	$\frac{2t_{35}}{2n}+26$	ns
Serial Interface Signals: SERIN+, SERIN–						
57	t_J†	SERIN± Peak to Peak Input Jitter Tolerance (Note 16)			5	ns
Miscellaneous Signals: X_1 (Note 15)						
60	t_{PW}	X_1 Pulse Width HIGH		35		ns
61	t_{PW}	X_1 Pulse Width LOW		35		ns

Note:
CLK (pin 19) must be connected to CNB (pin 24).

Notes: *

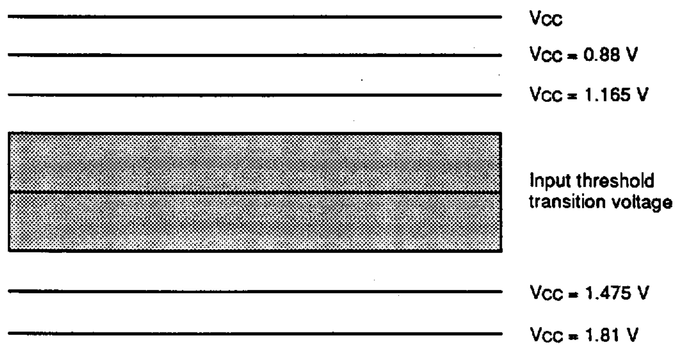
1. For conditions shown as Min. or Max., use the appropriate value specified under operating range.
2. The clock fall to serial output delay is typically 3 bit times.
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. If the CNB↑ to CLK↑ setup time is violated, IGM will stay LOW.
6. Voltage applied to either SERIN± pins must not be above V_{CC} nor below +2.5 V to assure proper operation.
7. t_4 guarantees that data is latched. ACK (t_{11}) timing may not be valid.
8. If t_{11} is not met, ACK response and timing are not guaranteed, but data will still be latched on STRB↑ (see t_4).
9. Measured with device in Test mode while monitoring output logic states.
10. For the TAXI Transmitter, "n" is determined by the following table:

DMS	TLS	"n"
GND	OPEN	n = 1; 8 Bit Test Mode 2
	GND/VCC	n = 10; 8 Bit Local/Test Mode 1
VCC	OPEN	n = 1; 9 Bit Test Mode 2
	GND/VCC	n = 11; 9 Bit Local/Test Mode 1
Open or $\frac{1}{2}$ VCC	OPEN	n = 1; 10 Bit Test Mode 2
	GND/VCC	n = 12; 10 Bit Local/Test Mode 1

11. t_6 (Internal Byte Boundary to CLK↓) is created by the variation of internal STRB propagation delays relative to internal byte boundaries over temperatures and V_{CC}. The internal byte boundary determines the byte in which data will come out (SEROUT±). If STRB occurs before the byte boundary, then the data will be sent out two bytes later. If STRB occurs after the byte boundary, then the output data will be delayed by one additional byte.
12. X_1 Pulse Width is measured at a point where CLK output equals t_2 or t_3.
13. For the TAXI Transmitter, 'Data' is either $DI_0 - DI_7$, DI_8/CI_3, DI_9/CI_2, $CI_0 - CI_1$. For the TAXI Receiver, 'STRB' is either CSTRB or DSTRB and 'Data' is either $DO_0 - DO_7$, DO_8/CO_3, DO_9/CO_2, $CO_0 - CO_1$.
14. For the TAXI Receiver, 'n' is determined by the state of the DMS and SERIN– inputs. When SERIN– is held below V_{THT} max or left open, n=1. When SERIN– is held above 0.25 V and when:

DMS	SERIN–	"n"
GND	< V_{THTMAX} or OPEN	n = 1; 8 Bit Test Mode
	> 2.5 V	n = 10; 8 Bit Local Mode
VCC	< V_{THTMAX} or OPEN	n = 1; 9 Bit Test Mode
	> 2.5 V	n = 11; 9 Bit Local Mode
Open or $\frac{1}{2}$ VCC	< V_{THTMAX} or OPEN	n = 1; 10 Bit Test Mode
	> 2.5 V	n = 12; 10 Bit Local Mode

15. Jitter on X_1 input must be less than ±0.2 ns to ensure that automatic test equipment can properly measure device switching characteristics. The X1 input frequency will determine the byte rate reference for the receiver byte clock.
16. This specification is the sum of Data Dependent Jitter, Duty Cycle Distortion, and Random Jitter.
18. ACK delay is determined by t_{13} when the input latch is empty or by t_{15} when the latch is full (Busy mode). Also note that ACK will not rise if STRB does not remain HIGH until ACK rises.
19. If t_{47A} (CNB↓ to CLK↑ setup) is violated, then output data will occur one byte time later.
20. All timing references are made with respect to +1.5 V for TTL–level signals or to the 50% point between V_{OH} and V_{OL} for ECL signals. ECL input rise and fall times must be 2 ns ± 0.2 ns between 20% and 80% points. TTL input rise and fall times must be 2 ns between 1 V and 2 V.
21. Device thresholds on the SERIN (+/–) pin(s) are verified during production test by ensuring that the input threshold is less than V_{IHS} (min) and greater than V_{ILS} (max). The figure below shows the acceptable range (shaded area) for the transition voltage.

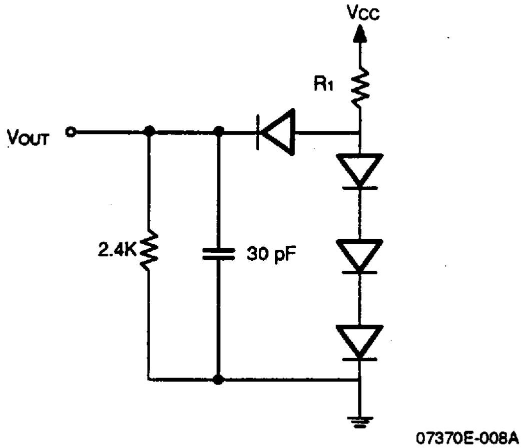


22. Switching Characteristics are tested during 8-bit local mode operation.
23. The limit for this parameter cannot be derived from t_{37} and t_{42}.
24. This specification does not apply during reacquisition when CLK stretch can occur.

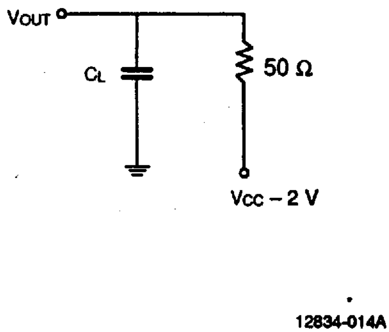
† This parameter is guaranteed but is not included in production tests.

* Notes listed correspond to the respective references made in the DC Characteristics and the Switching Characteristics tables.

SWITCHING TEST CIRCUITS



TTL Output Load



ECL Output Load

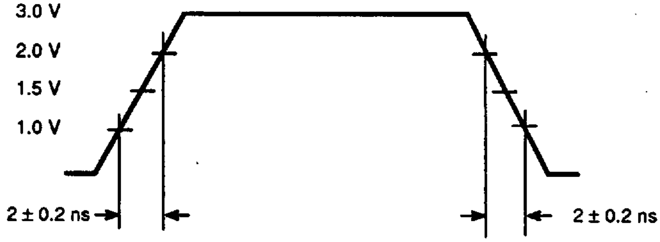
Notes:

1. R_1 = 500 Ω for the I_{OL} = 8 mA
2. All diodes IN916 or IN3064, or equivalent
3. C_L = 30 pF includes scope probe, wiring and stray capacitances without device in test fixture.
4. AMD uses constant current (A.T.E.) load configurations and forcing functions. This figure is for reference only.

Notes:

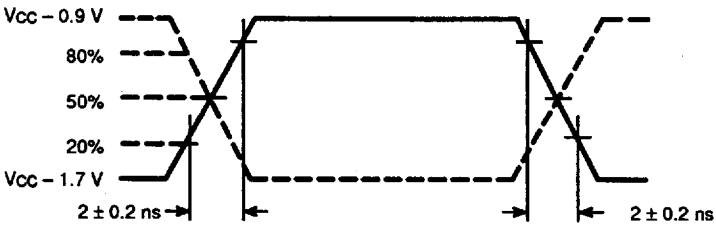
1. $C_L \leq 3$ pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. AMD uses Automatic test equipment load configurations and forcing functions. This figure is for reference only.

SWITCHING TEST WAVEFORMS



12834-015B

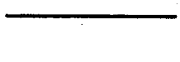
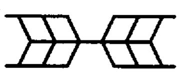
TTL Input Waveform



12834-016B

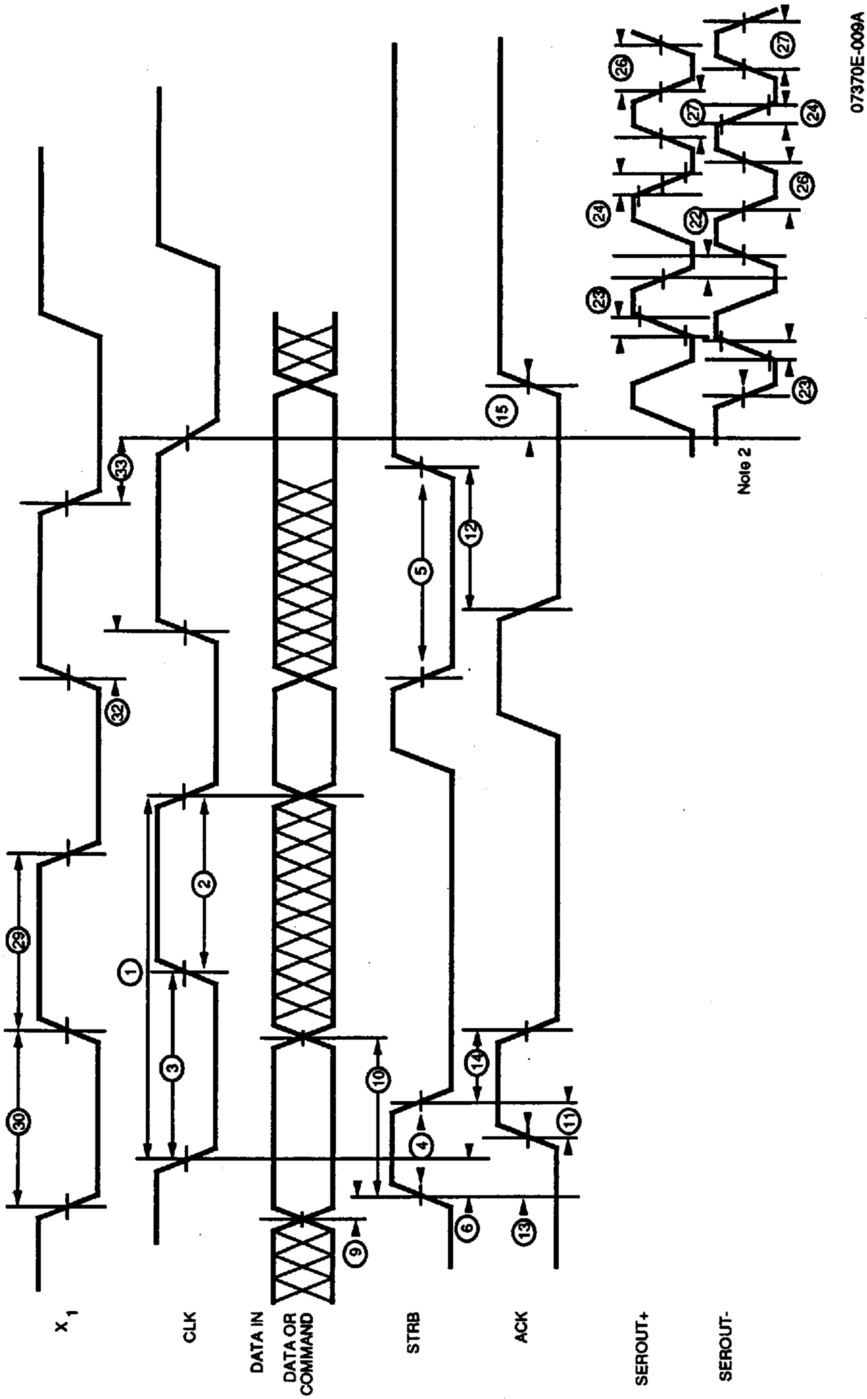
ECL Input Waveform

SWITCHING TEST WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care Any Change Permitted	Changing State Unknown
	Does Not Apply	Center Line is High Impedence "Off" State

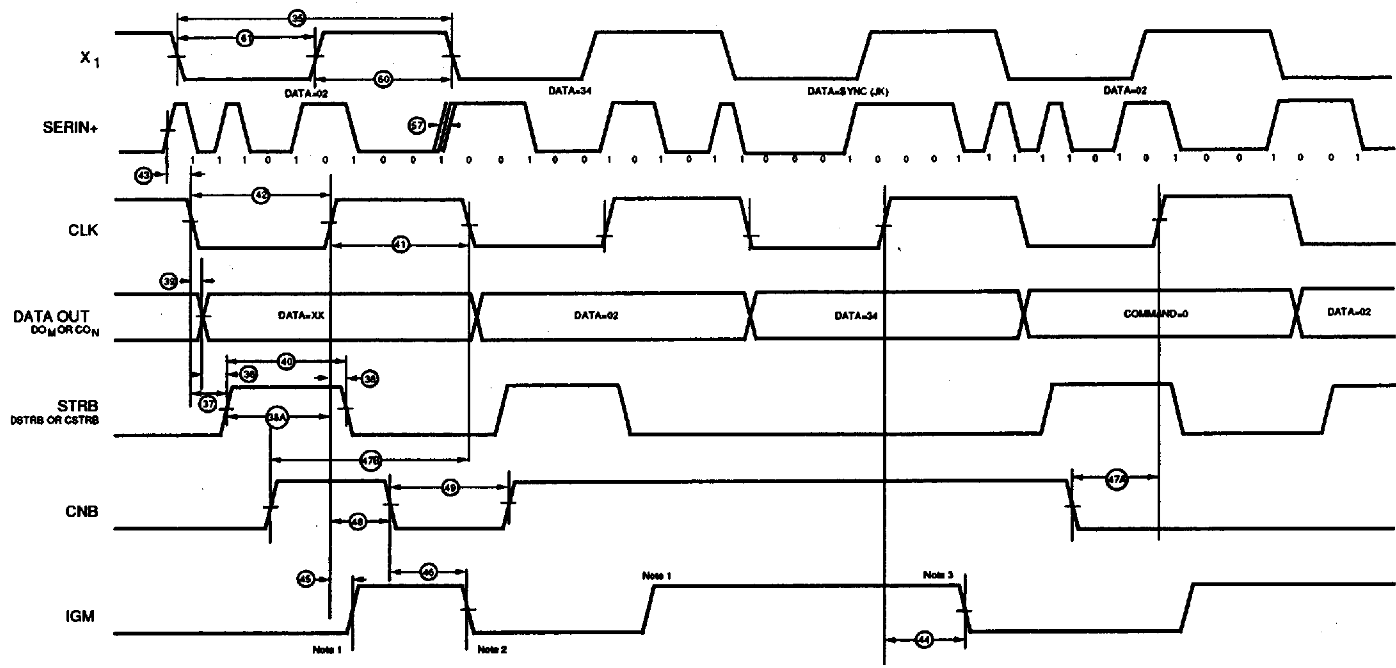
KS000010

SWITCHING WAVEFORMS



Am7968 TAXIchip Transmitter AC

SWITCHING WAVEFORMS (Continued)



07370E-010A

Notes:

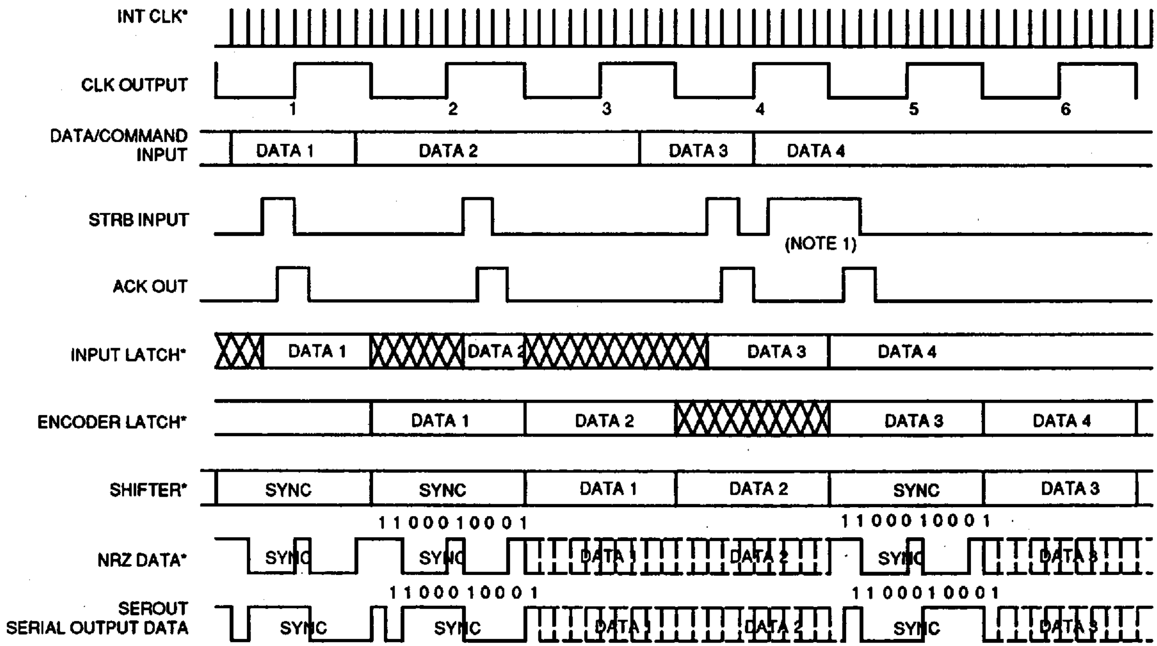
1. IGM rises because CNB = 1 and SERIN = first half of non-sync byte.
2. IGM falls because CNB falls.
3. IGM falls because SERIN = first half of sync byte.

This diagram illustrates how timing relationships are measured. Functional operation is clarified on following pages.

Am7969 TAXIchip Receiver AC

SWITCHING WAVEFORMS (Continued)

TAXIchip Transmitter



07370E-011A

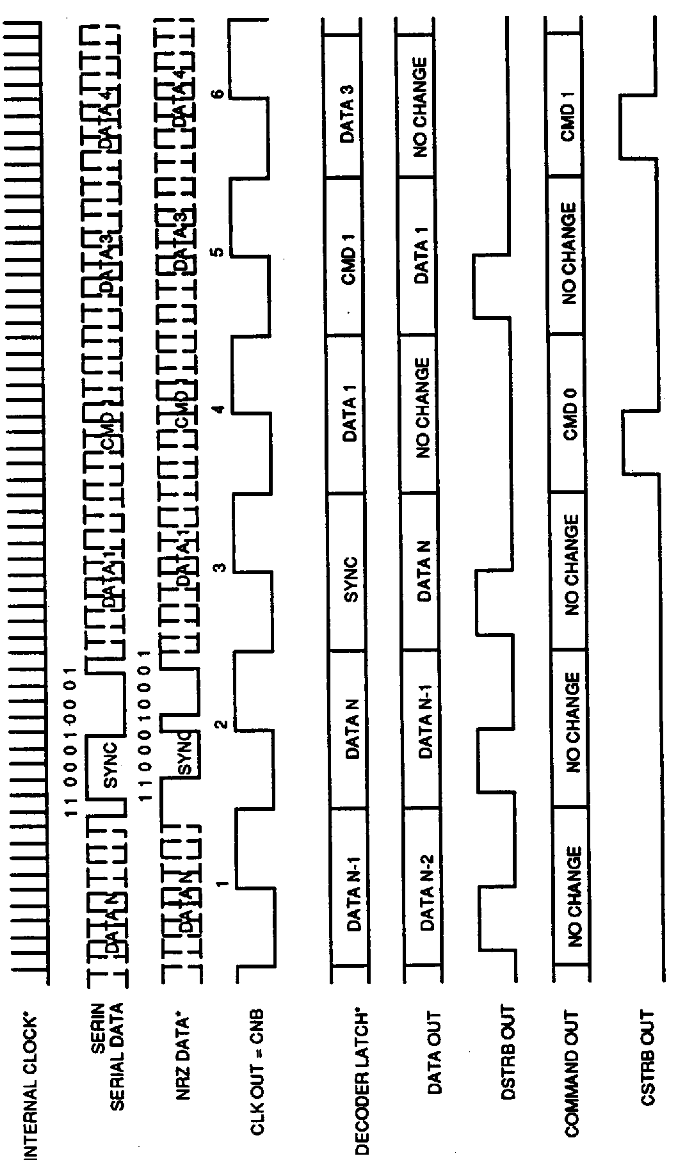
Note:

1. The input Latch is BUSY when the second STRB comes in; the internal STRB-ACK is delayed until the next CLK window. Refer to Figure 3.

STRB to SEROUT Timing
(8-Bit Local Mode)
*Internal Signals

SWITCHING WAVEFORMS (Continued)

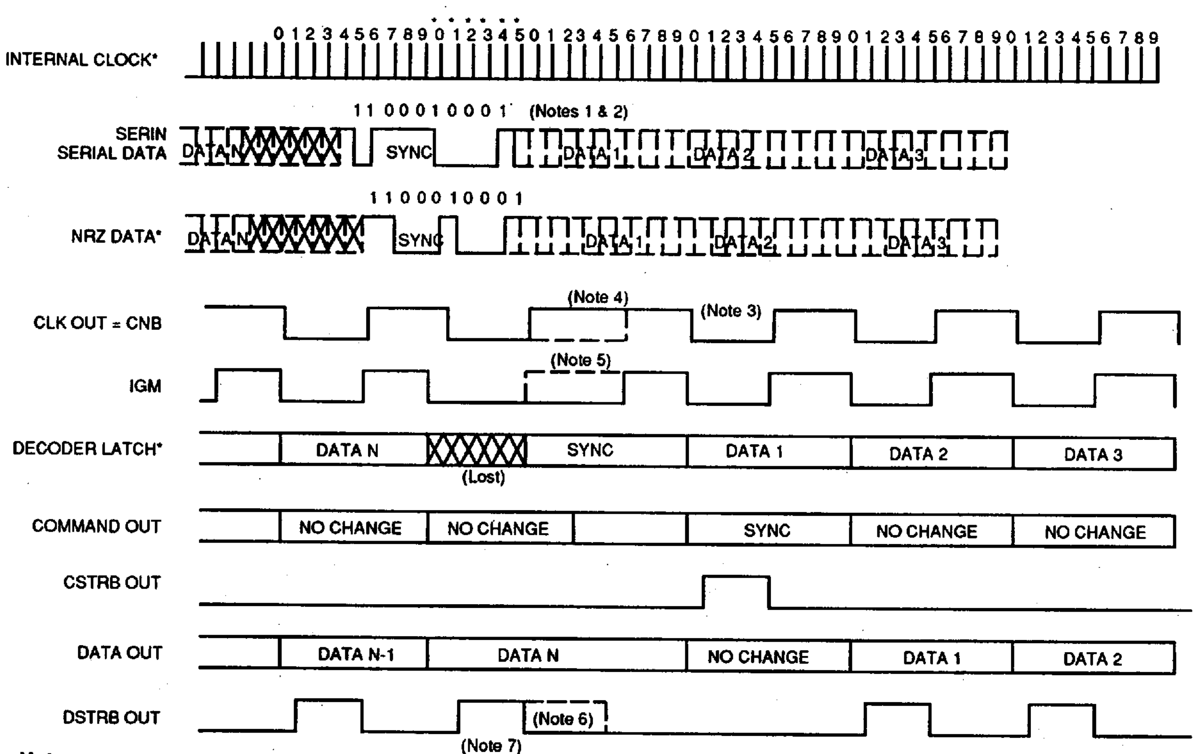
TAXIchip Receiver



TAXIchip Receiver Timing
(8-Bit Local Mode)

07370E-012A

SWITCHING WAVEFORMS (Continued)



07370E-006A

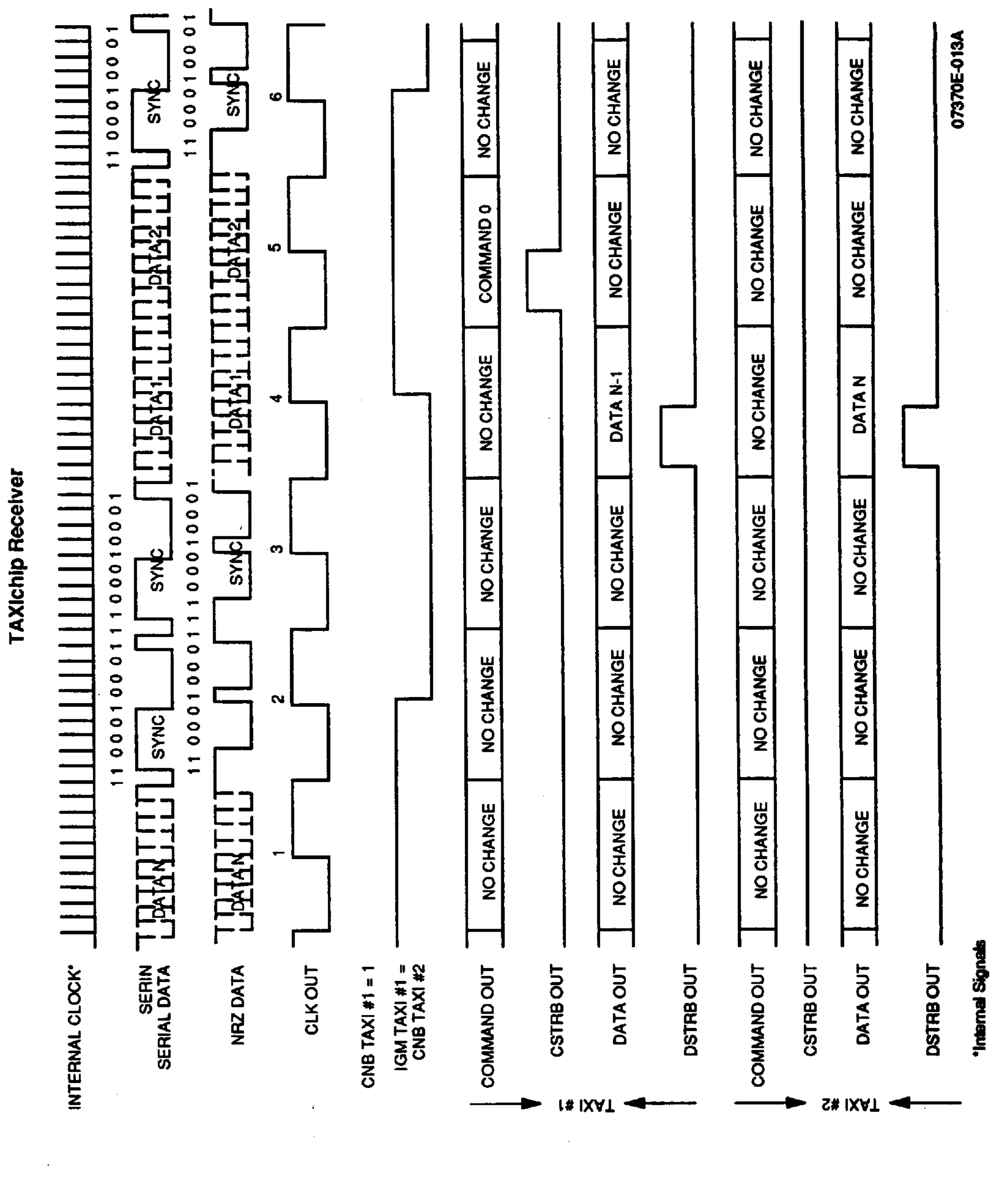
Notes:

*Internal Signals

1. Sync detected in Shifter, but not synchronized with internal state machine.
2. State machine re-synched to new sync position.
3. Clock output delayed to new position.
4. The LOW time or HIGH time gets stretched depending on what state of the internal machine is reset.
5. IGM rises at the 6.5th state of the state machine.
6. Strobe falls at the rising edge of the clock out.
7. Strobe may be shifted one bit time if the state machine is reset at state 1.

TAXIchip Receiver Timing (8-Bit Mode/Local) Showing External Effect of SYNC Error

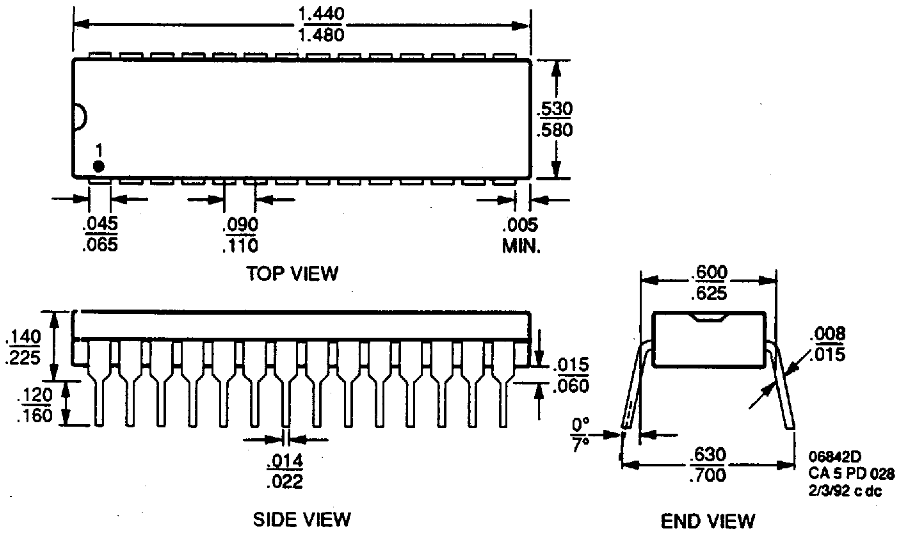
SWITCHING WAVEFORMS (Continued)



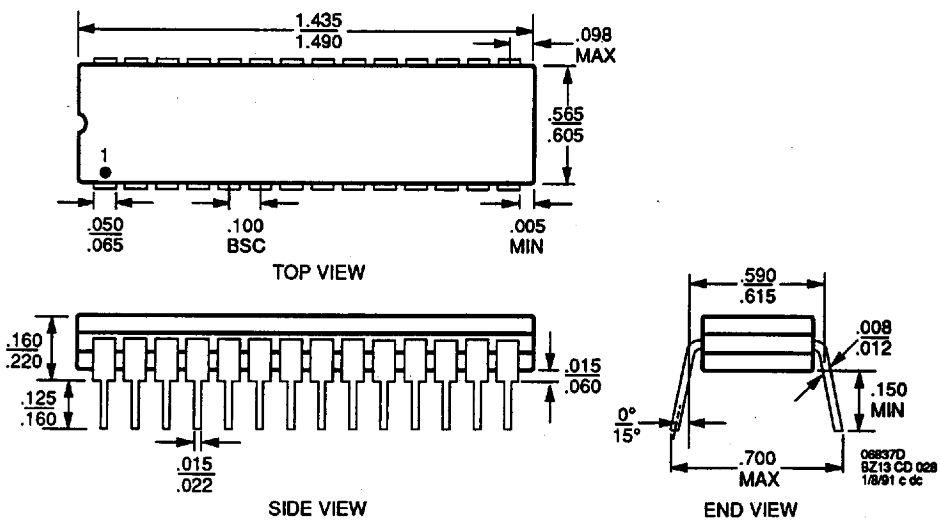
TAXIchip Receiver Timing
(8-Bit Cascade Mode)

PHYSICAL DIMENSIONS*

PD 028

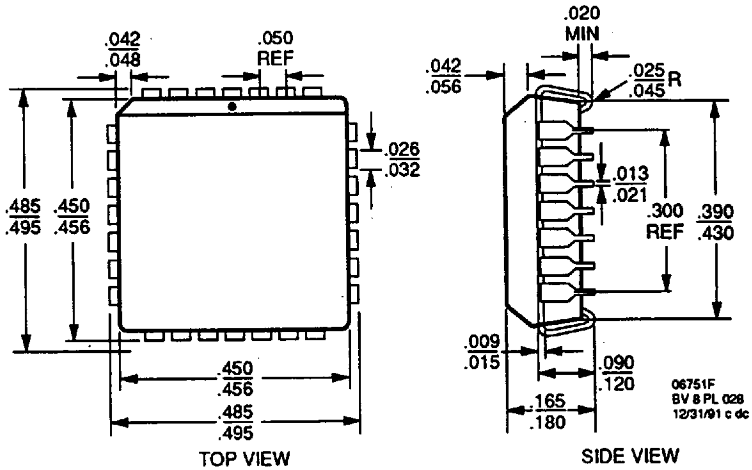


CD 028

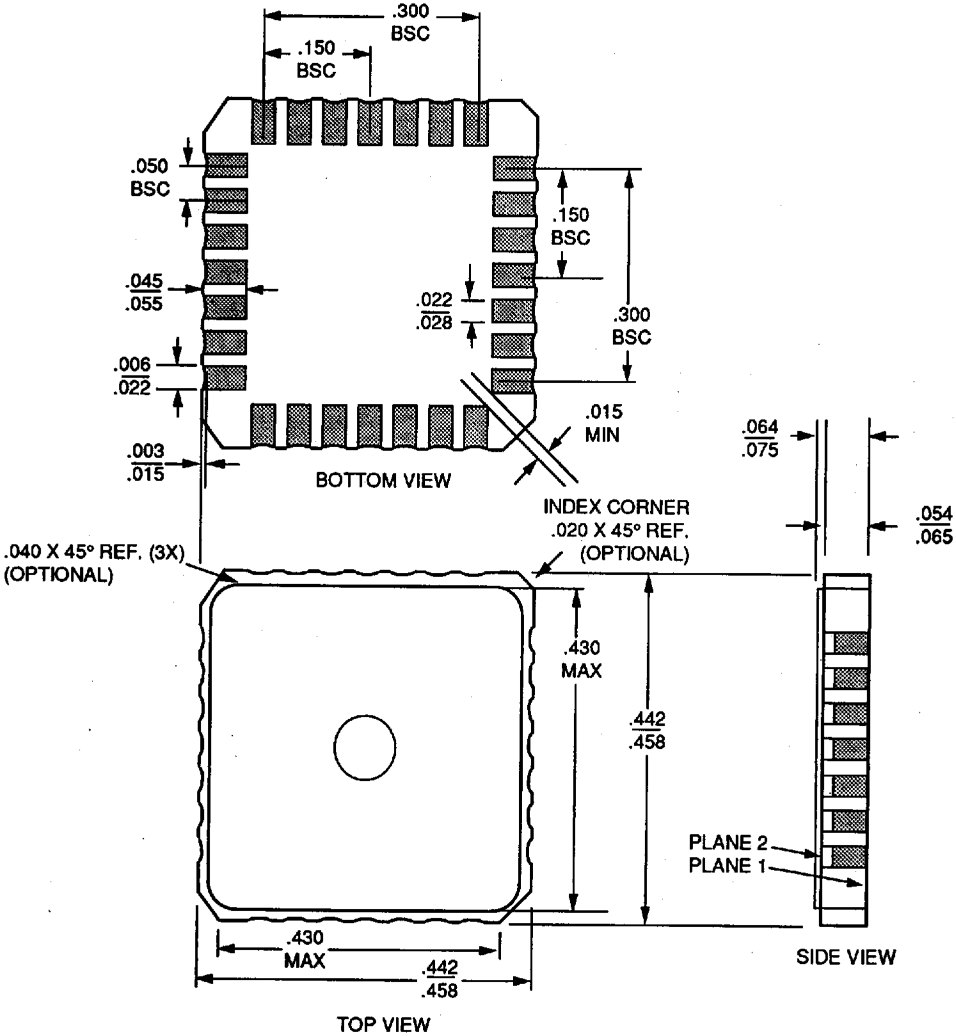


*For reference only. All dimensions measured in inches. BSC is an ANSI standard for Basic Space Centering.

PHYSICAL DIMENSIONS
PL 028



PHYSICAL DIMENSIONS
CLT028



07703C