PRELIMINARY

Am27LV010/Am27LV010B

1 Megabit (131,072 x 8-Bit) CMOS EPROM

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Single +3.3 V power supply**
  - Regulated power supply 3.0 V–3.6 V
  - Unregulated power supply 2.7 V–3.6 V (for battery operated systems)
- **Low power consumption:**
  - 10 µA typical CMOS standby current
  - 90 µW maximium standby power
  - 54 mW maximum power at 5 MHz
- **Fast access time—120 ns**
- **JEDEC-approved pinout**
  - Pin compatible with 5.0 V 1 Mbit EPROM
  - Easy upgrade from 28-pin EPROMs
- **Fast Flashrite™ programming**
  - Typical programming time of 16 seconds
- **Latch-up protected to 100 mA from –1 V to Vcc +1 V**
- **High noise immunity**
- **Compact 32-pin DIP package requires no hardware change for upgrades to 8 Mbit**
- **Versatile features for simple interfacing**
  - Both CMOS and TTL input/output compatibility
  - Two line control functions

GENERAL DESCRIPTION

The Am27LV010 is a low voltage, low power 1 Mbit, ultraviolet erasable, progammable read-only memory, organized as 128K words by 8 bits per word.

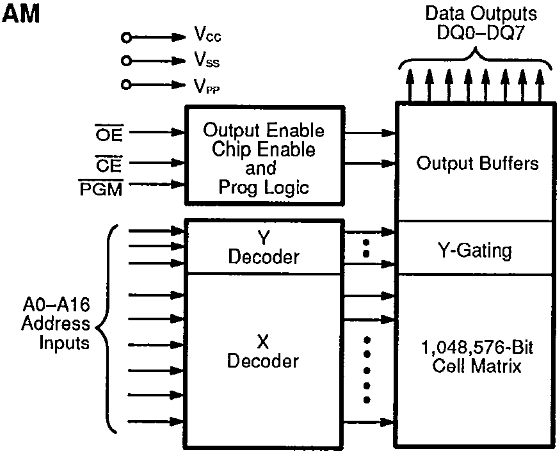
The Am27LV010 operates from a single power supply of 3.3 V and is offered with two power supply tolerances. The Am27LV010 has a Vcc tolerance range of 3.3 V ± 0.3 V making it suitable for use in systems that have regulated power supplies. The Am27LV010B has a voltage supply range of 2.7 V–3.6 V making it an ideal part for battery operated systems.

Maximum power consumption of the Am27LV010 in standby mode is only 90 µW. If the device is constantly accessed at 5 MHz, then the maximum power consumption increases to 54 mW. These power ratings are significantly lower than typical EPROMs. Also, as power consumption is proportional to voltage squared, 3.3 V devices consume at least 57% less power than their 5.0 V counterparts. Due to its lower current and voltage, the Am27LV010 is well-suited for battery operated and portable systems as it extends the battery life in these systems. Typical applications are notebook and hand-held computers as well as cellular phones.

The Am27LV010 is packaged in the industry standard 32-pin windowed ceramic DIP and LCC packages, as well as one-time programmable (OTP) packages. This device is pin-compatible with the 5.0 V devices.

The Am27LV010 uses AMD's Flashrite™ programming algorithm (100 µs pulses) resulting in typical programming time of 16 seconds. This device is manufactured on AMD's sub-micron process technology which provides high speed, low power and high noise immunity.

BLOCK DIAGRAM



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This document contains information on a product under development at Advanced Micro Devices, Inc. The information is intended to help you to evaluate this product. AMD reserves the right to change or discontinue work on this proposed product without notice.

Publication# 17341 Rev. A Amendment/0
Issue Date: July 1993

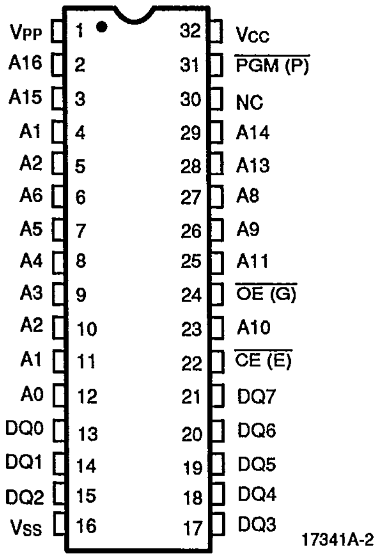
PRODUCT SELECTOR GUIDE

Family Part No	Am27LV010/Am27LV010B				
Ordering Part No:					
Am27LV010 (3.0 V – 3.6 V)	-120	-150	-200	-250	-300
Am27LV010B (2.7 V – 3.6 V)	-150	-150	-200	-250	-300
Max Access Time (ns)	120	150	200	250	300
$\overline{\text{CE (E)}}$ Access (ns)	120	150	200	250	300
$\overline{\text{OE (G)}}$ Access (ns)	50	65	75	100	120

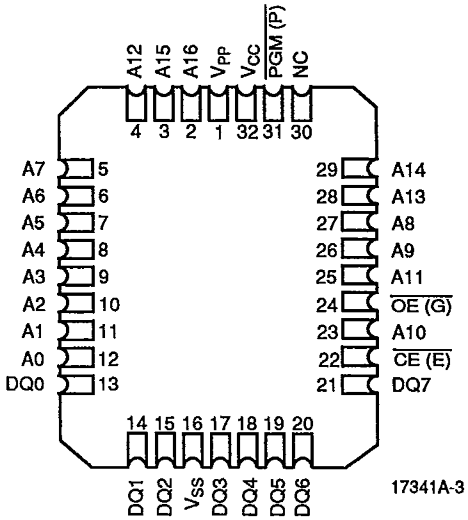
CONNECTION DIAGRAMS

Top View

DIP



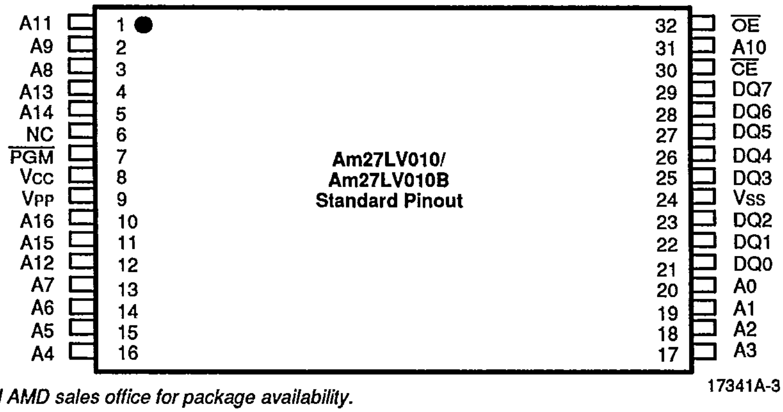
PLCC/LCC



Notes:

1. *JEDEC nomenclature is in parenthesis.*
2. *The 32-pin DIP to 32-pin LCC configuration varies from the JEDEC 28-pin DIP to 32-pin LCC configuration.*

TSOP*

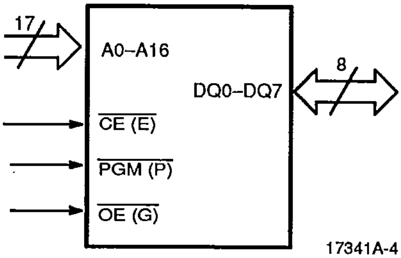


**Contact local AMD sales office for package availability.*

PIN DESCRIPTION

A0–A16 = Address Inputs
$\overline{\text{CE}}$ (E) = Chip Enable Input
DQ0–DQ7 = Data Input/Outputs
NC = No Internal Connect
$\overline{\text{OE}}$ (G) = Output Enable Input
$\overline{\text{PGM}}$ (P) = Program Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Supply Voltage
V_{SS} = Ground

LOGIC SYMBOL



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ORDERING INFORMATION
EPROM Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

AM27LV010 **-120** **D** **C** **B**

OPTIONAL PROCESSING
Blank = Standard processing
B = Burn-in

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)
E = Extended Commercial (–55°C to +125°C)

PACKAGE TYPE
D = 32-Pin Ceramic DIP (CDV032)
L = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLV032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27LV010 – 1 Megabit (131,072 x 8-Bit) Low Voltage CMOS EPROM with 3.0 V–3.6 V Vcc Tolerance
Am27LV010B –1 Megabit (131,072 x 8-Bit) Low Voltage CMOS EPROM with 2.7 V–3.6 V Vcc Tolerance

Valid Combinations	
AM27LV010-120	DC, DCB, LC, LCB
AM27LV010-150	DC, DCB, DE, DEB, DI, DIB, LC, LI, LE, LEB
AM27LV010-200	
AM27LV010-250	
AM27LV010-300	
AM27LV010B-150	
AM27LV010B-200	
AM27LV010B-250	
AM27LV010B-300	

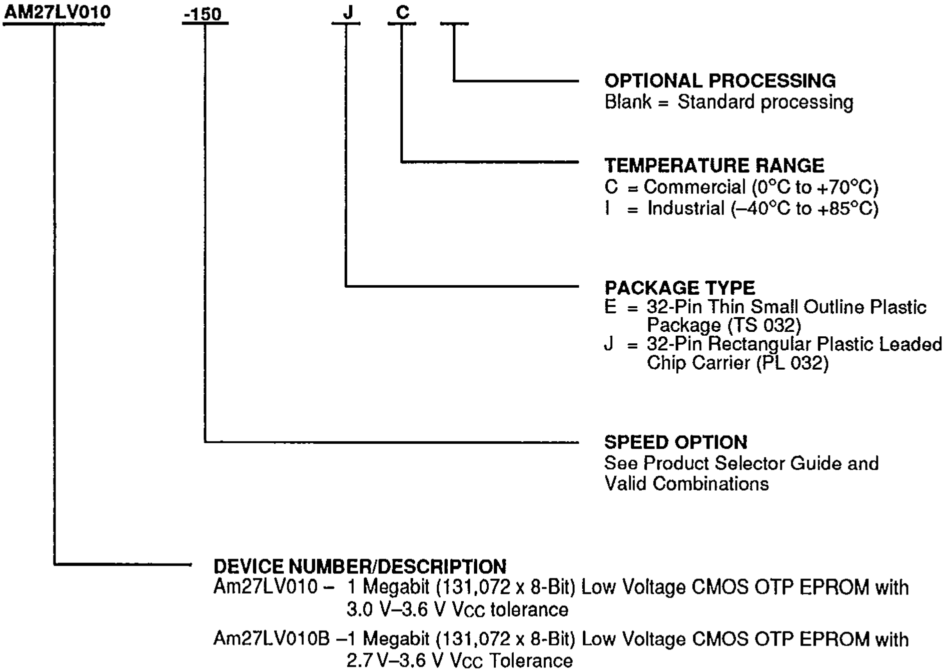
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

OTP Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



AM27LV010 -150 J C

OPTIONAL PROCESSING
Blank = Standard processing

TEMPERATURE RANGE
C = Commercial (0°C to +70°C)
I = Industrial (–40°C to +85°C)

PACKAGE TYPE
E = 32-Pin Thin Small Outline Plastic Package (TS 032)
J = 32-Pin Rectangular Plastic Leaded Chip Carrier (PL 032)

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27LV010 – 1 Megabit (131,072 x 8-Bit) Low Voltage CMOS OTP EPROM with 3.0 V–3.6 V V_{CC} tolerance
Am27LV010B –1 Megabit (131,072 x 8-Bit) Low Voltage CMOS OTP EPROM with 2.7 V–3.6 V V_{CC} Tolerance

Valid Combinations	
AM27LV010-150	JC, EC, JI, EI
AM27LV010-200	
AM27LV010-250	
AM27LV010-300	
AM27LV010B-200	
AM27LV010B-250	
AM27LV010B-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

MILITARY ORDERING INFORMATION
APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:

AM27LV010 -150 /B X A

LEAD FINISH
A = Hot Solder Dip

PACKAGE TYPE
X = 32-Pin Ceramic DIP (CDV032)
U = 32-Pin Rectangular Ceramic Leadless Chip Carrier (CLV032)

DEVICE CLASS
/B = Class B

SPEED OPTION
See Product Selector Guide and Valid Combinations

DEVICE NUMBER/DESCRIPTION
Am27LV010 – 1 Megabit (131,072 x 8-Bit) Low Voltage CMOS EPROM with 3.0 V –3.6 V V_{CC} Tolerance
Am27LV010B –1 Megabit (131,072 x 8-Bit) Low Voltage CMOS EPROM with 2.7 V –3.6 V V_{CC} Tolerance

Valid Combinations	
AM27LV010-150	/BXA, /BUA
AM27LV010-200	
AM27LV010-250	
AM27LV010-300	
AM27LV010B-250	
AM27LV010B-300	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

FUNCTIONAL DESCRIPTION

Erasing the Am27LV010

In order to clear all locations of their programmed contents, it is necessary to expose the Am27LV010 to an ultraviolet light source. A dosage of 15 W seconds/cm^2 is required to completely erase an Am27LV010. This dosage can be obtained by exposure to an ultraviolet lamp — wavelength of 2537 Å — with intensity of 12,000 µW/cm^2 for 15 to 20 minutes. The Am27LV010 should be directly under and about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the Am27LV010, and similar devices, will erase with light sources having wavelengths shorter than 4000 Å. Although erasure times will be much longer than with UV sources at 2537 Å, nevertheless the exposure to fluorescent light and sunlight will eventually erase the Am27LV010 and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package window should be covered by an opaque label or substance.

Programming the Am27LV010

Upon delivery, or after each erasure, the Am27LV010 has all 1,048,576 bits in the "ONE", or HIGH state. "ZEROs" are loaded into the Am27LV010 through the procedure of programming.

The programming mode is entered when 12.75 V ± 0.25 V is applied to the V_{PP} pin, $\overline{CE}$ and $\overline{PGM}$ are at V_{IL} and $\overline{OE}$ is at V_{IH}.

For programming, the data to be programmed is applied 8 bits in parallel to the data output pins.

The Flashrite programming algorithm reduces programming time by using initial 100 µs pulses followed by a byte verification to determine whether the byte has been successfully programmed. If the data does not verify, an additional pulse is applied for a maximum of 25 pulses. This process is repeated while sequencing through each address of the EPROM.

The Flashrite programming algorithm programs and verifies at V_{CC} = 6.25 V and V_{PP} = 12.75 V. After the final address is completed, all bytes are compared to the original data with V_{CC} = V_{PP} = 5.25 V. Am27LV010 can be programmed using the same algorithm as the 5 V counterpart 27C010.

Please refer to Section 6 for programming flow chart and characteristics.

Program Inhibit

Programming of multiple Am27LV010s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs of the parallel Am27LV010 may be common. A TTL low-level program pulse applied to an Am27LV010 $\overline{CE}$ input with V_{PP} = 12.75 ± 0.25 V, $\overline{PGM}$ LOW, and $\overline{OE}$ HIGH will program that Am27LV010. A high-level $\overline{CE}$ input inhibits the other Am27LV010s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify should be performed with $\overline{OE}$ and $\overline{CE}$ at V_{IL}, $\overline{PGM}$ at V_{IH}, and V_{PP} between 12.5 V and 13.0 V.

Auto Select Mode

The auto select mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25°C ± 5°C ambient temperature range that is required when programming the Am27LV010.

To activate this mode, the programming equipment must force 12.0 ± 0.5 V on address line A9 of the Am27LV010. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. All other address lines must be held at V_{IL} during auto select mode.

Byte 0 (A0 = V_{IL}) represents the manufacturer code, and Byte 1 (A0 = V_{IH}), the device identifier code. For the Am27LV010, these two identifier bytes are given in the Mode Select table. All identifiers for manufacturer and device codes will possess odd parity, with the MSB (DQ7) defined as the parity bit.

Read Mode

The Am27LV010 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been LOW and addresses have been stable for at least $t_{ACC} - t_{OE}$.

Standby Mode

The Am27LV010 has a CMOS standby mode which reduces the maximum V_{CC} current to 25 µA. It is placed in CMOS-standby when $\overline{CE}$ is at V_{CC} ± 0.3 V. The Am27LV010 also has a TTL-standby mode which reduces the maximum V_{CC} current to 0.6 mA. It is placed in TTL-standby when $\overline{CE}$ is at V_{IH}. When in standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

Mixed Power Supply System

Am27LV020 (in 3.0 V to 3.6 V regulated power supply) can be intefaced with 5 V system only when the I/O pins (DQ0–DQ7) are not driven by the 5 V system. V_{IHmax} = V_{CCLV} + 2.2 V for address and clock pins and V_{IHmax} = V_{CCLV} + 0.5 V for I/O pins should be followed to avoid CMOS latch-up condition

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function is provided to allow for:

- Low memory power dissipation
- Assurance that output bus contention will not occur

It is recommended that $\overline{CE}$ be decoded and used as the primary device-sele cting function, while $\overline{OE}$ be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on EPROM arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode	Pins	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	A0	A9	V_{PP}	Outputs
Read		V_{IL}	V_{IL}	X	X	X	X	D_{OUT}
Output Disable		V_{IL}	V_{IH}	X	X	X	X	High Z
Standby (TTL)		V_{IH}	X	X	X	X	X	High Z
Standby (CMOS)		$V_{CC} \pm 0.3$ V	X	X	X	X	X	High Z
Program		V_{IL}	V_{IH}	V_{IL}	X	X	V_{PP}	D_{IN}
Program Verify		V_{IL}	V_{IL}	V_{IH}	X	X	V_{PP}	D_{OUT}
Program Inhibit		V_{IH}	X	X	X	X	V_{PP}	High Z
Auto Select (Note 3)	Manufacturer Code	V_{IL}	V_{IL}	X	V_{IL}	V_H	X	01H
	Device Code	V_{IL}	V_{IL}	X	V_{IH}	V_H	X	0EH

Notes:

1. *X can be either V_{IL} or V_{IH}*
2. *$V_H = 12.0\ V \pm 0.5\ V$*
3. *A1–A8 = A10–A16 = V_{IL}*
4. *See DC Programming Characteristics for V_{PP} voltage during programming.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature:	
OTP Products	–65°C to +125°C
All Other Products	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Voltage with Respect to V_{SS}:	
All pins except A9, V_{PP}, and V_{CC} (Note 1)	–0.6 V to V_{CC} + 0.6 V
A9 and V_{PP} (Note 2)	–0.6 V to 13.5 V
V_{CC}	–0.6 V to 7.0 V

Notes:

1. *During transitions, the input may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*
2. *During transitions, A9 and V_{CC} may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. A9 and V_{PP} must not exceed 13.5 V for any period of time.*

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. This is a stress rating only; functional operation of the devices at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices	
Case Temperature (T_C)	0°C to +70°C
Industrial (I) Devices	
Case Temperature (T_C)	–40°C to +85°C
Extended Commercial (E) Devices	
Case Temperature (T_C)	–55°C to +125°C
Military (M) Devices	
Case Temperature (T_C)	–55°C to +125°C
Supply Read Voltages:	
V_{CC} for Am27LV010	+3.0 V to +3.6 V
V_{CC} for Am27LV010B	+2.7 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 2, 3 and 4) (for APL products, Group A, Subgroups 1, 2, 3, 7 and 8 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
TTL and CMOS Inputs for V_{CC} = 3.0 V to 3.6 V						
V_{OH}	Output HIGH Voltage	I_{OH} = –2.0 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.0 mA			0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}	C/I Devices		5	µA
			E/M Devices		5	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz	C/I Devices		15	mA
		I_{OUT} = 0 mA (Open Outputs)	E/M Devices		20	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}	TTL		0.6	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} ± 0.3 V	CMOS		25	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
CMOS Inputs for V_{CC} = 2.7 V to 3.6 V						
V_{OH}	Output HIGH Voltage	I_{OH} = –20 µA		V_{CC} – 0.1		V
V_{OL}	Output LOW Voltage	I_{OL} = 20 µA			0.1	V
V_{IH}	Input HIGH Voltage			0.7 V_{CC}	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage			–0.3	0.2 V_{CC}	V
I_{LI}	Input Load Current	V_{IN} = 0 V to +V_{CC}	C/I Devices		1.0	µA
			E/M Devices		1.0	
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to +V_{CC}	C/I Devices		5	µA
			E/M Devices		5	
I_{CC1}	V_{CC} Active Current (Note 3)	$\overline{CE}$ = V_{IL}, f = 5 MHz, I_{OUT} = 0 mA (Open Outputs)	C/I Devices		15	mA
			E/M Devices		20	
I_{CC2}	V_{CC} TTL Standby Current	$\overline{CE}$ = V_{IH}	TTL		0.6	mA
I_{CC3}	V_{CC} CMOS Standby Current	$\overline{CE}$ = V_{CC} + 0.3 V			25	µA
I_{PP1}	V_{PP} Current During Read	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, V_{PP} = V_{CC}			100	µA

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. ***Caution:** The Am27LV010 must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*
3. *I_{CC1} is tested with $\overline{OE}$ = V_{IH} to simulate open outputs.*
4. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

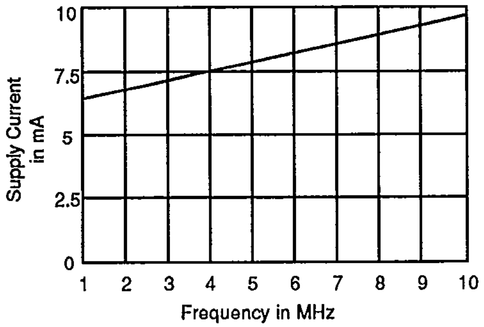


Figure 1. Typical Supply Current vs. Frequency
Vcc = 3.6 V, T = 25°C

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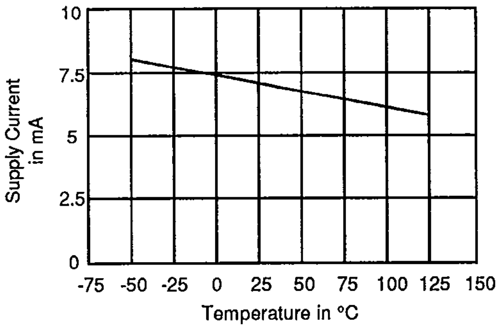

Figure 2. Typical Supply Current vs. Temperature
Vcc = 3.6 V, f = 5 MHz

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CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	CDV032		CLV032		TS 032		Unit
			Typ	Max	Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	$V_{IN} = 0$ V	10	12	8	10	10	12	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0$ V	12	15	9	12	12	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *$T_A = +25°C$, $f = 1$ MHz.*

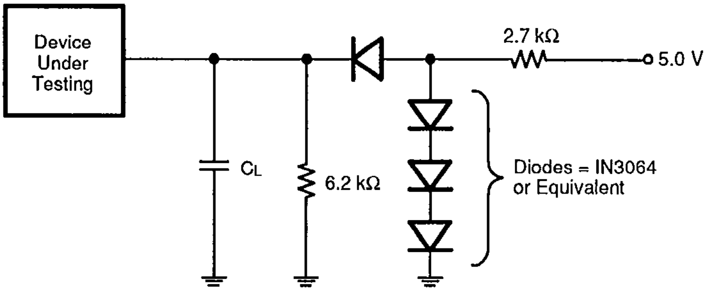
SWITCHING CHARACTERISTICS over operating ranges unless otherwise specified (Notes 1, 3 and 4) (for APL products, Group A, Subgroups 9, 10 and 11 are tested unless otherwise noted)

JEDEC	Standard	Parameter Description	Test Conditions		Am27LV010/Am27LV010B -120	-150	-200	-250	-300	Unit
t_{AVQV}	t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$	Min						ns
				Max	120	150	200	250	300	
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	$\overline{OE} = V_{IL}$	Min						ns
				Max	120	150	200	250	300	
t_{GLQV}	t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	Min	–	–	–	–	–	ns
				Max	50	65	75	100	120	
t_{EHQZ} t_{GHQZ}	t_{DF}	Chip Enable HIGH or Output Enable HIGH, whichever comes first, to Output Float (Note 2)		Min	0	0	0	0	0	ns
				Max	40	50	60	60	60	
t_{AXQX}	t_{OH}	Output Hold from Addresses, $\overline{CE}$, or $\overline{OE}$, whichever occurred first		Min	0	0	0	0	0	ns
				Max	–	–	–	–	–	

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *This parameter is only sampled and not 100% tested.*
3. ***Caution:*** *The Am27LV010 must not be removed from, or inserted into, a socket when V_{PP} or V_{CC} is applied.*
4. *Output Load: 1 TTL gate and $C_L = 100$ pF*
   Input Rise and Fall Times: 20 ns
   Input Pulse Levels: 0.40 V to 2.4 V
   Timing Measurement Reference Level—Inputs: 0.8 V and 2.0 V
   Outputs: 0.8 V and 2.0 V

SWITCHING TEST CIRCUIT



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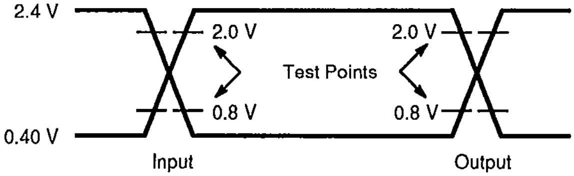
CL = 100 pF including jig capacitance

SWITCHING TEST WAVEFORM



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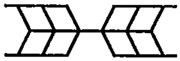
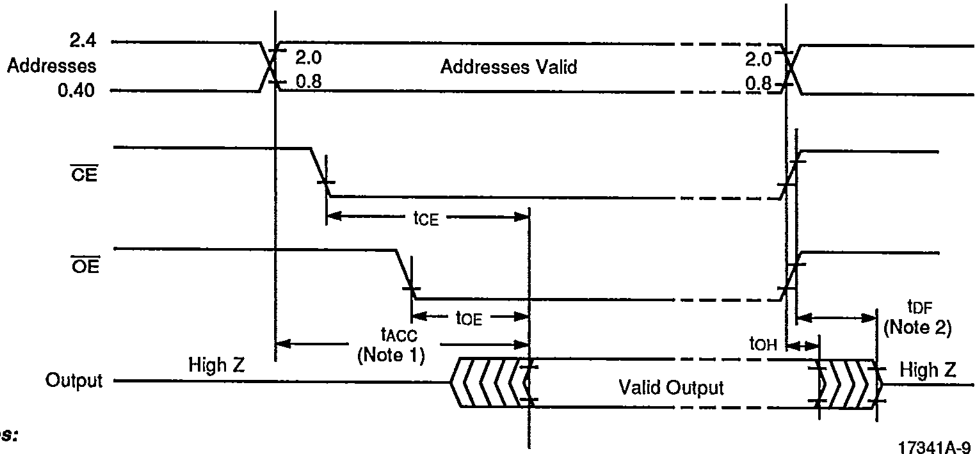
AC Testing: Inputs are driven at 2.4 V for a Logic “1” and 0.40 V for a Logic “0”. Input pulse rise and fall times are ≤ 20 ns.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must Be Steady	Will Be Steady
	May Change from H to L	Will Be Changing from H to L
	May Change from L to H	Will Be Changing from L to H
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance "Off" State

KS000010

SWITCHING WAVEFORM



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Notes:

1. $\overline{OE}$ *may be delayed up to* $t_{ACC} - t_{OE}$ *after the falling edge of the addresses without impact on* t_{ACC}.
2. t_{DF} *is specified from* $\overline{OE}$ *or* $\overline{CE}$*, whichever occurs first.*

PROGRAMMING FLOW CHART

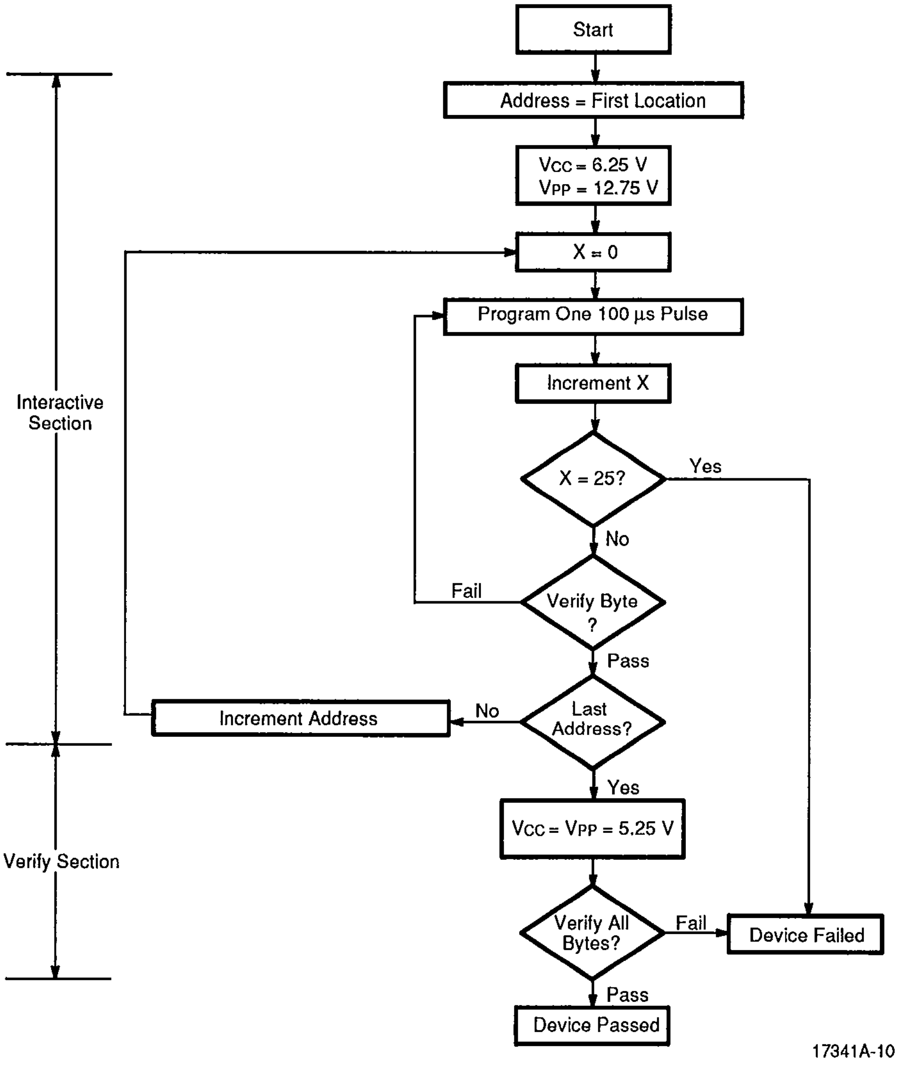


Figure 1. Flashrite Programming Flow Chart

DC PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2 and 3)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}		10.0	µA
V_{IL}	Input LOW Level (All Inputs)		–0.3	0.8	V
V_{IH}	Input HIGH Level		3.0	V_{CC} + 0.5	V
V_{OL}	Output LOW Voltage During Verify	I_{OL} = 2.1 mA		0.45	V
V_{OH}	Output HIGH Voltage During Verify	I_{OH} = –400 µA	2.4		V
V_H	A_9 Auto Select Voltage		11.5	12.5	V
I_{CC}	V_{CC} Supply Current (Program & Verify)			50	mA
I_{PP}	V_{PP} Supply Current (Program)	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$		30	mA
V_{CC}	Flashrite Supply Voltage		6.00	6.50	V
V_{PP}	Flashrite Programming Voltage		12.5	13.0	V

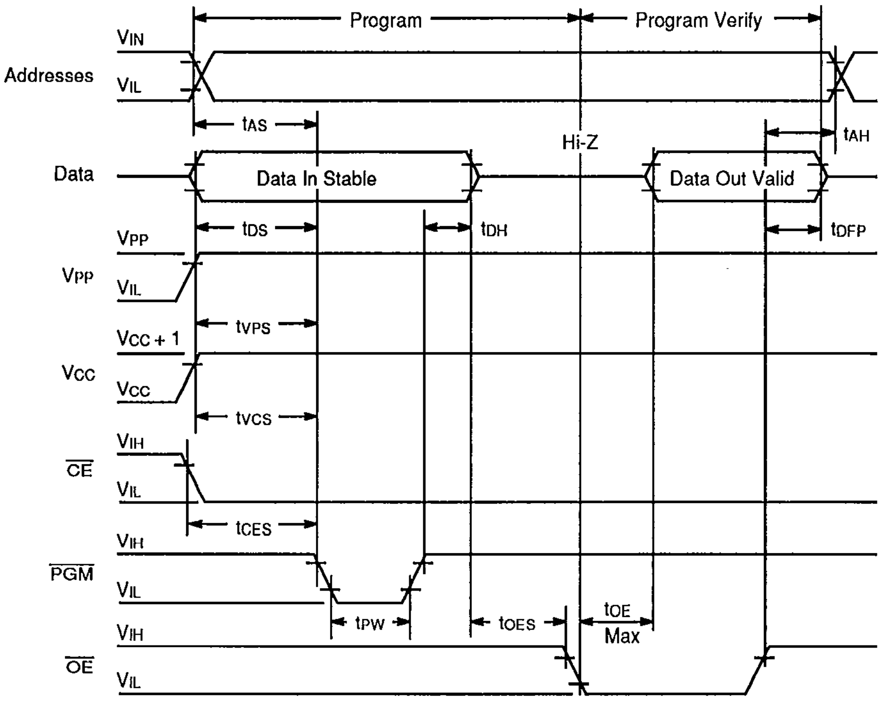
SWITCHING PROGRAMMING CHARACTERISTICS (T_A = +25°C ±5°C) (Notes 1, 2 and 3)

Parameter Symbols					
JEDEC	Standard	Parameter Description	Min	Max	Unit
t_{AVEL}	t_{AS}	Address Setup Time	2		µs
t_{DZGL}	t_{OES}	$\overline{OE}$ Setup Time	2		µs
t_{DVEL}	t_{DS}	Data Setup Time	2		µs
t_{GHAX}	t_{AH}	Address Hold Time	0		µs
t_{EHDX}	t_{DH}	Data Hold Time	2		µs
t_{GHQZ}	t_{DFP}	Output Enable to Output Float Delay	0	130	ns
t_{VPS}	t_{VPS}	V_{PP} Setup Time	2		µs
t_{ELEH1}	t_{PW}	$\overline{PGM}$ Initial Program Pulse Width	95	105	µs
t_{VCS}	t_{VCS}	V_{CC} Setup Time	2		µs
t_{ELPL}	t_{CES}	$\overline{CE}$ Setup Time	2		µs
t_{GLQV}	t_{OE}	Data Valid from $\overline{OE}$		150	ns

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *When programming the Am27LV010, a 0.1 µF capacitor is required across V_{PP} and ground to suppress spurious voltage transients which may damage the device.*
3. *Programming characteristics are sampled but not 100% tested at worst-case conditions.*

INTERACTIVE AND FLASHRITE PROGRAMMING ALGORITHM WAVEFORM (Notes 1 and 2)



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Notes:

1. *The input timing reference level is 0.8 V for V_{IL} and 3 V for V_{IH}.*
2. *t_{OE} and t_{DFP} are characteristics of the device, but must be accommodated by the programmer.*