1.1 Scope.

This specification covers the detail requirements of a monolithic quad, 8-bit, voltage output, digital-to-analog converter with output buffer amplifiers and double-buffered interface logic on-chip. Each D/A converter has a separate reference input terminal.

1.2 Part Number.

The complete part numbers per Tables 1 and 2 of this specification are as follows:

Device	Part Number[1]
−1	AD7225T(X)/883B
−2	AD7225U(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-24	24-Pin Cerdip
E	E-28A	28-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = +25°C unless otherwise noted)

V_{DD} to AGND	−0.3V, +17V
V_{DD} to DGND	−0.3V, +17V
V_{DD} to V_{SS}	−0.3V, +24V
AGND to DGND	−0.3V, V_{DD}
Digital Input Voltage to DGND	−0.3V, V_{DD}
V_{REF} to AGND	−0.3V, V_{DD}
V_{OUT} to AGND	V_{SS}, V_{DD}
Power Dissipation	
Up to +75°C	500mW
Derates above +75°C	2mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-24 and E-28A
θ_{JA} = 125°C/W for Q-24 and E-28A

AD7225—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	−1, 2	8					Bits
Total Unadjusted Error	E_T	−1	2	2	2		V_{DD} = +14V; V_{SS} = −5V; V_{REF} = +10V	± LSB max
		−2	1	2	1	1		
Relative Accuracy	RA	−1	1	1	1		V_{DD} = +14V; V_{SS} = −5V; V_{REF} = +10V	± LSB max
		−2	0.5	1	0.5	0.5		
Differential Nonlinearity	DNL	−1, 2	1	1	1		V_{DD} = +14V; V_{SS} = −5V; V_{REF} = +10V Guaranteed Monotonic to 8-Bits	± LSB max
Full Scale Error	A_E	−1	1	1	1		V_{DD} = +14V; V_{SS} = −5V; V_{REF} = +10V	± LSB max
		−2	0.5	1	0.5	0.5		
Zero Code Error		−1	30	25	30		V_{DD} = 16.5V; 11.4V and 14V	± mV max
		−2	20	25	20	15	V_{SS} = −5V; V_{REF} = V_{DD} − 4	
Voltage Output Settling Time	t_{SL}	−1, 2	5				V_{REF} = +10V; Settling Time to ± 1/2LSB	µs max
Voltage Output Slew Rate	t_{SR}	−1, 2	2.5					V/µs min
Minimum Load Resistance	$R_{L,MIN}$	−1, 2	2				V_{OUT} = +10V; V_{DD} = +14V	kΩ min
Reference Input Resistance	R_{IN}	−1, 2	11	11	11		V_{DD} = 14V	kΩ min
Reference Input Capacitance	C_{IN}	−1, 2	100				Occurs when each DAC is loaded with all 1's	pF max
Channel-to-Channel Isolation		−1, 2	60				V_{REF} = +10V p-p Sinewave @ 10kHz	dB min
AC Feedthrough		−1, 2	70				V_{REF} = −10V p-p Sinewave @ 10kHz	−dB max
Digital Input High Voltage	V_{IH}	−1, 2	2.4	2.4	2.4		V_{DD} = +14V	V min
Digital Input Low Voltage	V_{IL}	−1, 2	0.8	0.8	0.8		V_{DD} = +14V and 11.4V	V max
Digital Input Leakage Current	I_{IN}	−1, 2	1	1	1		V_{IN} = 0V or V_{DD}; V_{DD} = 16.5V	± µA max
Digital Input Capacitance	C_{IN}	−1, 2	8					pF max
Write Pulse Width, t_1	t_{WR}	−1, 2	150					ns min
Address to Write Setup Time, t_2	t_{AS}	−1, 2	0					ns min
Address to Write Hold Time, t_3	t_{AH}	−1, 2	0					ns min
Data Valid to Write Setup Time, t_4	t_{DS}	−1, 2	90					ns min
Data Valid to Write Hold Time, t_5	t_{DH}	−1, 2	10					ns min
Load DAC Pulse Width, t_6	t_{LDAC}	−1, 2	150					ns min
Power Supply Current	I_{DD}	−1, 2	12	12	12		Outputs Unloaded, V_{IN} = V_{IL} or V_{IH}	mA max
	I_{SS}	−1, 2	10	10	10		V_{DD} = 16.5V; V_{SS} = −5.5V; V_{REF} = 12.5V	

NOTE: DUAL SUPPLY OPERATION

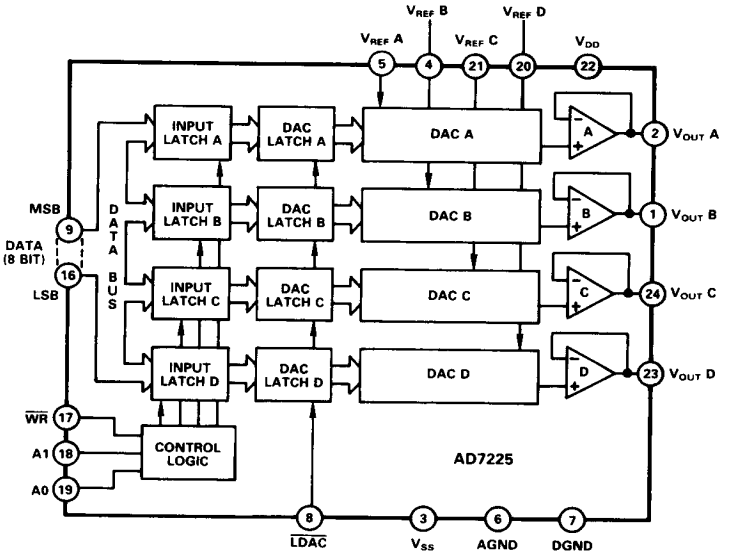
[1] V_{DD} = +11.4V to 16.5V; V_{SS} = −5V ± 10%; AGND = DGND = 0V; V_{REF} = +2V to (V_{DD} − 4V) unless otherwise stated.

Table 2.

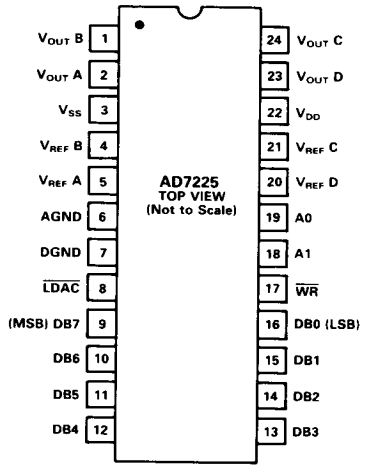
Test	Symbol	Device	Design Limit T_{min}, T_{max}	Sub Group 1	Sub Group 2,3	Sub Group 4	Test Condition[1]	Units
Resolution	RES	−1,2	8					Bits
Total Unadjusted Error	E_T	−1	2	2	2		V_{DD} = +14V	± LSB max
		−2	1	2	1	1		
Differential Nonlinearity	DNL	−1,2	1	1	1		V_{DD} = +14V Guaranteed Monotonic to 8-Bits	± LSB max
Voltage Output Settling Time Positive Full Scale Change		−1,2	5				Settling Time to ± 1/2LSB	µs max
Negative Full Scale Change			7					
Voltage Output Slew Rate	t_{SR}	−1,2	2.0					V/µs min
Minimum Load Resistance	R_{LMIN}	−1,2	2				V_{OUT} = +10V; V_{DD} = +15V	kΩ min
Reference Input Resistance	R_{IN}	−1,2	11				V_{DD} = 14V	kΩ min
Reference Input Capacitance	C_{IN}	−1,2	100				Occurs when each DAC is loaded with all 1's	pF max
Channel-to-Channel Isolation		−1,2	60				V_{REF} = +10V p-p Sinewave @ 10kHz	dB min
AC Feedthrough		−1,2	70				V_{REF} = −10V p-p Sinewave @ 10kHz	−dB max
Digital Input High Voltage	V_{IH}	−1,2	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	−1,2	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	−1,2	1				V_{IN} = 0V or V_{DD}; V_{DD} = 16.5V	± µA max
Digital Input Capacitance	C_{IN}	−1,2	8					pF max
Write Pulse Width, t_1	t_{WR}	−1,2	150					ns min
Address to Write Setup Time, t_2	t_{AS}	−1,2	0					ns min
Address to Write Hold Time, t_3	t_{AH}	−1,2	0					ns min
Data Valid to Write Setup Time, t_4	t_{DS}	−1,2	90					ns min
Data Valid to Write Hold Time, t_5	t_{DH}	−1,2	10					ns min
Load DAC Pulse Width, t_6	t_{LDAC}	−1,2	150					ns min
Power Supply Current	I_{DD}	−1,2	12				Outputs Unloaded, V_{IN} = V_{IL} or V_{IH}	mA max

NOTE: SINGLE SUPPLY OPERATION
[1] V_{DD} = +15V ± 5%; V_{SS} = AGND = DGND = 0V; V_{REF} = +10V unless otherwise stated.

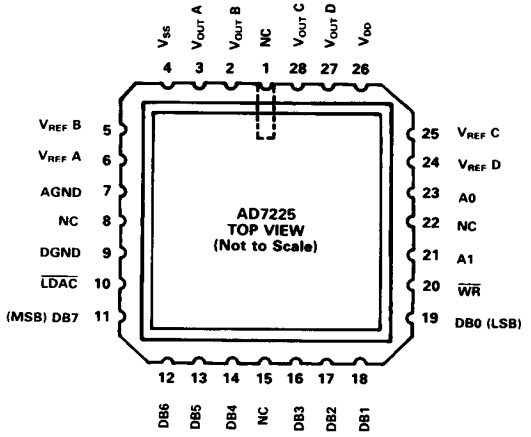
3.2.1 Functional Block Diagram and Terminal Assignments.



Q Package (Cerdip)



E Package (LCC)

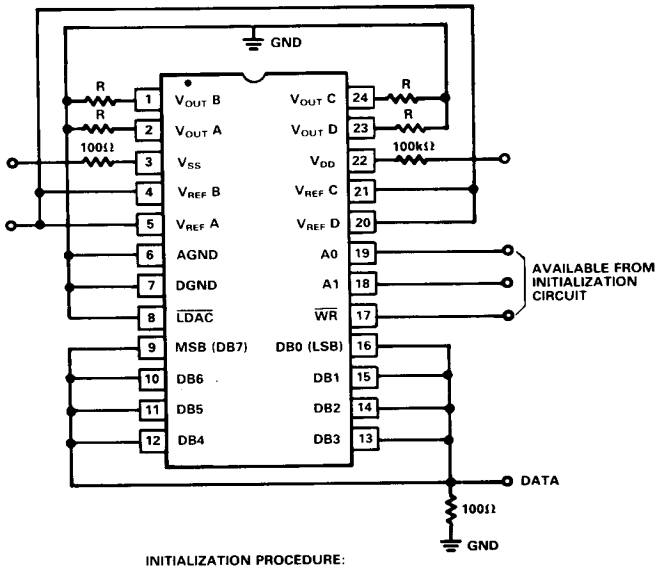


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (49).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



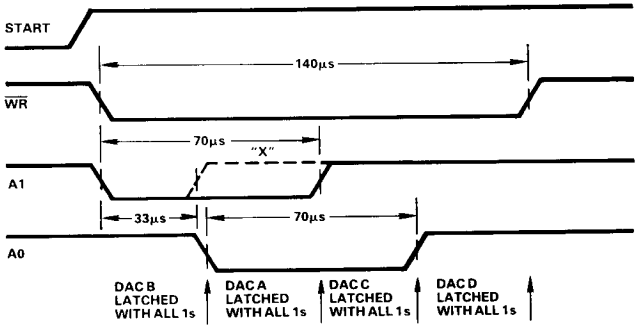
V_{DD} = +15V
V_{SS} = −5V
V_{REF} = +10V
DATA = V_{DD}
R = 10kΩ
I_{DD} ≐ 7mA
I_{SS} ≐ −5mA
I_{REF} ≐ 1mA

INITIALIZATION PROCEDURE:

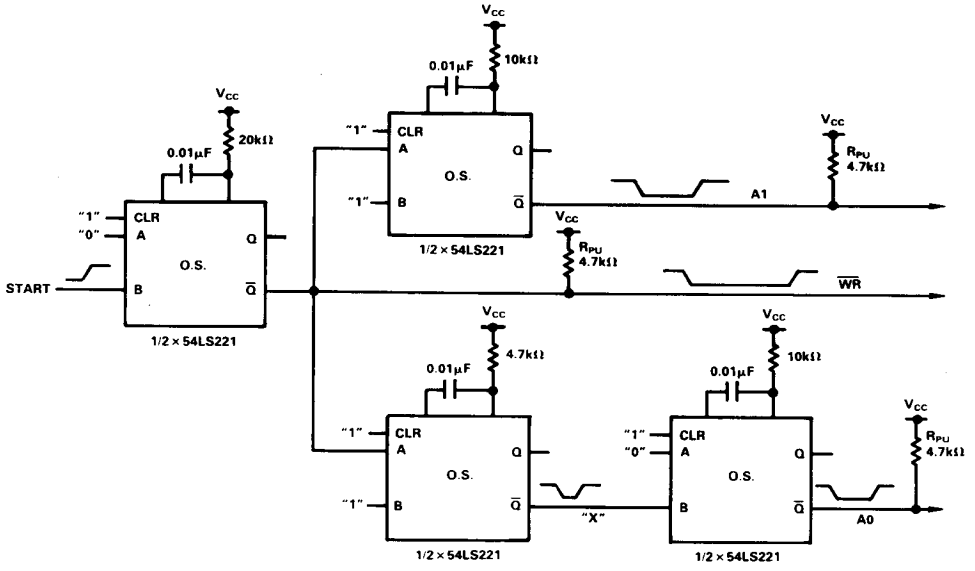
V_{DD} is turned on first, then V_{SS}, followed by V_{REF}. The V_{CC} of the initialization circuit is turned on. The START line is taken from "low" to "high", whereupon $\overline{WR}$ goes "low" for 140µs. During this time, A0 and A1 go through the following states:

A1	A0	DAC ADDRESSED
GND	V_{CC}	DAC B
GND	GND	DAC A
V_{CC}	GND	DAC C
V_{CC}	V_{CC}	DAC D

Thus, all four DACs are loaded with all 1's.



Timing Diagram and Initialization Circuit



Initialization Circuit

5.0 Interface Logic Information.

The AD7225 contains two registers per DAC, an input register and a DAC register. Address lines A0 and A1 select which input register will accept data from the input port. When the $\overline{WR}$ signal is LOW, the input latches of the selected DAC are transparent. The data is latched into the addressed input register on the rising edge of $\overline{WR}$. Table 3 shows the addressing for the input registers on the AD7225.

Table 3. AD7225 Addressing

A1	A0	Selected Input Register
L	L	DAC A Input Register
L	H	DAC B Input Register
H	L	DAC C Input Register
H	H	DAC D Input Register

Table 4. AD7225 Truth Table

$\overline{WR}$	$\overline{LDAC}$	Function
H	H	No Operation. Device Not Selected
L	H	Input Register of Selected DAC Transparent
	H	Input Register of Selected DAC Latched
H	L	All Four DAC Registers Transparent (i.e., Outputs Respond to Data Held in Respective Input Registers). Input Registers are Latched
H		All Four DAC Registers Latched
L	L	DAC Registers and Selected Input Register Transparent Output follows Input Data for Selected Channel

Only the data held in the DAC register determines the analog output of the converter. The $\overline{LDAC}$ signal is common to all four DACs and controls the transfer of information from the input registers to the DAC registers. Data is latched into all four DAC registers simultaneously on the rising edge of $\overline{LDAC}$. The $\overline{LDAC}$ signal is level triggered and therefore the DAC registers may be made transparent by tying $\overline{LDAC}$ LOW (in this case the outputs of the converters will respond to the data held in their respective input latches). $\overline{LDAC}$ is an asynchronous signal and is independent of $\overline{WR}$. This is useful in many applications. However, in systems where the asynchronous $\overline{LDAC}$ can occur during a write cycle (or vice versa) care must be taken to ensure that incorrect data is not latched through to the output. In other words, if $\overline{LDAC}$ is activated prior to the rising edge of $\overline{WR}$ (or $\overline{WR}$ occurs during $\overline{LDAC}$), then $\overline{LDAC}$ must stay LOW for t_6 or longer after $\overline{WR}$ goes HIGH to ensure correct data is latched through to the output. Table 4 shows the truth table for AD7225 operation. Figure 1 shows the input control logic for the part and the write cycle timing diagram is given in Figure 2.

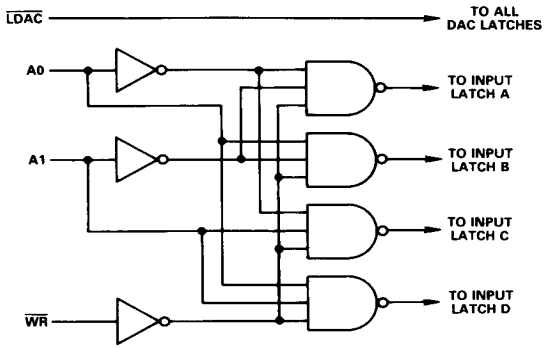


Figure 1. Input Control Logic

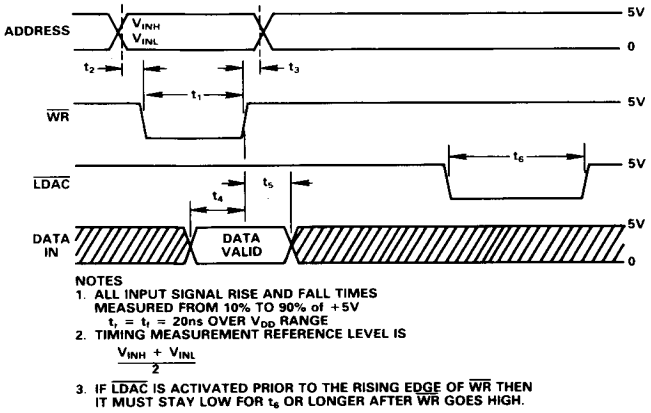


Figure 2. Write Cycle Timing Diagram