

1.1 Scope.

This specification covers the detail requirement for a 12-bit multiplying, quad, voltage output, digital-to-analog converter with readback and selectable modes.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number ¹
-1	AD664SD-UNI/883B
-2	AD664SD-BIP/883B
-3	AD664TD-UNI/883B
-4	AD664TD-BIP/883B
-5	AD664TE/883B
-6	AD664TJ/883B

NOTE

¹See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

Type	Package	Description
D	D-28	28-Pin Ceramic DIP
E	E-44A	44-Pin LCC
J	J-44	44-Pin JLCC

1.3 Absolute Maximum Ratings. ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{LL} to DGND	0 to +7 V
V_{CC} to DGND	0 to +18 V
V_{EE} to DGND	-18 V to 0 V
Soldering	+300°C, 10 sec
Power Dissipation	1000 mW
AGND to DGND	-1 V to +1 V
Reference Input	$V_{REF} \leq 10 \text{ V}$ and $V_{REF} \leq (V_{CC} - 2 \text{ V}, V_{EE} + 2 \text{ V})$
V_{CC} to V_{EE}	0 to +36 V
Digital Inputs	-0.3 V to +7 V
Analog Outputs	Indefinite Shorts to V_{CC} , V_{LL} , V_{EE} and GND

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC}	$= 25^\circ\text{C/W}$ for D-28
θ_{JA}	$= 60^\circ\text{C/W}$ for D-28
θ_{JC}	$= 42^\circ\text{C/W}$ for E-44A
θ_{JA}	$= 125^\circ\text{C/W}$ for E-44A
θ_{JC}	$= 3.6^\circ\text{C/W}$ for J-44

AD664—SPECIFICATIONS

Table 1.

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2, 3, 4, 5, 6	12	12	12			Bits
Relative Accuracy	RA	-1, 2	3/4	3/4	1			±LSB max
		-3, 4	1/2	3/4	1	1/2		
		-5, 6	1/2	1/2	3/4			
Differential Nonlinearity	DNL	-1, 2	3/4	3/4	1		Major Carry Errors	±LSB max
		-3, 4	1/2	3/4	1	1/2		
		-5, 6	1/2	1/2	1			
Gain Error	A _E	-1, 2	7	7			All Bits On	±LSB max
		-3, 4	5	7		5		
		-5, 6	5	5				
Gain Tempco	TCA _E	-1, 2	12		12		All Bits On	±ppm/°C max
		-3, 4, 5, 6	10		10			
Unipolar Offset Error	V _{OS}	-1	2	2			All Bits Off	±LSB max
		-3	1	2		1		
		-5, 6	1	1				
Unipolar Offset Tempco	TCV _{OS}	-1	3		3		All Bits Off	±ppm/°C max
		-3, 5, 6	2		2			
Bipolar Zero Error ²	B _{PZE}	-2	3	3			MSB On, All Others Off	±LSB max
		-4	2	3		2		
		-5, 6	2	2				
Bipolar Zero Tempco	TC _{PZE}	-2	12		12		MSB On, All Others Off	ppm/°C max
		-4, 5, 6	10		10			
Reference Input Resistance	R _{IN}	-1, 2, 3, 4, 5, 6	1.3					kΩ min
			2.6					kΩ max
Ref Voltage Range ³	V _{REF}	-1, 2, 3, 4, 5, 6	V _{EE} +2, V _{CC} -2					Volts
Voltage Output, UNI ⁴	V _{OU}	-1, 3, 5, 6	0, V _{CC} -2					Volts
Voltage Output, BIP ⁴	V _{OB}	-2, 4, 5, 6	V _{CC} -2, V _{EE} +2					Volts
Output Current	I _{OUT}	-1, 2, 3, 4, 5, 6	5					mA min
I Short Circuit	I _{SC}	-1, 2, 3, 4, 5, 6	40					mA max
Output Voltage Settling Time	t _{SL}	-1, 2, 3, 4, 5, 6	10					μs max
Power Supply Current	I _{LL}	-1, 2, 3, 4, 5, 6	6	6			V _{IH} = +2, V _{IL} = 0.8	mA max
			1	1			V _{IH} = V _{LL} , V _{IL} = 0	
	I _{CC}	-1, 2, 3, 4, 5, 6	15	15			I _{CC} : All Bits On	
	I _{EE}	-1, 2, 3, 4, 5, 6	19	19			I _{CC} : All Bits Off	
Gain Matching Error ⁵	mA _E	-1, 2	6	6				±LSB max
		-3, 4	4	6		4		
		-5, 6	4	4				
Offset Matching Error ⁶	mV _{OS}	-1	2	2				±LSB max
		-3	1	2		1		
		-5, 6	1	1				
Bipolar Zero Matching Error ⁷	mB _{PZE}	-2	3	3				±LSB max
		-4	2	3		2		
		-5, 6	2	2				

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Digital In High Voltage	V_{IH}	-1, 2, 3, 4, 5, 6	2.0	2.0	2.0			Volts min
Digital In Low Voltage	V_{IL}	-1, 2, 3, 4, 5, 6	0.8	0.8	0.8			Volts max
Digital In High Current	I_{IH}	-1, 2, 3, 4, 5, 6	10 10 10 10	10 10 10 10	10 10 10 10		$V_{IN} = V_{LL}$: Data Inputs $\overline{CS}/DS0/DS1/\overline{RST}/RD/LS$ $\overline{MS}/TR^8$ $QS0/QS1/QS2^8$	$\pm \mu A$ max $\pm \mu A$ max $\pm \mu A$ min $+ \mu A$ max
Digital In Low Current	I_{IL}	-1, 2, 3, 4, 5, 6	10 10 10 10	10 10 10 10	10 10 10 10		$V_{IN} = DGND$: Data Inputs $\overline{CS}/DS0/DS1/\overline{RST}/RD/LS$ $\overline{MS}/TR^8$ $QS0/QS1/QS2^8$	$\pm \mu A$ max $\pm \mu A$ max $- \mu A$ max $\pm \mu A$ max
Digital Out Low Voltage	V_{OL}	-1, 2, 3, 4, 5, 6	0.4	0.4	0.4			+ Volts max
Digital Out High Voltage	V_{OH}	-1, 2, 3, 4, 5, 6	2.4	2.4	2.4			+ Volts min
Power Supply Gain Sensitivity	PSGS	-1, 2, 3, 4, 5, 6		5 5 5			$11.4 V \leq V_{CC} \leq 16.5 V$ $-16.5 V \leq V_{EE} \leq -11.4 V$ $4.5 V \leq V_{LL} \leq 5.5 V$	$\pm ppm/\%$

NOTES

¹ $V_{CC} = +15 V$, $V_{EE} = -15 V$, 50 Ω resistor Pin 6 to Pin 7, A0, A1, A2, A3, $\overline{CS}$ = Logic "0," $V_{IH} = 2.0 V$, $V_{IL} = 0.8 V$, unipolar configuration.

²Bipolar zero error is the difference from the ideal output (0 volts) and the actual output voltage with code 100 000 000 000 applied to the inputs.

³For $V_{CC} < 12 V$ and $V_{EE} > -12 V$. Voltage not to exceed 10 V maximum.

⁴A minimum power supply of $\pm 12.0 V$ is required for 0 to +10 V and $\pm 10 V$ operation. A minimum power supply of $\pm 11.4 V$ is required for -5 V to +5 V operation.

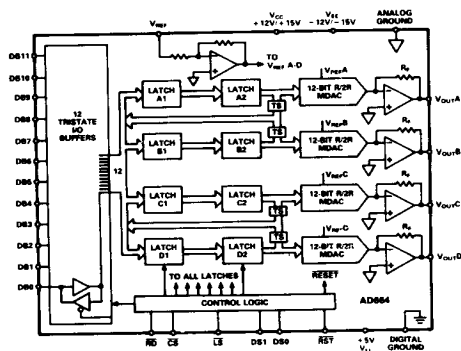
⁵Gain error matching is the largest difference in gain error between any two DACs in one package.

⁶Offset error matching is the largest difference in offset error between any two DACs in one package.

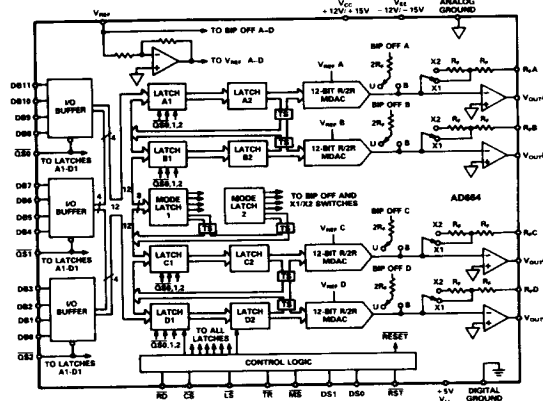
⁷Bipolar zero matching is the largest difference in bipolar zero error between any two DACs in one package.

⁸44-pin versions only.

3.2.1 Functional Block Diagrams and Terminal Assignments.

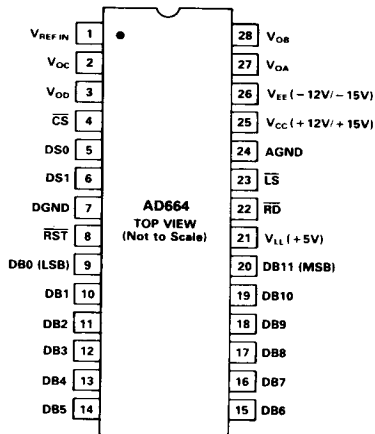


28-Pin Block Diagram

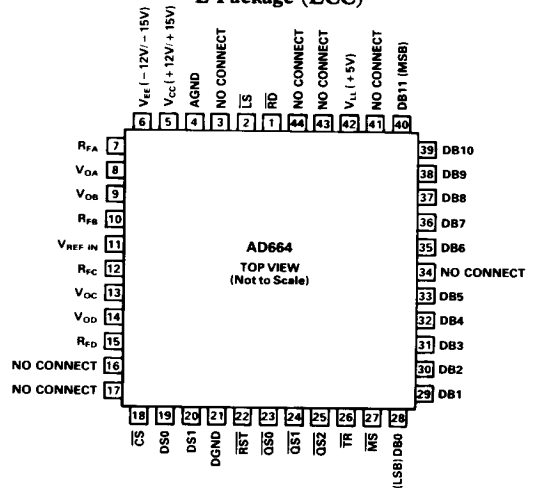


44-Pin Block Diagram

D Package (DIP)



**J Package (JLCC)
and
E Package (LCC)**



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (56).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

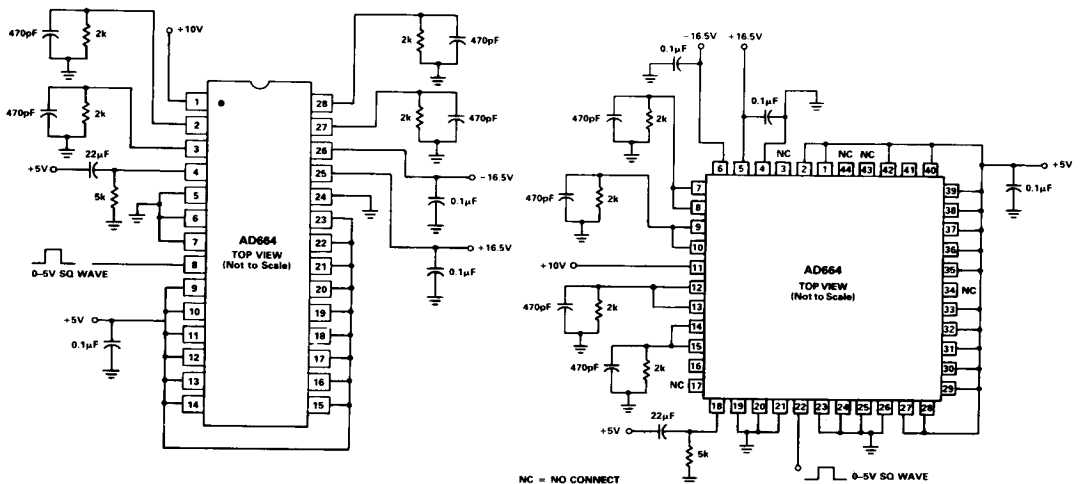


Table 2.

Digital Timing Specifications

Parameter	Symbol	Limit		Units
		+25°C (Min)	−55°C to +125°C (Min)	
Data Input (Figure 1)				
CS Pulse Width	t _{CW}	80	100	ns
Data Setup	t _{DS}	0	0	ns
Data Hold	t _{DH}	15	15	ns
Address Setup	t _{AS}	0	0	ns
Address Hold	t _{AH}	15	15	ns
LS Setup	t _{LS}	0	0	ns
LS Hold	t _{LH}	15	15	ns
Data Input (Figure 3)				
Data Setup	t _{DS}	0	0	ns
Data Hold	t _{DH}	0	0	ns
LS Width	t _{LW}	60	80	ns
LS Setup	t _{LS}	0	0	ns
CS Hold	t _{CH}	30	50	ns
Address Setup	t _{AS}	0	0	ns
Address Hold	t _{AH}	0	0	ns
Mode Select (Figure 5)				
MS Setup	t _{MS}	0	0	ns
Address Setup	t _{AS}	0	0	ns
Data Setup	t _{DS}	0	0	ns
LS Width	t _{LW}	60	70	ns
CS Hold	t _{CH}	70	80	ns
Data Hold	t _{DH}	0	0	ns
MS Hold	t _{MH}	0	0	ns
Mode Select (Figure 7)				
MS Setup	t _{MS}	0	0	ns
MS Hold	t _{MH}	15	15	ns
LS Setup	t _{LS}	0	0	ns
Data Setup	t _{DS}	0	0	ns
CS Width	t _W	80	100	ns
LS Hold	t _{LH}	15	15	ns
Data Hold	t _{DH}	15	15	ns
Readback (Figure 8, 10)				
Address Setup	t _{AS}	0	0	ns
Address Hold	t _{AH}	0	0	ns
RD Setup	t _{RS}	0	0	ns
RD Hold	t _{RH}	0	0	ns
MS Setup	t _{MS}	0	0	ns
MS Hold	t _{MH}	0	0	ns
Data Access	t _{DV}	150	180	ns
Data Release	t _{DF}	60	75	ns
Transparent Operation (Figure 11) (44-Pin Version Only)				
Address Setup	t _{AS}	0	0	ns
Quad Select Setup	t _{QS}	0	0	ns
Transparent Setup	t _{TS}	0	0	ns
Transparent Width	t _{TW}	80	90	ns
Chip Select Hold	t _{CH}	90	110	ns
Data Hold	t _{DH}	0	0	ns
Quad Select Hold	t _{QH}	0	0	ns
Asynchronous Reset (Figure 12)				
Reset Width	t _{RW}	80	100	ns

NOTES

¹For $t_{LS} > 0$, the width of $\overline{LS}$ must be increased by the same amount that t_{LS} is greater than 0 ns.

Timing specifications are relative to $\overline{CS}$. $V_{CC} = +15$ V, $V_{EE} = -15$ V, $V_{REF} = +10$ V, $V_{IH} = 2.4$ V, $V_{IL} = 0.4$ V. Specifications are guaranteed but not tested. Refer to Figures 1-12.

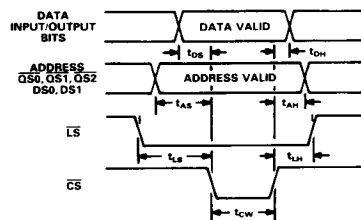


Figure 1. Preload First Rank of a DAC

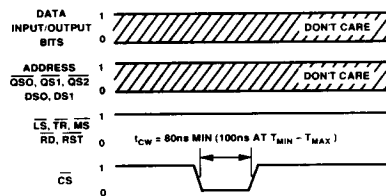


Figure 2. Update Second Rank of a DAC

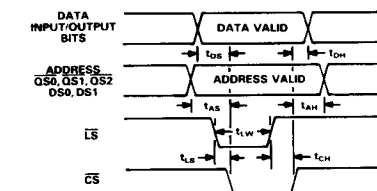


Figure 3. Update Output of a Single DAC

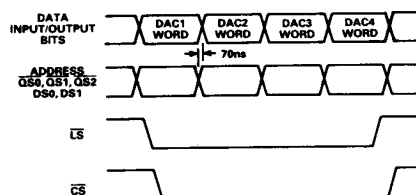


Figure 4. Update All DAC Outputs

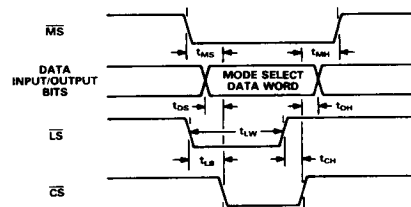


Figure 5. Load and Update Mode of One DAC

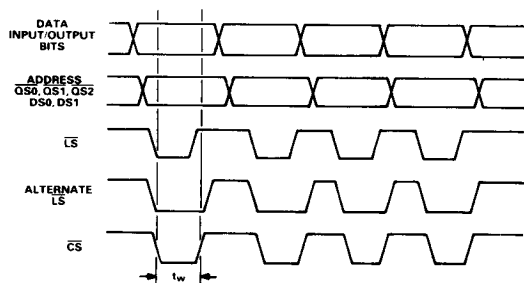


Figure 6. Load and Update Multiple DACs

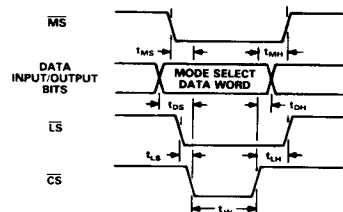


Figure 7. Preload Mode Select Register

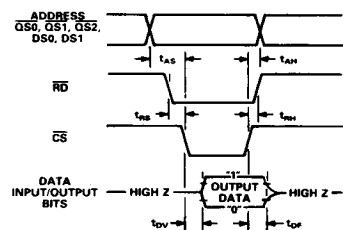


Figure 8. DAC Input Code Readback

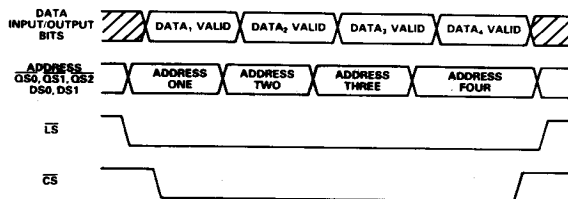


Figure 9. Preload First Rank Registers

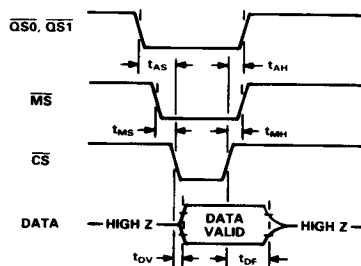


Figure 10. Mode Select Readback

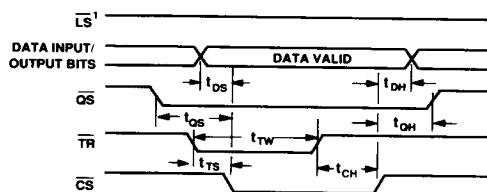


Figure 11. Fully Transparent Mode

Table 3. AD664 Truth Table

Function	DS1, DS0	Ls	Ms	TR	Q50, I, Z ¹	RD	Cs	RST
Load 1st Rank								
DACA	00	0	1	1	Select Quad	1	1→0	1
DACB	01	0	1	1	Select Quad	1	1→0	1
DACC	10	0	1	1	Select Quad	1	1→0	1
DACD	11	0	1	1	Select Quad	1	1→0	1
Load 2nd Rank	XX	1	1	1	XXX	1	1→0	1
Read 2nd Rank	Select D/A	X	1	1	Select Quad	0	1→0	1
Reset	XX	X	X	X	XXX	X	X	0
Transparent ¹								
All DACs	XX	1	1	0	000	1	1→0	1
DACA	00	0	1	0	000	1	1→0	1
DACB	01	0	1	0	000	1	1→0	1
DACC	10	0	1	0	000	1	1→0	1
DACD	11	0	1	0	000	1	1→0	1
Mode Select ^{1, 2}								
1st Rank	XX	0	0	1	00X	1	1→0	1
2nd Rank	XX	1	0	1	XXX	1	1→0	1
Readback Mode ¹	XX	X	0	1	00X	0	1→0	1

NOTES

X = Don't care. ¹For 44-pin versions only. ²For Ms, TR, Ls=0, a Ms 1st write occurs.

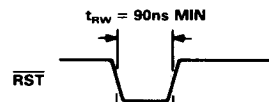


Figure 12. Asynchronous Reset Operation