NEC

MOS INTEGRATED CIRCUIT

μPD780065

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD780065 is a product of the μPD780065 Subseries in the 78K/0 Series. It is ideal for controlling CD-TEXT supporting audio equipment. Since it incorporates 5 KB of RAM, it is also ideal for control operations that require memory.

A flash memory version (μPD78F0066) that can be operated using the same power supply voltage range as that of the mask ROM version as well as a variety of development tools are also available.

Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.

μPD780065 Subseries User's Manual: U13420E
78K/0 Series User's Manual Instructions: U12326E

FEATURES

- Internal ROM: 40 KB
- Internal high-speed RAM: 1024 bytes
- Internal expansion RAM: 4096 bytes
- Buffer RAM: 32 bytes
- Minimum instruction execution time can be changed from high speed (0.24 μs) to ultra-low speed (122 μs).
- I/O ports: 60
- 8-bit resolution A/D converter: 8 channels
- Serial interface: 4 channels
  - 3-wire serial I/O mode: 1 channel
  - 3-wire serial I/O mode (a maximum 32-byte automatic transmit/receive function is incorporated.): 1 channel
  - 2-wire serial I/O mode: 1 channel
  - UART mode: 1 channel
- Timer: 5 channels
  - 16-bit timer/event counter: 1 channel
  - 8 bit timer/event counter: 2 channels
  - Watch timer: 1 channel
  - Watchdog timer: 1 channel
- Power supply voltage: V_{DD} = 2.7 to 5.5 V

APPLICATIONS

CD-TEXT supported car audios

Document No. U13732EJ1V0DS00 (1st edition)
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Printed in Japan

The mark ★ shows major revised points.

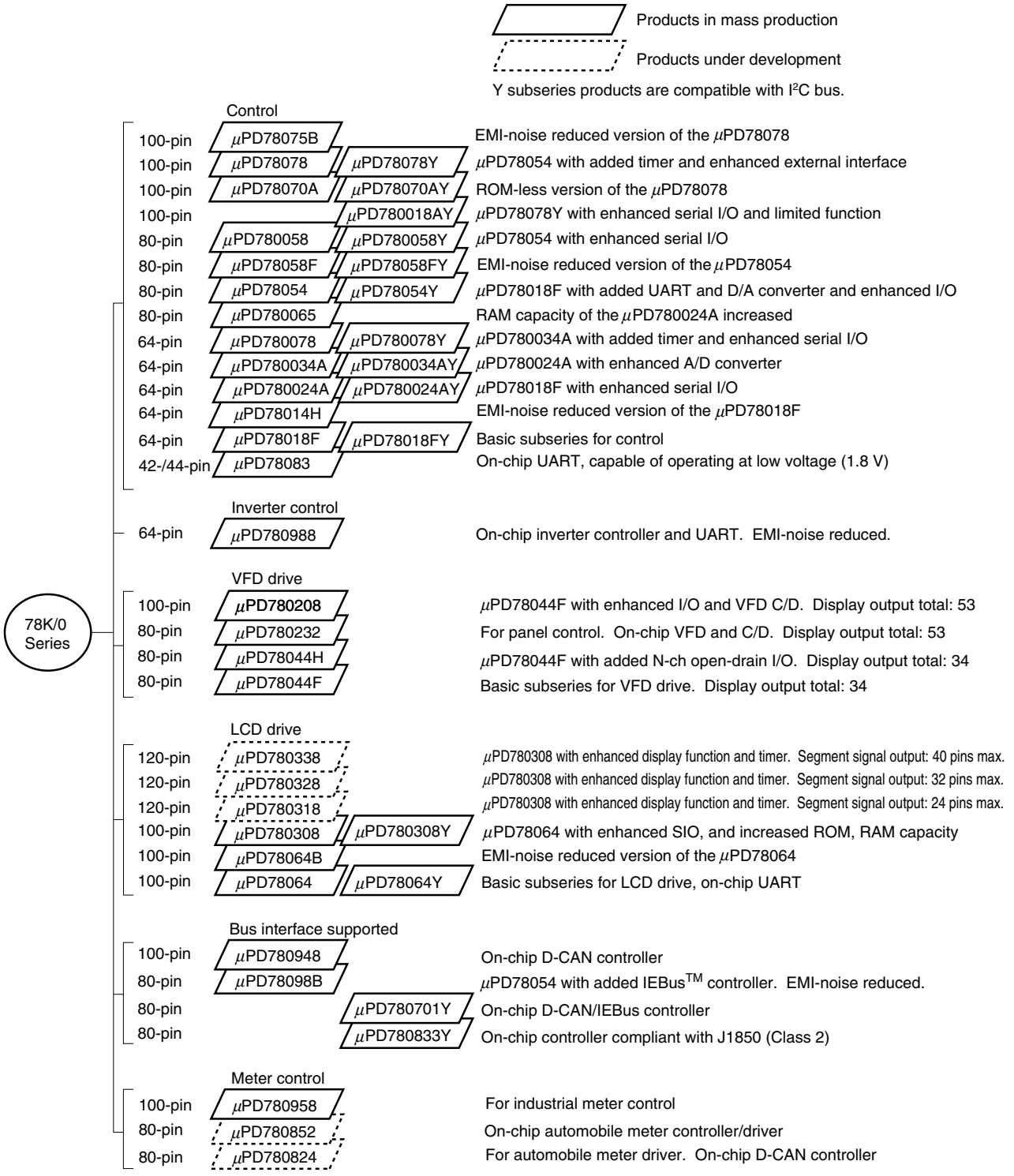
ORDERING INFORMATION

Part Number	Package
μPD780065GC-×××-8BT	80-pin plastic QFP (14 × 14)

Remark ××× indicates ROM code suffix.

★ 78K/0 SERIES LINEUP

The products in the 78K/0 Series are listed below. The names enclosed in boxes are subseries names.



Remark VFD (Vacuum Fluorescent Display) is referred to as FIP™ (Fluorescent Indicator Panel) in some documents, but the functions of the two are same.

The major functional differences between the subseries are listed below.

Subseries Name \ Function		ROM Capacity	Timer				8-Bit A/D	10-Bit A/D	8-Bit D/A	Serial Interface	I/O	V_{DD} MIN. Value	External Expansion
			8-Bit	16-Bit	Watch	WDT							
Control	μPD78075B	32 K to 40 K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	√
	μPD78078	48 K to 60 K											
	μPD78070A	—									61	2.7 V	
	μPD780058	24 K to 60 K	2 ch							3 ch (time division UART: 1 ch)	68	1.8 V	
	μPD78058F	48 K to 60 K								3 ch (UART: 1 ch)	69	2.7 V	
	μPD78054	16 K to 60 K										2.0 V	
	μPD780065	40 K to 48 K							—	4 ch (UART: 1 ch)	60	2.7 V	
	μPD780078	48 K to 60 K		2 ch			—	8 ch		3 ch (UART: 2 ch)	52	1.8 V	
	μPD780034A	8 K to 32 K		1 ch						3 ch (UART: 1 ch)	51		
	μPD780024A						8 ch	—					
	μPD78014H									2 ch	53		
	μPD78018F	8 K to 60 K											
	μPD78083	8 K to 16 K		—	—					1 ch (UART: 1 ch)	33		—
Inverter control	μPD780988	16 K to 60 K	3 ch	**Note**	—	1 ch	—	8 ch	—	3 ch (UART: 2 ch)	47	4.0 V	√
VFD drive	μPD780208	32 K to 60 K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD780232	16 K to 24 K	3 ch	—	—		4 ch				40	4.5 V	
	μPD78044H	32 K to 48 K	2 ch	1 ch	1 ch		8 ch			1 ch	68	2.7 V	
	μPD78044F	16 K to 40 K								2 ch			
LCD drive	μPD780338	48 K to 60 K	3 ch	2 ch	1 ch	1 ch	—	10 ch	1 ch	2 ch (UART: 1 ch)	54	1.8 V	—
	μPD780328										62		
	μPD780318										70		
	μPD780308	48 K to 60 K	2 ch	1 ch			8 ch	—	—	3 ch (Time division UART: 1 ch)	57	2.0 V	
	μPD78064B	32 K								2 ch (UART: 1 ch)			
	μPD78064	16 K to 32 K											
Bus interface supported	μPD780948	60 K	2 ch	2 ch	1 ch	1 ch	8 ch	—	—	3 ch (UART: 1 ch)	79	4.0 V	√
	μPD78098B	40 K to 60 K		1 ch					2 ch		69	2.7 V	—
Meter control	μPD780958	48 K to 60 K	4 ch	2 ch	—	1 ch	—	—	—	2 ch (UART: 1 ch)	69	2.2 V	—
Dash board control	μPD780852	32 K to 40 K	3 ch	1 ch	1 ch	1 ch	5 ch	—	—	3 ch (UART: 1 ch)	56	4.0 V	—
	μPD780824	32 K to 60 K								2 ch (UART: 1 ch)	59		

Note 16-bit timer: 2 channels
10-bit timer: 1 channel

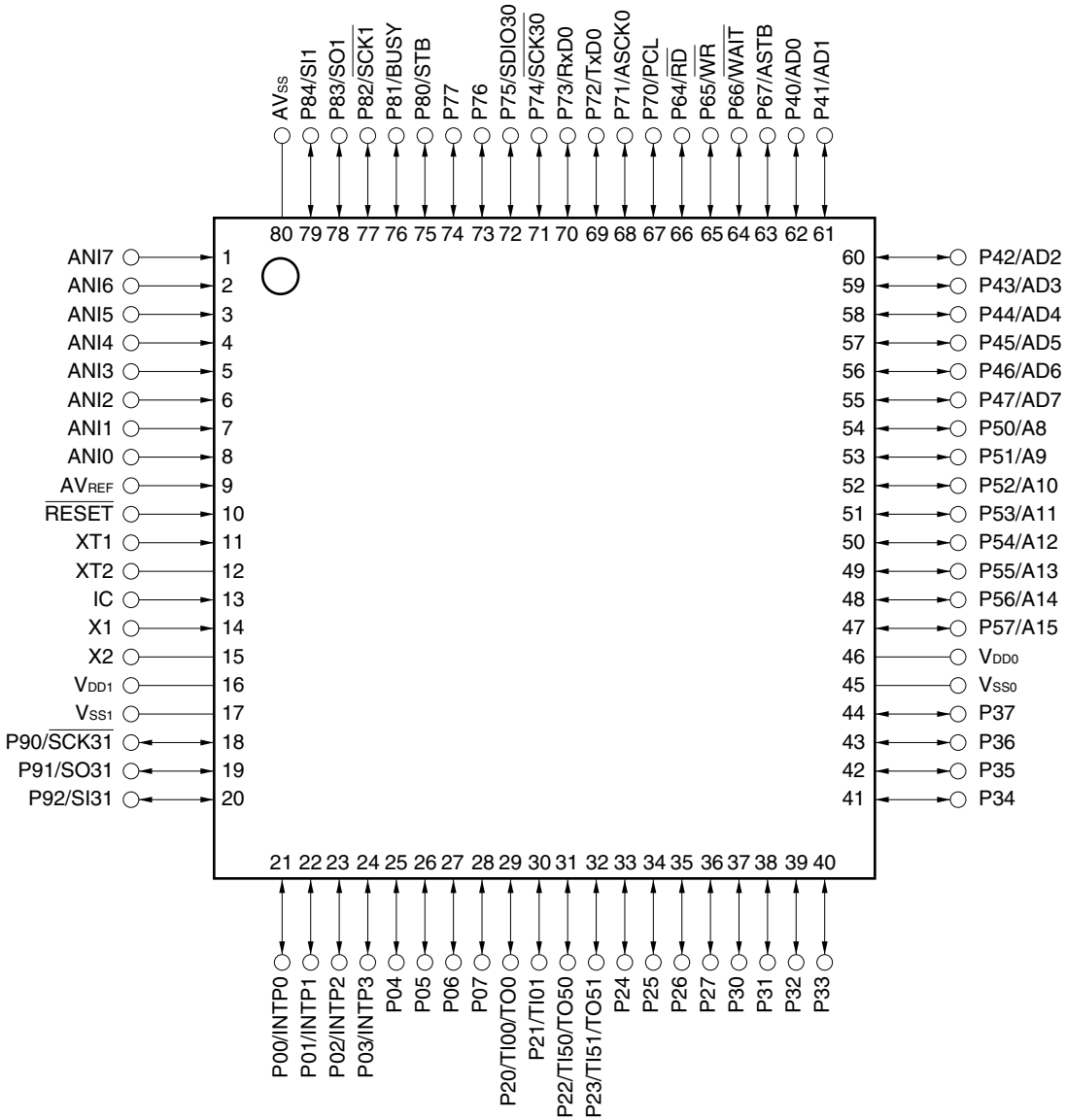
OVERVIEW OF FUNCTIONS

Item		Function
Internal memory	ROM	40 KB
	High-speed RAM	1024 bytes
	Expansion RAM	4096 bytes
	Buffer RAM	32 bytes
Memory space		64 KB
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		On-chip minimum instruction execution time variable function
	When main system clock selected	0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (at 8.38 MHz operation)
	When subsystem clock selected	122 μs (at 32.768 kHz operation)
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD correction, etc.
I/O ports		CMOS I/O: 60
A/D converter		8-bit resolution × 8 channels
Serial interface		• 3-wire serial I/O mode: 1 channel • 3-wire serial I/O mode (MAX. 32-byte on-chip automatic transmission/reception function): 1 channel • 2-wire serial I/O mode: 1 channel • UART mode: 1 channel
Timer		• 16-bit timer/event counter: 1 channel • 8-bit timer/event counter: 2 channels • Watch timer: 1 channel • Watchdog timer: 1 channel
Timer outputs		3 (8-bit PWM output capable: 2)
Clock output		65.5 kHz, 131 kHz, 262 kHz, 524 kHz, 1.05 MHz, 2.10 MHz, 4.19 MHz, 8.38 MHz (main system clock: at 8.38 MHz operation) 32.768 kHz (subsystem clock: at 32.768 kHz operation)
Vectored interrupt sources	Maskable	Internal: 14, external: 4
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V_{DD} = 2.7 to 5.5 V
Operating ambient temperature		T_A = –40 to +85°C
Package		80-pin plastic QFP (14 × 14)

CONTENTS

1. PIN CONFIGURATION (TOP VIEW)

- **80-pin plastic QFP (14 × 14)**
  μPD780065GC-×××-8BT



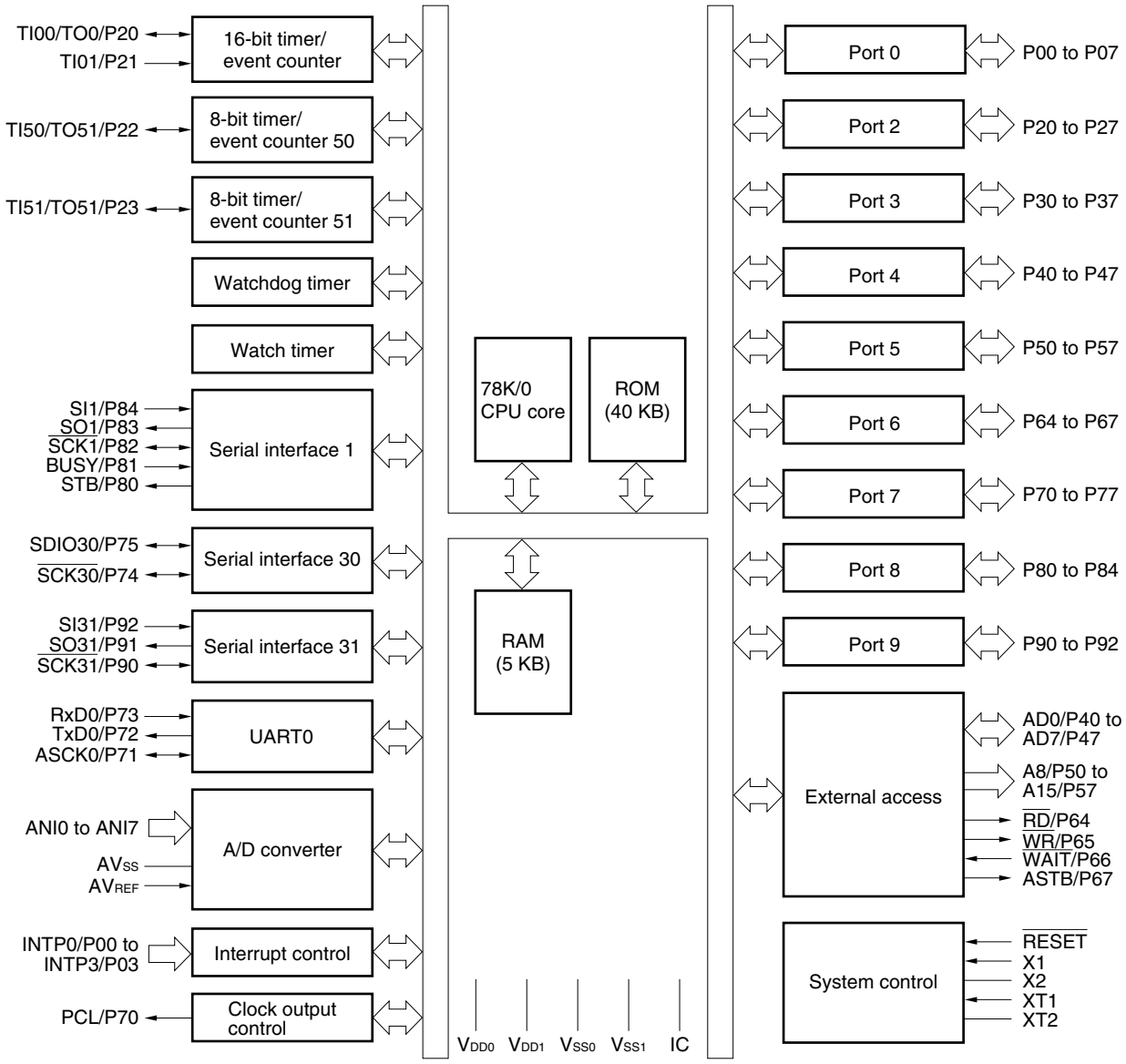
Cautions 1. Connect the IC (internally connected) pin directly to V_{SS0} or V_{SS1}.

2. Connect the AV_{SS} pin to V_{SS0}.

Remark When the μPD780065 is used in application fields that require reduction of the noise generated from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

A8 to A15:	Address bus	PCL:	Programmable clock
AD0 to AD7:	Address/data bus	$\overline{RD}$:	Read strobe
ANI0 to ANI7:	Analog input	$\overline{RESET}$:	Reset
ASCK0:	Asynchronous serial clock	RxD0:	Receive data
ASTB:	Address strobe	$\overline{SCK1}$, $\overline{SCK30}$, $\overline{SCK31}$:	Serial clock
AV_{REF}:	Analog reference voltage	SDIO30:	Serial data input/output
AV_{SS}:	Analog ground	SI1, SI31:	Serial input
BUSY:	Busy	SO1, SO31:	Serial output
IC:	Internally connected	STB:	Strobe
INTP0 to INTP3:	External interrupt input	TI00, TI01, TI50, TI51:	Timer input
P00 to P07:	Port 0	TO0, TO50, TO51:	Timer output
P20 to P27:	Port 2	TxD0:	Transmit data
P30 to P37:	Port 3	V_{DD0}, V_{DD1}:	Power supply
P40 to P47:	Port 4	V_{SS0}, V_{SS1}:	Ground
P50 to P57:	Port 5	$\overline{WAIT}$:	Wait
P64 to P67:	Port 6	$\overline{WR}$:	Write strobe
P70 to P77:	Port 7	X1, X2:	Crystal (main system clock)
P80 to P84:	Port 8	XT1, XT2:	Crystal (subsystem clock)
P90 to P92:	Port 9		

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 Port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
P00 to P03	I/O	Port 0 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	INTP0 to INTP3
P04 to P07				—
P20	I/O	Port 2 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	TI00/TO0
P21				TI01
P22				TI50/TO50
P23				TI51/TO51
P24 to P27				—
P30 to P37	I/O	Port 3 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	—
P40 to P47	I/O	Port 4 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	A8 to A15
P64	I/O	Port 6 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	$\overline{RD}$
P65				$\overline{WR}$
P66				$\overline{WAIT}$
P67				ASTB
P70	I/O	Port 7 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	PCL
P71				ASCK0
P72				TxD0
P73				RxD0
P74				$\overline{SCK30}$
P75				SDIO30
P76, P77				—
P80	I/O	Port 8 5-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	STB
P81				BUSY
P82				$\overline{SCK1}$
P83				SO1
P84				SI1
P90	I/O	Port 9 3-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by software.	Input	$\overline{SCK31}$
P91				SO31
P92				SI31

3.2 Non-Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0 to INTP3	Input	External interrupt request input by which the valid edge (rising edge, falling edge, or both rising edge and falling edge) can be specified	Input	P00 to P03
TI00	Input	External count clock input to 16-bit timer/event counter 0 Capture trigger signal input to capture register (CR01) of 16-bit timer/event counter	Input	P20/TO0
TI01		Capture trigger signal input to capture register (CR00) of 16-bit timer/event counter		P21
TI50		External count clock input to 8-bit timer/event counter 50		P22/TO50
TI51		External count clock input to 8-bit timer/event counter 51		P23/TO51
TO0	Output	16-bit timer/event counter 0 output	Input	P20/TI00
TO50		8-bit timer/event counter 50 output (can be used for 8-bit PWM output)		P22/TI50
TO51		8-bit timer/event counter 51 output (can be used for 8-bit PWM output)		P23/TI51
SI1	Input	Serial interface SIO1 serial data input	Input	P84
SI31	Input	Serial interface SIO31 serial data input		P92
SO1	Output	Serial interface SIO1 serial data output	Input	P83
SO31	Output	Serial interface SIO31 serial data output		P91
SDIO30	I/O	Serial interface SIO30 serial data input/output	Input	P75
$\overline{\text{SCK1}}$	I/O	Serial interface SIO1 serial clock input/output	Input	P82
$\overline{\text{SCK30}}$		Serial interface SIO30 serial clock input/output	Input	P74
$\overline{\text{SCK31}}$		Serial interface SIO31 serial clock input/output	Input	P90
BUSY	Input	Busy input for serial interface SIO1 automatic transmission/reception	Input	P81
STB	Output	Strobe output for serial interface SIO1 automatic transmission/reception	Input	P80
RxD0	Input	Serial data input for asynchronous serial interface	Input	P73
TxD0	Output	Serial data output for asynchronous serial interface	Input	P72
ASCK0	Input	Serial clock input for asynchronous serial interface	Input	P71
PCL	Output	Clock output (for trimming of main system clock and subsystem clock)	Input	P70
AD0 to AD7	I/O	Lower address/data bus for expanding memory externally	Input	P40 to P47
A8 to A15	Output	Higher address bus for expanding memory externally	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for read operation of external memory	Input	P64
$\overline{\text{WR}}$	Output	Strobe signal output for write operation of external memory	Input	P65
$\overline{\text{WAIT}}$	Input	Inserting wait for accessing external memory	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory	Input	P67
ANI0 to ANI7	Input	A/D converter analog input	Input	—

3.2 Non-Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
AV_{REF}	Output	A/D converter reference voltage input (can be used for analog power supply)	—	—
AV_{SS}	—	A/D converter ground potential. Make this pin the same potential as V_{SS0} or V_{SS1}.	—	—
$\overline{RESET}$	Input	System reset input	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation	—	—
XT2	—		—	—
V_{DD0}	—	Positive power supply for ports	—	—
V_{DD1}	—	Ground potential of ports	—	—
V_{SS0}	—	Positive power supply (except ports)	—	—
V_{SS1}	—	Ground potential (except ports)	—	—
IC	—	Internally connected. Connect this pin directly to V_{SS0} or V_{SS1}.	—	—

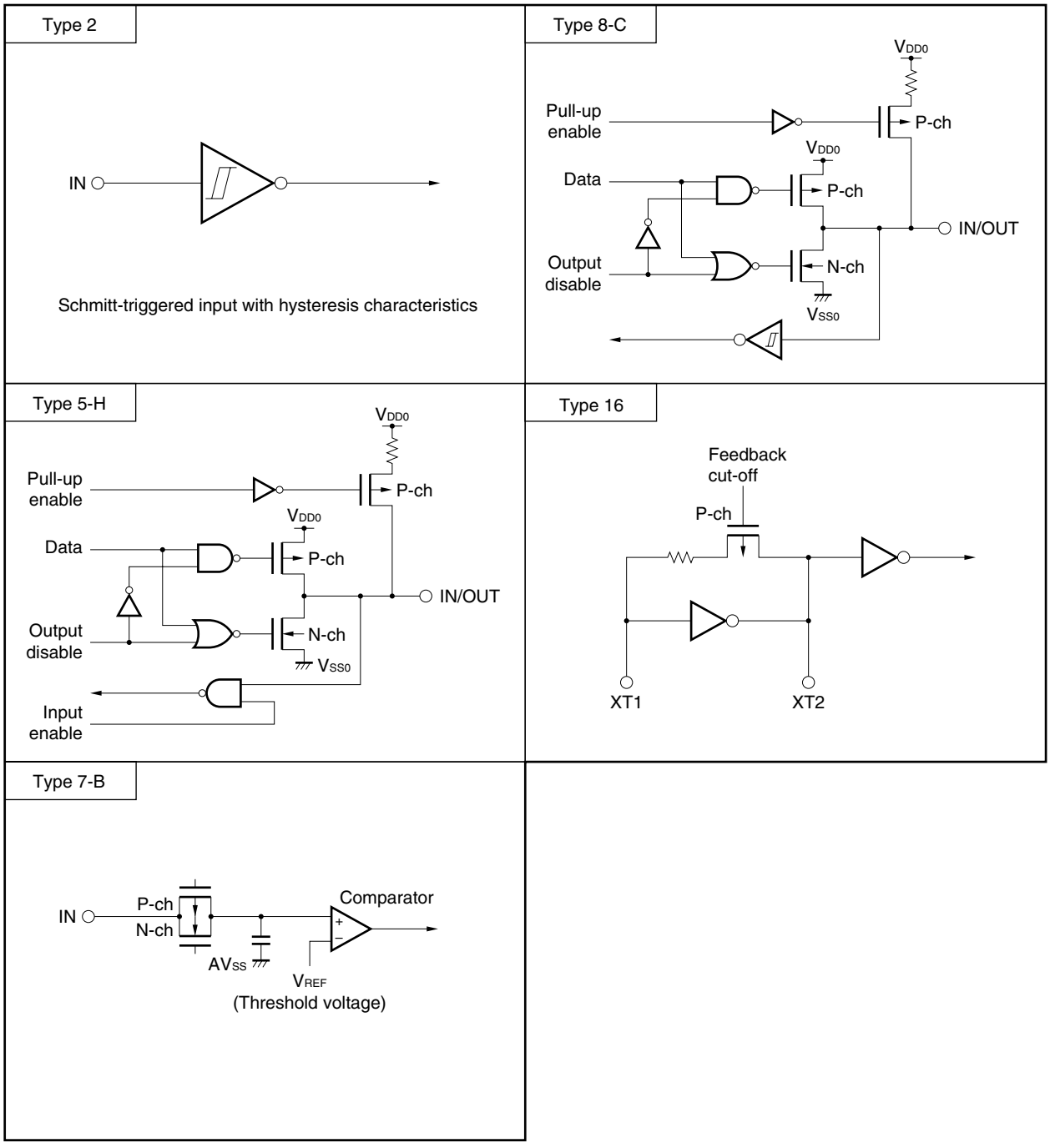
★ 3.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and recommended connections of unused pins are shown in Table 3-1.
For the I/O circuit configuration of each type, refer to Figure 3-1.

Table 3-1. Pin I/O Circuit Types and Recommended Connection of Unused Pins

Pin Name	I/O Circuit Type	I/O	Recommended Connections of Unused Pins
P00/INTP0 to P03/INTP3	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor. Output: Leave open.
P04 to P07			
P20/T100/TO0			Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P21/T101			
P22/TI50/TO50			
P23/TI51/TO51			
P24 to P27			
P30 to P37			
P40/AD0 to P47/AD7	5-H		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P50/A8 to P57/A15			Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P64/$\overline{RD}$			
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
P70/PCL			
P71/ASCK0	8-C		
P72/TxD0	5-H		
P73/RxD0	8-C		
P74/$\overline{SCK30}$			
P75/SDIO30	5-H		
P76, P77	8-C		
P80/STB	5-H		
P81/BUSY	8-C		
P82/$\overline{SCK1}$			
P83/SO1	5-H		
P84/SI1	8-C		
P90/$\overline{SCK31}$			
P91/SO31	5-H		
P92/SI31	8-C		
ANI0 to ANI7	7-B	Input	Independently connect to V_{DD0} or V_{SS0}.
XT1	16		Connect to V_{DD0}.
XT2		—	Leave open.
$\overline{RESET}$	2	Input	—
AV_{REF}	—	—	Connect to V_{SS0} or V_{SS1}.
AV_{SS}			
IC			Directly connect to V_{SS0} or V_{SS1}.

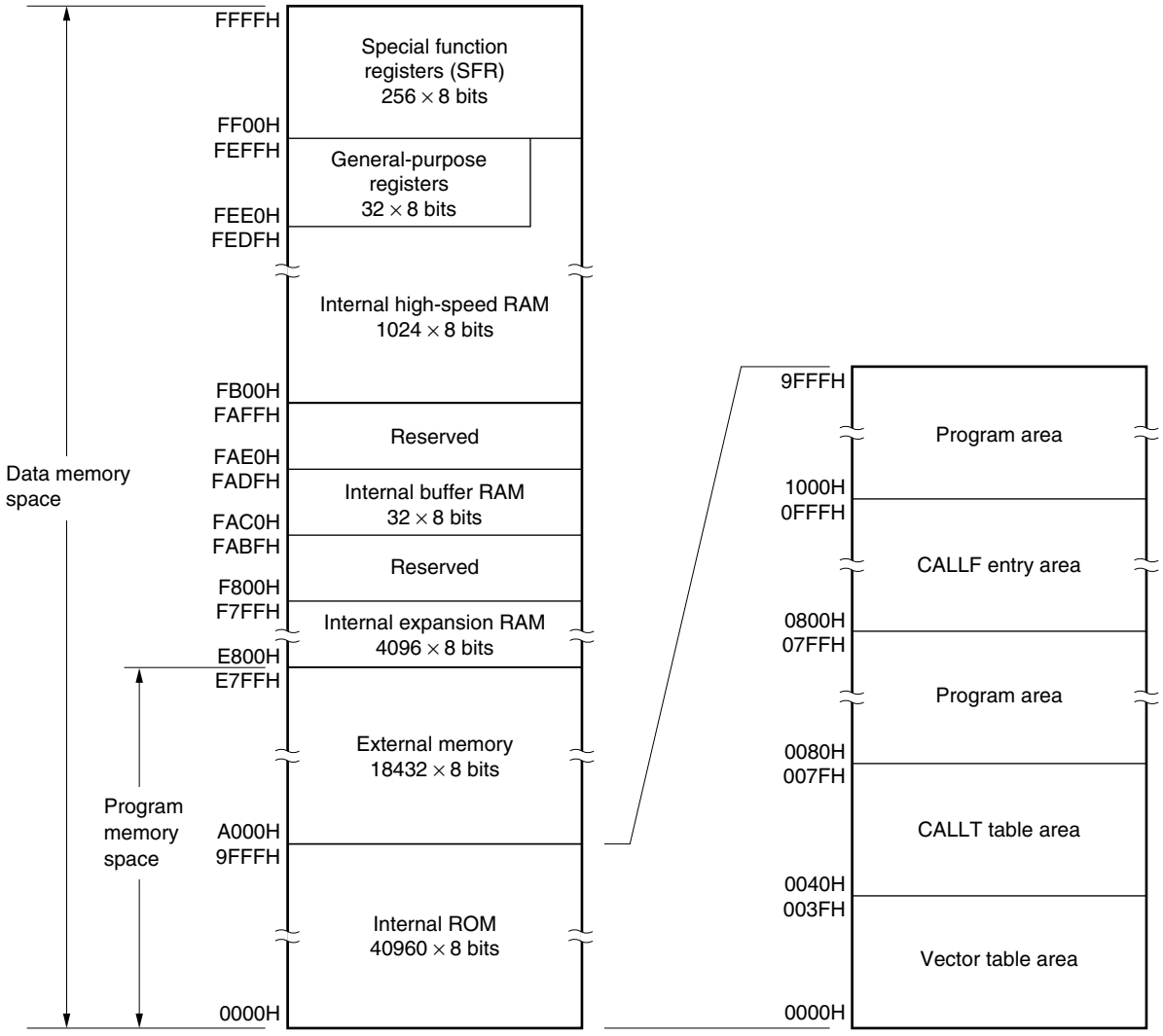
Figure 3-1. Pin I/O Circuits



4. MEMORY SPACE

Figure 4-1 shows the memory map of the μPD780065.

Figure 4-1. Memory Map



5. FEATURES OF PERIPHERAL HARDWARE

5.1 Ports

There are 60 CMOS I/O ports.

Table 5-1. Port Functions

Name	Pin Name	Function
Port 0	P00 to P07	I/O port. Input/output can be specified in 1-bit units.
Port 2	P20 to P27	Use of an on-chip pull-up resistor can be specified by software.
Port 3	P30 to P37	
Port 4	P40 to P47	
Port 5	P50 to P57	
Port 6	P64 to P67	
Port 7	P70 to P77	
Port 8	P80 to P84	
Port 9	P90 to P92	

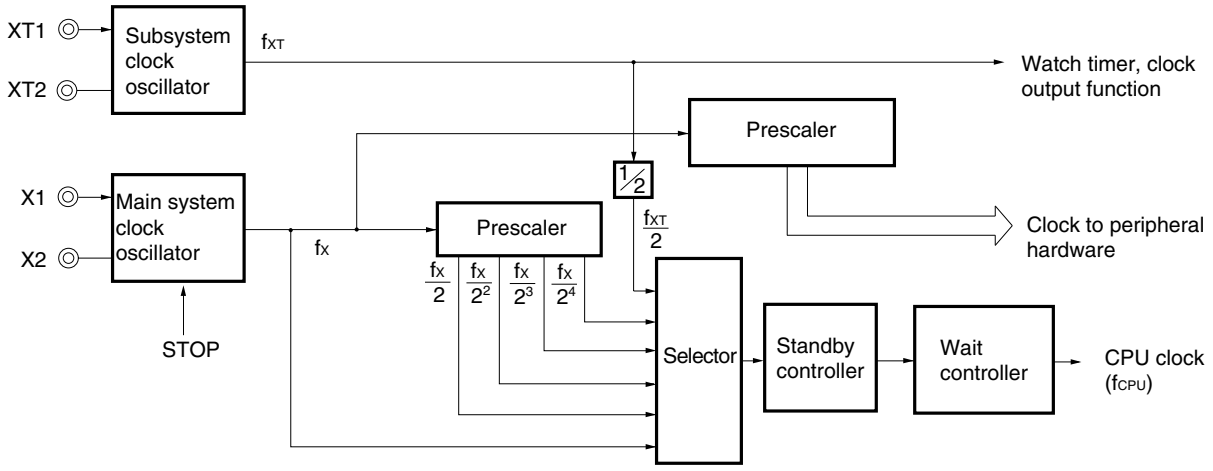
5.2 Clock Generator

A system clock generator is incorporated.

The minimum instruction execution time can be changed.

- 0.24 μs/0.48 μs/0.95 μs/1.91 μs/3.81 μs (main system clock: at 8.38 MHz operation)
- 122 μs (subsystem clock: at 32.768 kHz operation)

Figure 5-1. Block Diagram of Clock Generator



5.3 Timer/Event Counter

Five timer/event counter channels are incorporated.

- 16-bit timer/event counter: 1 channel
- 8-bit timer/event counter: 2 channels
- Watch timer: 1 channel
- Watchdog timer: 1 channel

Table 5-2. Operations of Timer/Event Counter

		16-Bit Timer/ Event Counter 0	8-Bit Timer/ Event Counter 50, 51	Watch Timer	Watchdog Timer
Operation mode					
	Interval timer	1 channel	2 channels	1 channel[Note 1]	1 channel[Note 2]
	External event counter	1 channel	2 channels	—	—
Function					
	Timer output	1 output	2 outputs	—	—
	PWM output	—	2 outputs	—	—
	PPG output	1 output	—	—	—
	Pulse width measurement	2 inputs	—	—	—
	Square wave output	1 output	2 outputs	—	—
	Interrupt source	2	2	2	1

Notes 1. The watch timer can perform both watch timer and interval timer functions at the same time.

2. The watchdog timer has the watchdog timer and interval timer functions. However, use the watchdog timer by selecting either the watchdog timer function or the interval timer function.

Figure 5-2. Block Diagram of 16-bit Timer/Event Counter 0

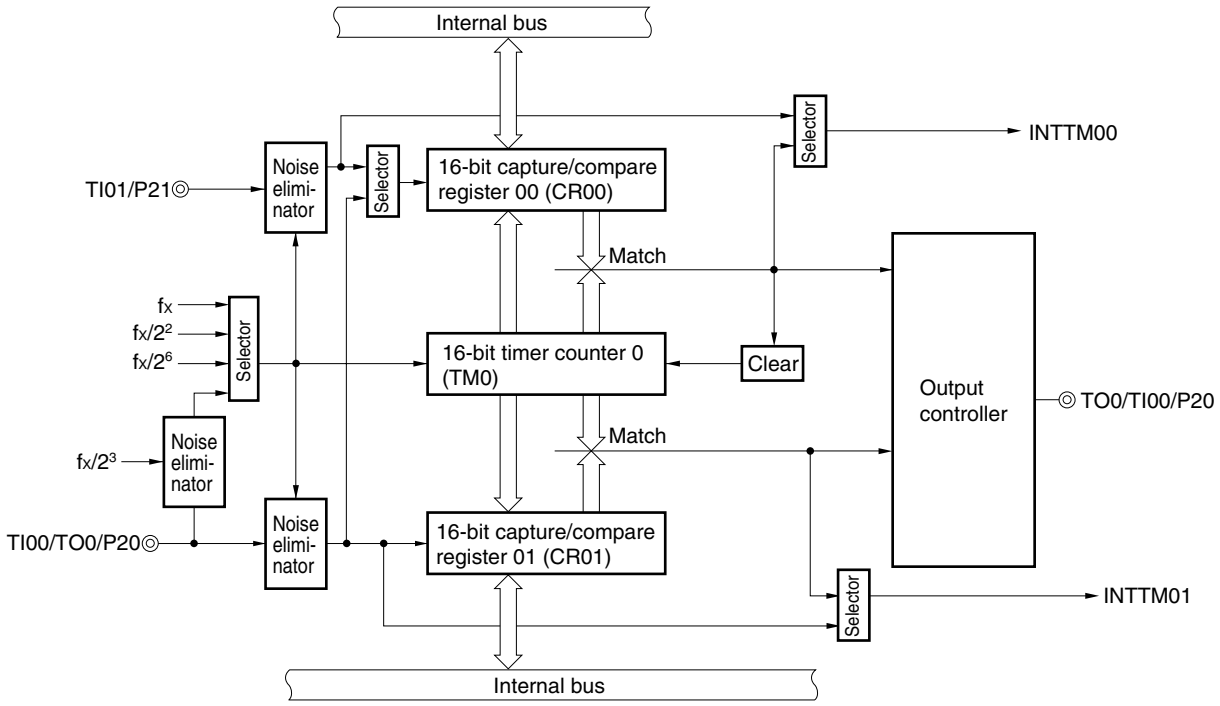


Figure 5-3. Block Diagram of 8-bit Timer/Event Counter 50

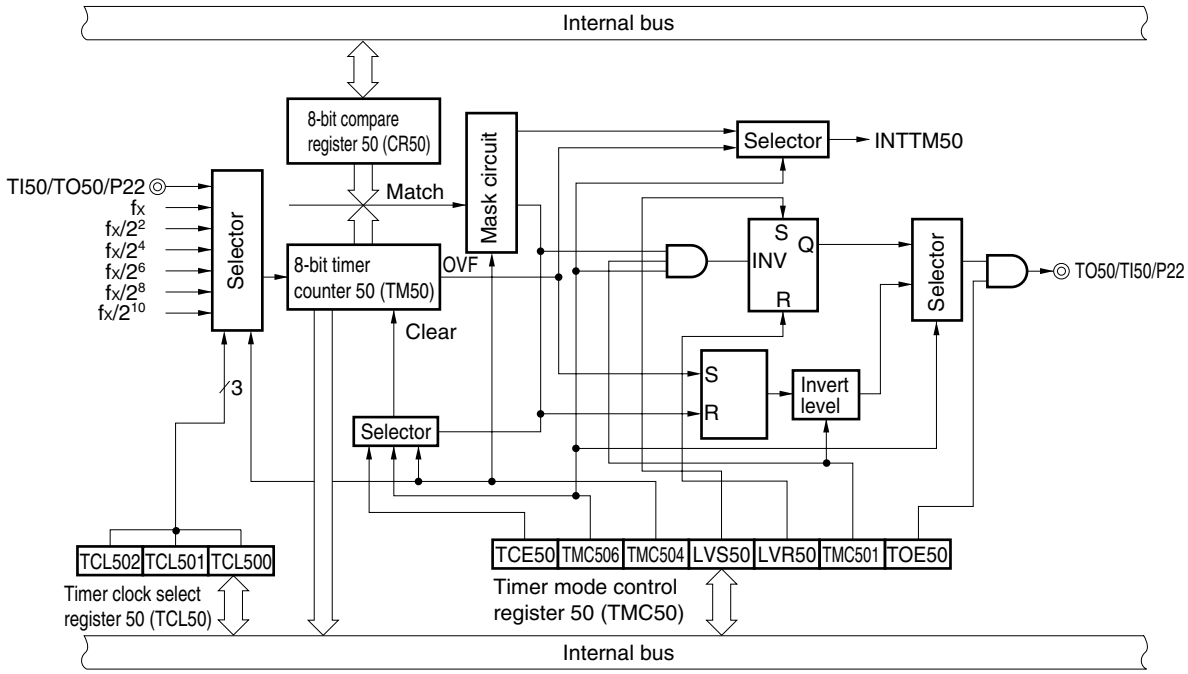


Figure 5-4. Block Diagram of 8-bit Timer/Event Counter 51

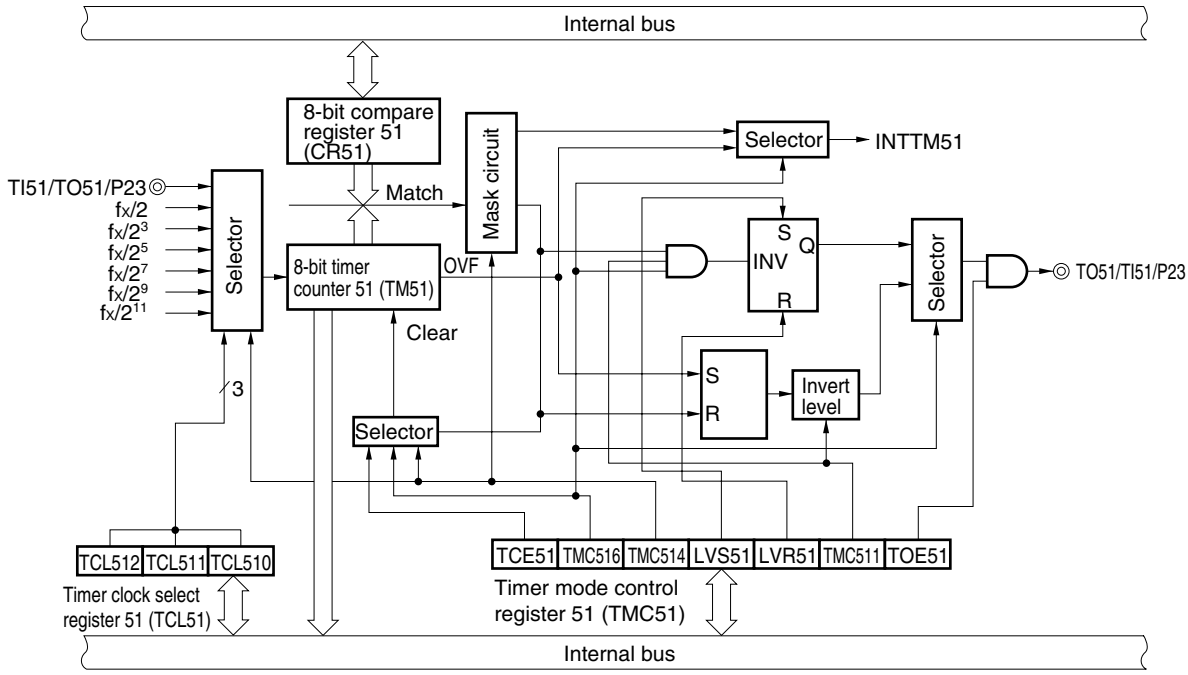


Figure 5-5. Block Diagram of Watch Timer

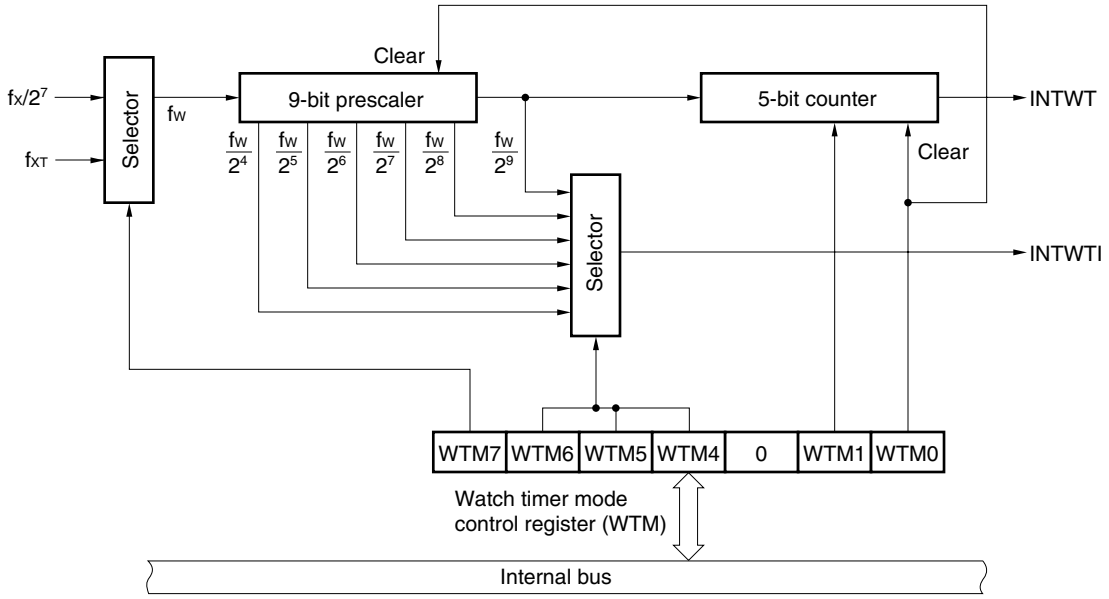
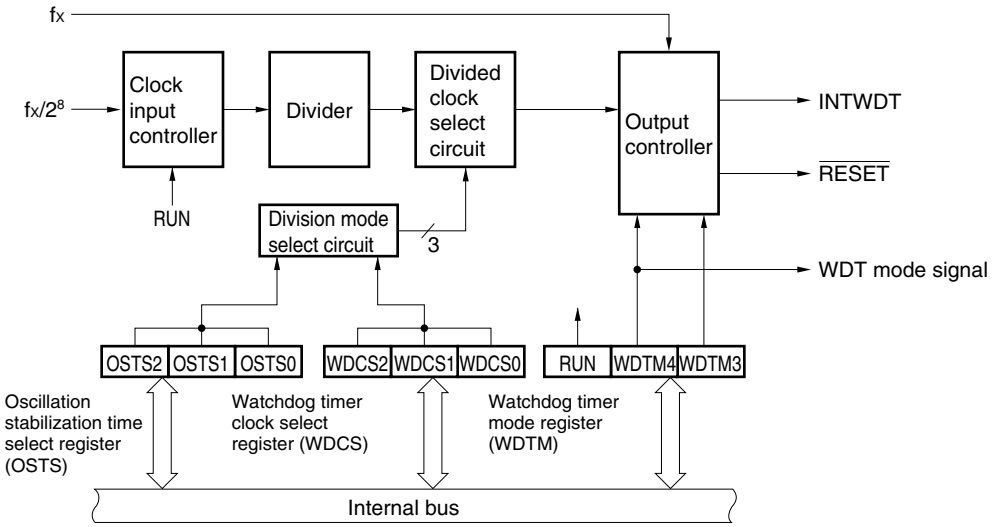


Figure 5-6. Block Diagram of Watchdog Timer



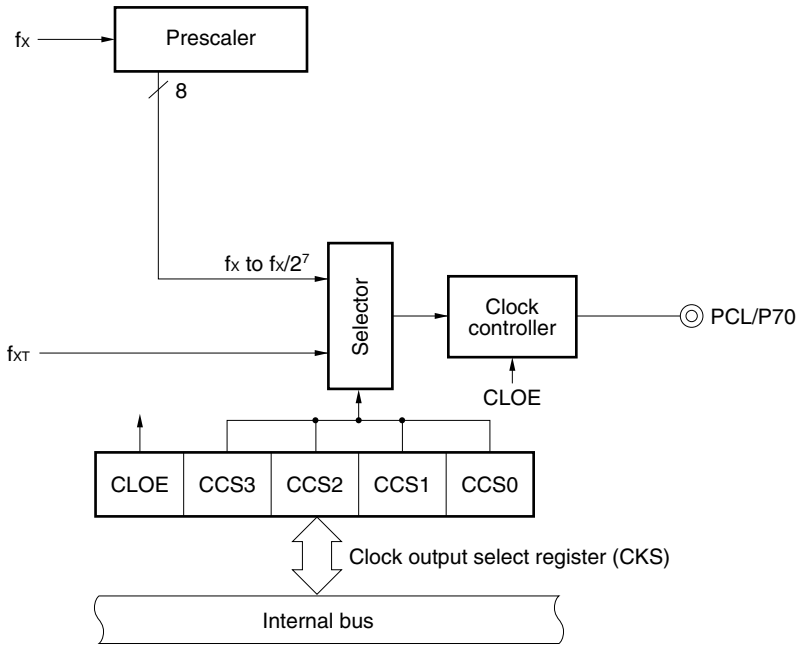
5.4 Clock Output Controller

A clock output controller (CKU) is incorporated.

Clocks with the following frequencies can be output as a clock output.

- 65.5 kHz/131 kHz/262 kHz/524 kHz/1.05 MHz/2.10 MHz/4.19 MHz/8.38 MHz (main system clock: at 8.38 MHz operation)
- 32.768 kHz (subsystem clock: at 32.768 kHz operation)

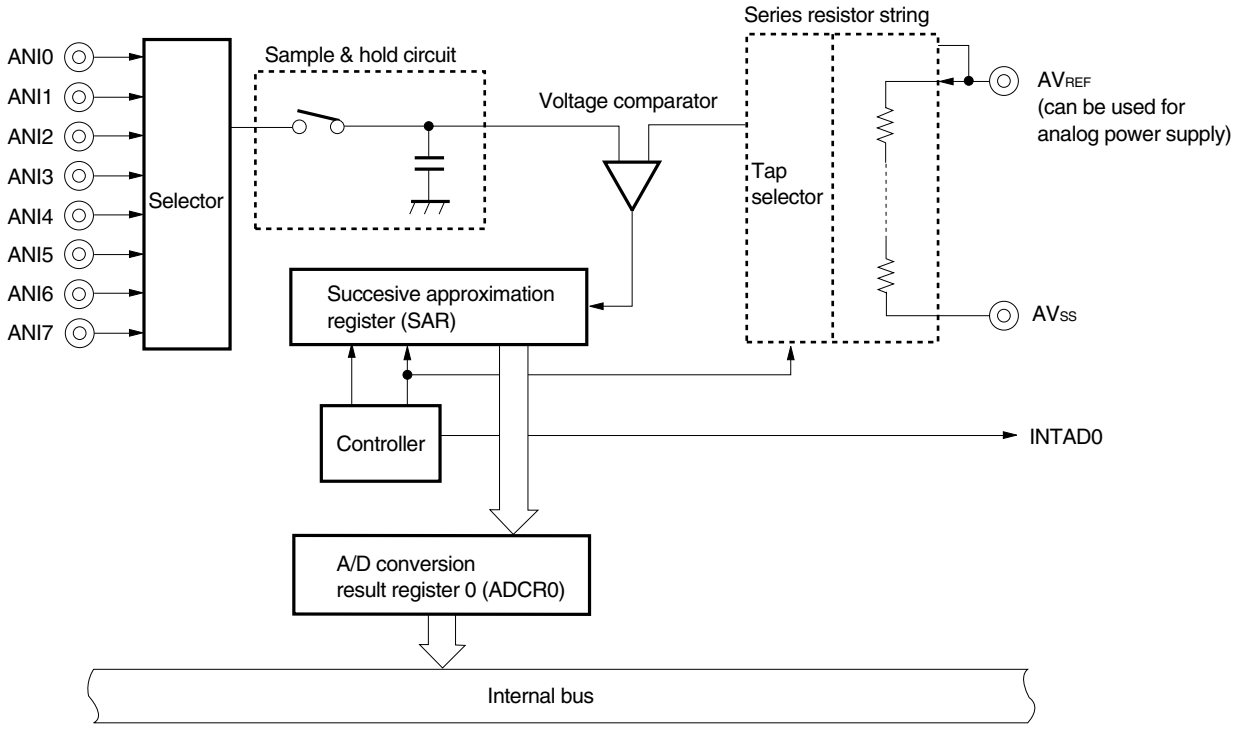
Figure 5-7. Block Diagram of Clock Output Controller CKU



5.5 A/D Converter

An A/D converter of 8-bit resolution × 8 channels is incorporated.

Figure 5-8. Block Diagram of A/D Converter



5.6 Serial Interface

Four serial interface channels are incorporated.

- Serial interface UART0: 1 channel
- Serial interface SIO1: 1 channel
- Serial interface SIO30: 1 channel
- Serial interface SIO31: 1 channel

(1) Serial interface UART0

Serial interface UART0 has two modes, asynchronous serial interface (UART) mode and infrared data transfer mode.

- **Asynchronous serial interface (UART) mode**

  This mode enables full-duplex operation wherein one byte of data is transmitted and received after the start bit.

  The on-chip dedicated UART baud rate generator enables communication using a wide range of selectable baud rates. In addition, a baud rate can be also defined by dividing the clock input to the ASCK0 pin.

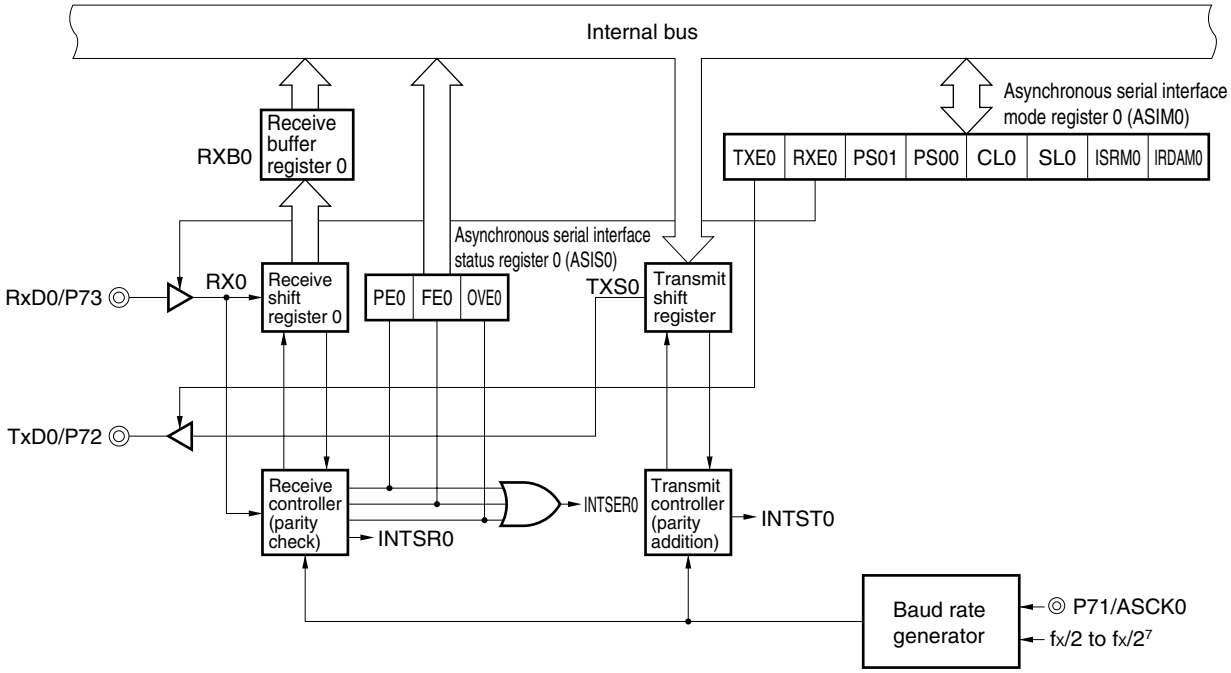
  The dedicated UART baud rate generator can also be used to generate a MIDI-standard baud rate (31.25 Kbps).

- **Infrared data transfer mode**

  This mode enables pulse output and pulse reception in data format.

  This mode can be used for office equipment applications such as personal computers.

Figure 5-9. Block Diagram of Serial Interface UART0



(2) Serial interface SIO1

Serial interface SIO1 has a 3-wire serial I/O mode and a 3-wire serial I/O mode with an auto-transmit/receive function.

- **3-wire serial I/O mode (MSB/LSB-first switching is possible)**

  This mode performs 8-bit data transfer via 3 lines: a serial clock line ($\overline{SCK1}$), serial output line (SO1), and serial input line (SI1).

  This mode can transmit and receive data simultaneously and allows the processing time of data transfer to be reduced.

  Since MSB-first or LSB-first is supported for the first bit of the 8-bit data for serial transfer, it is possible to connect the μPD780065 to both MSB-first devices and LSB-first devices.

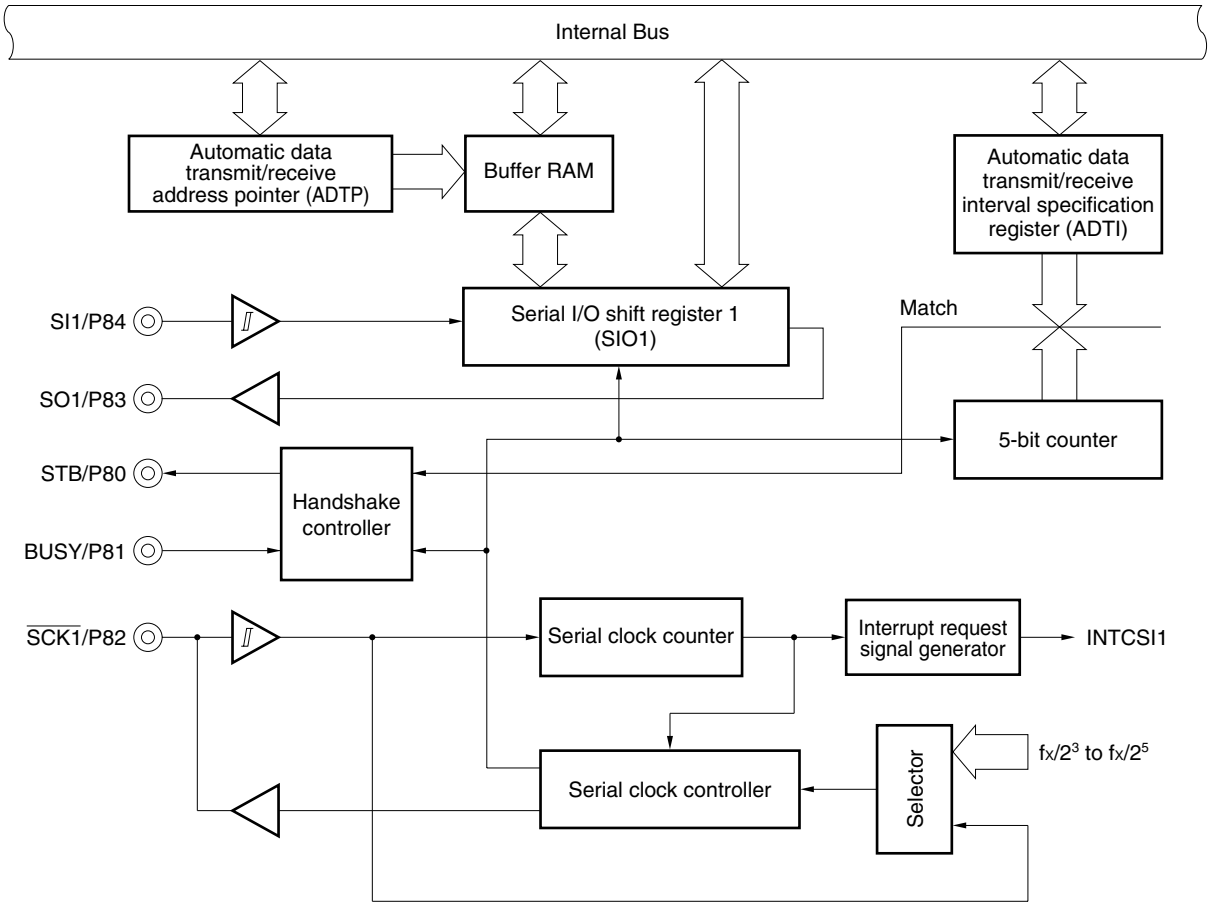
  3-wire serial I/O mode is effective when connecting to a peripheral I/O that incorporates a clock synchronous serial interface or a display controller, etc.

- **3-wire serial I/O mode with auto-transmit/receive function**

  This mode has the same functions as the 3-wire serial I/O mode above, but with an added auto transmit/receive function.

  A maximum of 32 bytes of data can be transmitted/received in this mode. This function allows hardware-based data transmission/reception to and from devices for OSD (On Screen Display) and devices that incorporate display controllers/drivers independently from the CPU. This mode, therefore, can reduce the burden on software.

Figure 5-10. Block Diagram of Serial Interface SIO1



(3) Serial interface SIO30

Serial interface SIO30 has a 2-wire serial I/O mode.

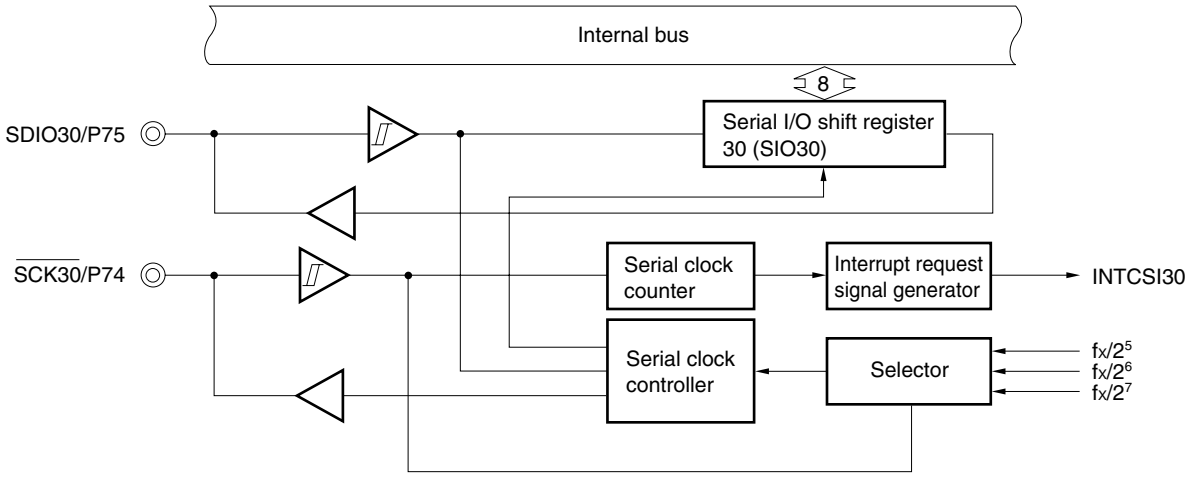
- **2-wire serial I/O mode (fixed as MSB first)**

  This is an 8-bit data transfer mode using two lines: a serial clock line ($\overline{\text{SCK30}}$) and a data I/O line (SDIO30).

  The first bit in 8-bit data in the serial transfer is fixed as MSB.

  The 2-wire serial I/O mode is useful for connection to a peripheral I/O that incorporates a clocked serial interface, a display controller, etc.

Figure 5-11. Block Diagram of Serial Interface SIO30



(4) Serial interface SIO31

Serial interface SIO31 has a 3-wire serial I/O mode.

- **3-wire serial I/O mode (fixed as MSB first)**

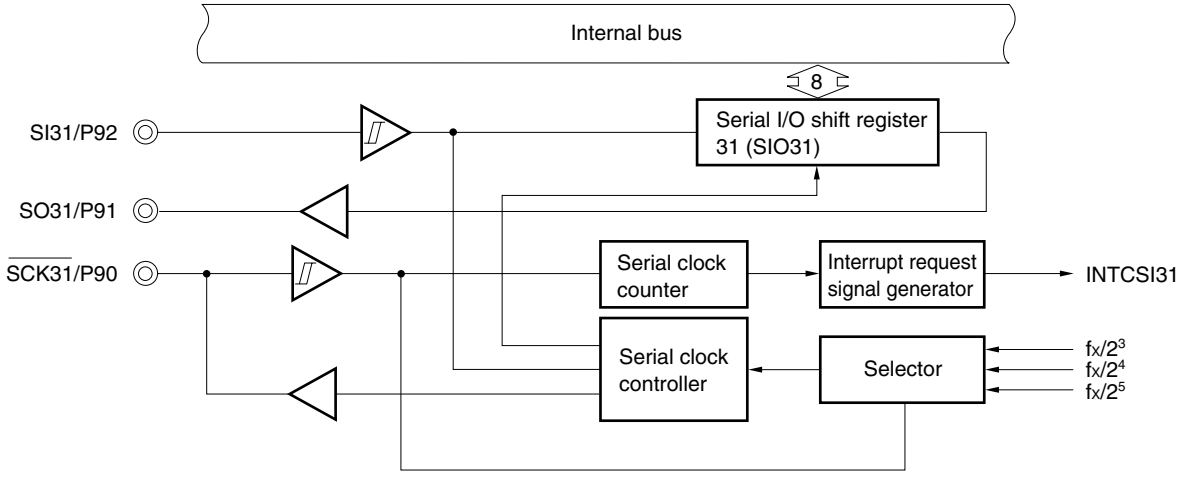
  This is an 8-bit data transfer mode using three lines: a serial clock line ($\overline{\text{SCK31}}$), serial output line (SO31), and serial input line (SI31).

  Since simultaneous transmit and receive operations are enabled in the 3-wire serial I/O mode, the processing time for data transfer is reduced.

  The first bit in 8-bit data in the serial transfer is fixed as MSB.

  The 3-wire serial I/O mode is useful for connection to a peripheral I/O device that incorporates a clocked serial interface, a display controller, etc.

Figure 5-12. Block Diagram of Serial Interface SIO31



6. INTERRUPT FUNCTIONS

The interrupt function consists of 20 interrupt sources and three interrupt types, as shown below.

- Non-maskable: 1
- Maskable: 18
- Software: 1

Table 6-1. Interrupt Source List

Interrupt Type	Default Priority[Note 1]	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type[Note 2]
		Name	Trigger			
Non-maskable	—	INTWDT	Watchdog timer overflow (watchdog timer mode 1 selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Watchdog timer overflow (interval timer mode selected)			(B)
	1	INTP0	Pin input edge detection	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTSER0	Generation of serial interface UART0 reception error	Internal	000EH	(B)
	6	INTSR0	End of serial interface UART0 reception		0010H	
	7	INTST0	End of serial interface UART0 transmission		0012H	
	8	INTCSI30	End of serial interface SIO30 transfer		0014H	
	9	INTCSI31	End of serial interface SIO31 transfer		0016H	
	10	INTCSI1	End of serial interface SIO1 transfer		0018H	
	11	INTTM00	Match of TM0 and CR00 (when CR00 is specified as compare register) or TI01 pin valid edge detection (when CR00 is specified as capture register)		001AH	
	12	INTTM01	Match of TM0 and CR01 (when CR01 is specified as compare register) or TI00 pin valid edge detection (when CR01 is specified as capture register)		001CH	
	13	INTTM50	Match of TM50 and CR50		001EH	
	14	INTTM51	Match of TM51 and CR51		0020H	
	15	INTWTI	Reference time interval signal from watch timer		0022H	
	16	INTWT	Watch timer overflow		0024H	
	17	INTAD0	End of conversion by A/D converter		0026H	
Software	—	BRK	BRK instruction execution	—	003EH	(D)

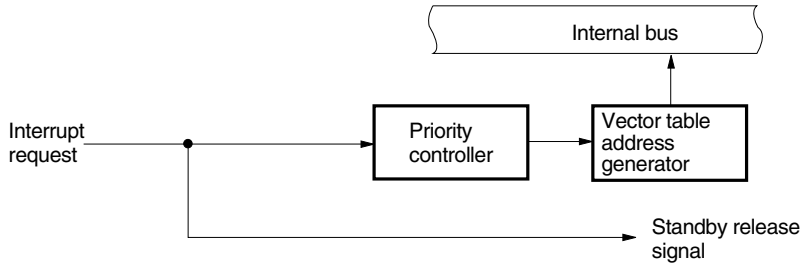
Notes 1. The default priority is a priority order when two or more maskable interrupt requests are generated simultaneously. 0 is the highest and 17 is the lowest.

2. Basic configuration types (A) to (D) correspond to (A) to (D) in Figure 6-1, respectively.

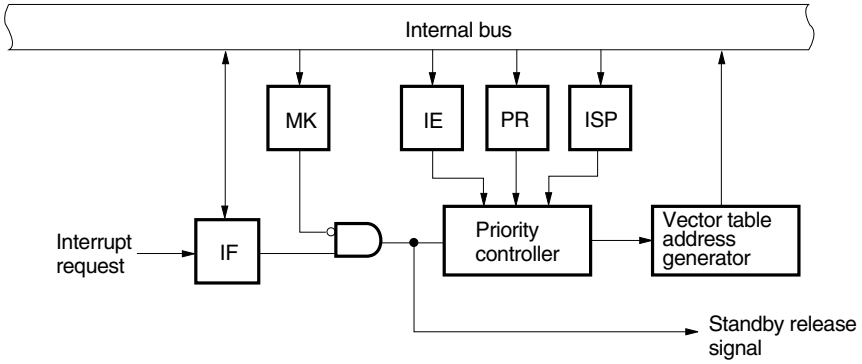
★ **Remark** Two watchdog timer interrupt sources (INTWDT): a non-maskable interrupt and a maskable interrupt (internal), are available, either of which can be selected.

Figure 6-1. Basic Configuration of Interrupt Function (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt (INTP0 to INTP3)

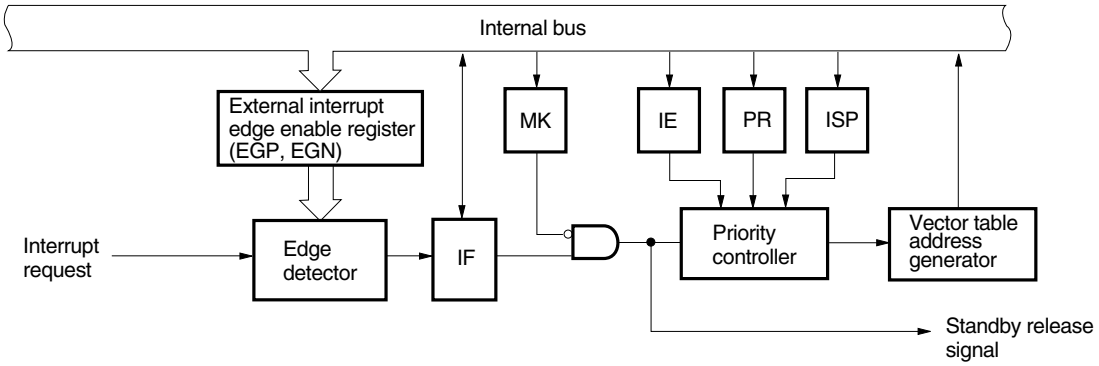
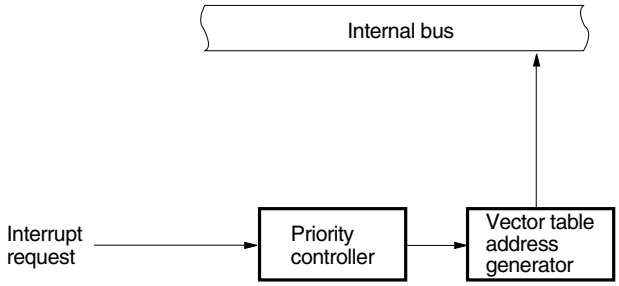


Figure 6-1. Basic Configuration of Interrupt Function (2/2)

(D) Software interrupt



IF: Interrupt request flag
IE: Interrupt enable flag
ISP: In-service priority flag
MK: Interrupt mask flag
PR: Priority specification flag

7. EXTERNAL DEVICE EXPANSION FUNCTION

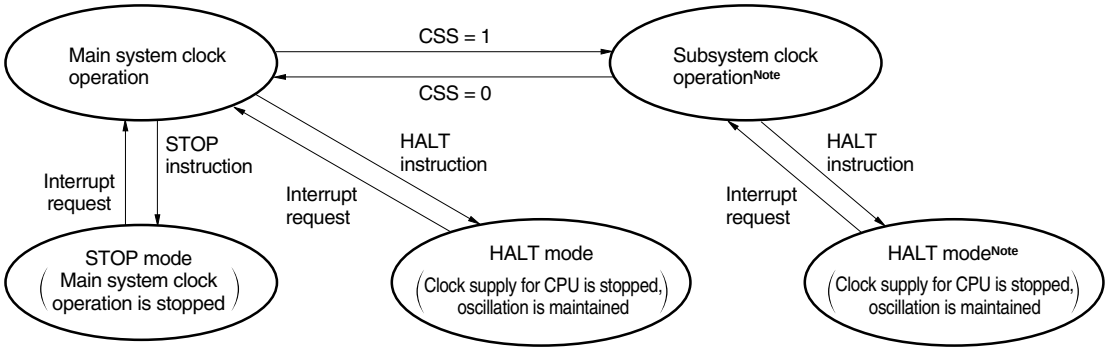
The external device expansion function is for connecting external devices to areas other than the internal ROM, RAM, and SFRs. Ports 4 to 6 are used for external device connection.

8. STANDBY FUNCTION

The following two standby modes are available for further reduction of system current consumption.

- HALT mode: In this mode, the CPU operation clock is stopped. The average current consumption can be reduced by intermittent operation by combining this mode with the normal operation mode.
- ★ STOP mode: In this mode, oscillation of the main system clock is stopped. All the operations performed on the main system clock are suspended, and only the subsystem clock is used, resulting in extremely small power consumption. This can be used only when the main system clock is operating (the subsystem clock oscillation cannot be stopped).

★ **Figure 8-1. Standby Function**



Note The current consumption can be reduced by stopping the main system clock. When the CPU is operating on the subsystem clock, set bit 7 (MCC) of the processor clock control register (PCC). The STOP instruction cannot be used.

Caution When the main system clock is stopped and the device is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

9. RESET FUNCTION

The following two reset methods are available.

- External reset by $\overline{\text{RESET}}$ signal input
- Internal reset by watchdog timer program loop time detection

10. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second operand / First operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

Second operand / First operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE or HL

(3) Bit manipulation instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second operand / First operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

Second operand / First operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

★ 11. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Conditions		Ratings	Unit
Supply voltage	V_{DD}			–0.3 to +6.5	V
	AV_{REF}			–0.3 to V_{DD} + 0.3	V
	AV_{SS}			–0.3 to +0.3	V
Input voltage	V_I	P00 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P84, P90 to P92, X1, X2, XT1, XT2, $\overline{\text{RESET}}$		–0.3 to V_{DD} + 0.3	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	ANI0 to ANI7	Analog input pin	AV_{SS} – 0.3 to AV_{REF0} + 0.3 and – 0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH}	Per pin		–10	mA
		Total for P00 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P80 to P84, P90 to P92		–15	mA
		Total for P70 to P77		–15	mA
Output current, low	I_{OL} **Note**	Per pin for P00 to P07, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P77, P80 to P84, P90 to P92	Peak value	20	mA
			rms value	10	mA
		Per pin for P50 to P57	Peak value	30	mA
			rms value	15	mA
		Total for P00 to P07, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P80 to P84, P90 to P92	Peak value	50	mA
			rms value	20	mA
		Total for P70 to P77	Peak value	20	mA
			rms value	10	mA
		Total for P50 to P57	Peak value	100	mA
			rms value	70	mA
Operating ambient temperature	T_A			–40 to +85	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note The rms value should be calculated as follows: [rms value] = [Peak value] × $\sqrt{\text{Duty}}$

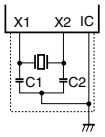
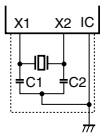
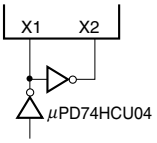
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_{IN}	f = 1 MHz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P00 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P84, P90 to P92			15	pF

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

Main System Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization timeNote 2	After V_{DD} reaches oscillation voltage range MIN.			4	ms
Crystal resonator		Oscillation frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		8.38	MHz
				1.0		5.0	
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V			10	ms
						30	
External clock		X1 input frequency (f_X)Note 1	V_{DD} = 4.5 to 5.5 V	1.0		8.38	MHz
						5.0	
		X1 input high-/low-level width (t_{XH}, t_{XL})	V_{DD} = 4.5 to 5.5 V	50		500	ns
				85		500	

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

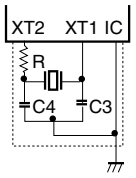
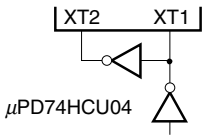
2. Time required to stabilize oscillation after reset or STOP mode release.

Cautions 1. When using the main system clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main system clock is stopped and the system is operating on the subsystem clock, wait until the oscillation stabilization time has been secured by the program before switching back to the main system clock.

Subsystem Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2	V_{DD} = 4.5 to 5.5 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT})Note 1		32		38.5	kHz
		XT1 input high-/low-level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. Indicates only oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} reaches oscillation voltage range MIN.

Cautions 1. When using the subsystem clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS1}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subsystem clock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main system clock oscillator. Particular care is therefore required with the wiring method when the subsystem clock is used.

Recommended Oscillator Constant

Main system clock: Ceramic resonator (T_A = –40 to +85°C)

Manufacturer	Part Number	Frequency (MHz)	Recommended Circuit Constant		Oscillation Voltage Range	
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	2.7	5.5
	CSA2.00MG040	2.00	100	100	2.7	5.5
	CST2.00MG040	2.00	On-chip	On-chip	2.7	5.5
	CSA3.58MG	3.58	30	30	2.7	5.5
	CST3.58MGW	3.58	On-chip	On-chip	2.7	5.5
	CSA4.19MG	4.19	30	30	2.7	5.5
	CST4.19MGW	4.19	On-chip	On-chip	2.7	5.5
	CSA5.00MG	5.00	30	30	2.7	5.5
	CST5.00MGW	5.00	On-chip	On-chip	2.7	5.5
	CSA8.00MTZ	8.00	30	30	2.7	5.5
	CST8.00MTW	8.00	On-chip	On-chip	2.7	5.5
	CSA8.00MTZ093	8.00	30	30	2.7	5.5
	CST8.00MTW093	8.00	On-chip	On-chip	2.7	5.5
	CSA8.38MTZ	8.38	30	30	2.7	5.5
	CST8.38MTW	8.38	On-chip	On-chip	2.7	5.5
	CSA8.38MTZ093	8.38	30	30	2.7	5.5
	CST8.38MTW093	8.38	On-chip	On-chip	2.7	5.5

Caution The oscillator constant and oscillation voltage range indicate conditions of stable oscillation. Oscillation frequency precision is not guaranteed. For applications requiring oscillation frequency precision, the oscillation frequency must be adjusted on the implementation circuit. For details, contact directly the manufacturer of the resonator used.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high	I_{OH}	Per pin				–1	mA
		All pins				–15	mA
Output current, low	I_{OL}	Per pin for P00 to P07, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P77, P80 to P84, P90 to P92				10	mA
		Per pin for P50 to P57				15	mA
		Total for P00 to P07, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P80 to P84, P90 to P92				20	mA
		Total for P50 to P57				70	mA
		Total for P70 to P77				10	mA
Input voltage, high	V_{IH1}	P04 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70, P72, P76, P77, P80, P81, P83, P91		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P71, P73 to P75, P82, P84, P90, P92, $\overline{\text{RESET}}$		0.8V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2		V_{DD} – 0.5		V_{DD}	V
	V_{IH4}	XT1, XT2	V_{DD} = 4.5 to 5.5 V	0.8V_{DD}		V_{DD}	V
				0.9V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}	P04 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70, P72, P76, P77, P80, P81, P83, P91		0		0.3V_{DD}	V
	V_{IL2}	P00 to P03, P71, P73 to P75, P82, P84, P90, P92, $\overline{\text{RESET}}$		0		0.2V_{DD}	V
	V_{IL3}	X1, X2		0		0.4	V
	V_{IL4}	XT1, XT2	V_{DD} = 4.5 to 5.5 V	0		0.2V_{DD}	V
				0		0.1V_{DD}	V
Output voltage, high	V_{OH1}	V_{DD} = 4.5 to 5.5 V, I_{OH} = –1 mA		V_{DD} – 1.0		V_{DD}	V
		I_{OH} = –100 μA		V_{DD} – 0.5		V_{DD}	V
Output voltage, low	V_{OL1}	P50 to P57	V_{DD} = 4.5 to 5.5 V, I_{OL} = 15 mA		0.4	2.0	V
		P00 to P07, P20 to P27, P30 to P37, P40 to P47, P64 to P67, P70 to P77, P80 to P84, P90 to P92	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	I_{OL} = 400 μA				0.5	V

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	$V_{IN} = V_{DD}$	P00 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P84, P90 to P92, $\overline{\text{RESET}}$			3	μA
	I_{LIH2}		X1, X2, XT1, XT2			20	μA
Input leakage current, low	I_{LIL1}	V_{IN} = 0 V	P00 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P84, P90 to P92, $\overline{\text{RESET}}$			–3	μA
	I_{LIL2}		X1, X2, XT1, XT2			–20	μA
Output leakage current, high	I_{LOH}	$V_{OUT} = V_{DD}$				3	μA
Output leakage current, low	I_{LOL}	V_{OUT} = 0 V				–3	μA
Software pull-up resistance	R	V_{IN} = 0 V, P00 to P07, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P84, P90 to P92		15	30	90	kΩ

Remark Unless otherwise specified, the characteristics of alternate-function pins are the same as those of port pins.

DC Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Power supply current[Note 1]	I_{DD1}	8.38 MHz crystal oscillation operating mode	V_{DD} = 5.0 V ± 10%[Note 2]	When A/D converter is stopped		5.5	11	mA
				When A/D converter is operating		6.5	13	mA
		5.00 MHz crystal oscillation operating mode	V_{DD} = 3.0 V ± 10%[Note 2]	When A/D converter is stopped		2	4	mA
				When A/D converter is operating		3	6	mA
	I_{DD2}	8.38 MHz crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10%[Note 2]	When peripheral functions are stopped		1.1	2.2	mA
				When peripheral functions are operating			4.7	mA
		5.00 MHz crystal oscillation HALT mode	V_{DD} = 3.0 V ± 10%[Note 2]	When peripheral functions are stopped		0.35	0.7	mA
				When peripheral functions are operating			1.7	mA
	I_{DD3}	32.768 kHz crystal oscillation operating mode[Note 3]		V_{DD} = 5.0 V ± 10%		40	80	μA
				V_{DD} = 3.0 V ± 10%		20	40	μA
	I_{DD4}	32.768 kHz crystal oscillation HALT mode[Note 3]		V_{DD} = 5.0 V ± 10%		30	60	μA
				V_{DD} = 3.0 V ± 10%		6	18	μA
	I_{DD5}	XT1 = V_{DD} STOP mode When feedback resistor is not used		V_{DD} = 5.0 V ± 10%		0.1	30	μA
				V_{DD} = 3.0 V ± 10%		0.05	10	μA

Notes 1. Total current through the internal power supply (V_{DD0}, V_{DD1}), including the peripheral operation current (except the current through pull-up resistors of ports and the AV_{REF} pin).

2. When the processor clock control register (PCC) is set to 00H.

3. When main system clock operation is stopped.

AC Characteristics

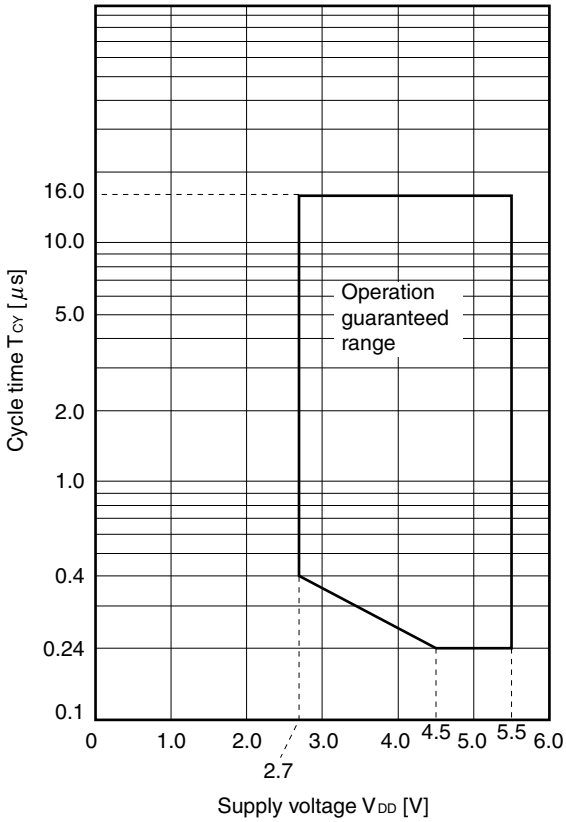
(1) Basic Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Cycle time (Minimum instruction execution time)	T_{CY}	Operating with main system clock	4.5 V ≤ V_{DD} ≤ 5.5 V	0.24		16	μs
			2.7 V ≤ V_{DD} < 4.5 V	0.4		16	μs
		Operating with subsystem clock		103.9 Note 1	122	125	μs
TI00, TI01 input high-/low-level width	t_{TIH0}, t_{TIL0}	3.5 V ≤ V_{DD} ≤ 5.5 V		$2/f_{sam}$ + 0.1 Note 2			μs
		2.7 V ≤ V_{DD} < 3.5 V		$2/f_{sam}$ + 0.2 Note 2			μs
TI50, TI51 input frequency	f_{TI5}			0		4	MHz
TI50, TI51 input high-/low-level width	t_{TIH5}, t_{TIL5}			100			ns
Interrupt request input high-/low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP3		1			μs
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

Notes 1. Value when the external clock is used. When a crystal resonator is used, it is 114 μs (MIN.).

2. Selection of f_{sam} = f_X, f_X/4, f_X/64 is possible using bits 0 and 1 (PRM00, PRM01) of prescaler mode register 0 (PRM0). However, if the TI00 valid edge is selected as the count clock, the value becomes f_{sam} = f_X/8.

T_{CY} vs. V_{DD} (main system clock operation)



(2) Read/Write Operation (T_A = –40 to +85°C, V_{DD} = 4.5 to 5.5 V)

(1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		0.3t_{CY}		ns
Address setup time	t_{ADS}		20		ns
Address hold time	t_{ADH}		6		ns
Data input time from address	t_{ADD1}			(2 + 2n) t_{CY} – 54	ns
	t_{ADD2}			(3 + 2n) t_{CY} – 60	ns
Address output time from $\overline{RD}\downarrow$	t_{RDAD}		0	100	ns
Data input time from $\overline{RD}\downarrow$	t_{RDD1}			(2 + 2n) t_{CY} – 87	ns
	t_{RDD2}			(3 + 2n) t_{CY} – 93	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.5 + 2n) t_{CY} – 33		ns
	t_{RDL2}		(2.5 + 2n) t_{CY} – 33		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			t_{CY} – 43	ns
	t_{RDWT2}			t_{CY} – 43	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			t_{CY} – 25	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(0.5 + n) t_{CY} + 10	(2 + 2n) t_{CY}	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		6		ns
$\overline{WR}$ low-level width	t_{WRL1}		(1.5 + 2n) t_{CY} – 15		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		6		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		2t_{CY} – 15		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		0.8t_{CY} – 15	1.2t_{CY}	ns
Address hold time from $\overline{RD}\uparrow$ at external fetch	t_{RDADH}		0.8t_{CY} – 15	1.2t_{CY} + 30	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		10	60	ns
Address hold time from $\overline{WR}\uparrow$	t_{WRADH}		0.8t_{CY} – 15	1.2t_{CY} + 30	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		0.8t_{CY}	2.5t_{CY} + 25	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		0.8t_{CY}	2.5t_{CY} + 25	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, A8 to A15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(2) Read/Write Operation (T_A = –40 to +85°C, V_{DD} = 2.7 to 4.5 V)

(2/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
ASTB high-level width	t_{ASTH}		$0.3t_{CY}$		ns
Address setup time	t_{ADS}		30		ns
Address hold time	t_{ADH}		10		ns
Input time from address to data	t_{ADD1}			$(2 + 2n)\ t_{CY} - 108$	ns
	t_{ADD2}			$(3 + 2n)\ t_{CY} - 120$	ns
Output time from $\overline{RD}\downarrow$ to address	t_{RDAD}		0	200	ns
Input time from $\overline{RD}\downarrow$ to data	t_{RDD1}			$(2 + 2n)\ t_{CY} - 148$	ns
	t_{RDD2}			$(3 + 2n)\ t_{CY} - 162$	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		$(1.5 + 2n)\ t_{CY} - 40$		ns
	t_{RDL2}		$(2.5 + 2n)\ t_{CY} - 40$		ns
Input time from $\overline{RD}\downarrow$ to $\overline{WAIT}\downarrow$	t_{RDWT1}			$t_{CY} - 75$	ns
	t_{RDWT2}			$t_{CY} - 60$	ns
Input time from $\overline{WR}\downarrow$ to $\overline{WAIT}\downarrow$	t_{WRWT}			$t_{CY} - 50$	ns
$\overline{WAIT}$ low-level width	t_{WTL}		$(0.5 + 2n)\ t_{CY} + 10$	$(2 + 2n)\ t_{CY}$	ns
Write data setup time	t_{WDS}		60		ns
Write data hold time	t_{WDH}		10		ns
$\overline{WR}$ low-level width	t_{WRL1}		$(1.5 + 2n)\ t_{CY} - 30$		ns
Delay time from ASTB↓ to $\overline{RD}\downarrow$	t_{ASTRD}		10		ns
Delay time from ASTB↓ to $\overline{WR}\downarrow$	t_{ASTWR}		$2t_{CY} - 30$		ns
Delay time from $\overline{RD}\uparrow$ to ASTB↑ at external fetch	t_{RDAST}		$0.8t_{CY} - 30$	$1.2t_{CY}$	ns
Hold time from $\overline{RD}\uparrow$ to address at external fetch	t_{RDADH}		$0.8t_{CY} - 30$	$1.2t_{CY} + 60$	ns
Write data output time from $\overline{RD}\uparrow$	t_{RDWD}		40		ns
Write data output time from $\overline{WR}\downarrow$	t_{WRWD}		20	120	ns
Hold time from $\overline{WR}\uparrow$ to address	t_{WRADH}		$0.8t_{CY} - 30$	$1.2t_{CY} + 60$	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{RD}\uparrow$	t_{WTRD}		$0.5t_{CY}$	$2.5t_{CY} + 50$	ns
Delay time from $\overline{WAIT}\uparrow$ to $\overline{WR}\uparrow$	t_{WTWR}		$0.5t_{CY}$	$2.5t_{CY} + 50$	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates the number of waits.

3. C_L = 100 pF (C_L indicates the load capacitance of the AD0 to AD7, AD8 to AD15, $\overline{RD}$, $\overline{WR}$, $\overline{WAIT}$, and ASTB pins.)

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(a) SIO3n 3-wire serial I/O mode ($\overline{SCK3n}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3n}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 5.5 V	954			ns
			1600			ns
$\overline{SCK3n}$ high-/low-level width	t_{KH1}, t_{KL1}	V_{DD} = 4.5 to 5.5 V	$t_{KCY1}/2$ – 50			ns
			$t_{KCY1}/2$ – 100			ns
SI3n setup time (to $\overline{SCK3n}\uparrow$)	t_{SIK1}	V_{DD} = 4.5 to 5.5 V	100			ns
			150			ns
SI3n hold time (from $\overline{SCK3n}\uparrow$)	t_{KSI1}		400			ns
Delay time from $\overline{SCK3n}\downarrow$ to SO3n output	t_{KSO1}	C = 100 pF[Note]			300	ns

Note C is the load to SO3n output capacitance of the $\overline{SCK3n}$ and SO3n output lines.

(b) SIO3n 3-wire serial I/O mode ($\overline{SCK3n}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK3n}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
$\overline{SCK3n}$ high-/low-level width	t_{KH2}, t_{KL2}	V_{DD} = 4.5 to 5.5 V	400			ns
			800			ns
SI3n setup time (to $\overline{SCK3n}\uparrow$)	t_{SIK2}		100			ns
SI3n hold time (from $\overline{SCK3n}\uparrow$)	t_{KSI2}		400			ns
Delay time from $\overline{SCK3n}\downarrow$ to SO3n output	t_{KSO2}	C = 100 pF[Note]			300	ns

Note C is the load capacitance of the SO3n output line.

Remark n = 0, 1

(3) Serial Interface (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V)

(c) SIO1 3-wire serial I/O mode ($\overline{SCK1}$... Internal clock output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY3}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH3}, t_{KL3}		$t_{KCY1}/2 - 50$			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK3}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI3}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO3}	C = 100 pF**Note**			300	ns

Note C is the load capacitance of the $\overline{SCK1}$ and SO1 output lines.

(d) SIO1 3-wire serial I/O mode ($\overline{SCK1}$... External clock input)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{SCK1}$ cycle time	t_{KCY4}		800			ns
$\overline{SCK1}$ high-/low-level width	t_{KH4}, t_{KL4}		400			ns
SI1 setup time (to $\overline{SCK1}\uparrow$)	t_{SIK4}		100			ns
SI1 hold time (from $\overline{SCK1}\uparrow$)	t_{KSI4}		400			ns
Delay time from $\overline{SCK1}\downarrow$ to SO1 output	t_{KSO4}	C = 100 pF**Note**			300	ns
SCK1 rise/fall time	t_R, t_F				1	μs

Note C is the load capacitance of the SO1 output line.

(e) UART mode (dedicated baud-rate generator output)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 4.5 to 5.5 V			131031	bps
					78125	bps

(f) UART mode (external clock input)

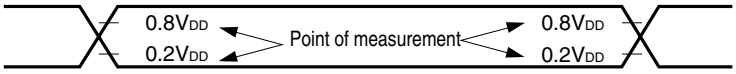
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
ASCK0 cycle time	t_{KCY5}	V_{DD} = 4.5 to 5.5 V	800			ns
			1600			ns
ASCK0 high-/low-level width	t_{KH5},	V_{DD} = 4.5 to 5.5 V	400			ns
	t_{KL5}		800			ns
Transfer rate		V_{DD} = 4.5 to 5.5 V			39063	bps
					19531	bps

(g) UART mode (infrared data transfer mode)

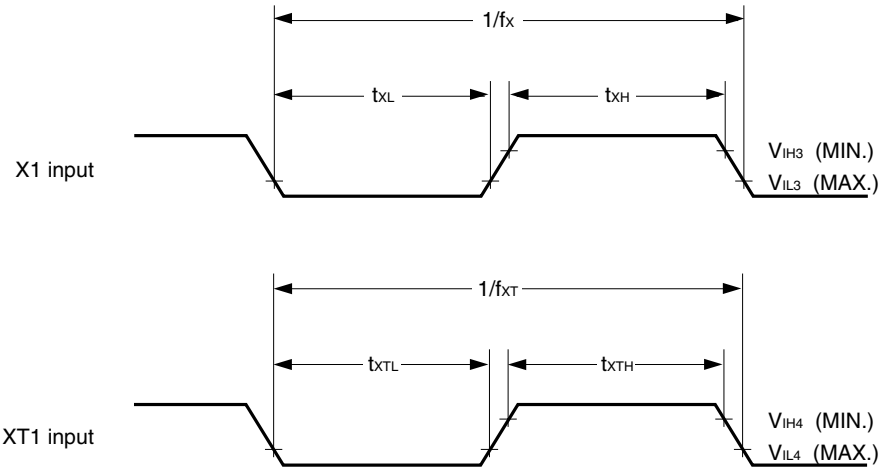
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		V_{DD} = 4.5 to 5.5 V			131031	bps
Bit rate allowable error		V_{DD} = 4.5 to 5.5 V			±0.87	%
Output pulse width		V_{DD} = 4.5 to 5.5 V	1.2		0.24/fbr[Note]	μs
Input pulse width		V_{DD} = 4.5 to 5.5 V	4/f_X			μs

Note fbr: Specified baud rate

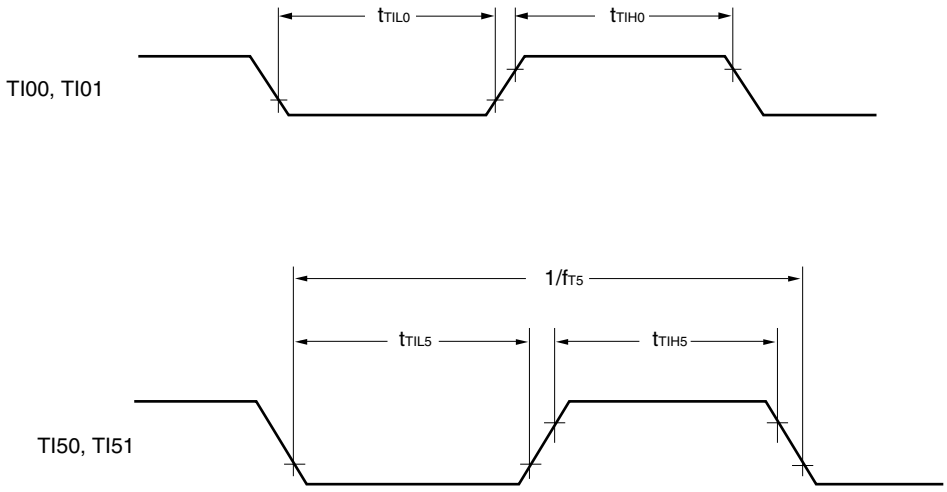
AC Timing Measurement Points (Excluding X1, XT1 Inputs)



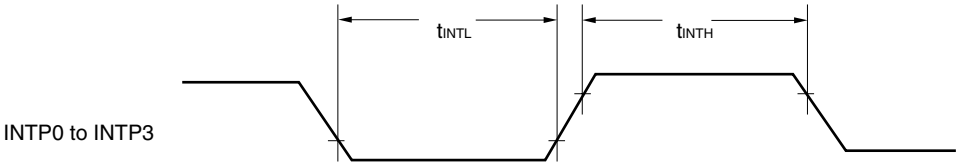
Clock Timing



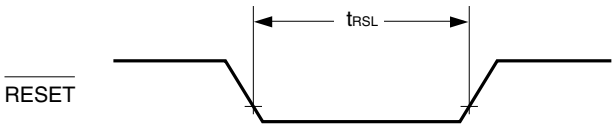
TI Timing



Interrupt Request Input Timing

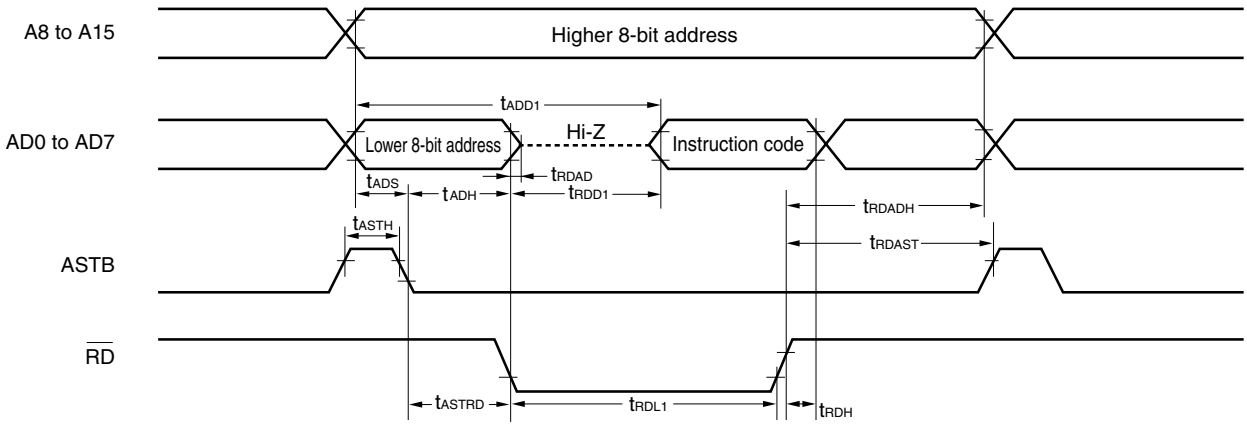


$\overline{\text{RESET}}$ Input Timing

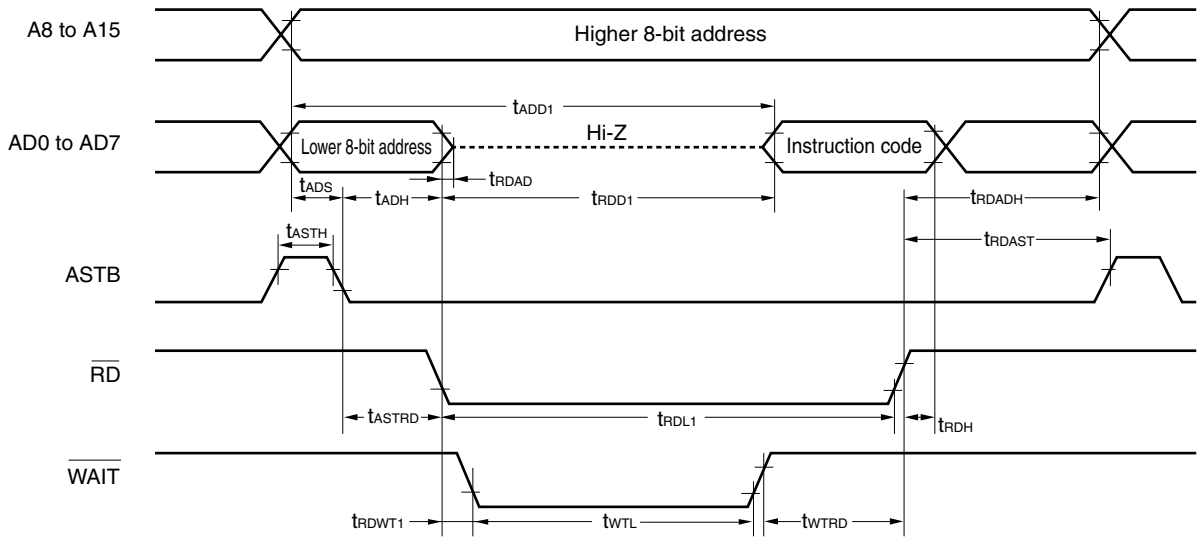


Read/Write Operation

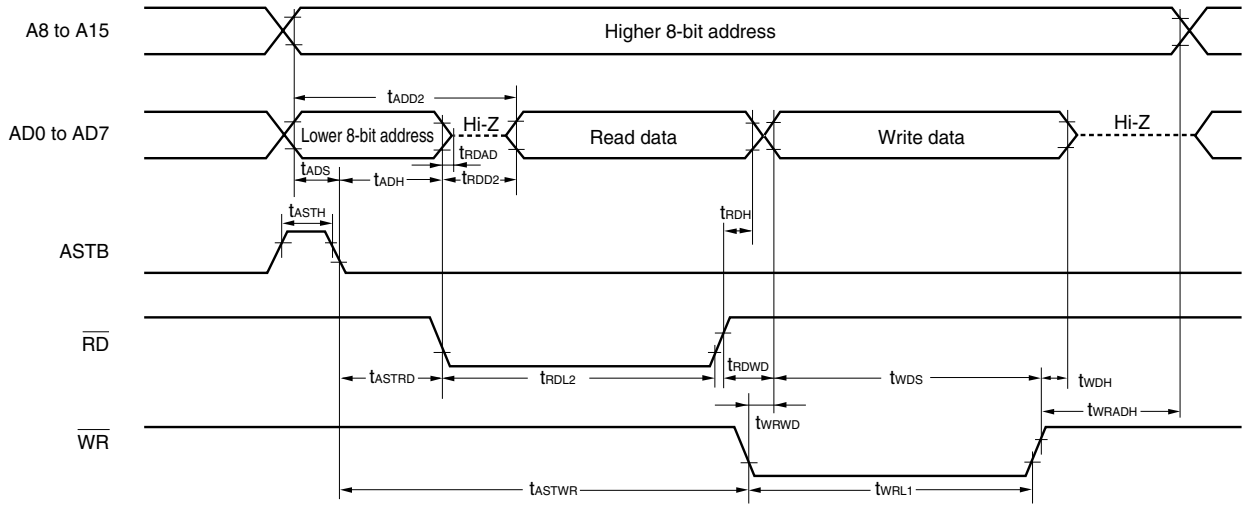
External fetch (no wait):



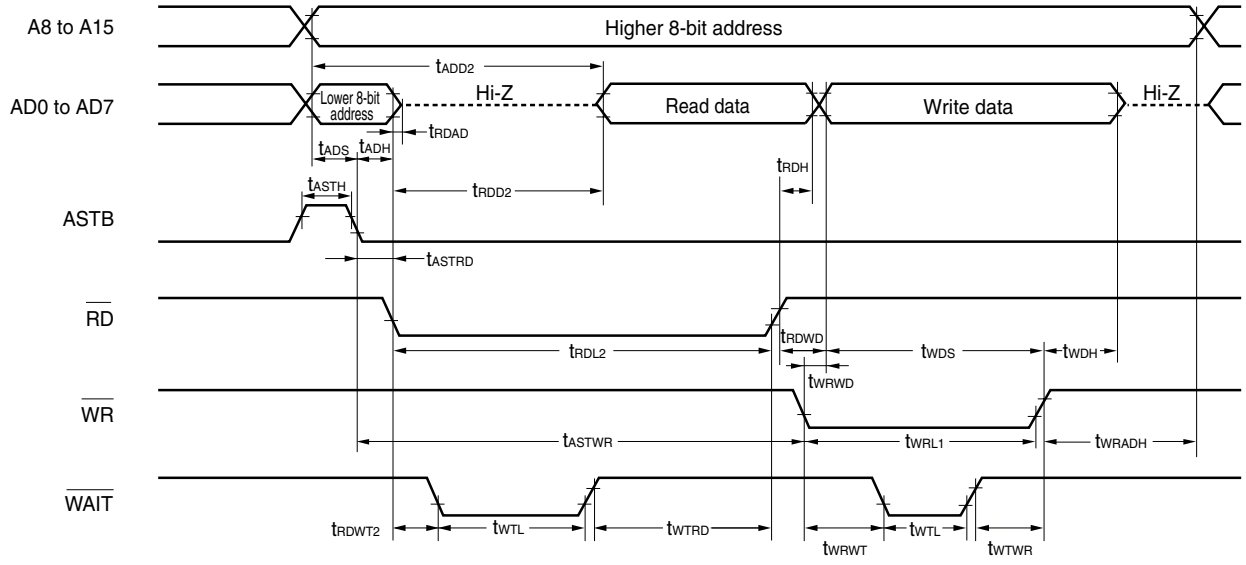
External fetch (wait insertion):



External data access (no wait):

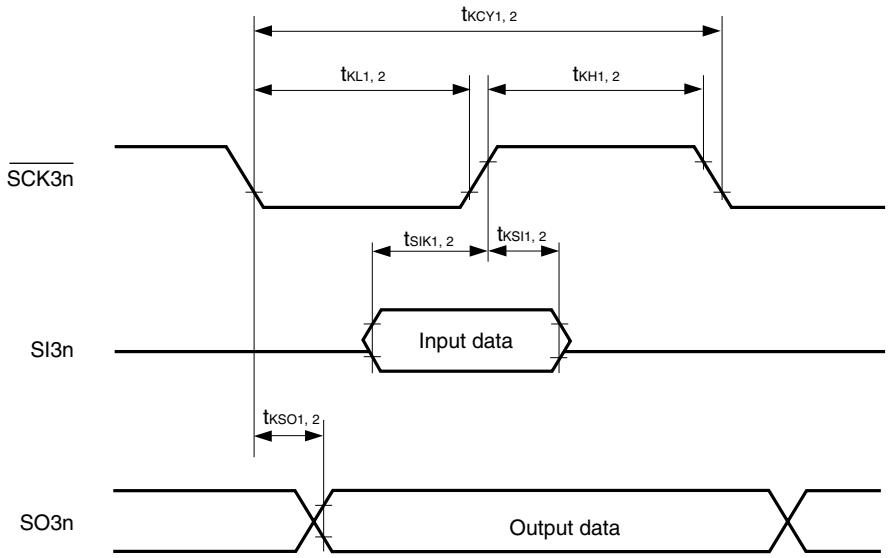


External data access (wait insertion):



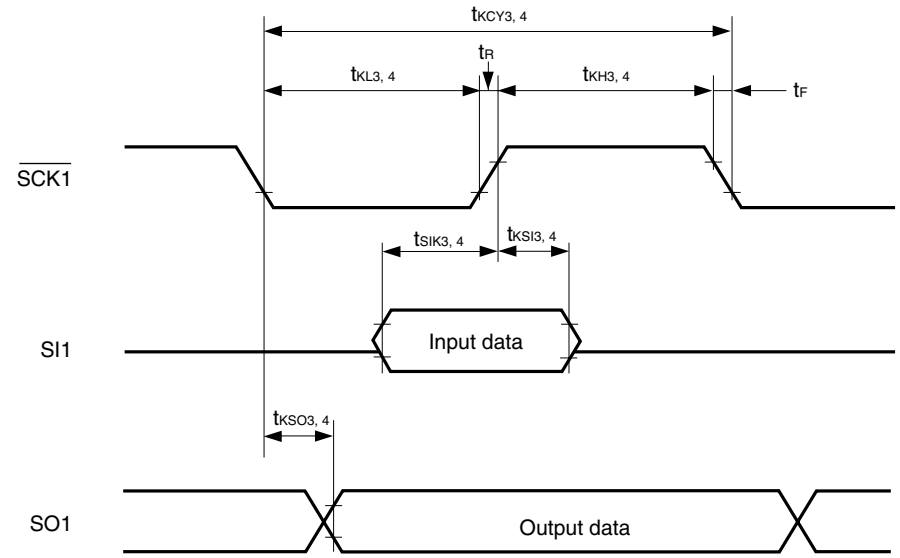
Serial Transfer Timing

SIO3n 3-wire serial I/O mode:

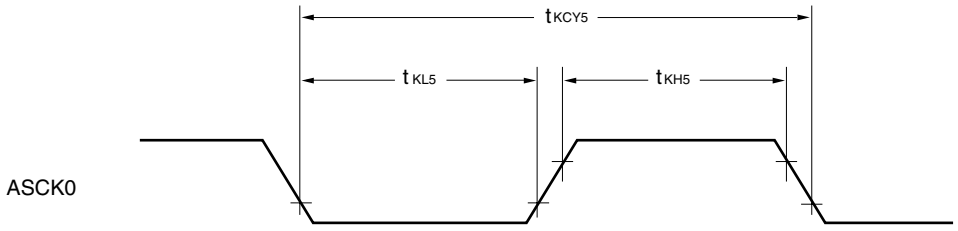


Remark n = 0, 1

SIO1 3-wire serial I/O mode:



UART mode (external clock input):



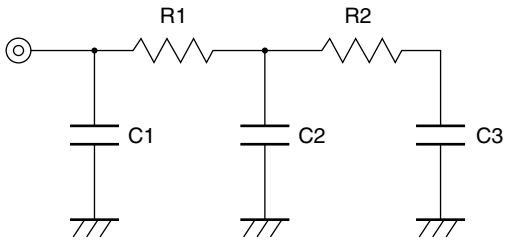
A/D Converter Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = AV_{REF} = 2.7 to 5.5 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			8	8	8	bit
Overall error[Note]					±0.6	%FSR
Conversion time	t_{CONV}		19		96	μs
Analog input voltage	V_{IAN}		0		AV_{REF}	V
Resistance between AV_{REF} and AV_{SS}	R_{REF}	When A/D converter not operating	20	40		kΩ

Note Excludes quantization error (±1/2 LSB). This value is indicated as a ratio to the full-scale value.

● **Analog input pin input impedance**

[Equivalent circuit]



[Parameter value]

[TYP.]

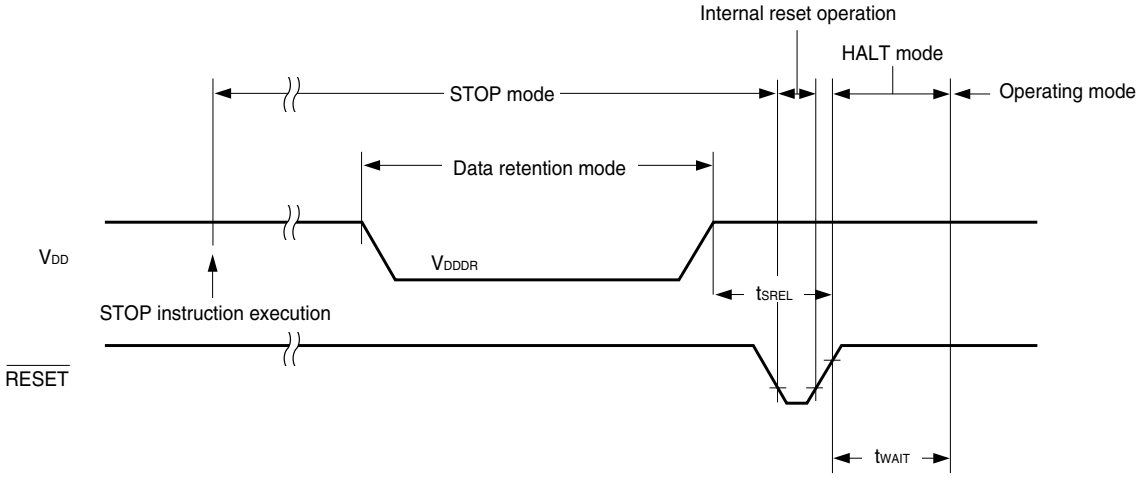
AV_{DD} [V]	R1 [kΩ]	R2 [kΩ]	C1 [pF]	C2 [pF]	C3 [pF]
2.7	12	8.0	3.0	3.0	2.0
4.5	4	2.7	3.0	1.4	2.0

Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics (T_A = –40 to +85°C)

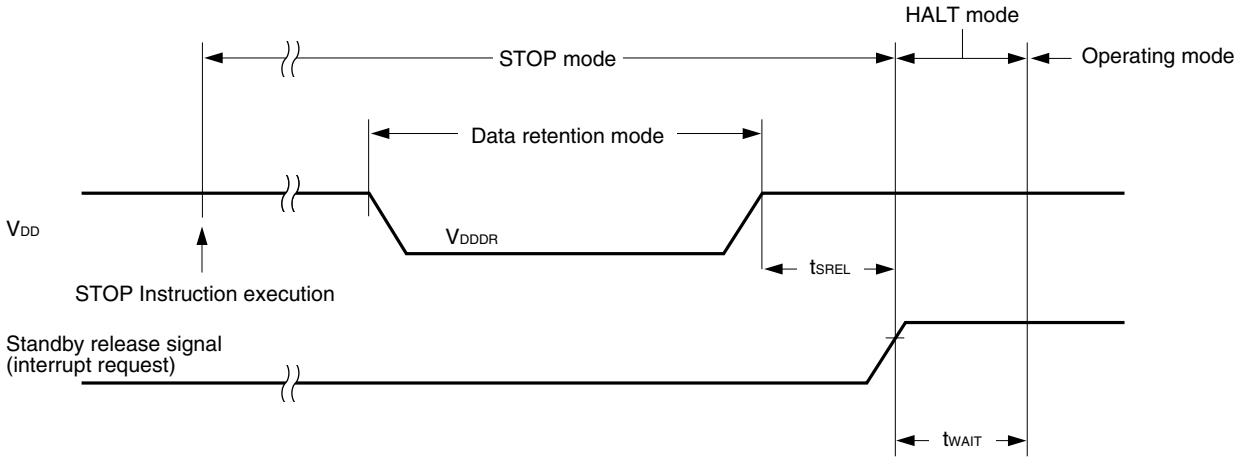
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage	V_{DDDR}		1.6		5.5	V
Data retention power supply current	I_{DDDR}	Subsystem clock stop (XT1 = V_{DD}) and feedback resistor disconnected		0.1	30	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		s
		Release by interrupt request		**Note**		s

Note Selection of $2^{12}/f_X$ and $2^{14}/f_X$ to $2^{17}/f_X$ is possible using bits 0 to 2 (OSTS0 to OSTS2) of the oscillation stabilization time select register (OSTS).

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

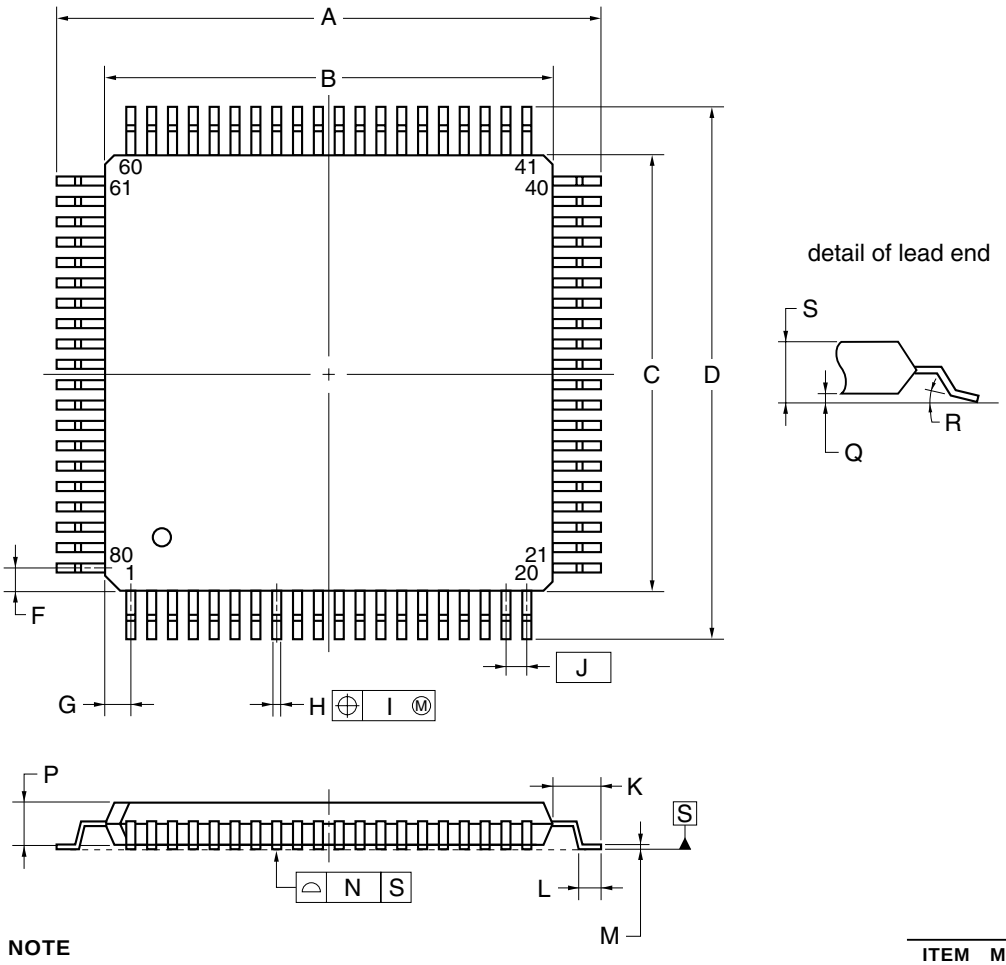


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Request Signal)



12. PACKAGE DRAWING

⋆ 80-PIN PLASTIC QFP (14x14)



NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

Remark The external dimensions and materials of the ES version are the same as those of the mass-produced version.

★ 13. RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

Table 13-1. Surface Mounting Type Soldering Conditions

μPD780065GC-×××-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less	IR35-00-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less	VP15-00-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for developing systems using the μPD780065 Subseries.
Refer to **(5) Cautions on using development tools.**

(1) Language processing software

RA78K0	Assembler package common to the 78K/0 Series
CC78K0	C compiler package common to the 78K/0 Series
DF780066	Device file for the μPD780065 Subseries
CC78K0-L	C compiler library source file common to the 78K/0 Series

(2) Flash memory writing tools

	Flashpro III (Part number: FL-PR3, PG-FP3)	Dedicated flash programmer for microcontrollers incorporating flash memory
★	FA-80GC	Adapter for flash memory writing

(3) Debugging tools

- **When using IE-78K0-NS in-circuit emulator**

	IE-78K0-NS	In-circuit emulator common to the 78K/0 Series
	IE-70000-MC-PS-B	Power supply unit for the IE-78K0-NS
★	IE-78K0-NS-PA	Performance board to enhance/extend the functions of the IE-78K0-NS
	IE-70000-98-IF-C	Adapter necessary when a PC-9800 series computer (except notebook-type PC) is used as the host machine (C bus supported)
★	IE-70000-CD-IF-A	PC card and interface cable necessary when a PC-9800 series notebook-type PC is used as the host machine (PCMCIA socket supported)
	IE-70000-PC-IF-C	Adapter necessary when an IBM PC/AT™ compatible is used as the host machine (ISA bus supported)
★	IE-70000-PCI-IF-A	Adapter necessary when a PC incorporating a PCI bus is used as the host machine
	IE-780066-NS-EM4[Note]	Emulation board to emulate the μPD780065 Subseries
	IE-78K0-NS-P01	I/O board necessary when emulating the μPD780065 Subseries
	NP-80GC	Emulation probe for an 80-pin plastic QFP (GC-8BT type)
	EV-9200GC-80	Conversion socket to connect the board of the target system for an 80-pin plastic QFP (GC-8BT type) and NP-80GC
	ID78K0-NS	Integrated debugger for the IE-78K0-NS
	SM78K0	System simulator common to the 78K/0 Series
★	DF780066	Device file for the μPD780065 Subseries

Note Under development

- **When using IE-78001-R-A in-circuit emulator**

IE-78001-R-A	In-circuit emulator common to the 78K/0 Series
★ IE-70000-98-IF-C	Adapter necessary when a PC-9800 series computer (except notebook-type PC) is used as the host machine (C bus supported)
★ IE-70000-PC-IF-C	Adapter necessary when an IBM PC/AT compatible is used as the host machine (ISA bus supported)
★ IE-70000-PCI-IF-A	Adapter necessary when a PC incorporating a PCI bus is used as the host machine
IE-78000-R-SV3	Interface adapter and cable necessary when an EWS is used as the host machine
IE-780066-NS-EM4[Note]	Emulation board to emulate the μPD780065 Subseries
IE-78K0-NS-P01	I/O board necessary when emulating the μPD780065 Subseries
★ IE-78K0-R-EX1	Emulation probe conversion board necessary when the IE-780066-NS-EM4 + IE-78K0-NS-P01 is used in the IE-78001-R-A
EP-78230GC-R	Emulation probe for an 80-pin plastic QFP (GC-8BT type)
EV-9200GC-80	Conversion socket to connect the board of the target system for an 80-pin plastic QFP (GC-8BT type) and EP-78230GC-R
ID78K0	Integrated debugger for the IE-78001-R-A
SM78K0	System simulator common to the 78K/0 Series
★ DF780066	Device file for the μPD780065 Subseries

Note Under development

(4) Real-time OS

RX78K0	Real-time OS for the 78K/0 Series
MX78K0	OS for the 78K/0 Series

★ **(5) Cautions on using development tools**

- The ID78K0-NS, ID78K0, and SM78K0 are used in combination with the DF780066.
- The CC78K0 and RX78K0 are used in combination with the RA78K0 and DF780066.
- FL-PR3, FA-80GC, and NP-80GC are products of Naito Densei Machida Mfg. Co., Ltd. (TEL: +81-44-822-3813).
- Refer to the **Single-chip Microcontroller Development Tool Selection Guide (U11069E)** for information on third party development tools.
- Host machines and OSs compatible with the software are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Japanese Windows™] IBM PC/AT compatibles [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™, Solaris™] NEWS™ (RISC) [NEWS-OS™]
RA78K0	√Note	√
CC78K0	√Note	√
ID78K0-NS	√	—
ID78K0	√	√
SM78K0	√	—
RX78K0	√Note	√
MX78K0	√Note	√

Note DOS based software

APPENDIX B. RELATED DOCUMENTS

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents Related to Devices

Document Name	Document No.
μPD780065 Subseries User's Manual	Under preparation
★ μPD780065 Data Sheet	This document
★ μPD78F0066 Data Sheet	Under preparation
78K/0 Series User's Manual Instruction	U12326E

★ Documents Related to Development Tools (User's Manuals)

Document Name		Document No.
RA78K0 Assembler Package	Operation	U11802E
	Language	U11801E
	Structured Assembly Language	U11789E
CC78K/0 C Compiler	Operation	U11517E
	Language	U11518E
IE-78K0-NS In-Circuit Emulator		U13731E
IE-78001-R-A In-Circuit Emulator		To be prepared
IE-780066-NS-EM4 Emulation Board		To be prepared
EP-78230 Emulation Probe		EEU-1515
SM78K0S, SM78K0 System Simulator Ver. 2.10 or Later Windows Based	Operation	U14611E
SM78K Series System Simulator Ver. 2.10 or Later	External Part User Open Interface Specifications	To be prepared
ID78K0-NS Integrated Debugger Ver. 2.00 or Later Windows Based	Operation	U14379E
ID78K0-NS, ID78K0S-NS Integrated Ver. 2.20 or Later Windows Based	Operation	U14910E
ID78K0 Integrated Debugger EWS Based	Reference	—
ID78K0 Integrated Debugger Windows Based	Reference	U11539E
	Guide	U11649E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document for designing.

Documents Related to Embedded Software (User's Manuals)

Document Name		Document No.
78K/0 Series Real-time OS	Basics	U11537E
	Installation	U11536E
OS for 78K/0 Series MX78K0	Basics	U12257E

Other Related Documents

Document Name	Document No.
★ SEMICONDUCTOR SELECTION GUIDE - Products & Packages - (CD-ROM)	X13769E
Semiconductor Device Mounting Technology Manual	C10535E
Quality Grades on NEC Semiconductor Devices	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892E

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Fax: 408-588-6130
800-729-9288

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