NEC

MOS INTEGRATED CIRCUIT

μPD23C64202L

64M-BIT SYNCHRONOUS MASK-PROGRAMMABLE ROM
4M-WORD BY 16-BIT (WORD MODE) / 2M-WORD BY 32-BIT (DOUBLE WORD MODE)

Description

The μPD23C64202L is a 67,108,864 bits synchronous mask-programmable ROM with multiplexed address bus. The word organization is selectable (WORD mode : 4,194,304 words by 16 bits, DOUBLE WORD mode : 2,097,152 words by 32 bits).

The μPD23C64202L is packed in 86-pin PLASTIC TSOP (II).

Features

- Fully synchronous mask-ROM; all signals referenced to a positive clock edge
- Word organization :

  4,194,304 words by 16 bits (WORD mode)

  2,097,152 words by 32 bits (DOUBLE WORD mode)
- Operation frequency : up to 100 MHz

Operation supply voltage V_{CC}	Clock frequency MHz	Access time from CLK ns (MAX.)	Operating current (Burst mode) mA (MAX.)	Standby current (CMOS level input) μA (MAX.)
★ 3.3 V ± 0.3 V	100	6	150	100
	83	8		
	66	9		
	50	9		
	33	9		

- Programmable wrap type : Sequential or Interleave
- Programmable burst length : 4, 8
- Programmable /CAS latency : 3, 4, 5 or 6
- Programmable /RAS latency : 1, 2
- Burst termination by BURST STOP command
- LVTTL compatible inputs and outputs

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Document No. M13945EJ5V0DS00 (5th edition)
Date Published August 2001 NS CP (K)
Printed in Japan

The mark ★ shows major revised points.

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Ordering Information

Part number	Package
μPD23C64202LG5-×××-9JH	86-pin PLASTIC TSOP (II) (10.16 mm (400))

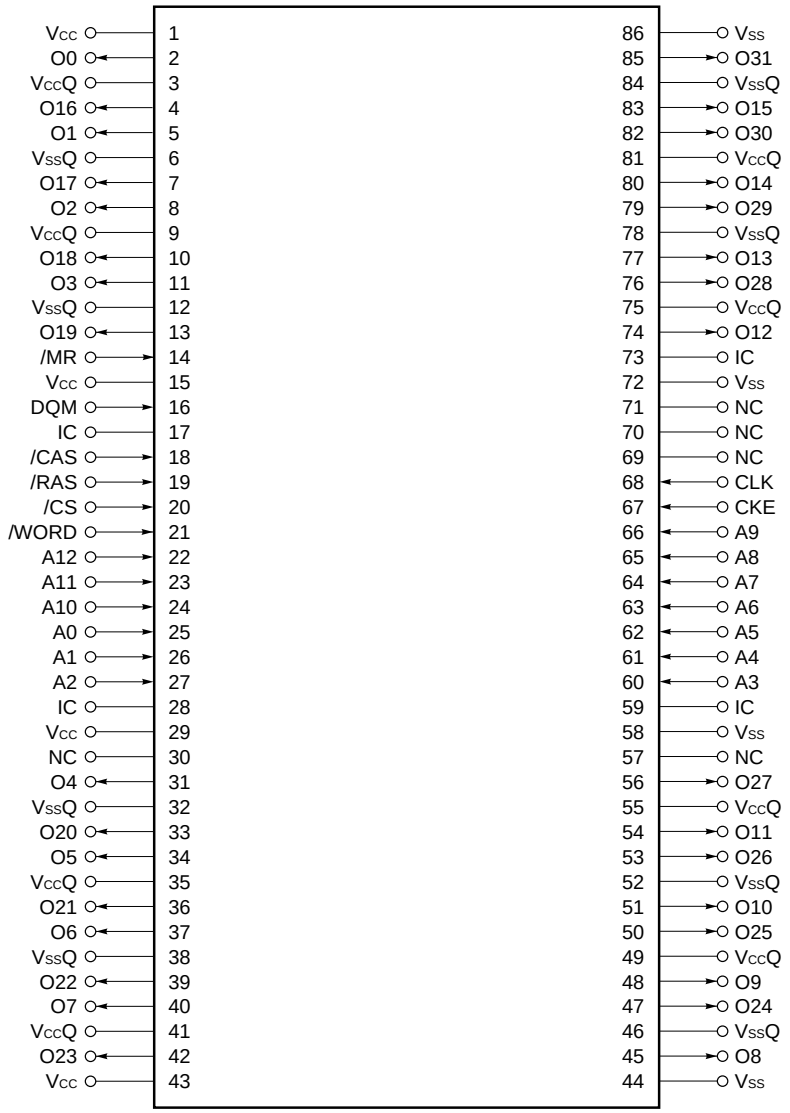
××× : ROM code suffix

Pin Configuration (Marking Side)

/xxx indicates active low signal.

86-pin PLASTIC TSOP (II) (10.16 mm (400))

[μPD23C64202LG5-×××-9JH]



Remarks 1. IC : Internally connected; leave this pin unconnected or connect to GND.

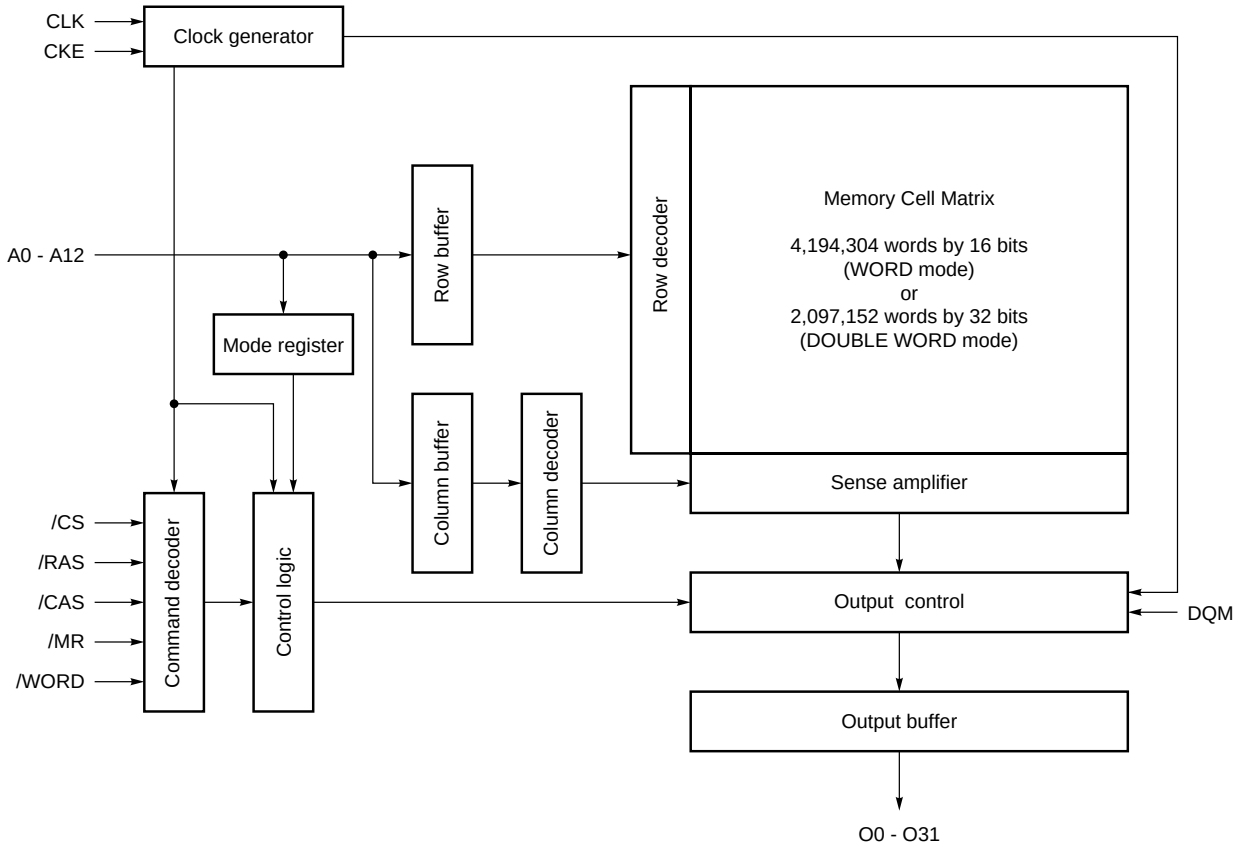
NC : Not internally connected; signal can be applied.

2. Refer to **13. Package Drawing** for the 1-pin index mark.

Pin Name

Symbol	Pin name	Pin number
CLK	Clock input	68
CKE	Clock enable input	67
/CS	Chip select	20
/RAS	Row address strobe	19
/CAS	Column address strobe	18
/MR	Mode register enable	14
/WORD	Mode select (DOUBLE WORD / WORD)	21
A0 - A12	Address inputs	25, 26, 27, 60, 61, 62, 63, 64, 65, 66, 24, 23, 22
O0 - O15, O16 - O31	Data outputs	2, 5, 8, 11, 31, 34, 37, 40, 45, 48, 51, 54, 74, 77, 80, 83, 4, 7, 10, 13, 33, 36, 39, 42, 47, 50, 53, 56, 76, 79, 82, 85
DQM	DQ mask enable	16
V_{CC}	Supply voltage (for internal circuit)	1, 15, 29, 43
$V_{CC}Q$	Supply voltage (for output buffer)	3, 9, 35, 41, 49, 55, 75, 81
V_{SS}	Ground (for internal circuit)	44, 58, 72, 86
$V_{SS}Q$	Ground (for output buffer)	6, 12, 32, 38, 46, 52, 78, 84
NC	No connection	30, 57, 69, 70, 71
IC	Internal connection	17, 28, 59, 73

Block Diagram



CONTENTS

1. Input / Output Pin Functions

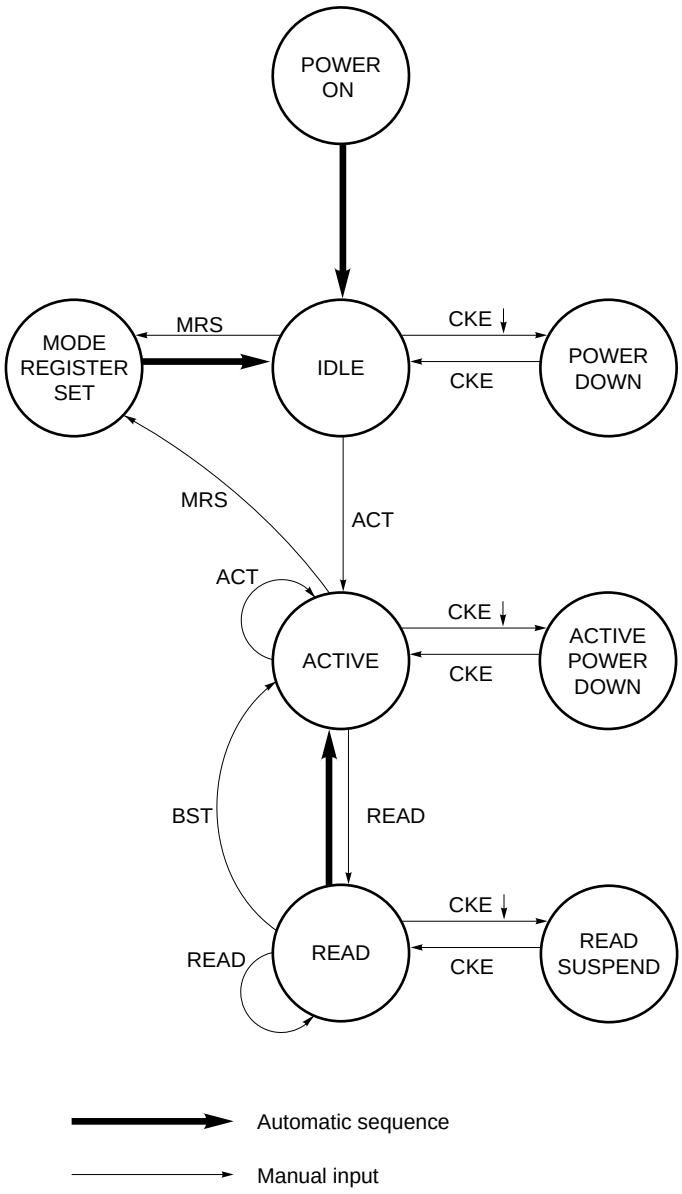
(1/2)

Pin name	Input / Output	Function
CLK (Clock input)	Input	CLK is the master clock input. Other inputs signals are referenced to the CLK rising edge.
CKE (Clock enable input)	Input	CKE determine validity of the next CLK (clock). If CKE is high, the next CLK rising edge is valid; otherwise, it is invalid. If the CLK rising edge is invalid, the internal clock is not issued and this device suspends operation. When this device is not in burst mode and CKE is negated, the device enters POWER DOWN mode. During POWER DOWN or READ SUSPEND mode, CKE must remain low.
/CS (Chip select)	Input	Command control signal. For details, refer to **4.2 Command Truth Table**. /CS low starts the command input cycle. When /CS is high, commands are ignored but operations continue.
/RAS (Row address strobe)	Input	Command control signal. For details, refer to **4.2 Command Truth Table**. Row address is determined by A0 - A12 at the CLK (clock) rising edge in the ROW ACTIVATE command cycle.
/CAS (Column address strobe)	Input	Command control signal. For details, refer to **4.2 Command Truth Table**. Column address is determined by A0 - A8 at the CLK rising edge in the READ command cycle. Column address is used differently in the WORD mode and the DOUBLE WORD mode, respectively. WORD mode (4M words by 16 bits) Column address : A0 - A8 DOUBLE WORD mode (2M words by 32 bits) Column address : A0 - A7
/MR (Mode register enable)	Input	Command control signal. For details, refer to **4.2 Command Truth Table**.
/WORD (Mode select)	Input	The pin for switching WORD mode and DOUBLE WORD mode. Low level : WORD mode (4M words by 16 bits) High level : DOUBLE WORD mode (2M words by 32 bits)
A0 - A12 (Address inputs)	Input	Address input pins. A0 - A12 are used differently in the WORD mode and the DOUBLE WORD mode, respectively. WORD mode (4M words by 16 bits) Row address : A0 - A12 Column address : A0 - A8 DOUBLE WORD mode (2M words by 32 bits) Row address : A0 - A12 Column address : A0 - A7 Also they are used as command control signal. For details, refer to **4.2 Command Truth Table**.
O0 - O15, O16 - O31 (Data outputs)	Output	Data output pins. O0 - O15, O16 - O31 are used differently in the WORD mode and the DOUBLE WORD mode, respectively. WORD mode (4M words by 16 bits) 16 bits data outputs to O0 - O15, and O16 - O31 are Hi-Z. DOUBLE WORD mode (2M words by 32 bits) 32 bits data outputs to O0 - O31.
DQM (DQ mask enable)	Input	DQM controls the output buffers like the /OE pin of an asynchronous mask ROM. DQM high and DQM low turn the output buffers off and on, respectively. DQM latency is 2 clocks.

(2/2)

Pin name	Input / Output	Function
V_{CC} (Supply voltage)	–	Power supply pin for internal circuits.
$V_{CC}Q$ (Supply voltage)	–	Power supply pin for the output buffers.
V_{SS} (Ground)	–	Ground pin for internal circuits.
$V_{SS}Q$ (Ground)	–	Ground pin for the output buffers.
NC (No connection)	–	Not internally connected (The signal can be applied).
IC (Internal connection)	–	Internally connected (Leave this pin unconnected or connect to GND).

2. Simplified State Diagram

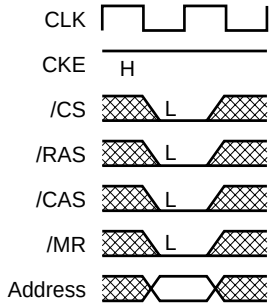


3. Commands

3.1 MODE REGISTER SET (MRS)

This device has a mode register that defines how the device operates. In this command, A0 through A6 are the data input pins. After power on, the mode register set command must be executed to initialize the device. During 2 clocks (t_{RSC}) following this command, this device cannot accept any other commands.

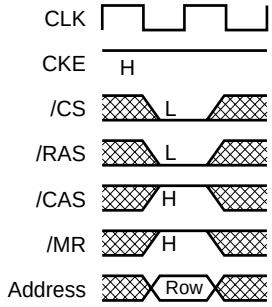
Figure of MODE REGISTER SET (MRS)



3.2 ROW ACTIVATE (ACT)

This command activates a row address selected by A0 - A12.

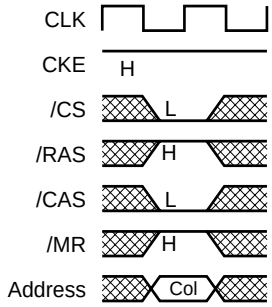
Figure of ROW ACTIVATE (ACT)



3.3 READ (READ)

Read data is available after /CAS latency requirements have been met. This command sets the burst start address given by the column address.

Figure of READ (READ)

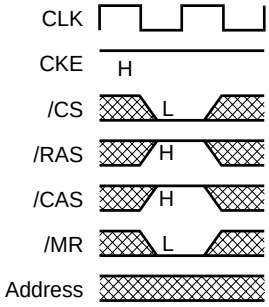


3.4 BURST STOP (BST)

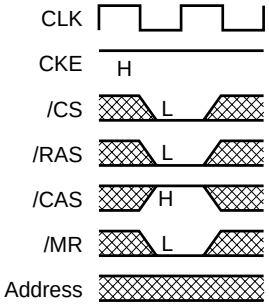
This command terminates the current burst operation.

Figure of BURST STOP (BST)

(Standard)

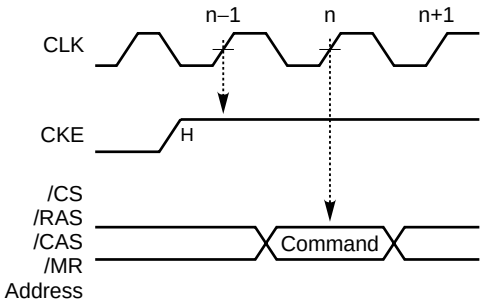


(SDRAM-precharge-like)



4. Truth Table

4.1 Clock Enable and Command



4.2 Command Truth Table

Function		Symbol	CKE		/CS	/RAS	/CAS	/MR	DQM	A0 - A12	/WORD
			n–1	n							
MODE REGISTER SET		MRS	H	×	L	L	L	L	×	Code	×
ROW ACTIVATE		ACT	H	×	L	L	H	H	×	RA	×
READ		READ	H	×	L	H	L	H	×	CA	×
BURST STOP	Standard	BST	H	×	L	H	H	L	×	×	×
	SDRAM-precharge-like		H	×	L	L	H	L	×	×	×
POWER DOWN	Entry	PWDN	H	L	×	×	×	×	×	×	×
	Exit		L	H	×	×	×	×	×	×	×
DQM		READ	H	×	×	×	×	×	V	×	×
No operation		NOP	H	×	H	×	×	×	×	×	×
			H	×	L	H	H	H	×	×	×
Organization control		–	H	×	L	H	L	H	×	CA	H or L
Illegal	(SDRAM write)	–	H	×	L	H	L	L	×	CA	×
	(SDRAM refresh)	–	H	×	L	L	L	H	×	×	×

Remark H : High level
L : Low level
× : Don't care (high or low level)
V : Valid data input
RA : Row address
CA : Column address

4.3 Operative Command Table

Current state	CKE	/CS	/RAS	/CAS	/MR	Address	Command	Action
IDLE	L	×	×	×	×	×	PWDN	Power down
(POWER-ON or	H	L	L	L	L	A0 - A6	MRS	Mode register accessing
MODE REGISTER SET)	H	L	L	H	H	RA	ACT	Row activating
	H	L	H	L	H	CA	READ	Illegal (ignored)
	H	L	H	H	L	×	BST	No operation
	H	L	L	H	L	×		
ACTIVE	L	×	×	×	×	×	–	Clock suspend
	H	L	L	L	L	A0 - A6	MRS	Mode register accessing
	H	L	L	H	H	RA	ACT	Row activating
	H	L	H	L	H	CA	READ	READ start
	H	L	H	H	L	×	BST	Illegal (ignored)
	H	L	L	H	L	×		
READ	L	×	×	×	×	×	–	Clock suspend / Power down
	H	L	L	L	L	A0 - A6	MRS	Mode register accessing
	H	L	L	H	H	RA	ACT	Row activating
	H	L	H	L	H	CA	READ	Next READ start
	H	L	H	H	L	×	BST	Burst stop
	H	L	L	H	L	×		
Any state	H	L	H	L	L	CA	–	Illegal
	H	L	L	L	H	×	–	Illegal
	H	H	×	×	×	×	NOP	No operation
	H	L	H	H	H	×	NOP	No operation

Remark H : High level

L : Low level

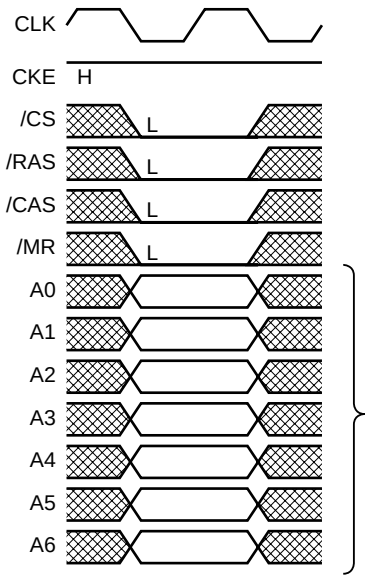
× : Don't care (high level or low level)

V : Valid data input

RA : Row address

CA : Column address

5. Mode Register Settings



/CAS latency

A5	A4	A3	/CAS latency
0	0	0	×
0	0	1	×
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	×
1	1	1	×

/RAS latency

A6	/RAS latency
0	1
1	2

A6	A5	A4	A3	A2	A1	A0

Wrap Type

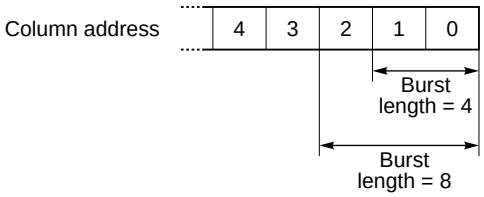
A2	Wrap type
0	Sequential
1	Interleave

Burst Length

A1	A0	Burst length
0	0	×
0	1	4
1	0	8
1	1	×

Remark ×: inhibited

Lower 2 or 3 bits of column address indicate starting column address of burst read.

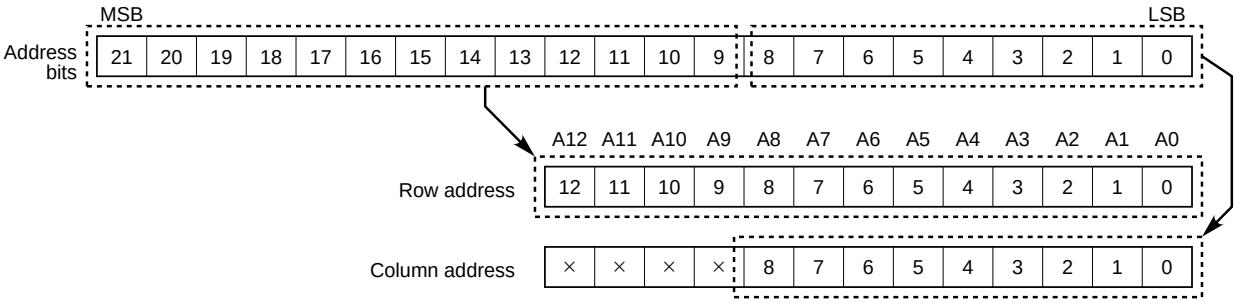


Burst Sequence

Burst length	Starting column address			Addressing sequence	
	A2	A1	A0	Sequential	Interleave
4		0	0	0 1 2 3	0 1 2 3
		0	1	1 2 3 0	1 0 3 2
		1	0	2 3 0 1	2 3 0 1
		1	1	3 0 1 2	3 2 1 0
8	0	0	0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0	0	1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0	1	0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0	1	1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1	0	0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1	0	1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1	1	0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1	1	1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0

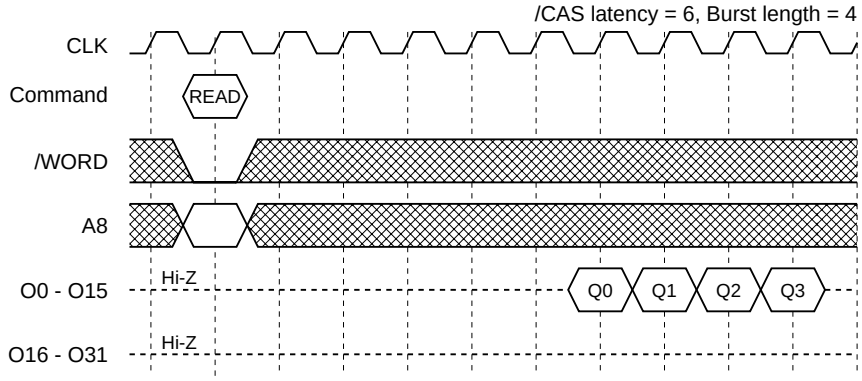
6. Word Modes

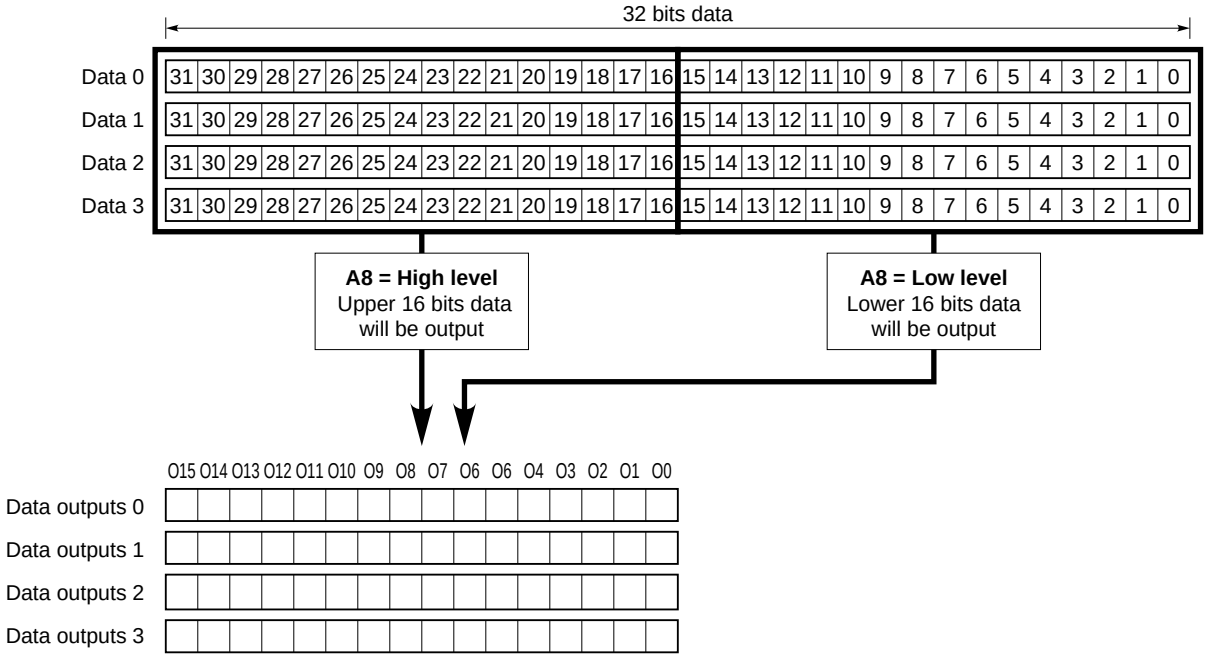
6.1 Addressing Map (WORD Mode)



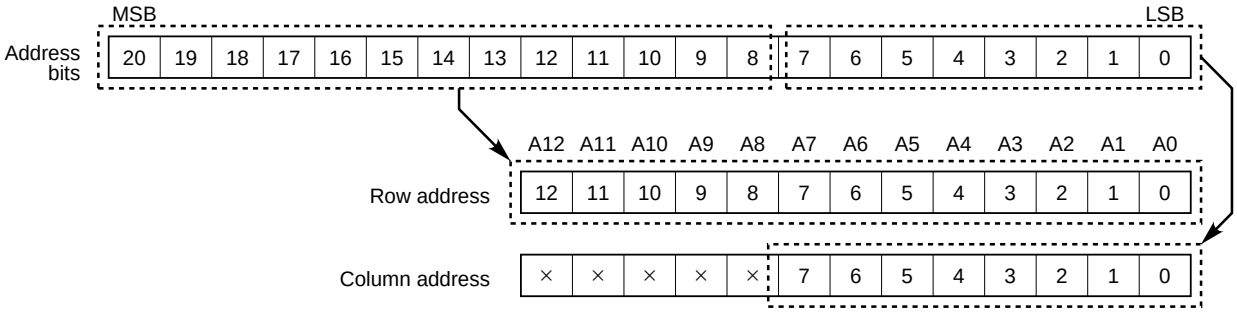
6.2 Data Output (WORD Mode)

When /WORD is set to low level, the device is set to WORD mode and 16-bit data will be output.



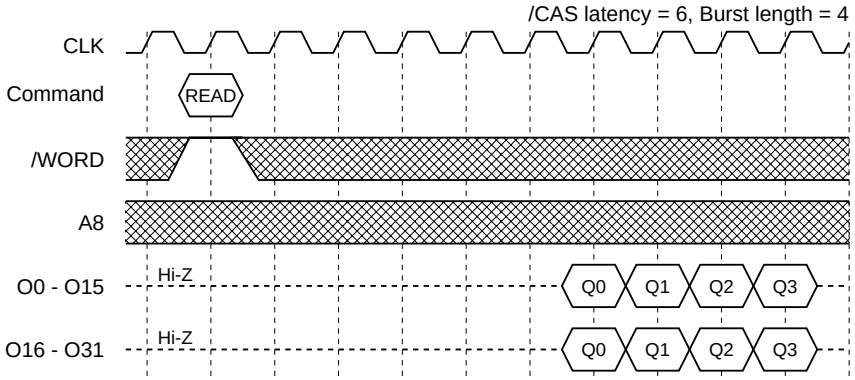


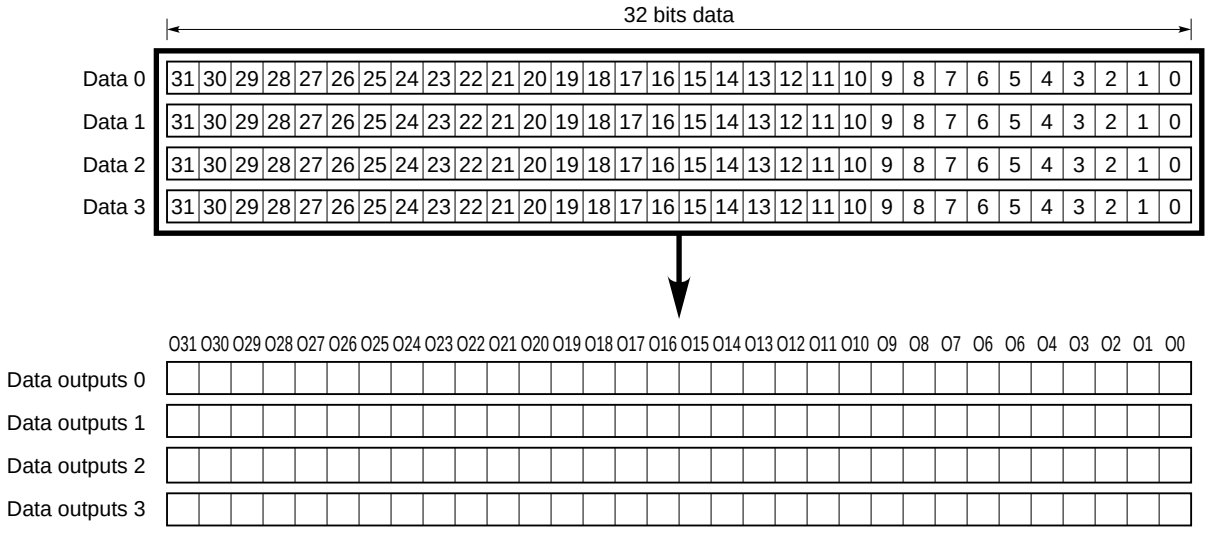
6.3 Addressing Map (DOUBLE WORD Mode)



6.4 Data Output (DOUBLE WORD Mode)

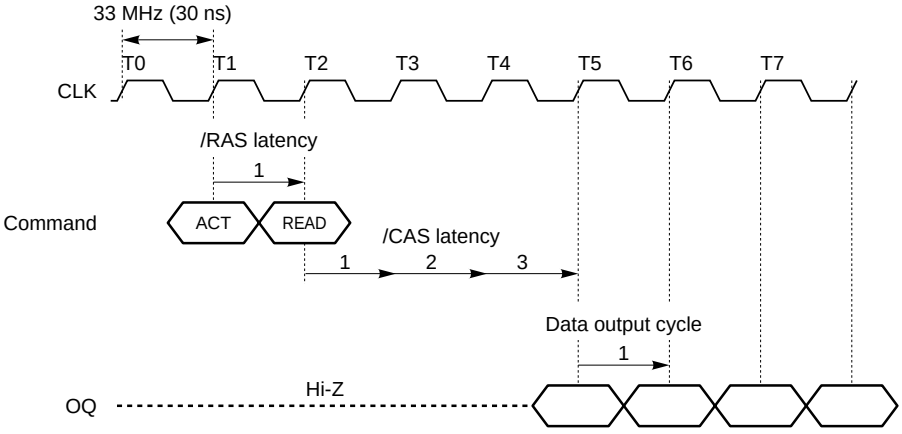
When /WORD is set to high level, the device is set to DOUBLE WORD mode and 32-bit data will be output.

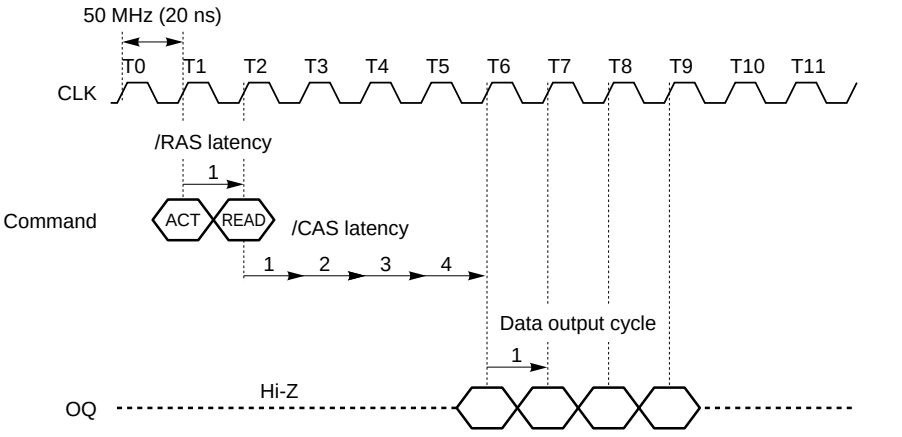


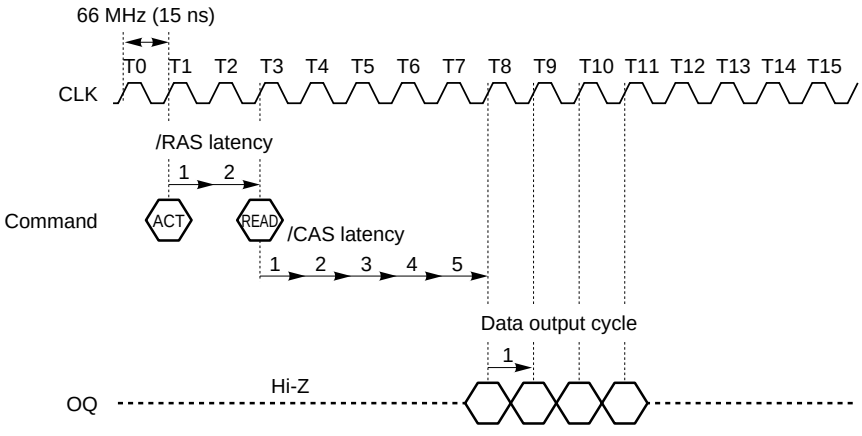


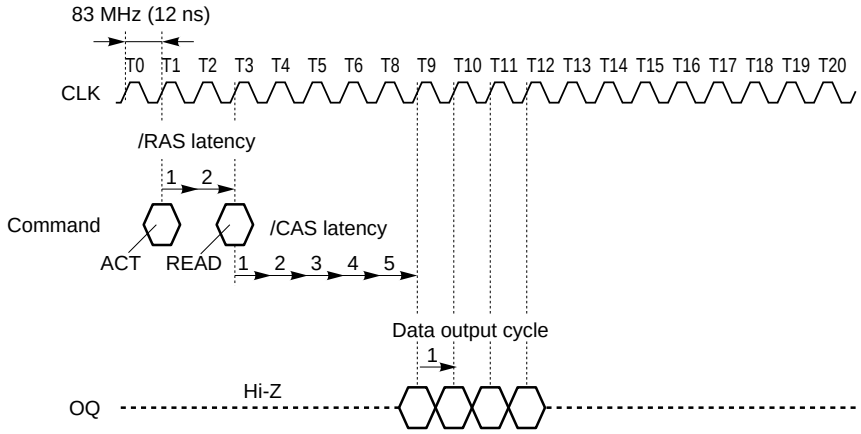
7. Relationship between Clock Frequency and /RAS Latency, /CAS Latency

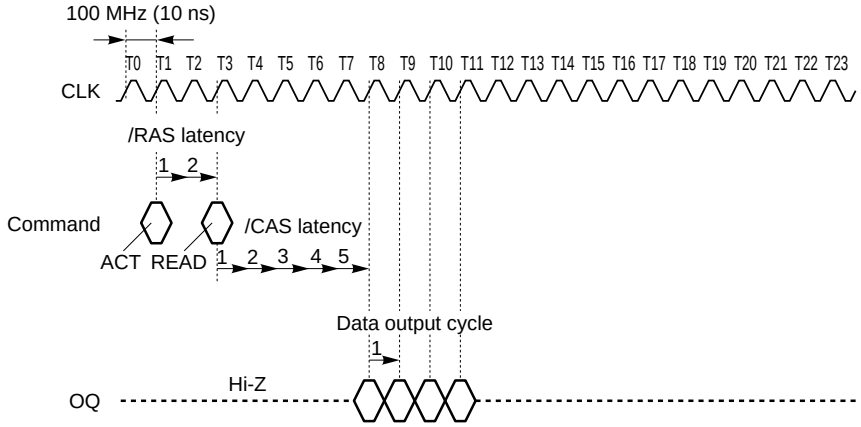
Clock frequency (Clock cycle time)	/RAS latency (MIN.)	/CAS latency (MIN.)	Data output cycle
33 MHz (30 ns)	1	3	1
50 MHz (20 ns)	1	4	1
66 MHz (15 ns)	2	5	1
83 MHz (12 ns)	2	5	1
100 MHz (10 ns)	2	5	1








83 MHz (12 ns)
T0 T1 T2 T3 T4 T5 T6 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20
CLK
/RAS latency
1 2
Command
/CAS latency
ACT READ 1 2 3 4 5
Data output cycle
1
Hi-Z
OQ


100 MHz (10 ns)
T0 T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22 T23
CLK
/RAS latency
1 2
Command
/CAS latency
ACT READ 1 2 3 4 5
Data output cycle
1
Hi-Z
OQ

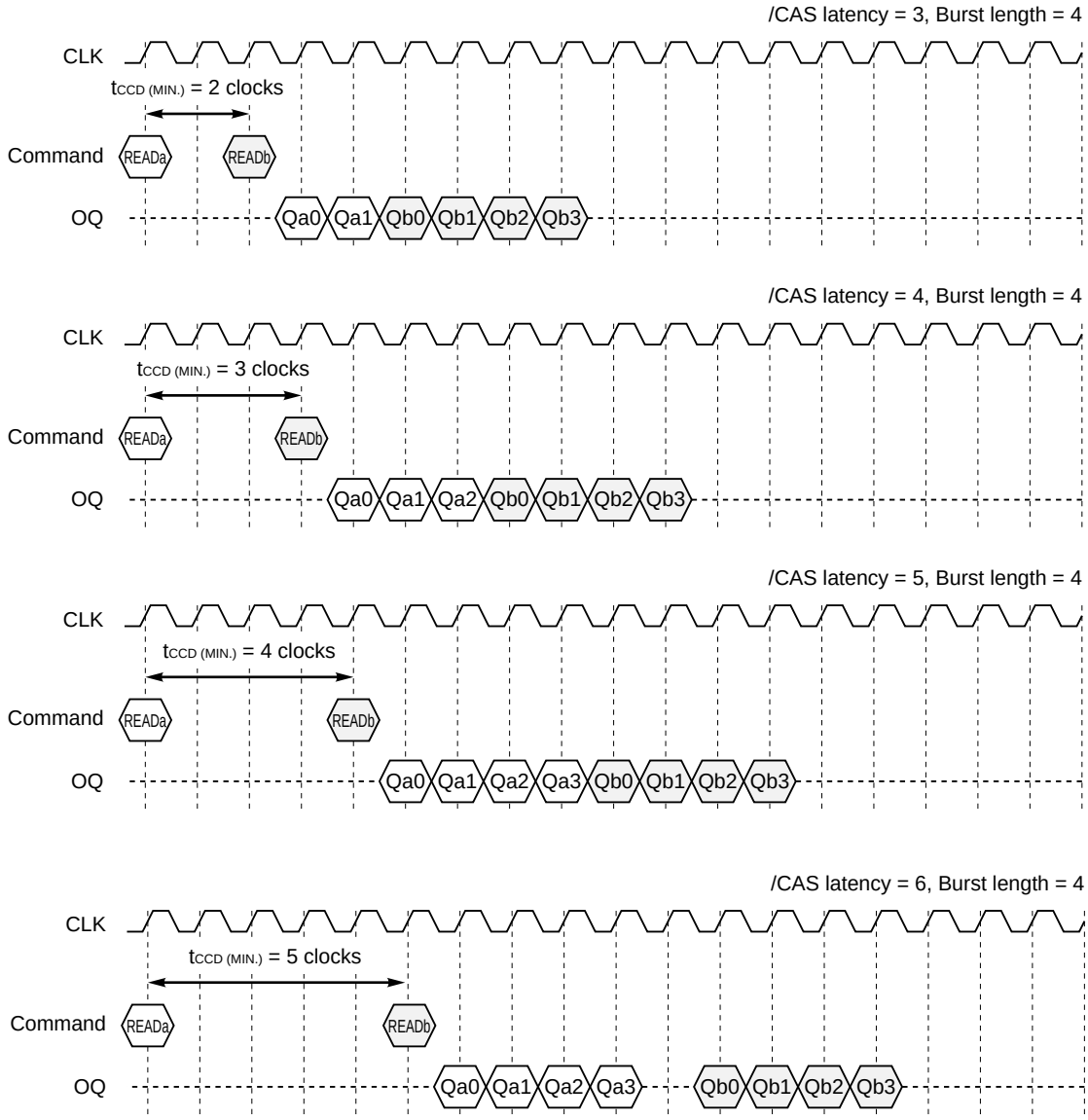
8. Command Interval

8.1 Relationship between Frequency, Parameter and Command Interval

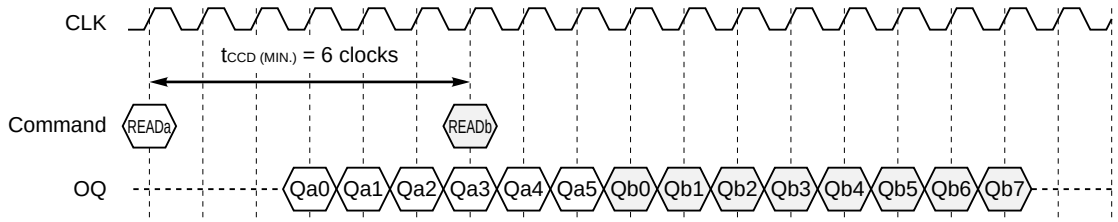
Frequency (t_{CK})	Burst length	/RAS latency (MIN.)	/CAS latency	READ to READ command interval t_{CCD} (MIN.)	READ to ROW ACTIVATE command interval (MIN.)		Unit
					Read data is NOT terminated	Read data is terminated	
100 MHz (10 ns)	4	2	5	4	4	4	CLK
			6	5	5	5	
	8		5	8	8	4	
			6	9	9	5	
83 MHz (12 ns)	4	2	5	4	4	4	CLK
			6	5	5	5	
	8		5	8	8	4	
			6	9	9	5	
66 MHz (15 ns)	4	2	5	4	4	4	CLK
			6	5	5	5	
	8		5	8	8	4	
			6	9	9	5	
50 MHz (20 ns)	4	1	4	3	3	3	CLK
			5	4	4	4	
			6	5	5	5	
	8		4	7	7	3	
			5	8	8	4	
			6	9	9	5	
33 MHz (30 ns)	4	1	3	2	2	2	CLK
			4	3	3	3	
			5	4	4	4	
			6	5	5	5	
	8		3	6	6	2	
			4	7	7	3	
			5	8	8	4	
			6	9	9	5	

8.2 READ to READ Command Interval (t_{CCD})

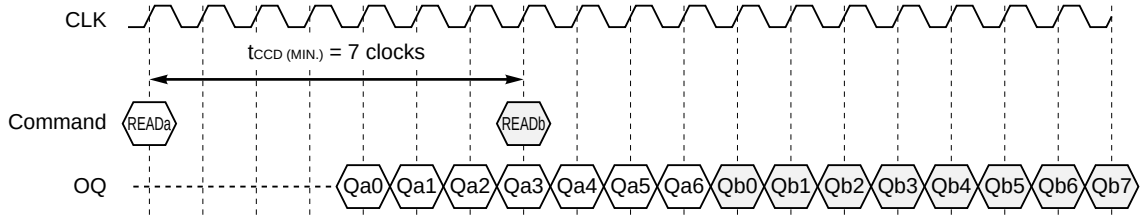
A minimum of t_{CCD} interval is required between two READ commands. For details, refer to **8.1 Relationship between Frequency, Parameter and Command Interval**.



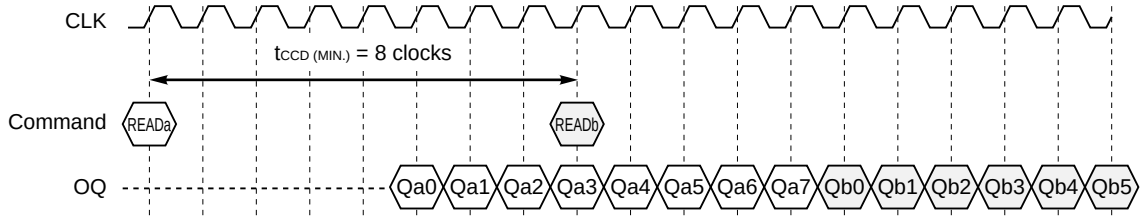
/CAS latency = 3, Burst length = 8



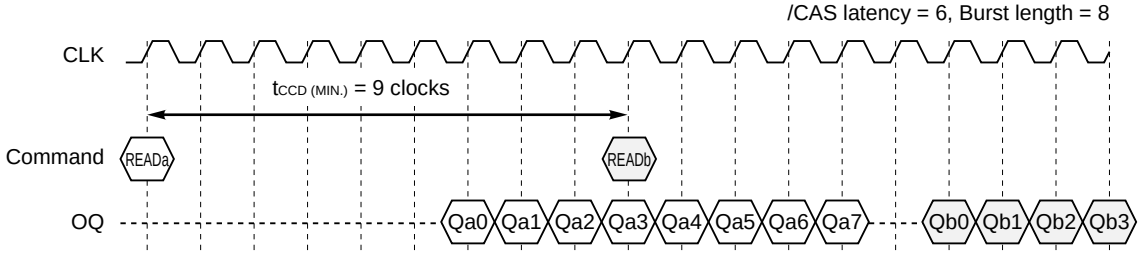
/CAS latency = 4, Burst length = 8



/CAS latency = 5, Burst length = 8



/CAS latency = 6, Burst length = 8

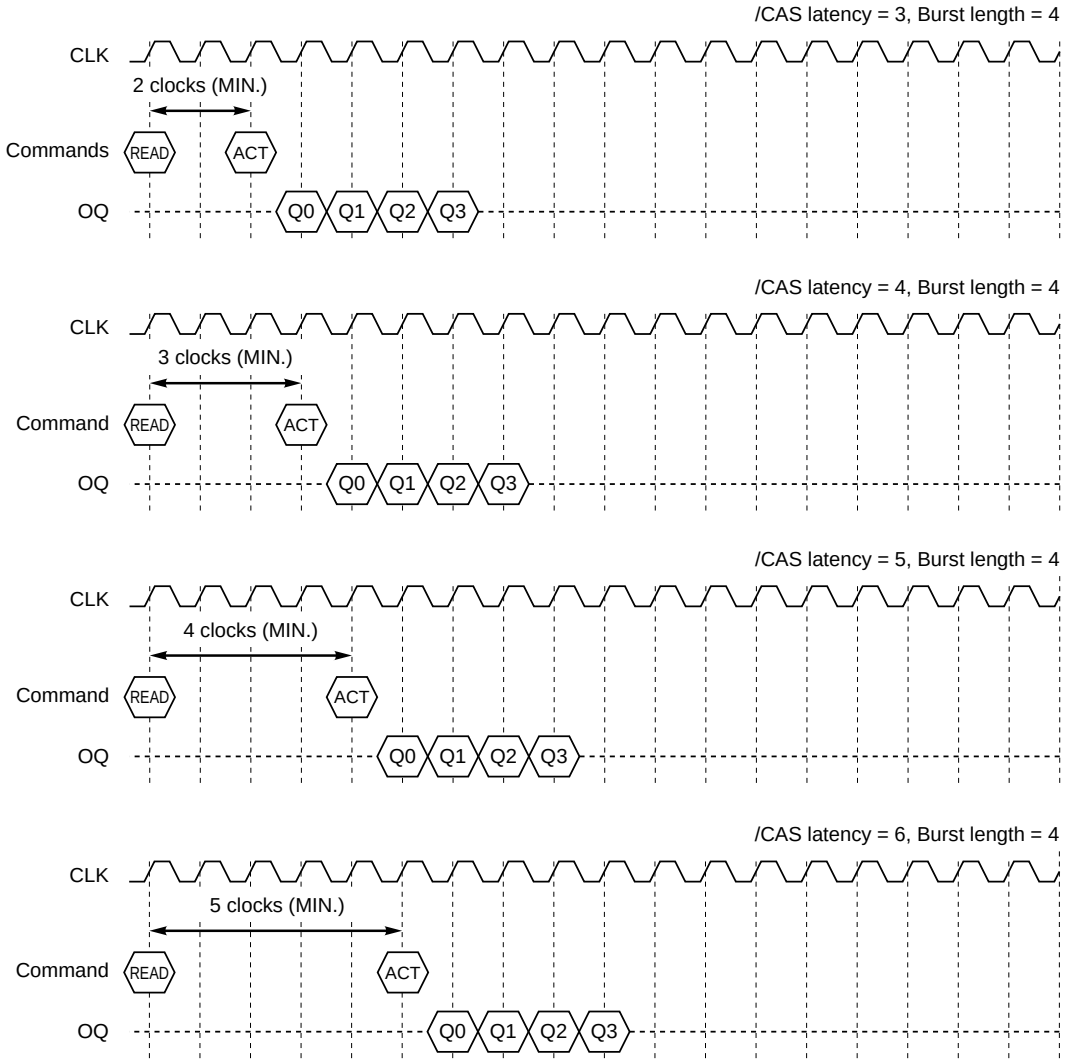


8.3 READ to ROW ACTIVATE Command Interval

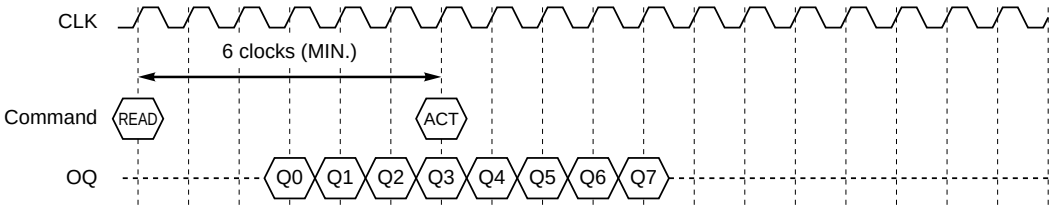
An interval required between READ and ROW ACTIVATE command differs according to whether burst data is terminated or NOT, before the ROW ACTIVATE command.

a. Read Data NOT Terminated

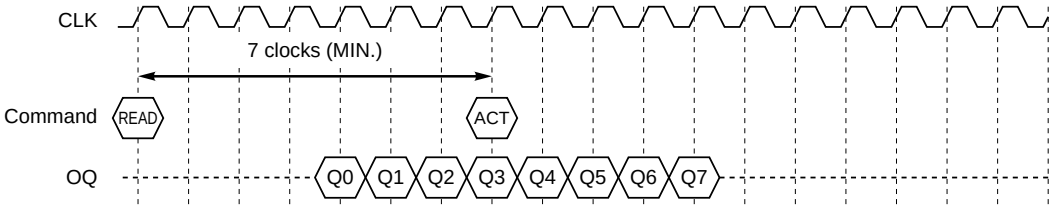
When read data is NOT terminated before the ROW ACTIVATE command, a required interval is as shown in **8.1 Relationship between Frequency, Parameter and Command Interval**.



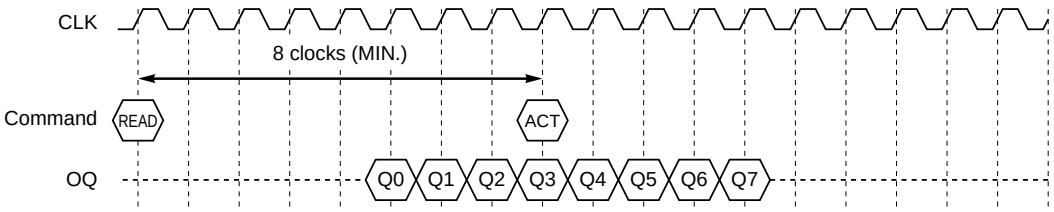
/CAS latency = 3, Burst length = 8



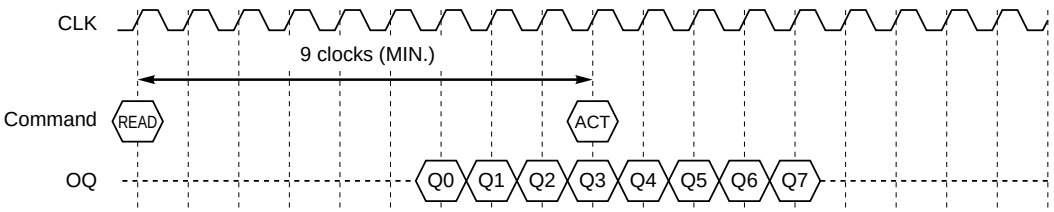
/CAS latency = 4, Burst length = 8



/CAS latency = 5, Burst length = 8

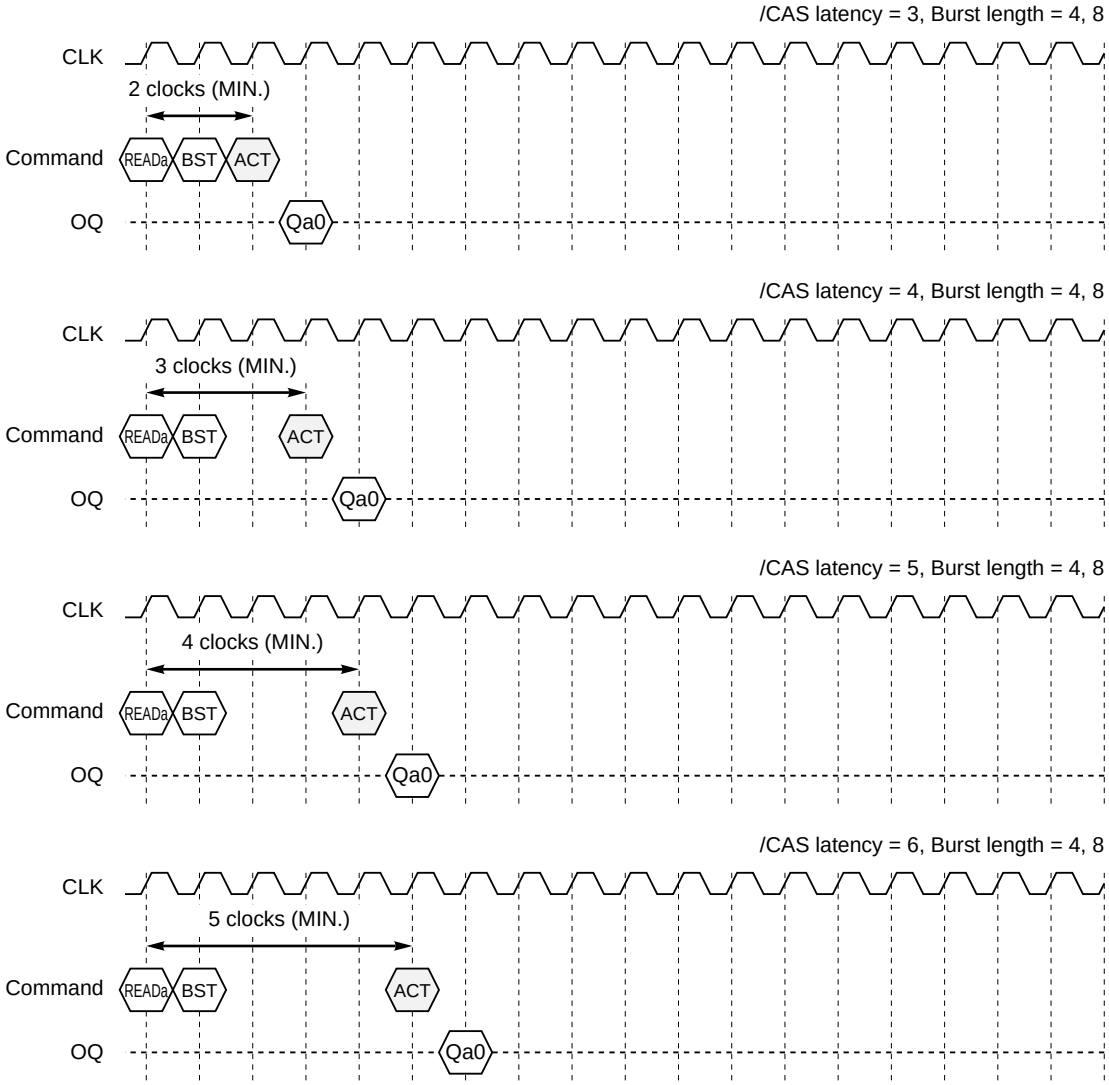


/CAS latency = 6, Burst length = 8



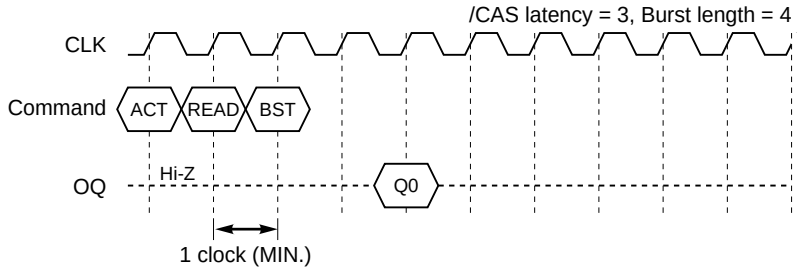
b. Read Data Terminated

When read data is terminated before the ROW ACTIVATE command, a required interval is one clock less than /CAS latency. For details, refer to **8.1 Relationship between Frequency, Parameter and Command Interval**.



8.4 READ to BURST STOP Command Interval

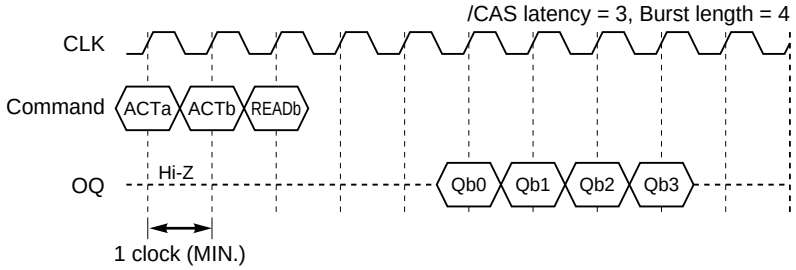
A minimum of one-clock interval is required between READ and BURST STOP command.



8.5 ROW ACTIVATE to ROW ACTIVATE Command Interval

A minimum of one-clock interval is required between two ROW ACTIVATE command.

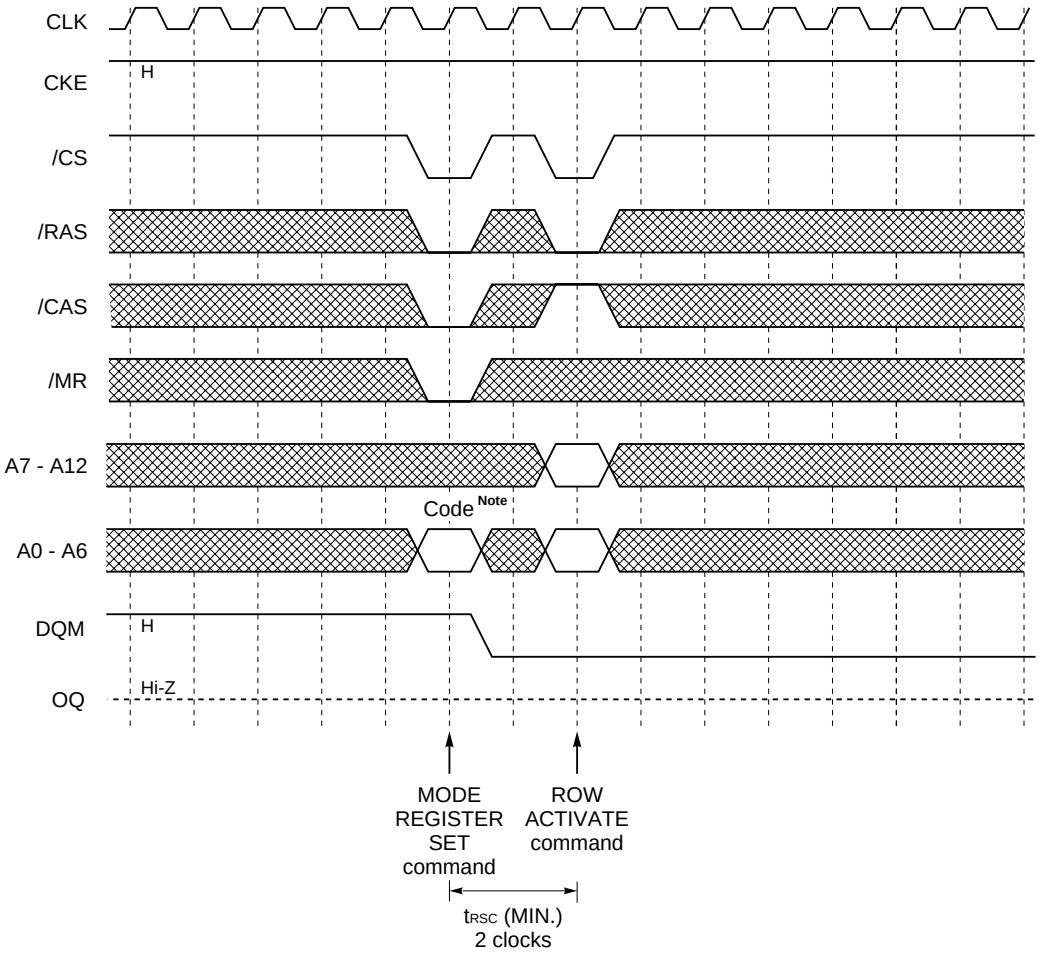
However, t_{RC} is required between two ROW ACTIVATE command for valid data output. See **12.1 Relationship between Frequency and Parameter** for details.



9. Power-On Sequence

This device must be powered-on in a manner as follows.

- CKE and DQM must be held at high level on power-on.
- On power-on, the mode register is set to default values; /RAS latency is set to 2, /CAS latency to 6, burst length to 4 and wrap type to sequential. To change these values, MODE REGISTER SET command is required.
- In order to keep all outputs to Hi-Z until the MODE REGISTER SET command is finished, DQM must be held at high level.

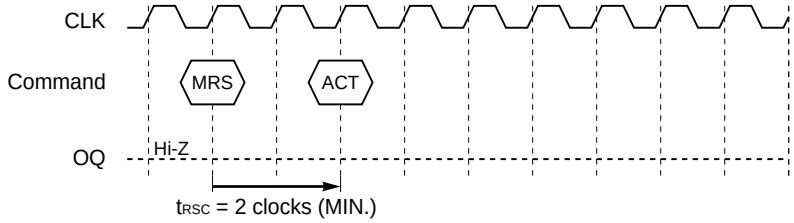


Note For details of input code, refer to **5. Mode Register Settings**.

10. Basic Operations

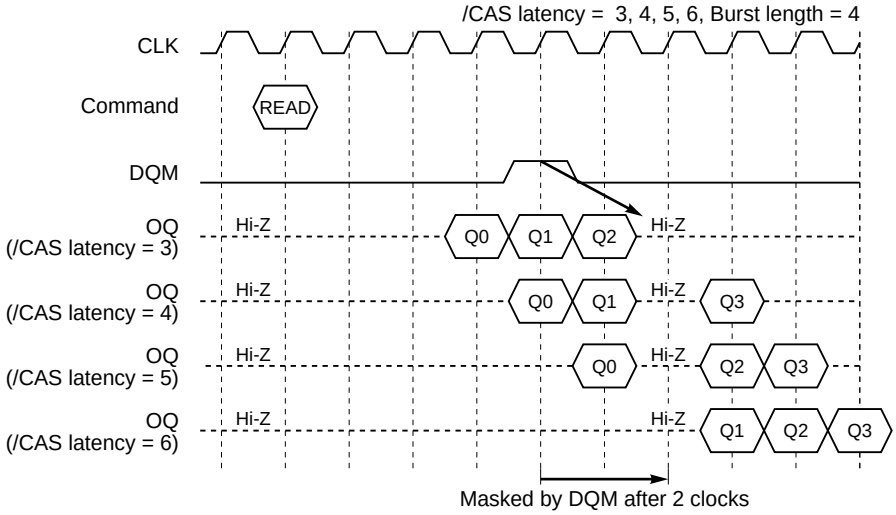
10.1 MODE REGISTER SET Command

A minimum of 2 clocks are required between MODE REGISTER SET command and others.



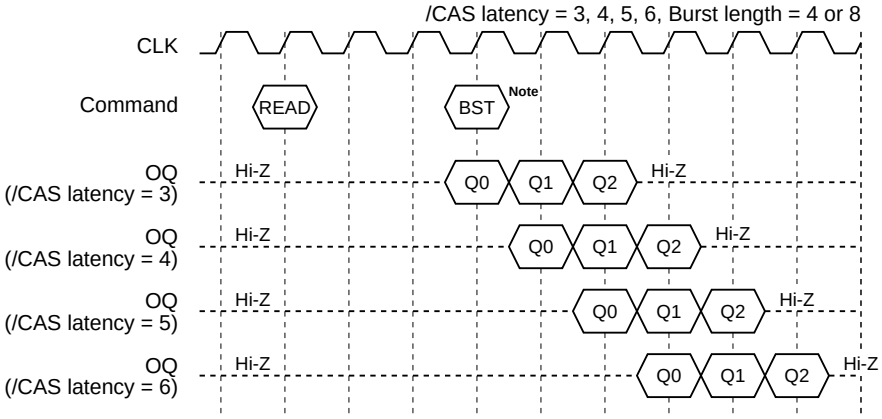
10.2 DQM Operation

Read data can be masked by setting DQM high level as follows.



10.3 Burst Termination

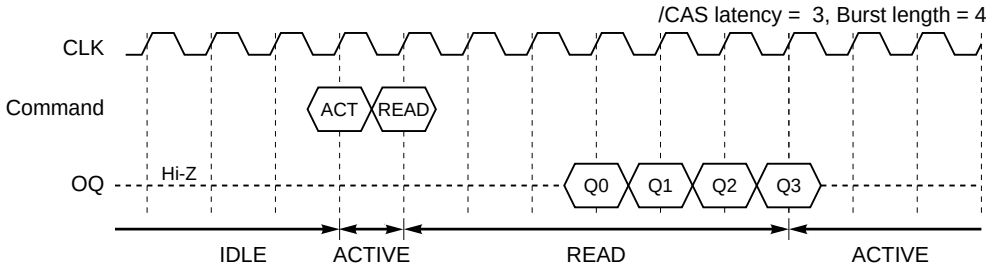
During a read cycle, when the BURST STOP command is issued, the burst read data will be terminated and the data bus will be Hi-Z after the /CAS latency. At least one-clock interval is required between READ and BURST STOP command regardless of the /CAS latency.



Note Both standard and SDRAM-precharge-like types of the BURST STOP command can be used.

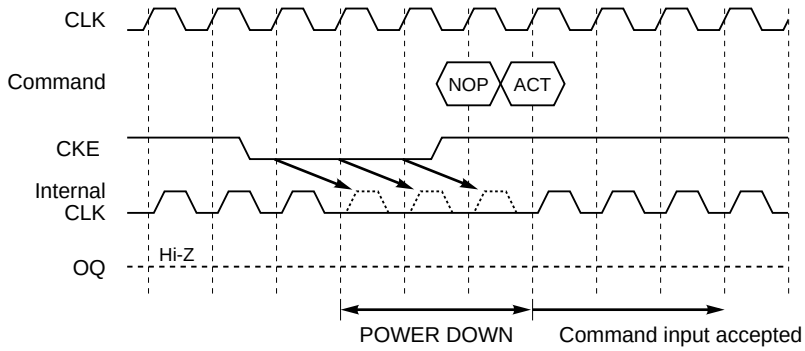
10.4 POWER DOWN and CLOCK SUSPEND Mode

Operation modes of this device is shown as follows. Refer to **2. Simplified State Diagram** for details.



10.4.1 POWER DOWN Mode

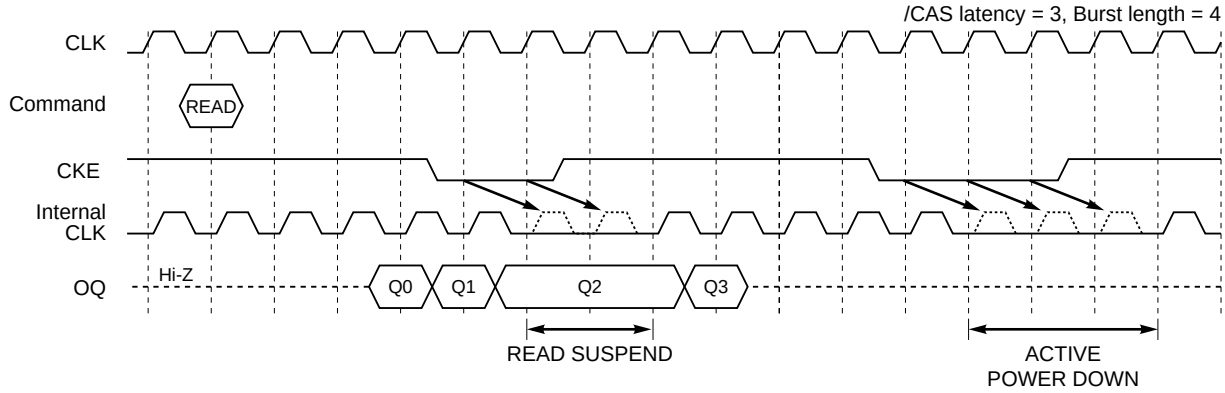
When CKE is held at low level in the IDLE state, the device will turn to the POWER DOWN (Standby) mode.



Remark Once the device had turned to the POWER DOWN mode, ROW ACTIVATE command is necessary in order to read data.

10.4.2 READ SUSPEND and ACTIVE POWER DOWN Mode

When CKE is held at low level in READ mode, the device will turn to the READ SUSPEND (Active standby) mode. When CKE is held at low level in ACTIVE mode, the device will turn to the ACTIVE POWER DOWN (Active standby) mode.



11. Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on power supply pin relative to GND	V_{CC}		–0.5 Note to +4.6	V
Voltage on any pin relative to GND	V_T		–0.5 Note to V_{CC} + 0.5 V, ≤ +4.6	V
Short circuit output current	I_O		50	mA
Power dissipation	P_D		1	W
Operating ambient temperature	T_A		0 to 70	°C
Storage temperature	T_{stg}		–55 to +150	°C

Note –1.0 V (MIN.) : 10 ns pulse width measured at 50% of pulse amplitude.

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}		3.0	3.3	3.6	V
High level input voltage	V_{IH}		2.0		V_{CC}+0.3 Note1	V
Low level input voltage	V_{IL}		–0.3 Note2		+0.8	V
Operating ambient temperature	T_A		0		70	°C

Notes 1. V_{CC} + 0.5 V (MAX.) : 10 ns pulse width measured at 50% of pulse amplitude.

2. –0.5 V (MIN.) : 10 ns pulse width measured at 50% of pulse amplitude.

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	All input pins			5	pF
Output capacitance	C_O	All output pins			7	pF

DC Characteristics (Recommended Operating Conditions unless Otherwise Noted)

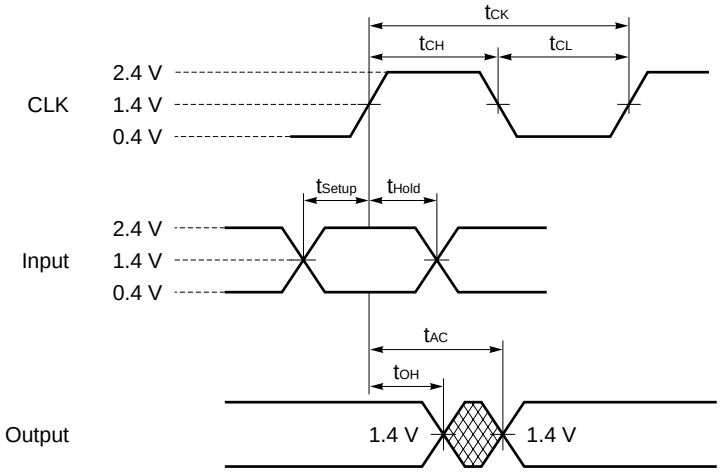
Parameter	Symbol	Test condition	MIN.	MAX.	Unit	Note
Standby current	$I_{CC3}P$	CKE ≤ $V_{IL\ (MAX.)}$, t_{CK} = 10 ns		3	mA	
in power down mode	$I_{CC3}PS$	CKE = 0 V, t_{CK} = 10 ns		100	μA	
Active standby current in non power down mode	$I_{CC3}N$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = 10 ns, /CS ≥ $V_{IH\ (MIN.)}$, input signals are changed one time during 10 ns.		50	mA	
	$I_{CC3}NS$	CKE ≥ $V_{IH\ (MIN.)}$, t_{CK} = ∞, input signals are stable.		10		
★ Operating current (Burst mode)	I_{CC4}	t_{CK} = 10 ns, I_O = 0 mA, /CAS latency = 5		150	mA	1
Input leakage current	$I_{I\ (L)}$	V_I = 0 to 3.6 V, all other pins not under test = 0 V	–10	+10	μA	
Output leakage current	$I_{O\ (L)}$	D_{OUT} is disabled, V_O = 0 to 3.6 V	–10	+10	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA	2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA		0.4	V	

Note 1. I_{CC4} depends on output loading and cycle rates. Specified values are obtained with output open. In addition to this, I_{CC4} is measured on condition that addresses are changed only one time during $t_{CK\ (MIN.)}$.

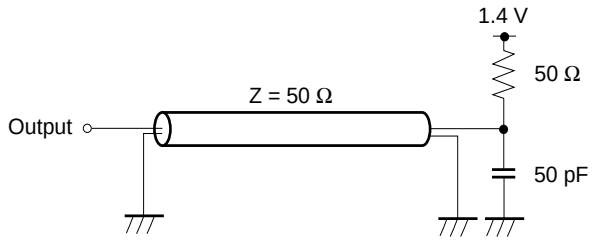
AC Characteristics (Recommended Operating Conditions unless Otherwise Noted)

AC Characteristics Test Conditions

- AC measurements assume t_T = 1 ns.
- Reference level for measuring timing of input signals is 1.4 V. Transition times are measured between V_{IH} and V_{IL}.
- If t_T is longer than 1 ns, reference level for measuring timing of input signals is $V_{IH\ (MIN.)}$ and $V_{IL\ (MAX.)}$.
- An access time is measured at 1.4 V.



Output Load



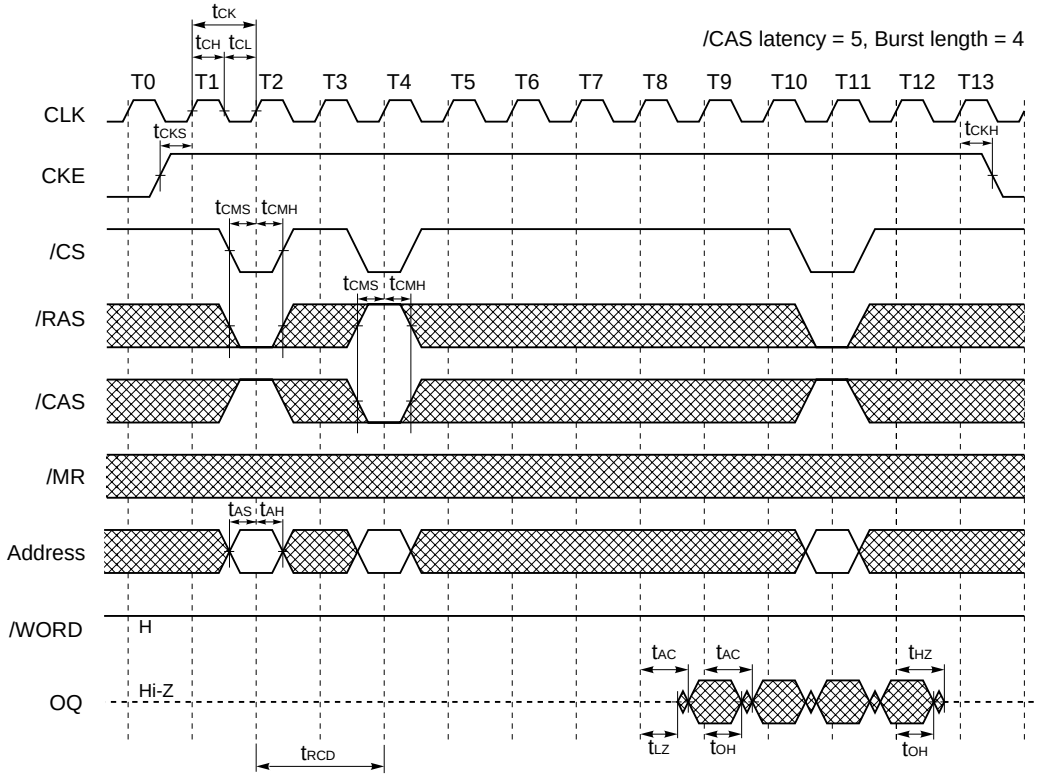
Asynchronous Characteristics

Parameter	Symbol	100 MHz		83 MHz		66 MHz		50 MHz		33 MHz		Unit
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Mode register set time	t_{RSC}	2		2		2		2		2		clock
/RAS to /CAS delay time (/RAS latency)	t_{RCD}	20		24		30		20		30		ns
Transition time	t_T	0.1	10.0	0.1	10.0	0.1	10.0	0.1	10.0	0.1	10.0	ns

Synchronous Characteristics

Parameter	Symbol	100 MHz		83 MHz		66 MHz		50 MHz		33 MHz		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock cycle time	t_{CK}	10		12		15		20		30		ns	
Access time from CLK	t_{AC}		6		8		9		9		9	ns	
CLK high level width	t_{CH}	4		4		4		4		4		ns	
CLK low level width	t_{CL}	4		4		4		4		4		ns	
Data-out hold time	t_{OH}	2.5		2.5		2.5		2.5		2.5		ns	
Data-out Low-Z time	t_{LZ}	0		0		0		0		0		ns	
Data-out Hi-Z time	t_{HZ}	2.5	6	2.5	8	2.5	9	2.5	9	2.5	9	ns	
Address setup time	t_{AS}	3		3		4		4		4		ns	
Address hold time	t_{AH}	1		1		2		2		2		ns	
CKE setup time	t_{CKS}	3		3		4		4		4		ns	
CKE hold time	t_{CKH}	1		1		2		2		2		ns	
CKE setup time (power down exit)	t_{CKSP}	$4+t_{CK}$		$4+t_{CK}$		$4+t_{CK}$		$4+t_{CK}$		$4+t_{CK}$		ns	
Command setup time (/CS, /RAS, /CAS, /MR, /WORD)	t_{CMS}	3		3		4		4		4		ns	
Command hold time (/CS, /RAS, /CAS, /MR, /WORD)	t_{CMH}	1		1		2		2		2		ns	

AC Parameters for Read Timing



12. Timing Charts

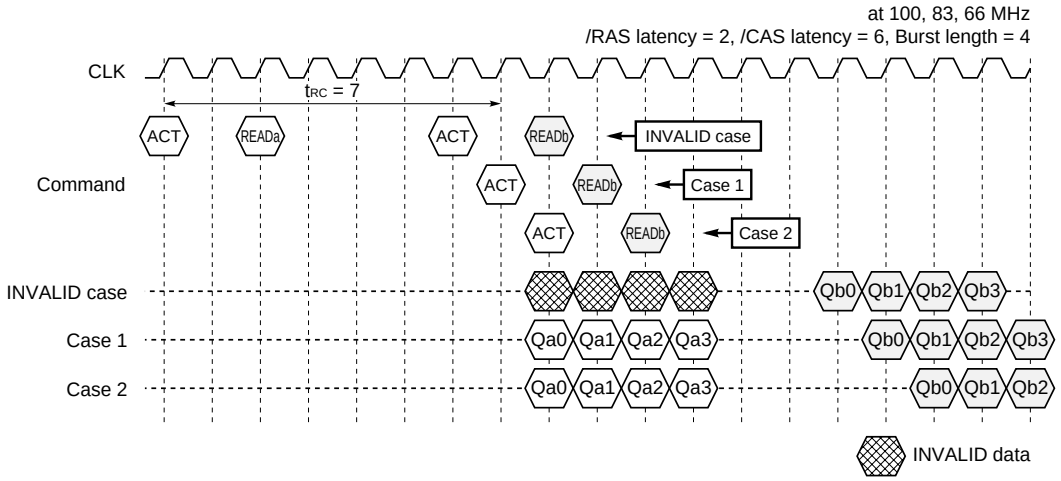
12.1 Relationship between Frequency and Parameter

Frequency (t_{CK})	/RAS latency (MIN.)	/CAS latency	Burst length	$t_{RC\ (MIN.)}$ Note1	$t_{CCD\ (MIN.)}$ Note2	Unit
100 MHz (10 ns)	2	5	4	6	4	CLK
		6		7	5	
		5	8	10	8	
		6		11	9	
83 MHz (12 ns)	2	5	4	6	4	CLK
		6		7	5	
		5	8	10	8	
		6		11	9	
66 MHz (15 ns)	2	5	4	6	4	CLK
		6		7	5	
		5	8	10	8	
		6		11	9	
50 MHz (20 ns)	1	4	4	4	3	CLK
		5		5	4	
		6		6	5	
		4	8	8	7	
		5		9	8	
		6		10	9	
33 MHz (30 ns)	1	3	4	3	2	CLK
		4		4	3	
		5		5	4	
		6		6	5	
		3	8	7	6	
		4		8	7	
		5		9	8	
		6		10	9	

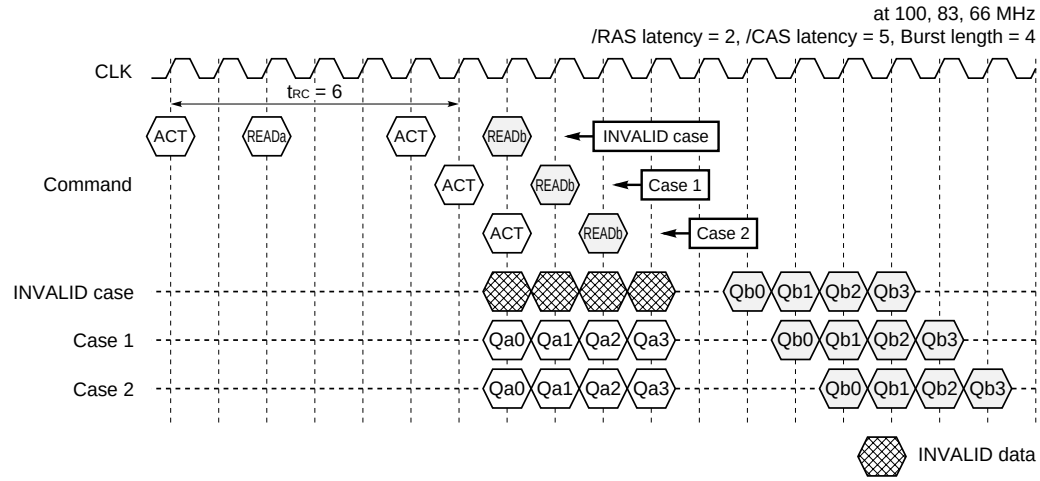
Notes 1. t_{RC} : ACT to ACT command period

2. t_{CCD} : READ to READ command period

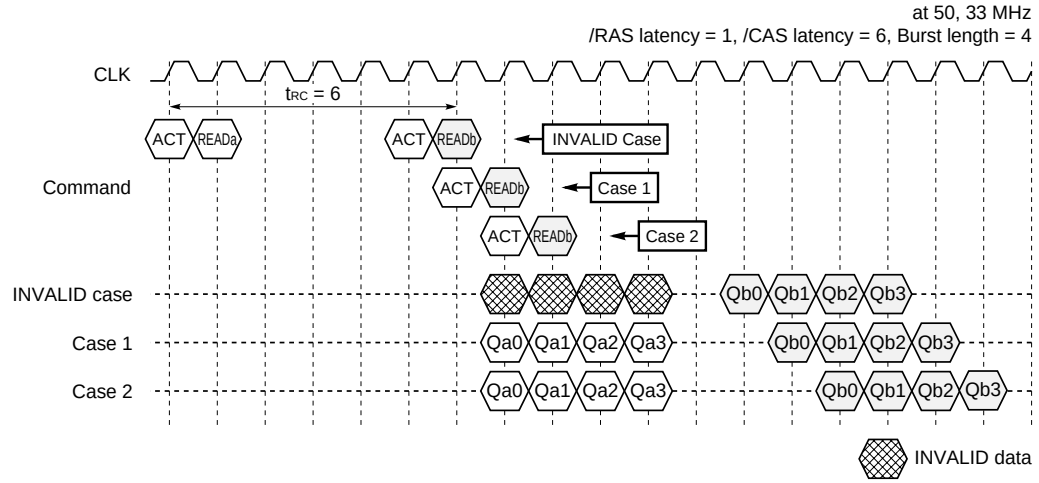
12.1.1 ROW ACTIVATE - READ - ROW ACTIVATE - READ (1-1)



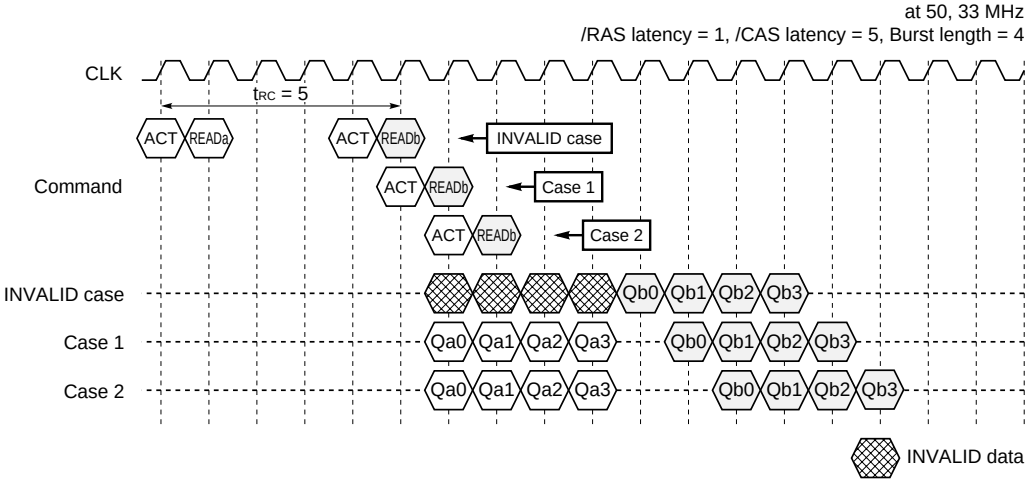
12.1.2 ROW ACTIVATE - READ - ROW ACTIVATE - READ (1-2)



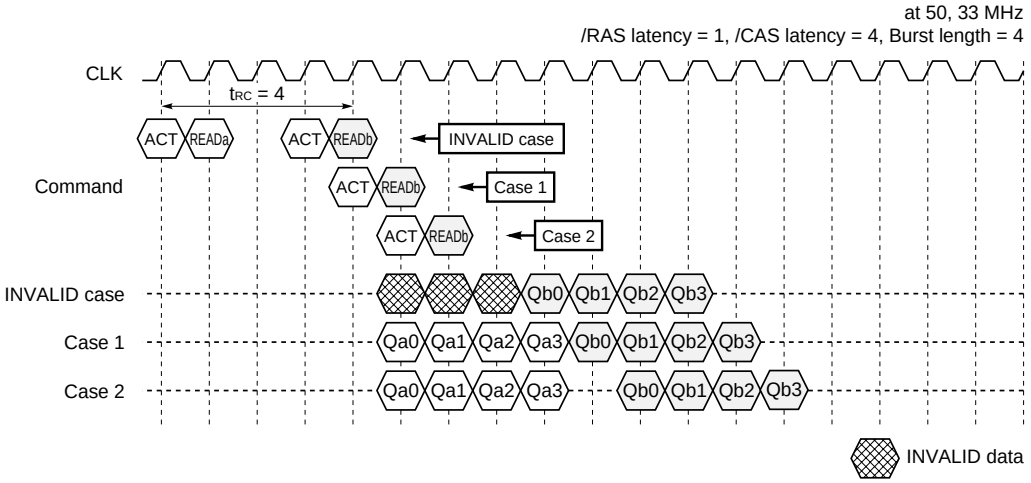
12.1.3 ROW ACTIVATE - READ - ROW ACTIVATE - READ (2-1)



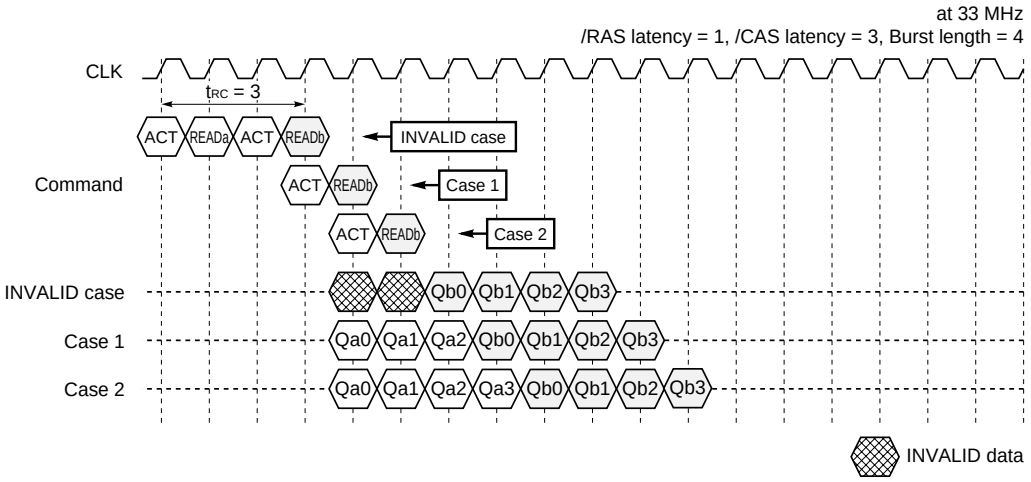
12.1.4 ROW ACTIVATE - READ - ROW ACTIVATE - READ (2-2)



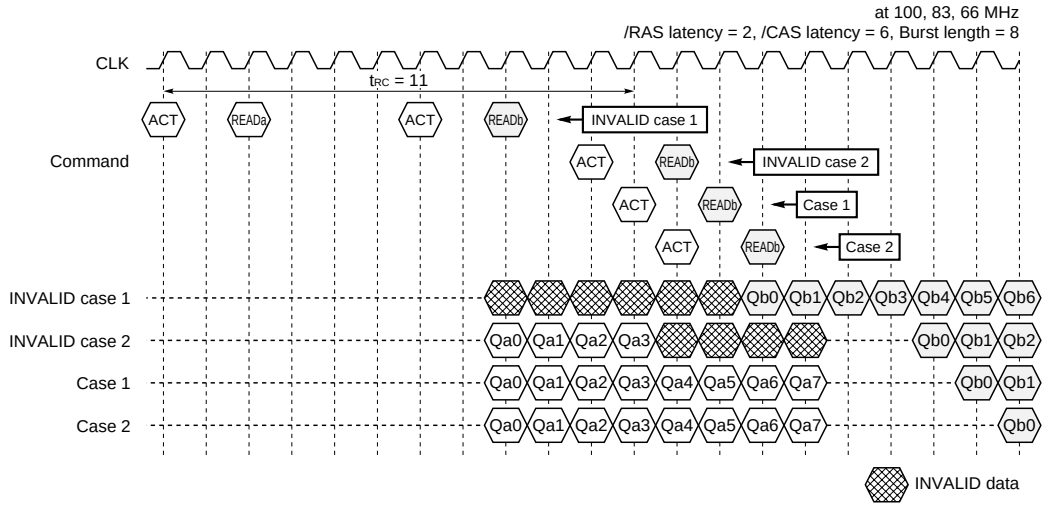
12.1.5 ROW ACTIVATE - READ - ROW ACTIVATE - READ (2-3)



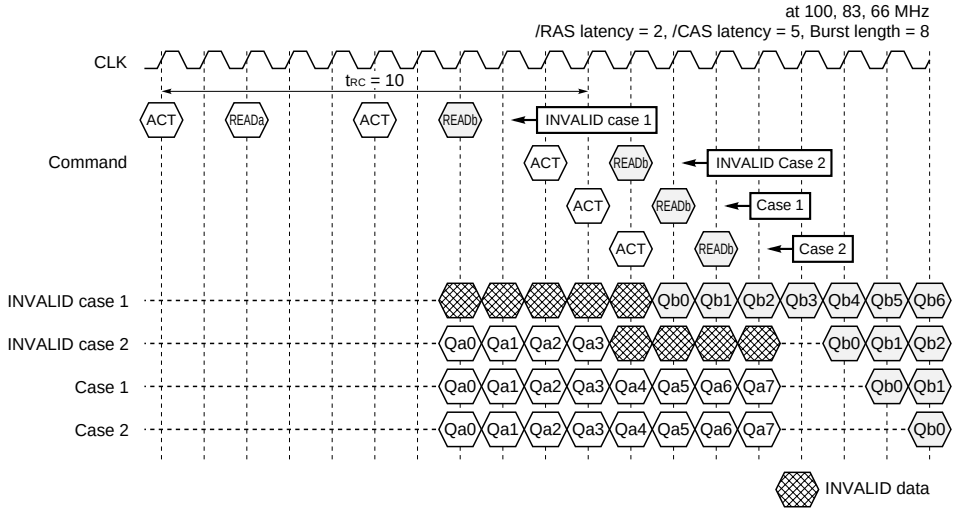
12.1.6 ROW ACTIVATE - READ - ROW ACTIVATE - READ (2-4)



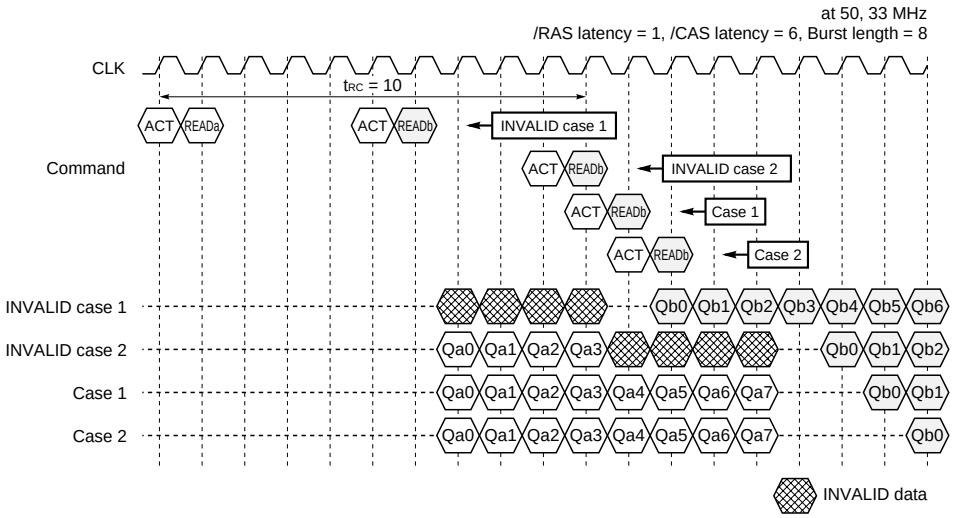
12.1.7 ROW ACTIVATE - READ - ROW ACTIVATE - READ (3-1)



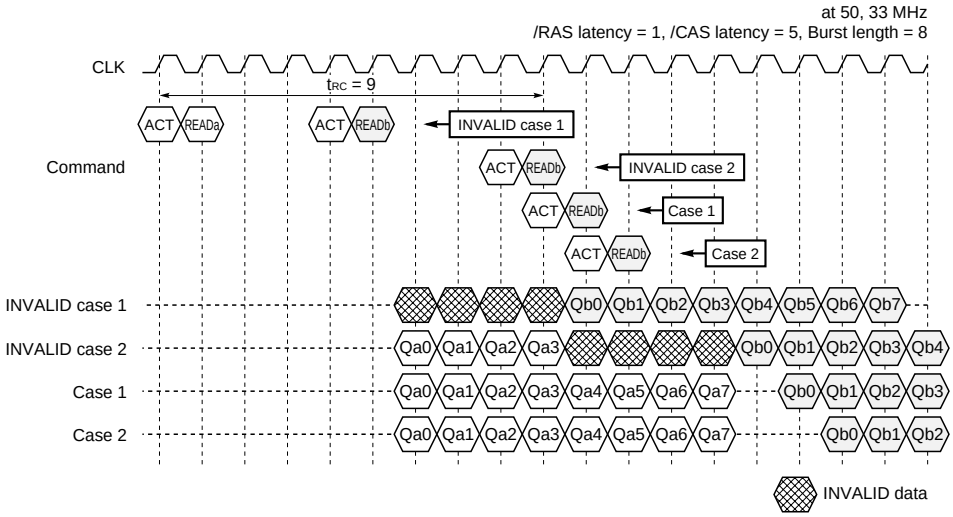
12.1.8 ROW ACTIVATE - READ - ROW ACTIVATE - READ (3-2)



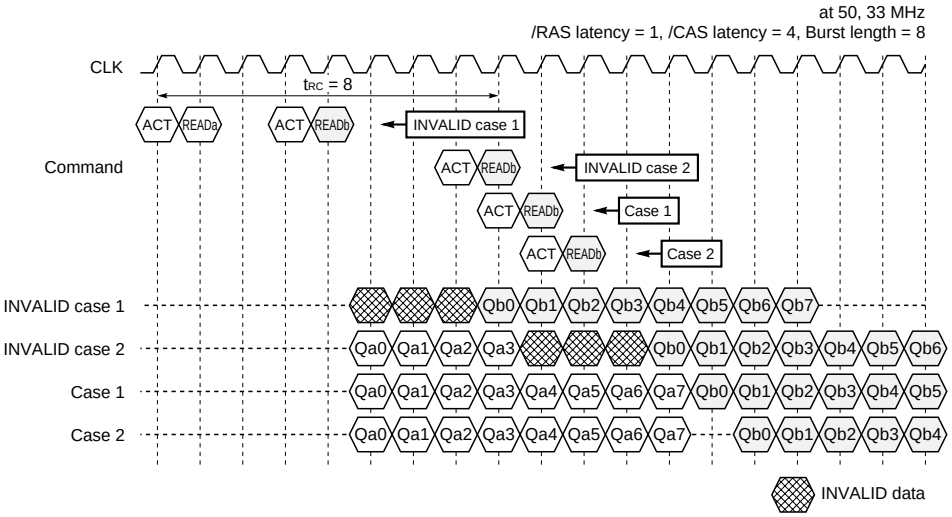
12.1.9 ROW ACTIVATE - READ - ROW ACTIVATE - READ (4-1)



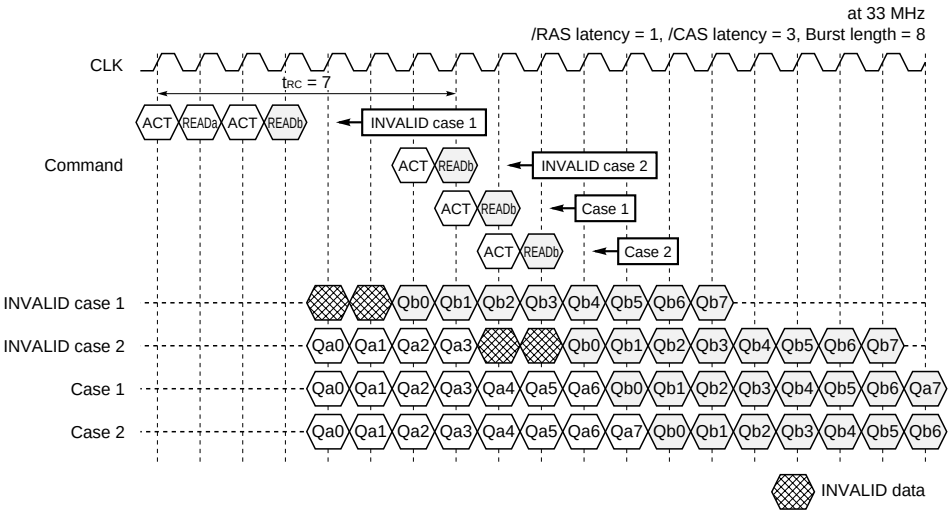
12.1.10 ROW ACTIVATE - READ - ROW ACTIVATE - READ (4-2)



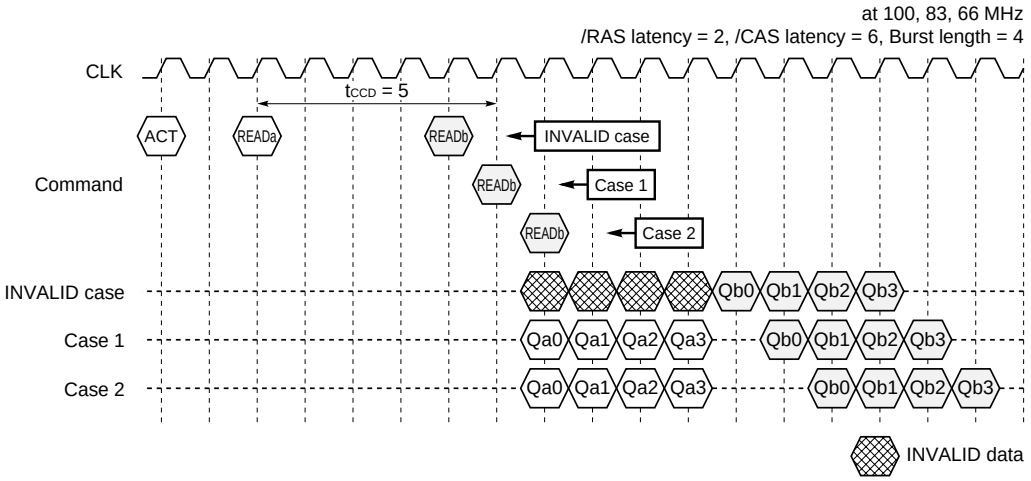
12.1.11 ROW ACTIVATE - READ - ROW ACTIVATE - READ (4-3)



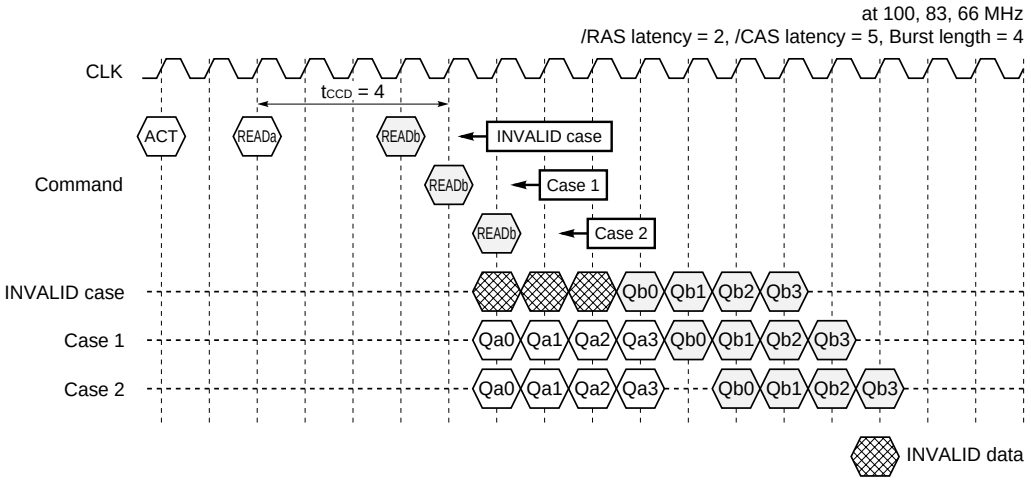
12.1.12 ROW ACTIVATE - READ - ROW ACTIVATE - READ (4-4)



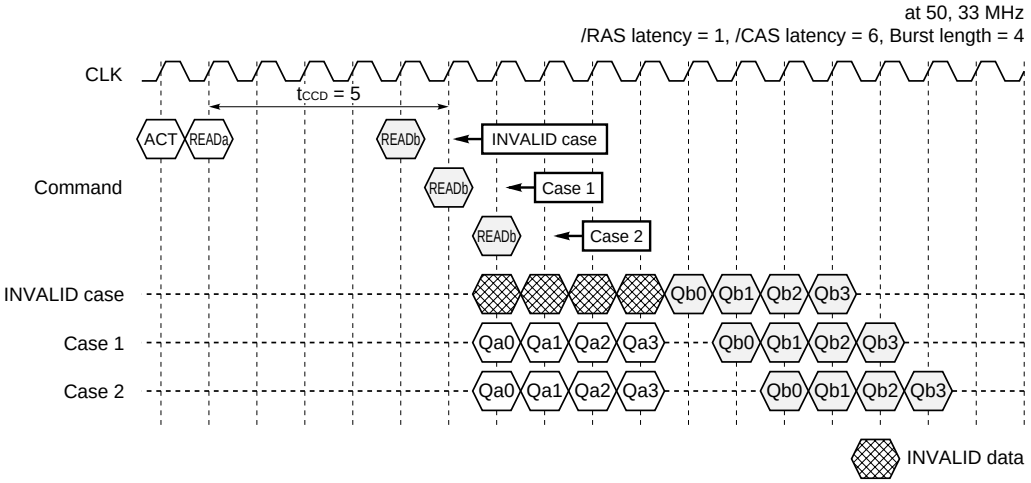
12.1.13 ROW ACTIVATE - READ - READ (1-1)



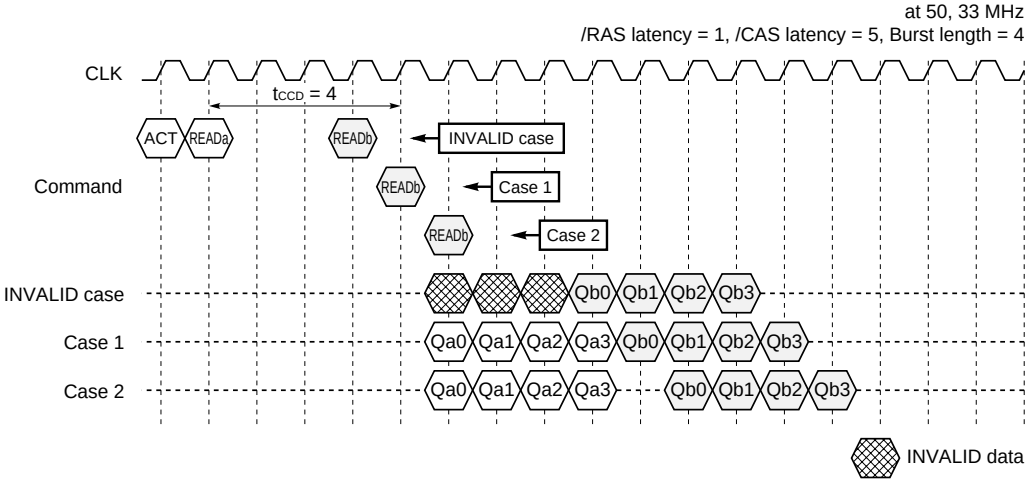
12.1.14 ROW ACTIVATE - READ - READ (1-2)



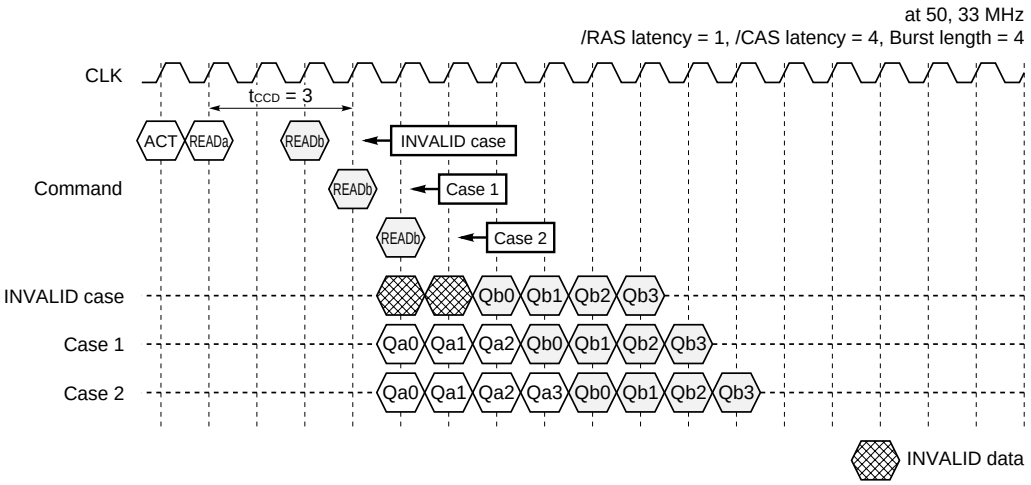
12.1.15 ROW ACTIVATE - READ - READ (2-1)



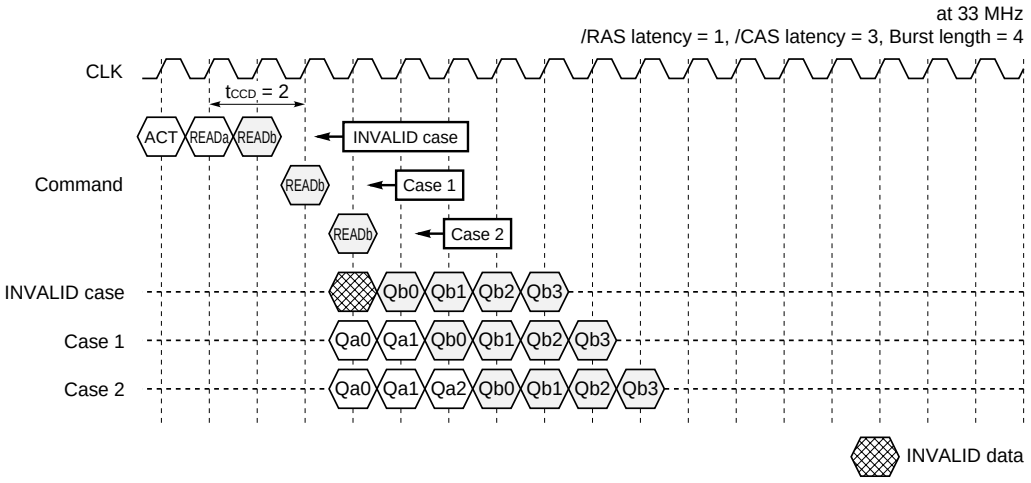
12.1.16 ROW ACTIVATE - READ - READ (2-2)



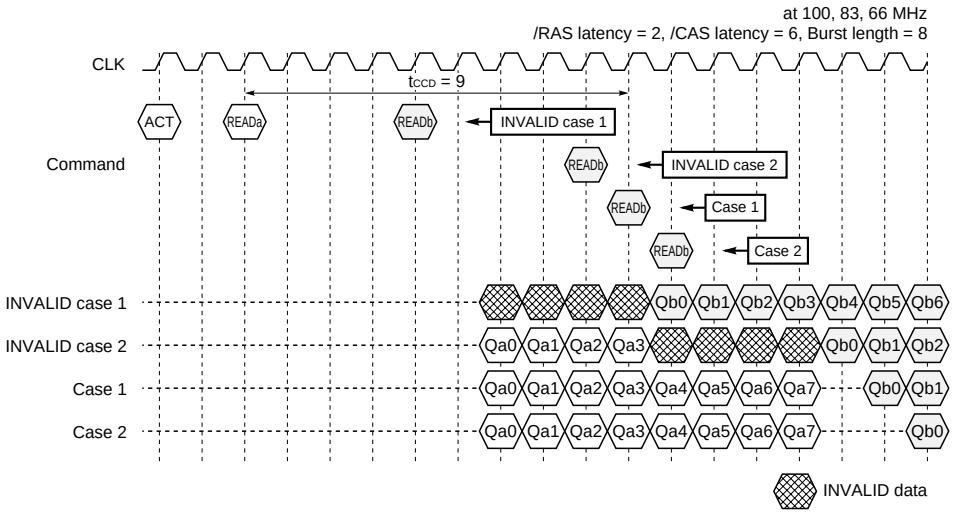
12.1.17 ROW ACTIVATE - READ - READ (2-3)



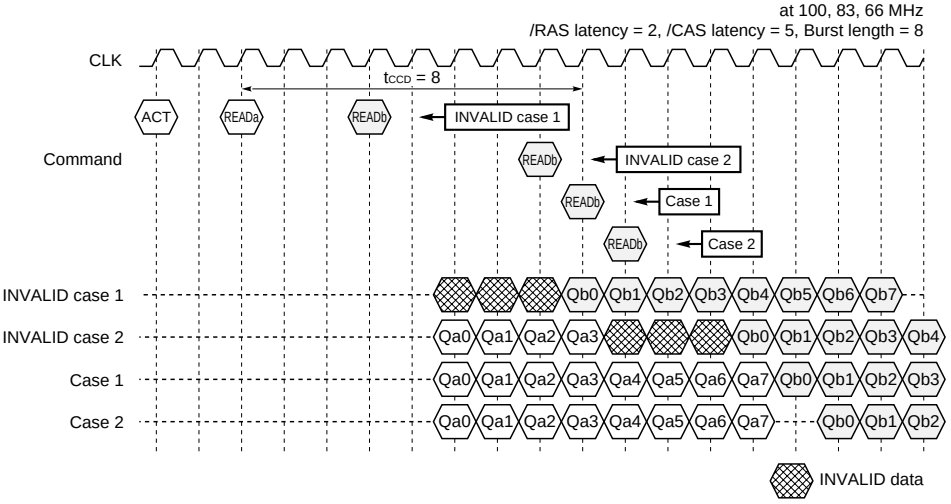
12.1.18 ROW ACTIVATE - READ - READ (2-4)



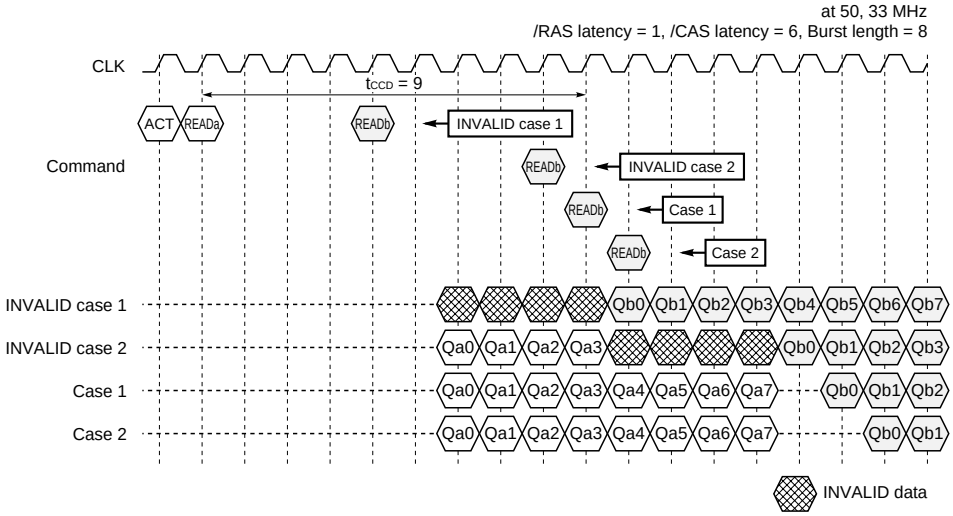
12.1.19 ROW ACTIVATE - READ - READ (3-1)



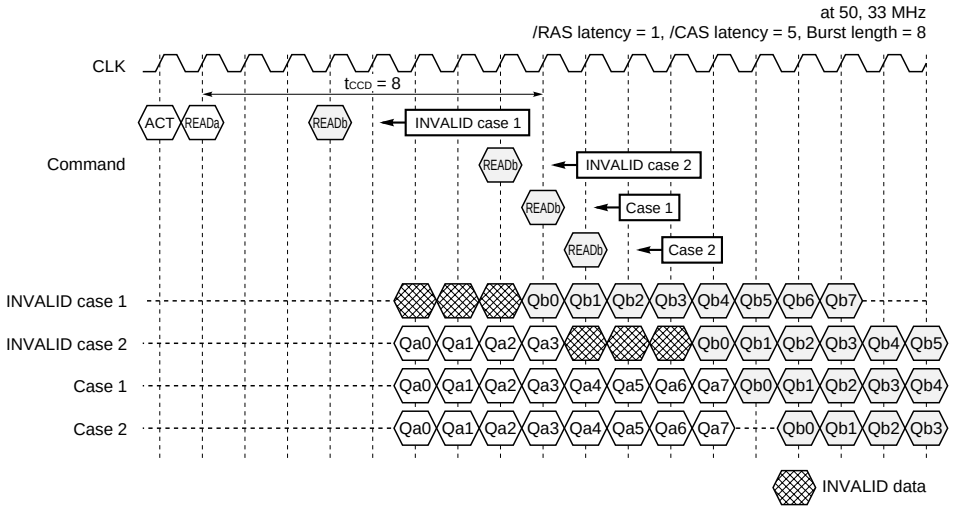
12.1.20 ROW ACTIVATE - READ - READ (3-2)



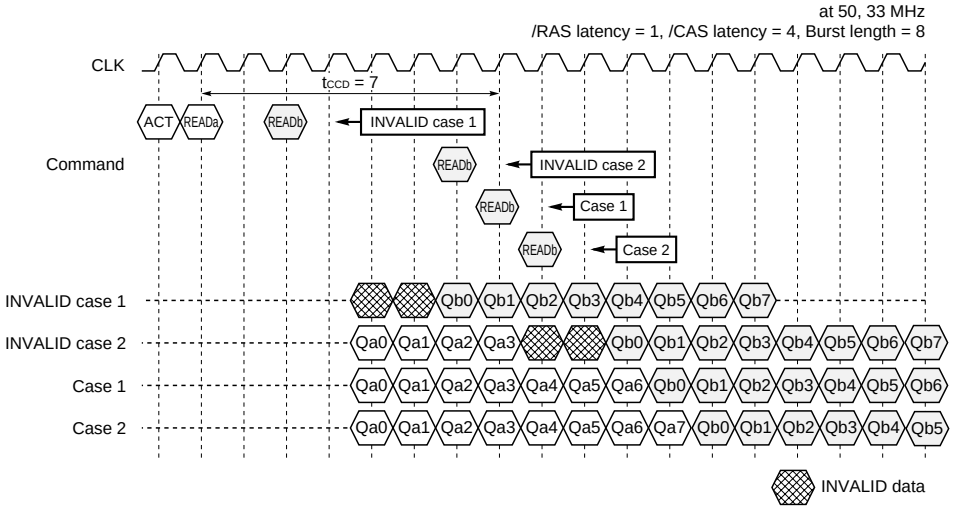
12.1.21 ROW ACTIVATE - READ - READ (4-1)



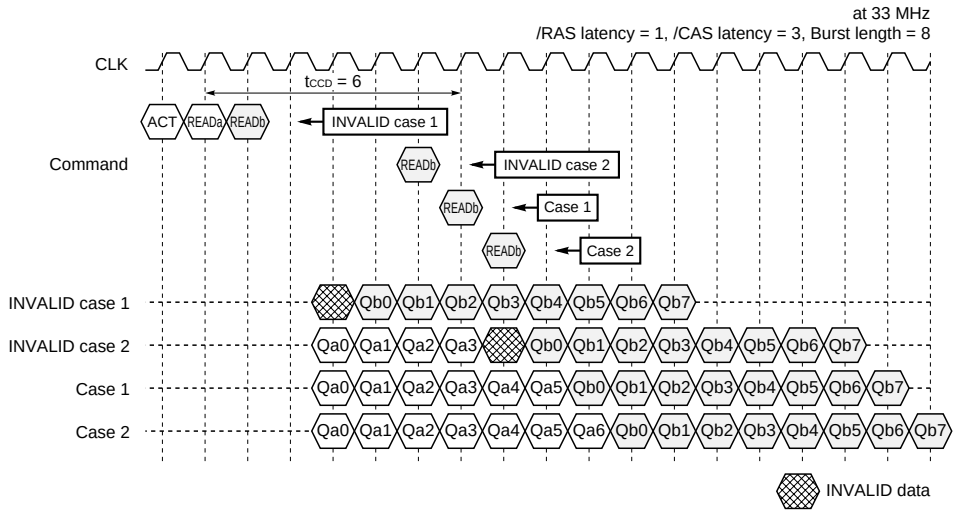
12.1.22 ROW ACTIVATE - READ - READ (4-2)



12.1.23 ROW ACTIVATE - READ - READ (4-3)

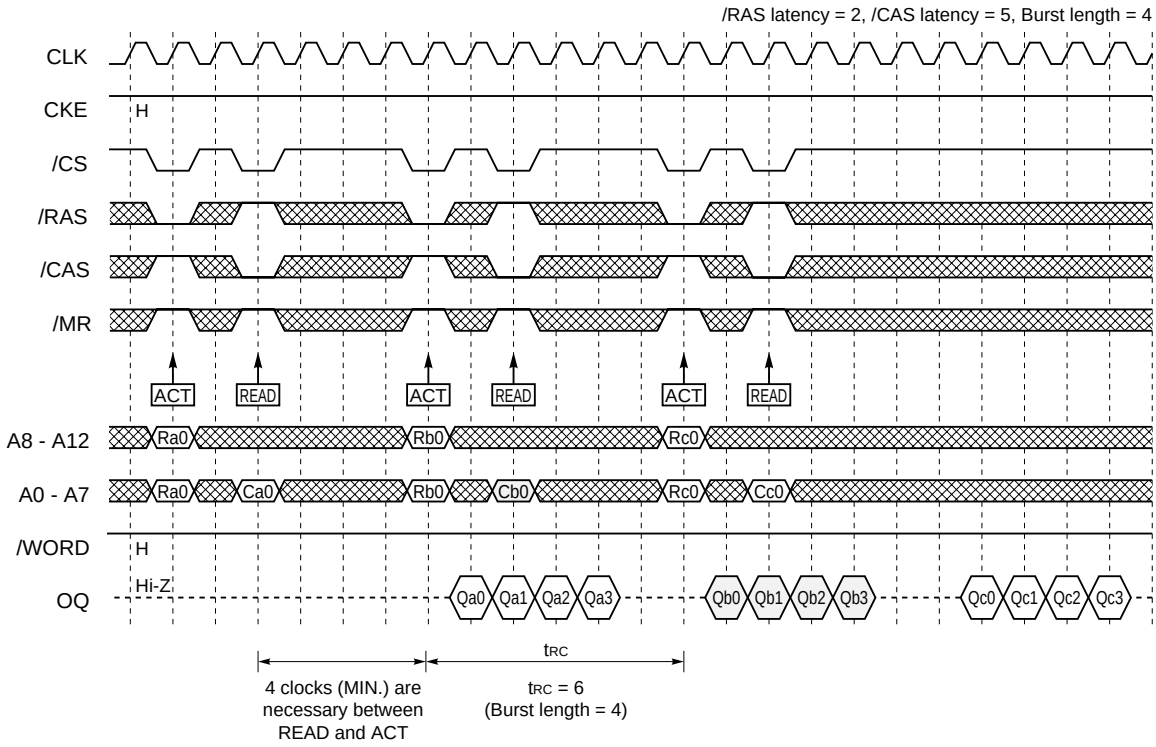


12.1.24 ROW ACTIVATE - READ - READ (4-4)

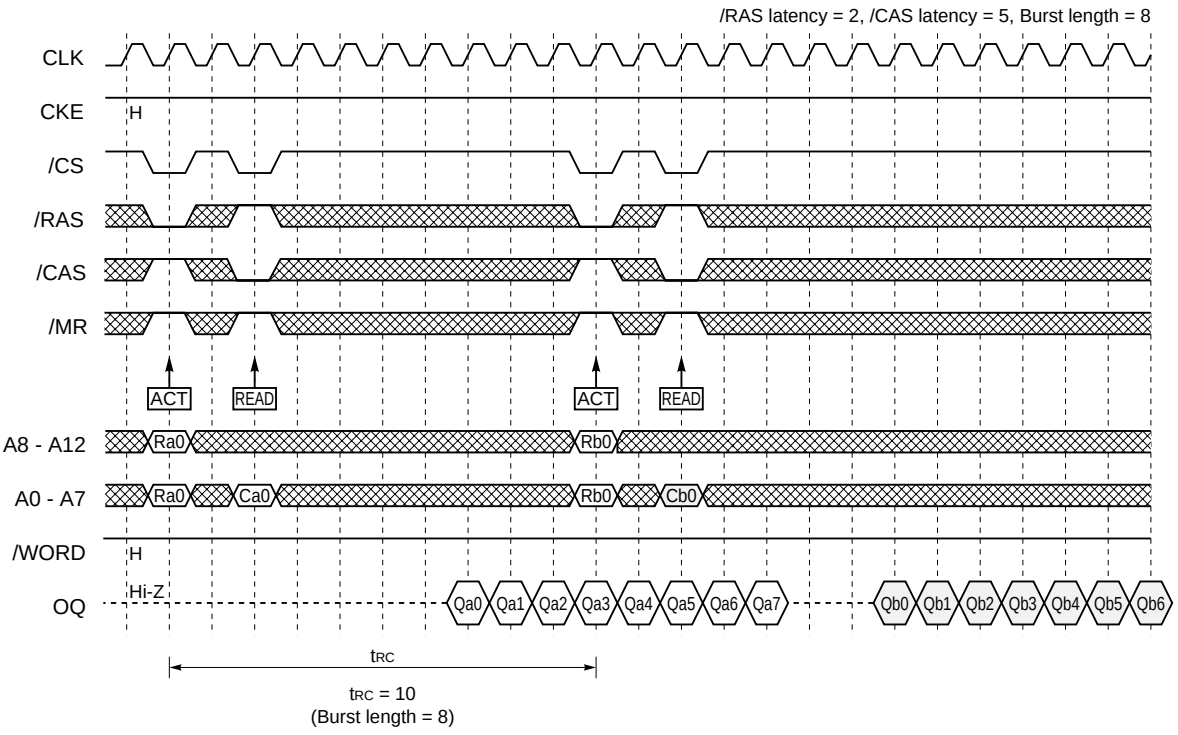


12.2 Random Row Read Timing

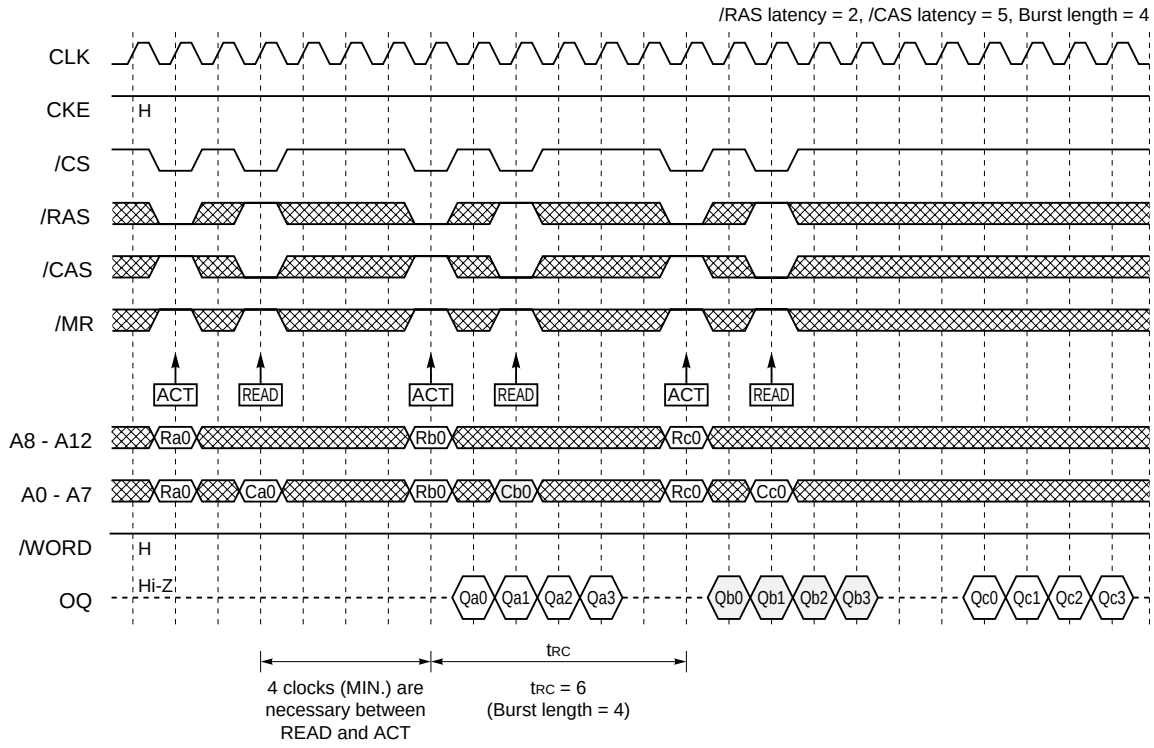
12.2.1 at 100 MHz (2-5-1-1-1)



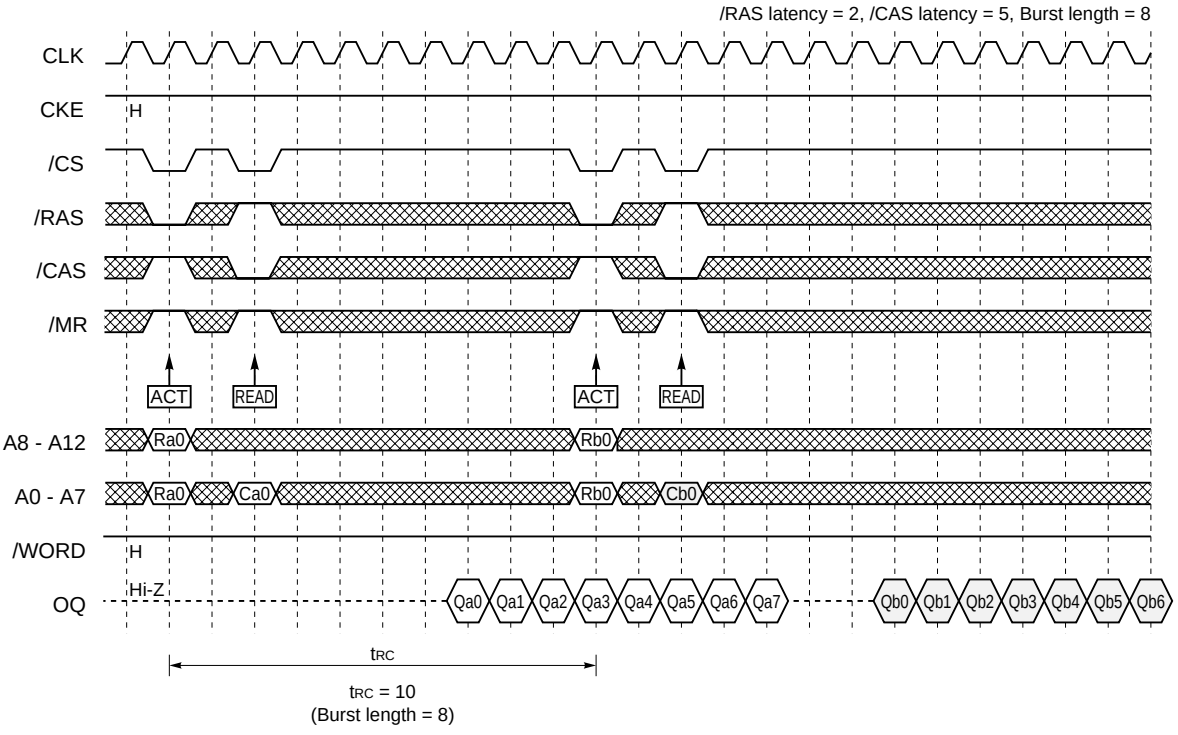
12.2.2 at 100 MHz (2-5-1-1-1-1-1-1-1)



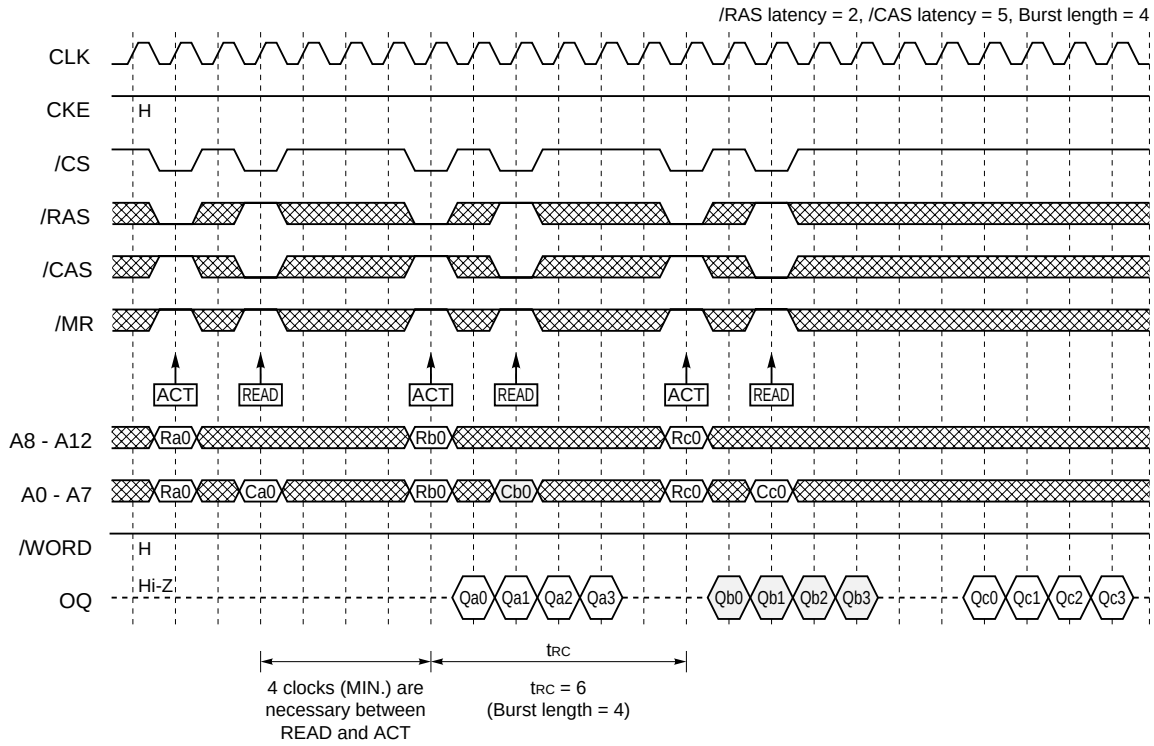
12.2.3 at 83 MHz (2-5-1-1-1)



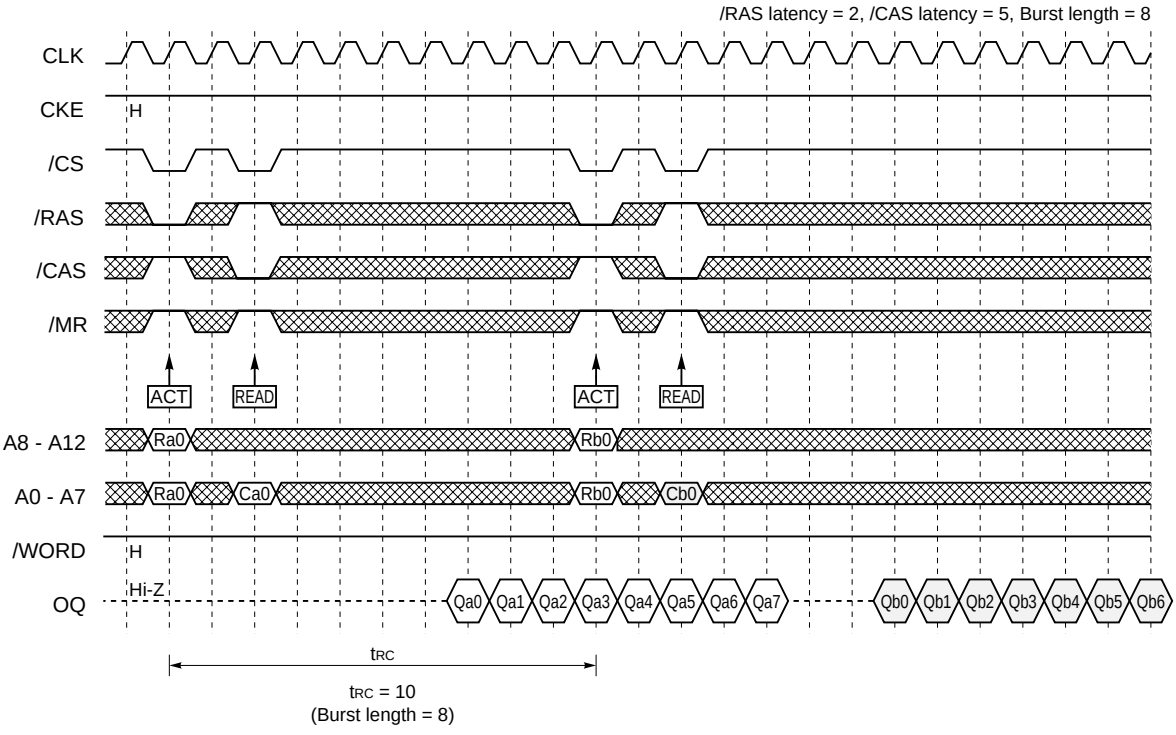
12.2.4 at 83 MHz (2-5-1-1-1-1-1-1)



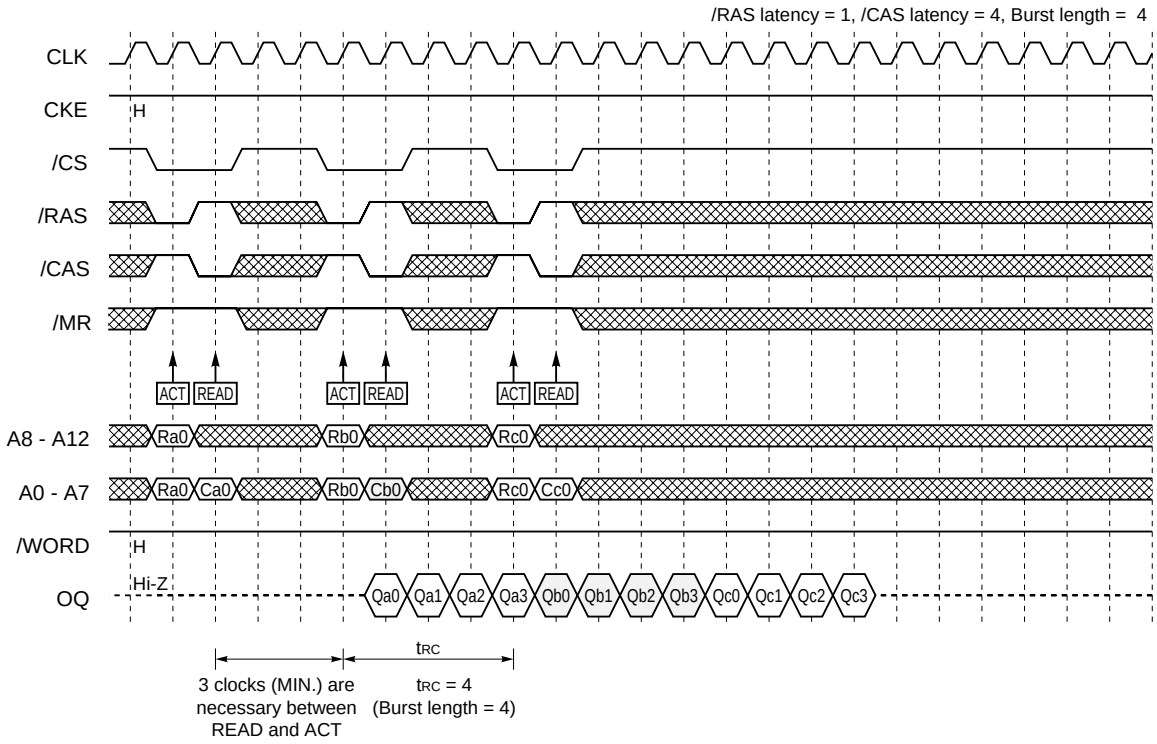
12.2.5 at 66 MHz (2-5-1-1-1)



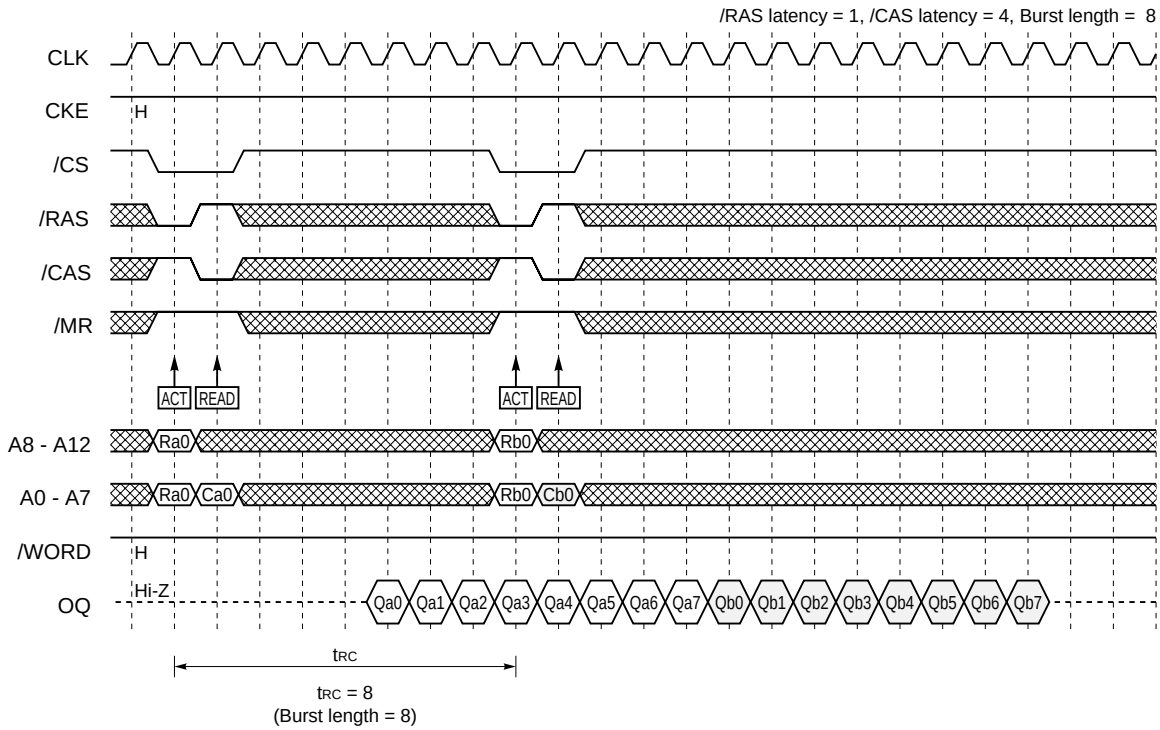
12.2.6 at 66 MHz (2-5-1-1-1-1-1-1-1)



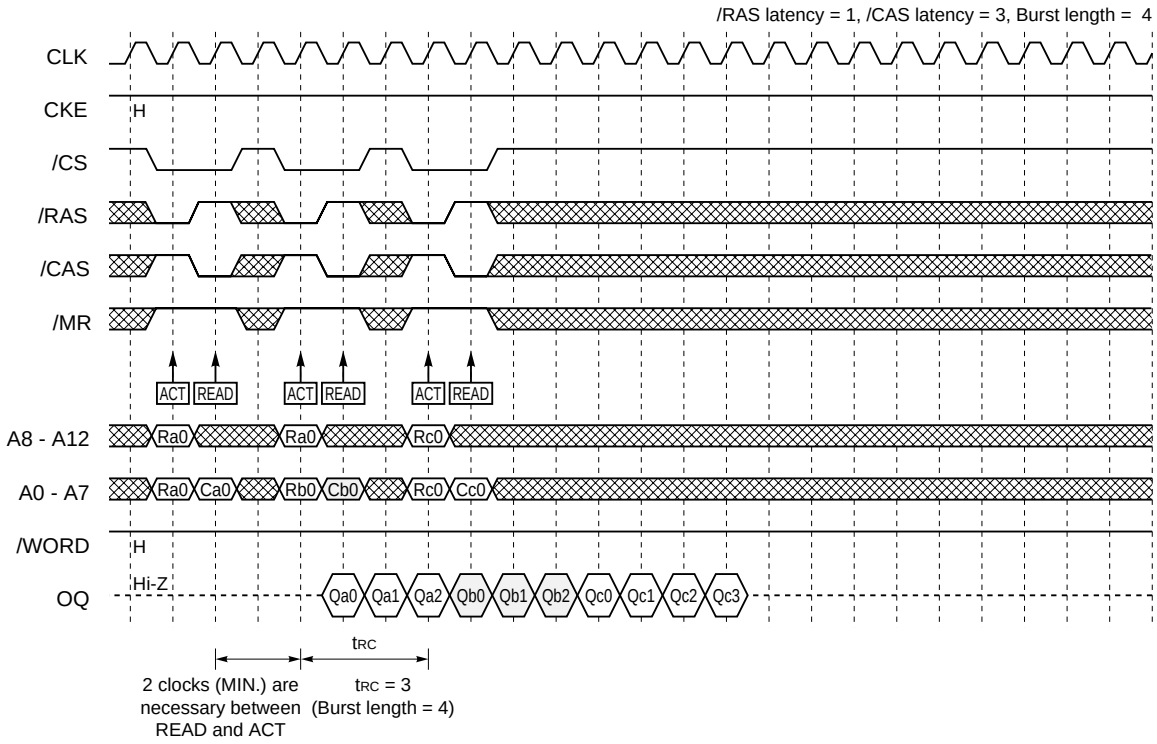
12.2.7 at 50 MHz (1-4-1-1-1)



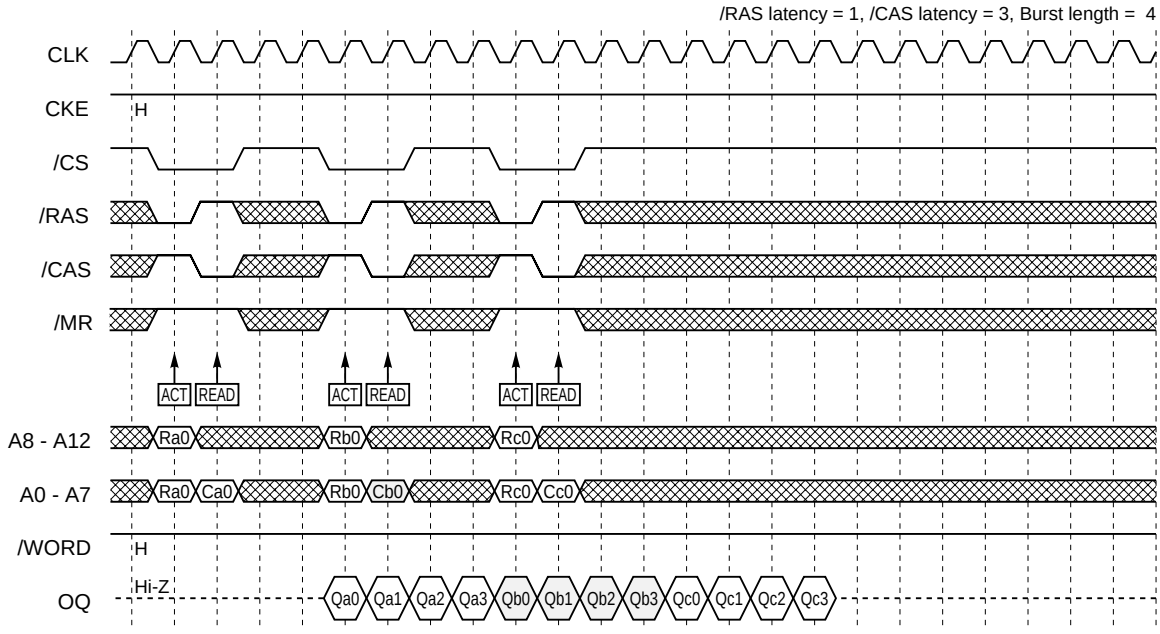
12.2.8 at 50 MHz (1-4-1-1-1-1-1-1-1)



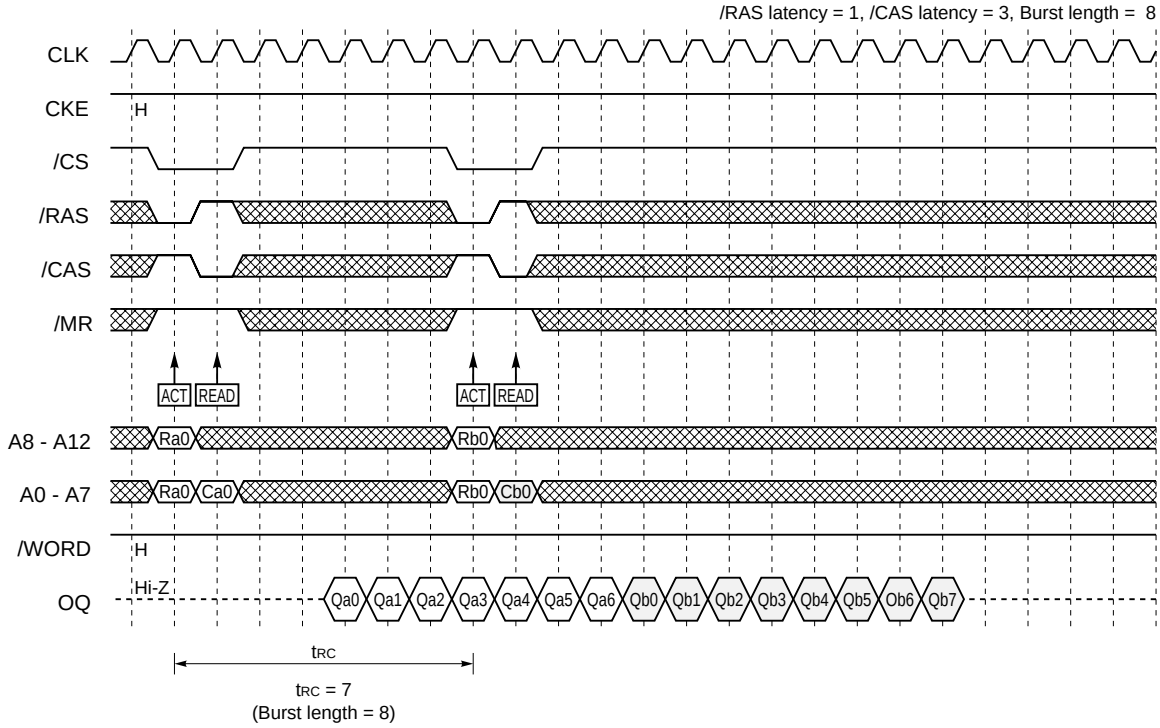
12.2.9 at 33 MHz (1-3-1-1-1)



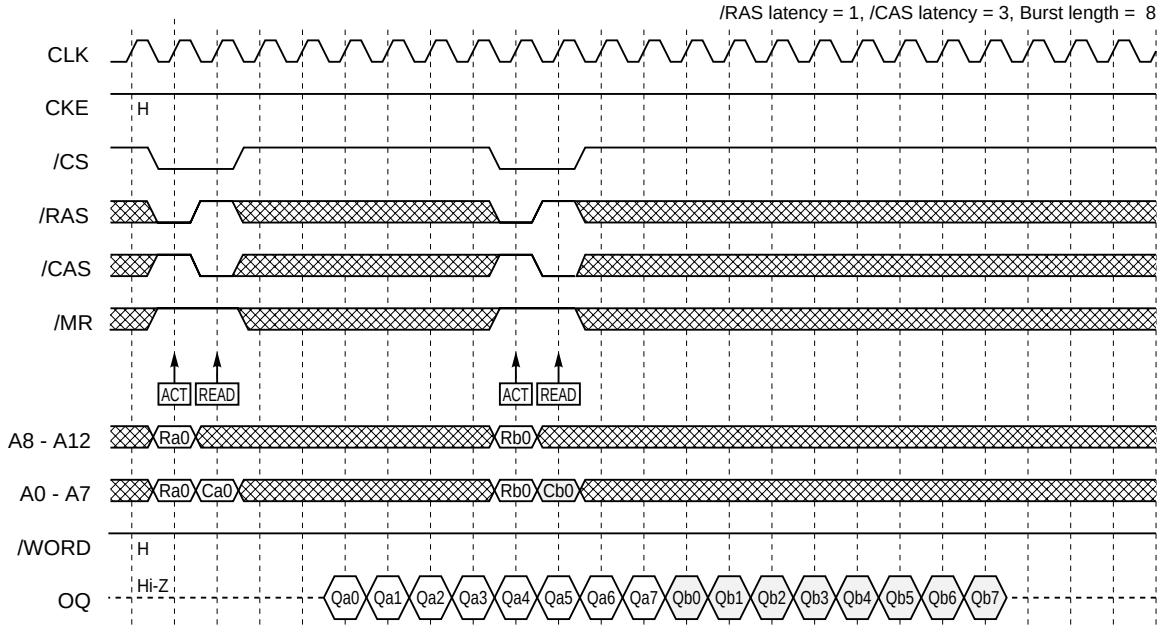
12.2.10 at 33 MHz (1-3-1-1-1)



12.2.11 at 33 MHz (1-3-1-1-1-1-1-1-1)

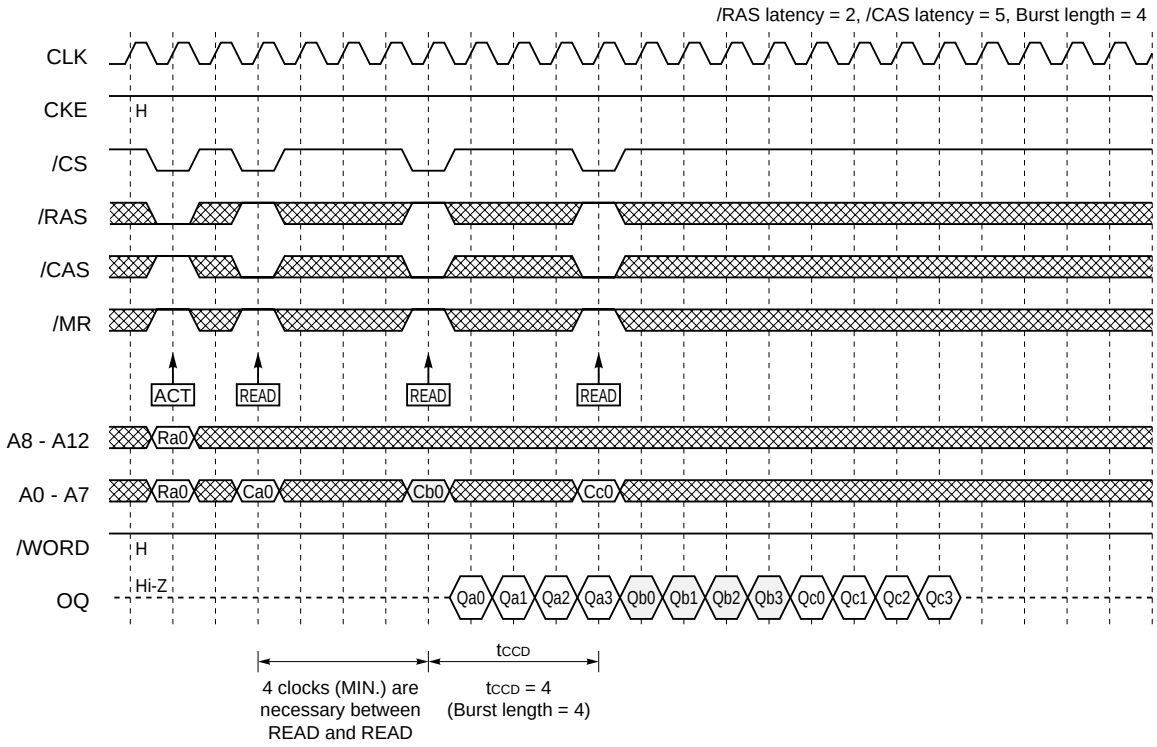


12.2.12 at 33 MHz (1-3-1-1-1-1-1-1-1)

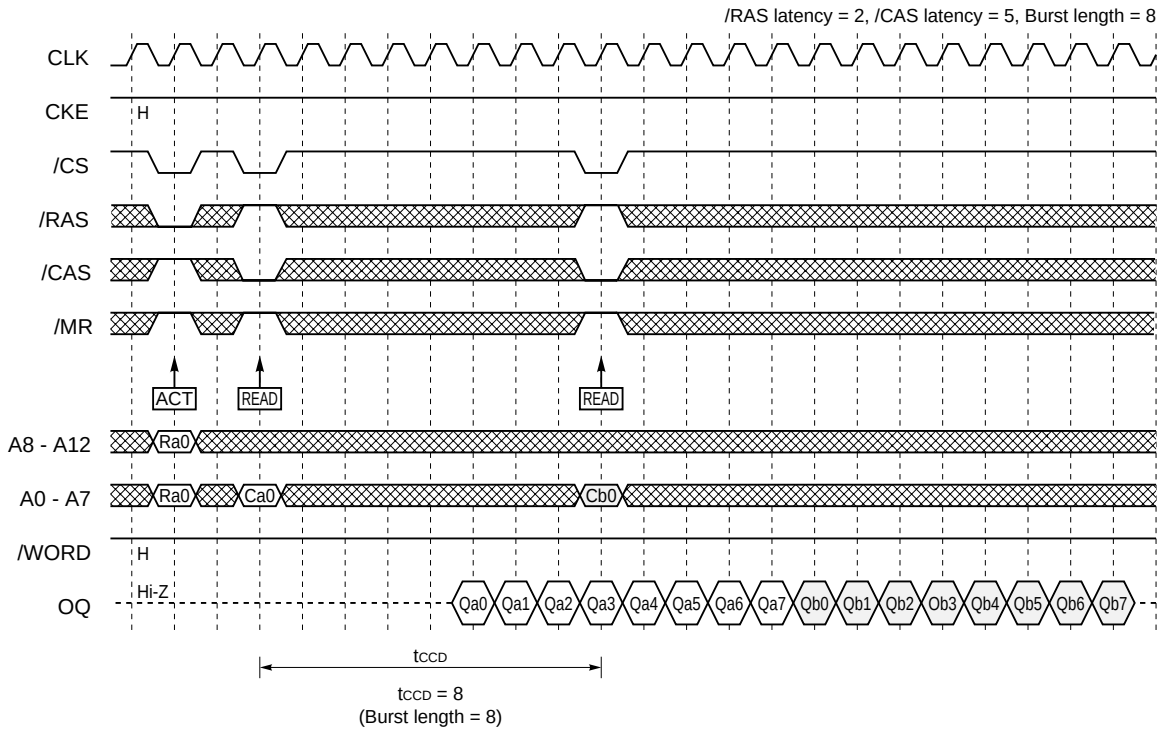


12.3 Random Column Read Timing

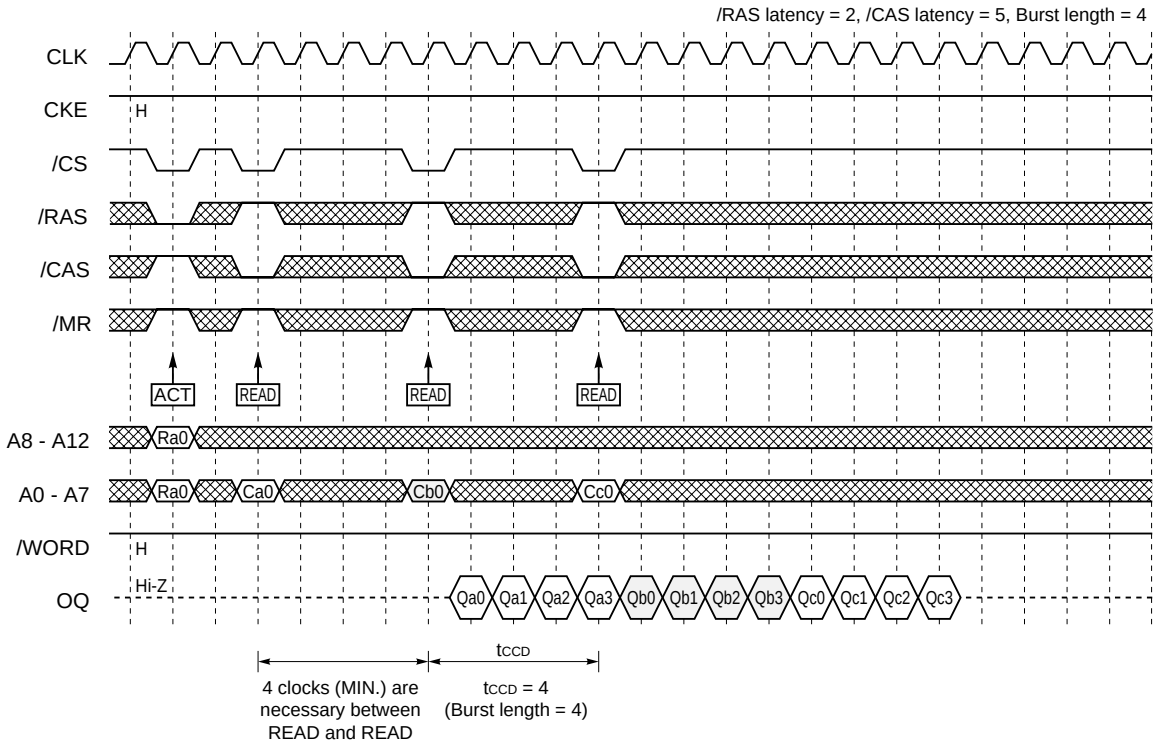
12.3.1 at 100 MHz (2-5-1-1-1)



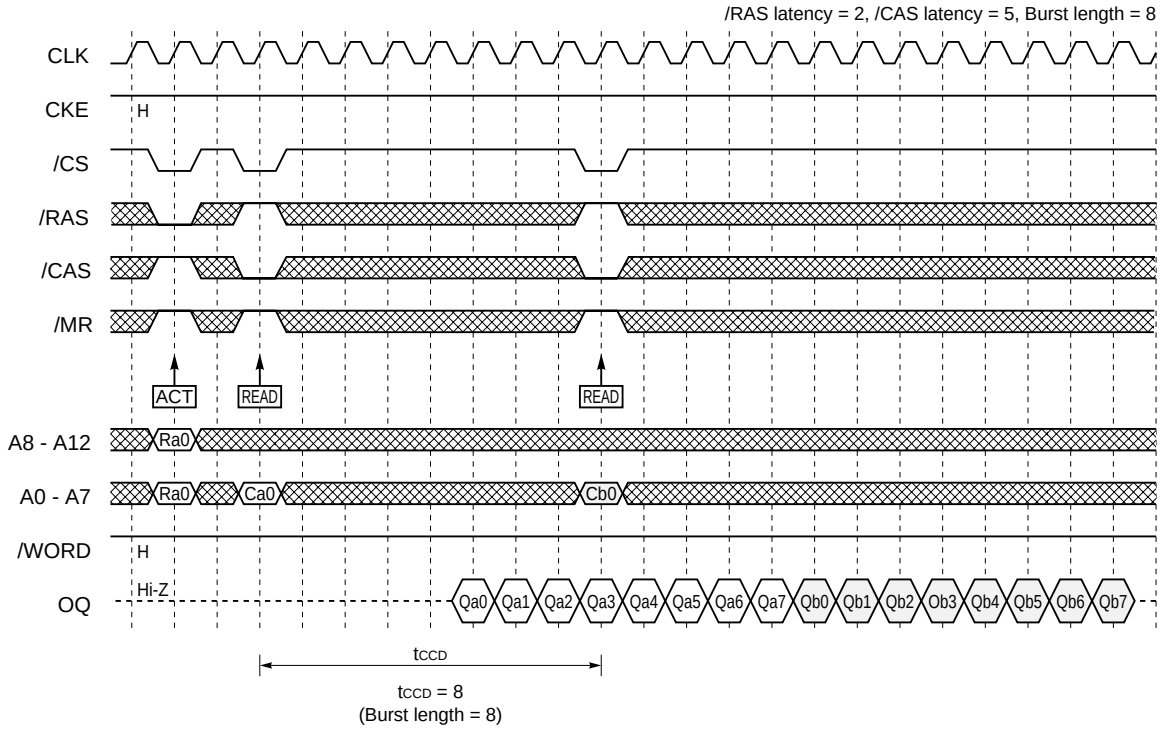
12.3.2 at 100 MHz (2-5-1-1-1-1-1-1)



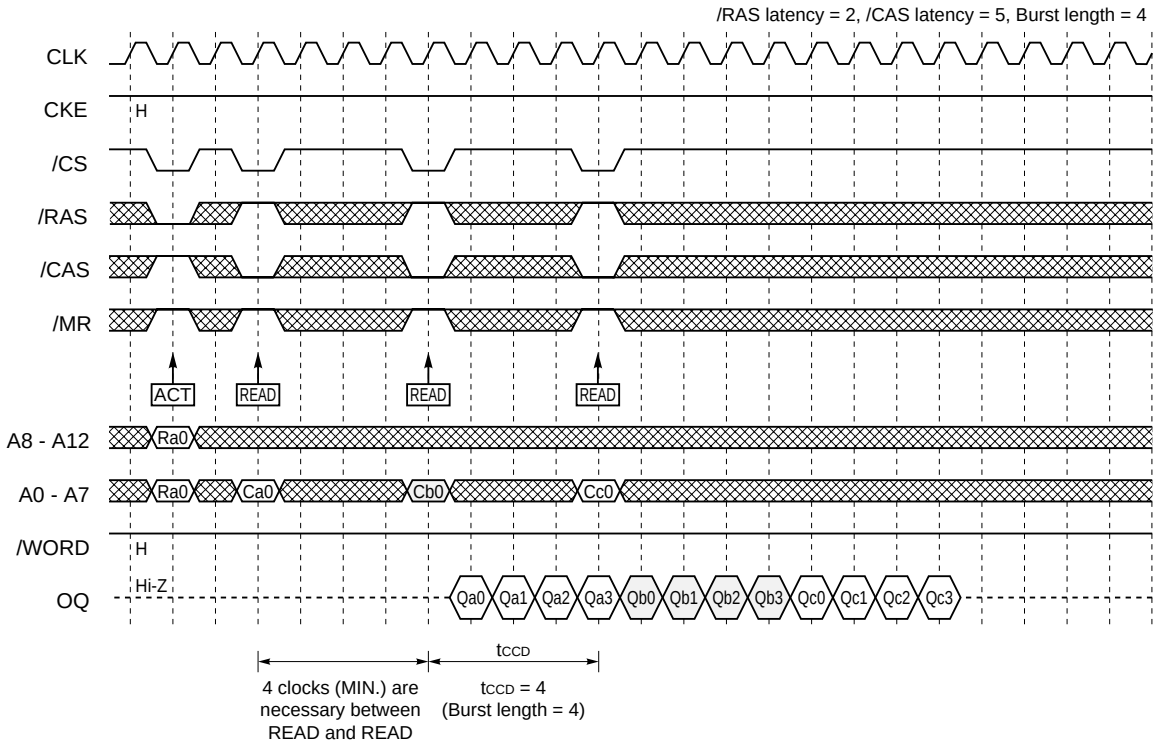
12.3.3 at 83 MHz (2-5-1-1-1)



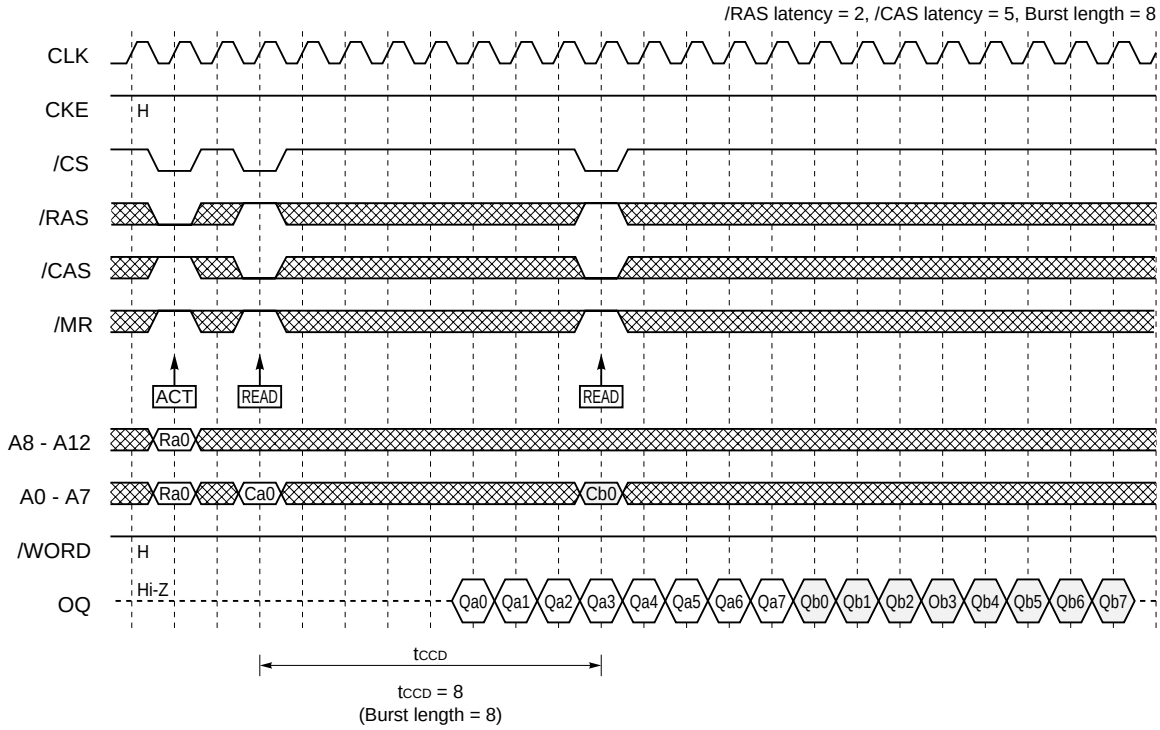
12.3.4 at 83 MHz (2-5-1-1-1-1-1-1-1)



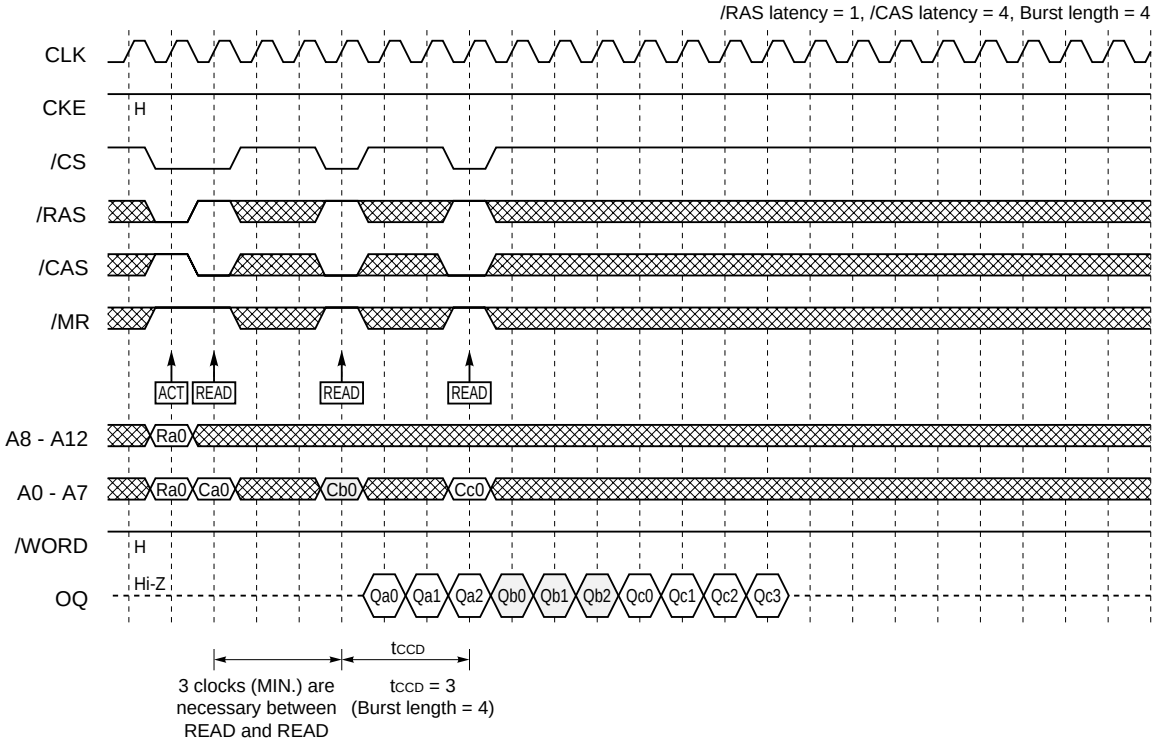
12.3.5 at 66 MHz (2-5-1-1-1)



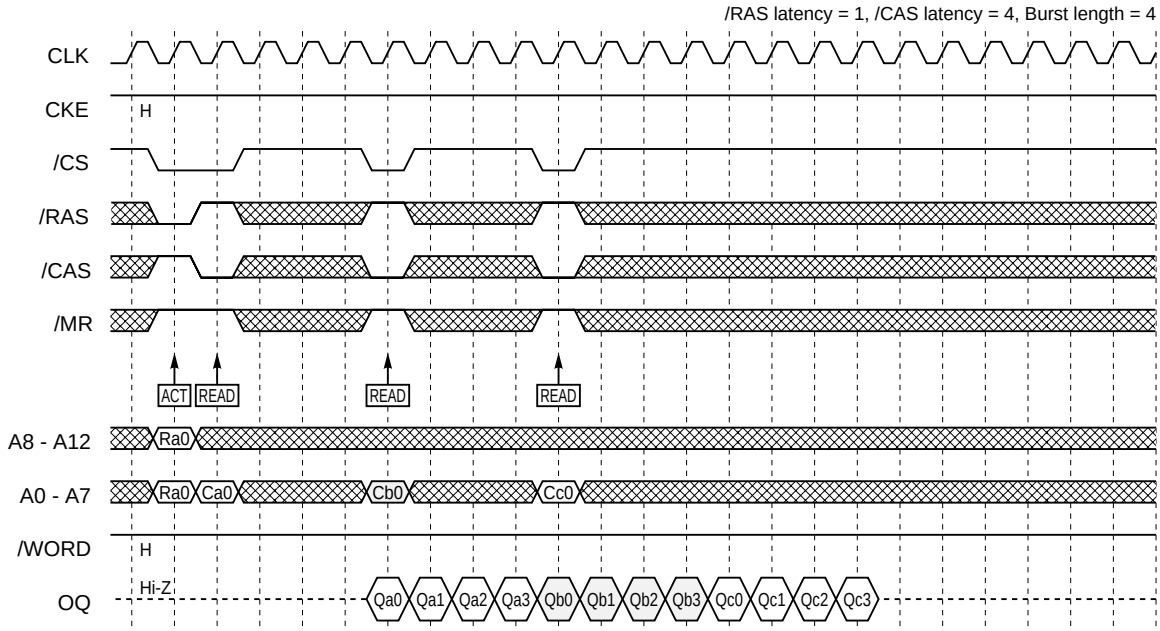
12.3.6 at 66 MHz (2-5-1-1-1-1-1-1-1)



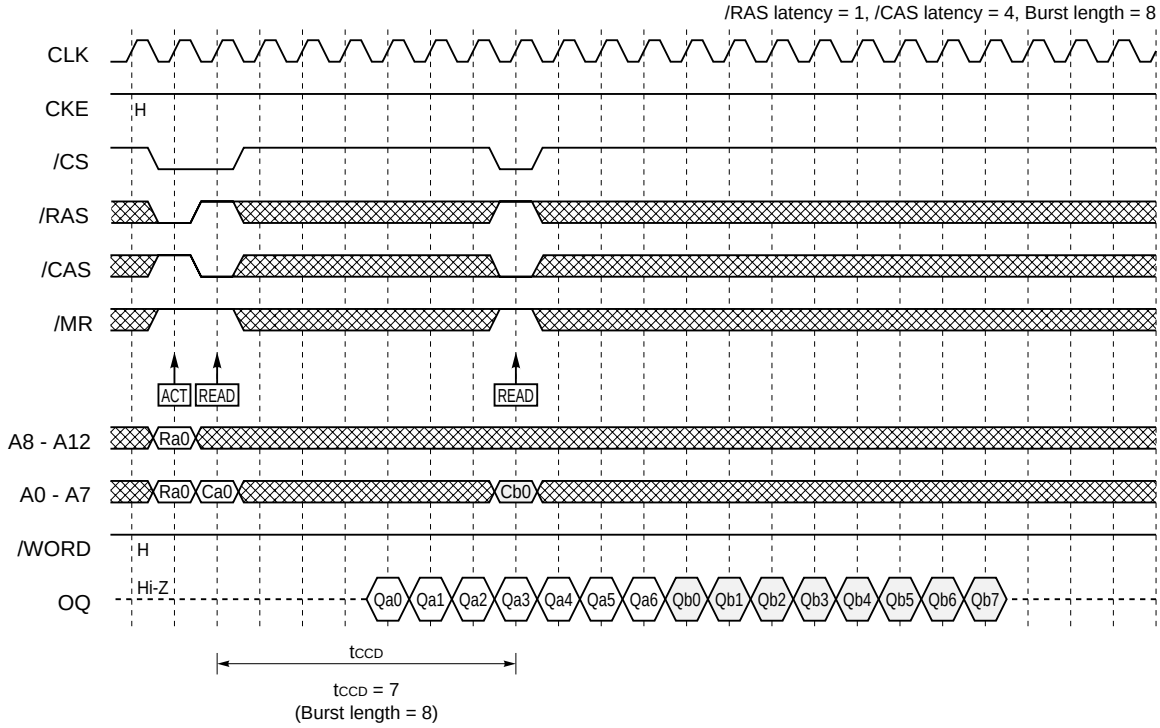
12.3.7 at 50 MHz (1-4-1-1-1)



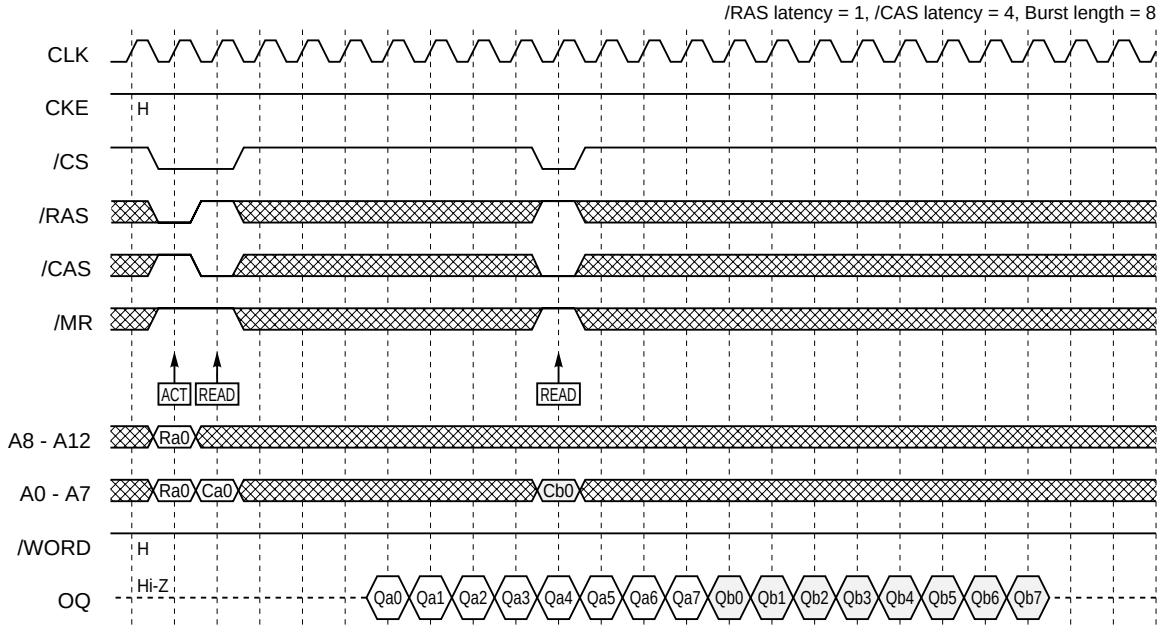
12.3.8 at 50 MHz (1-4-1-1-1)



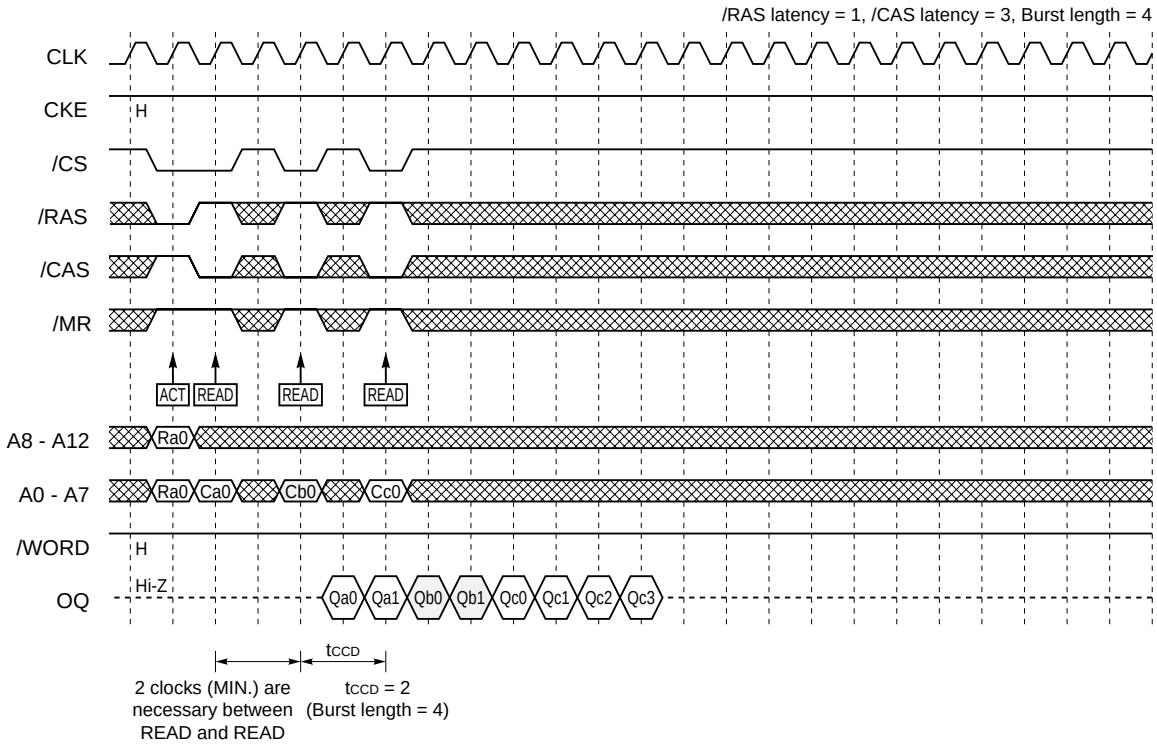
12.3.9 at 50 MHz (1-4-1-1-1-1-1-1-1)



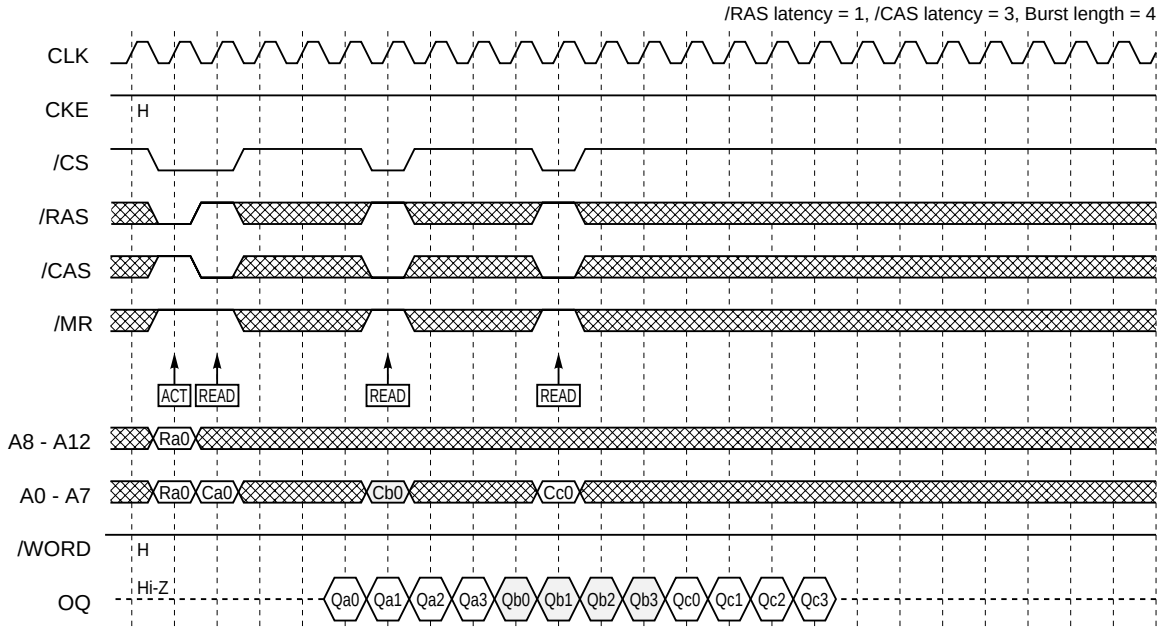
12.3.10 at 50 MHz (1-4-1-1-1-1-1-1-1)



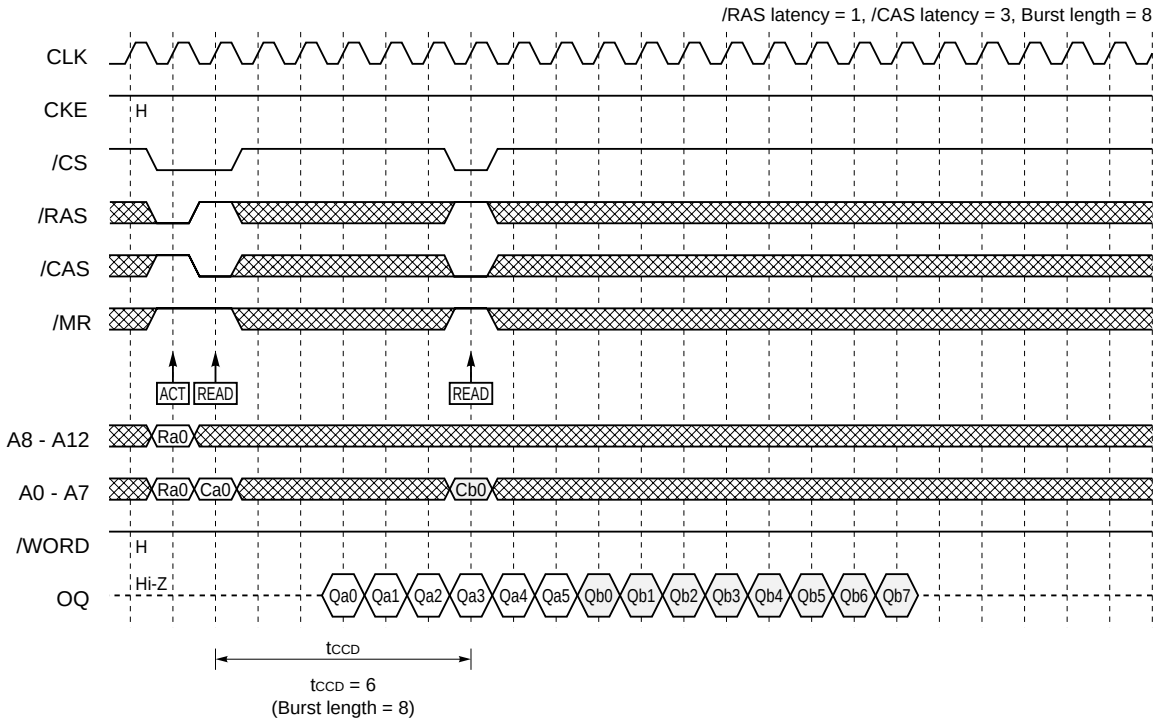
12.3.11 at 33 MHz (1-3-1-1-1)



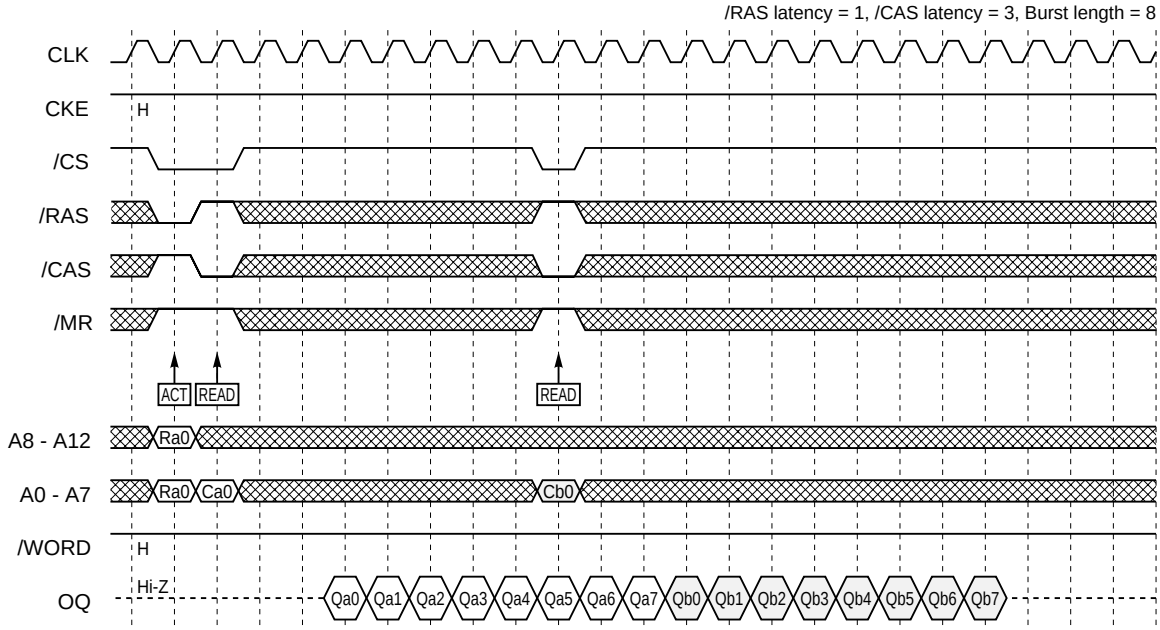
12.3.12 at 33 MHz (1-3-1-1-1)



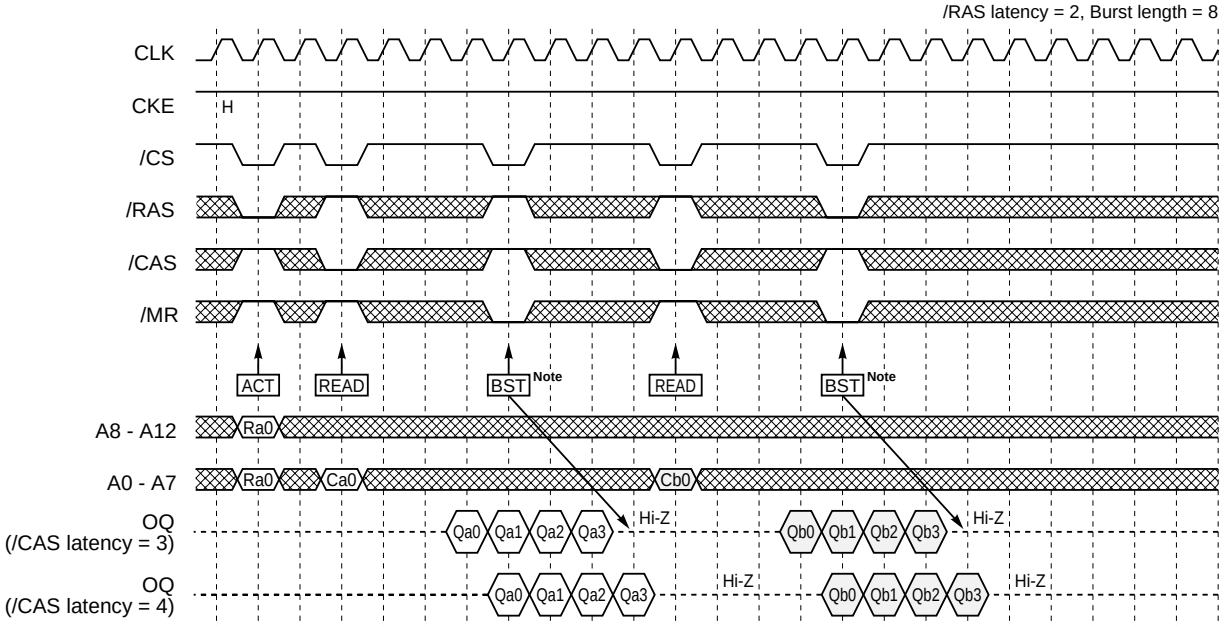
12.3.13 at 33 MHz (1-3-1-1-1-1-1-1-1)



12.3.14 at 33 MHz (1-3-1-1-1-1-1-1-1)

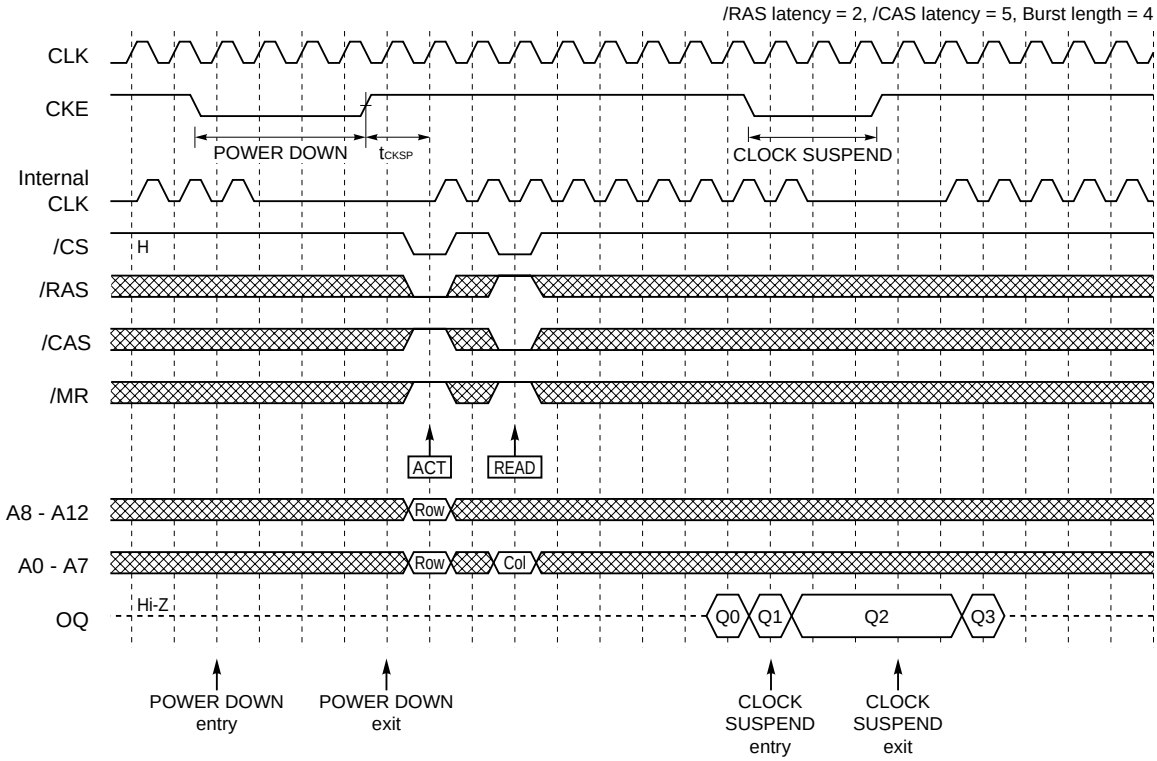


12.3.15 BURST STOP



Note Both standard and SDRAM-precharge-like types of the BURST STOP command can be used.

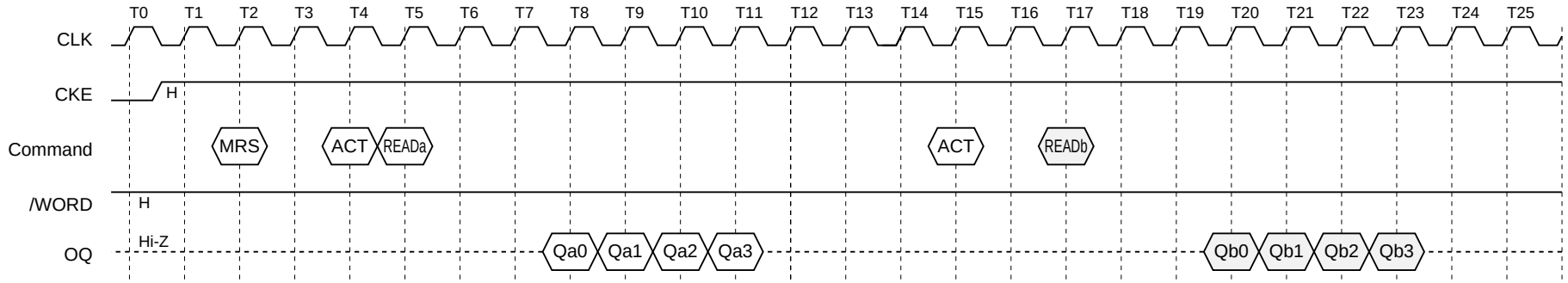
12.3.16 CLOCK SUSPEND and POWER DOWN



12.4 Command Combination Examples

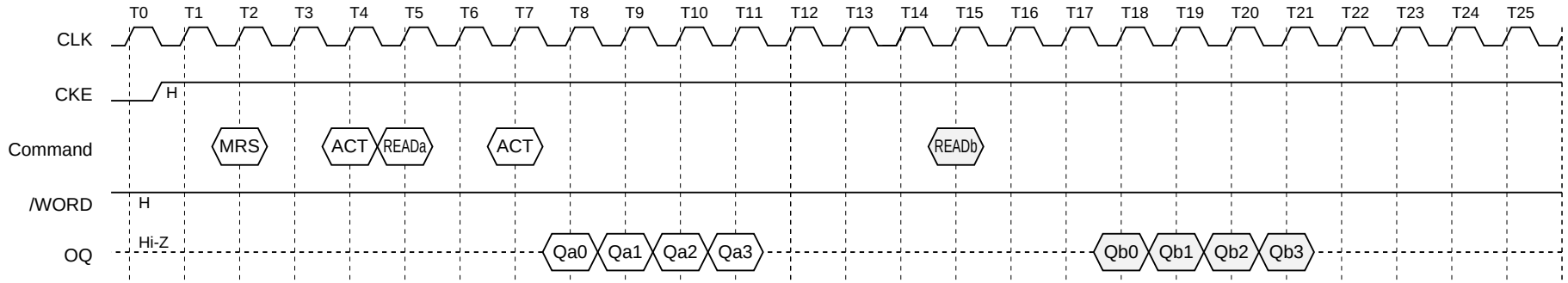
12.4.1 ROW ACTIVATE - READ (1)

/CAS latency = 3, Burst length = 4



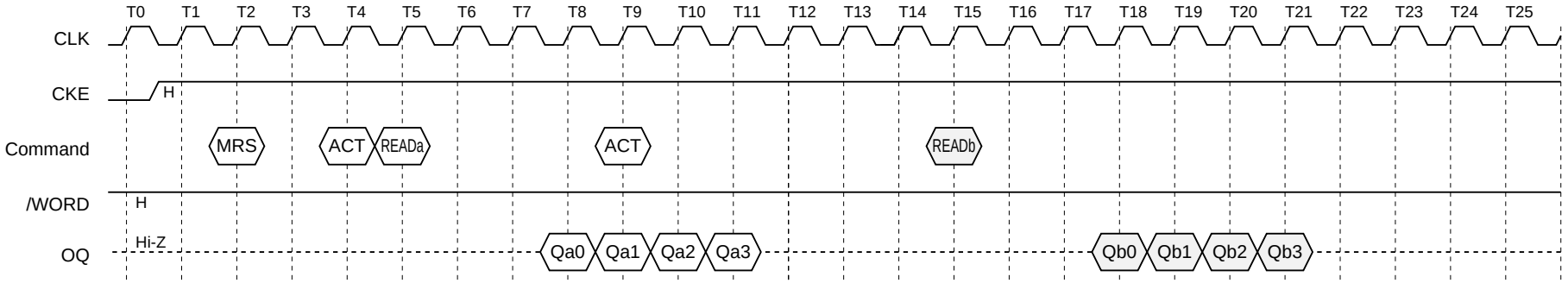
12.4.2 ROW ACTIVATE - READ (2)

/CAS latency = 3, Burst length = 4



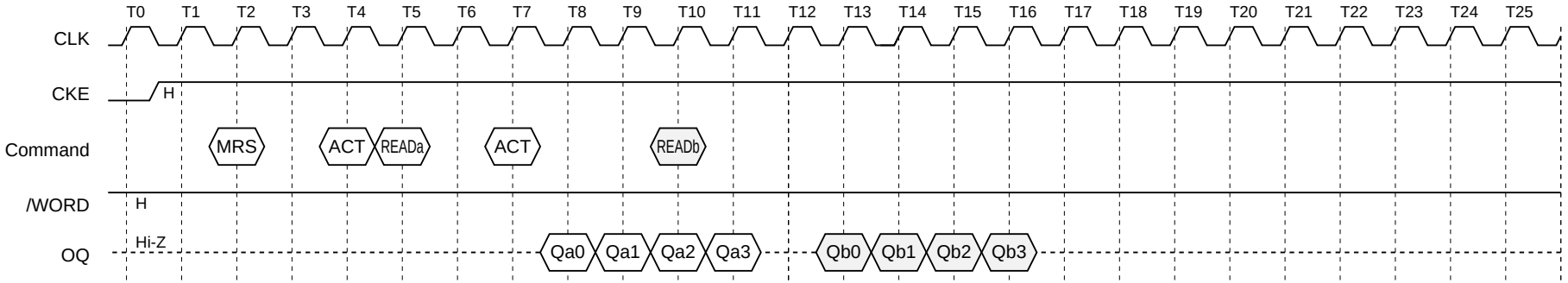
12.4.3 ROW ACTIVATE - READ (3)

/CAS latency = 3, Burst length = 4



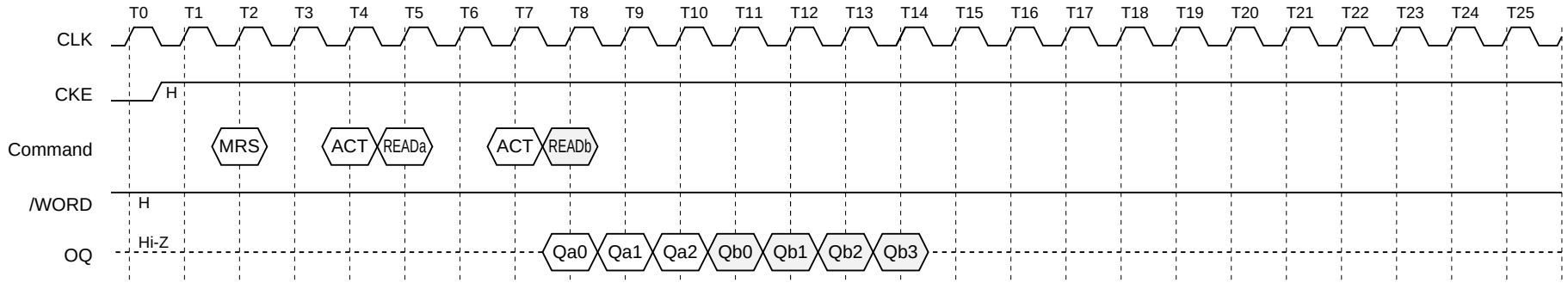
12.4.4 ROW ACTIVATE - READ (4)

/CAS latency = 3, Burst length = 4



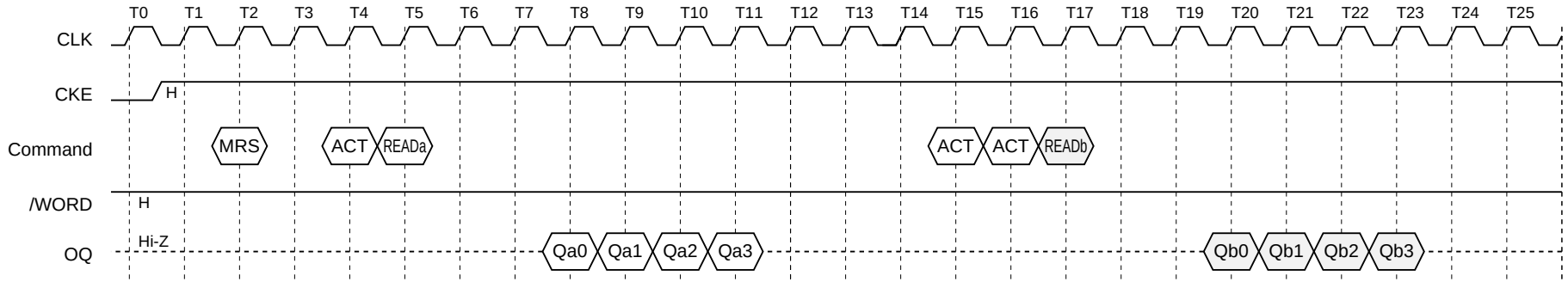
12.4.5 ROW ACTIVATE - READ (5)

/CAS latency = 3, Burst length = 4



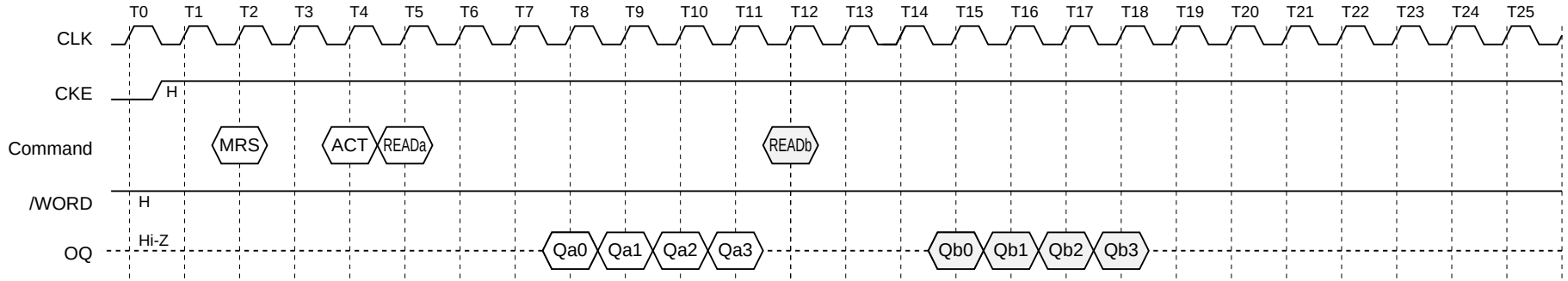
12.4.6 ROW ACTIVATE - ROW ACTIVATE

/CAS latency = 3, Burst length = 4



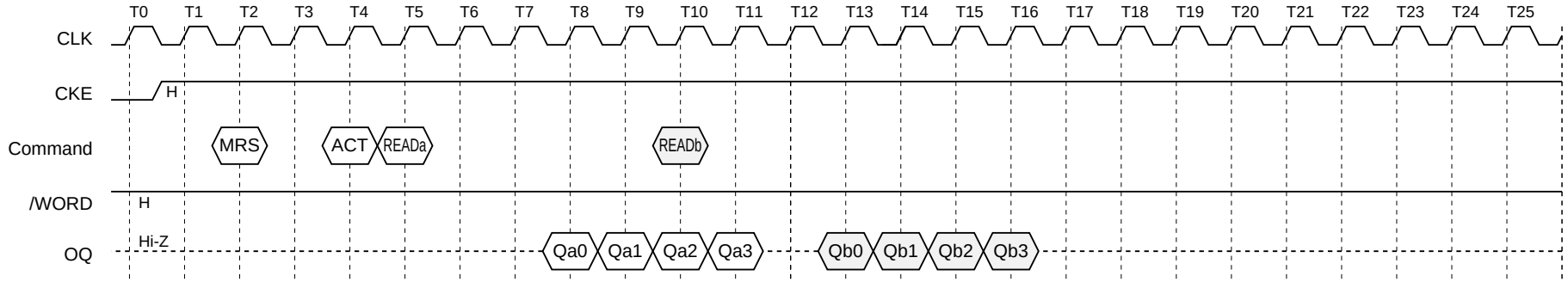
12.4.7 READ - READ (1)

/CAS latency = 3, Burst length = 4



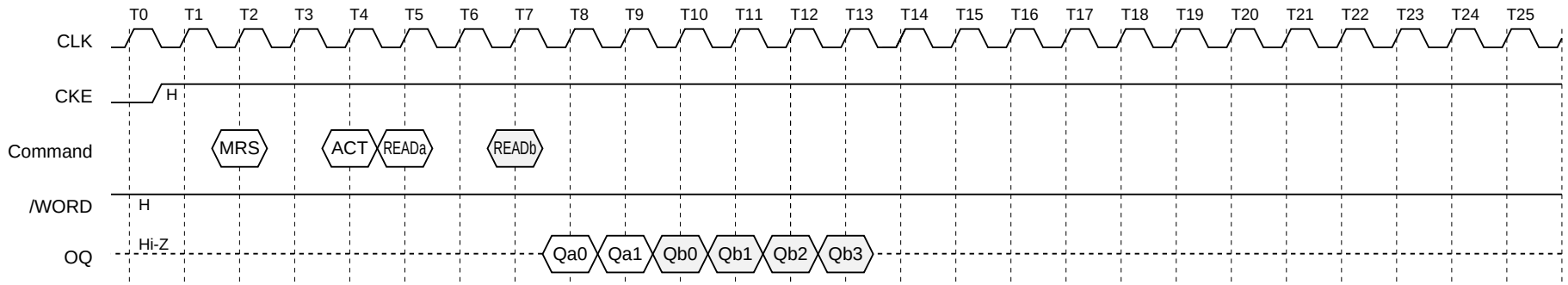
12.4.8 READ - READ (2)

/CAS latency = 3, Burst length = 4



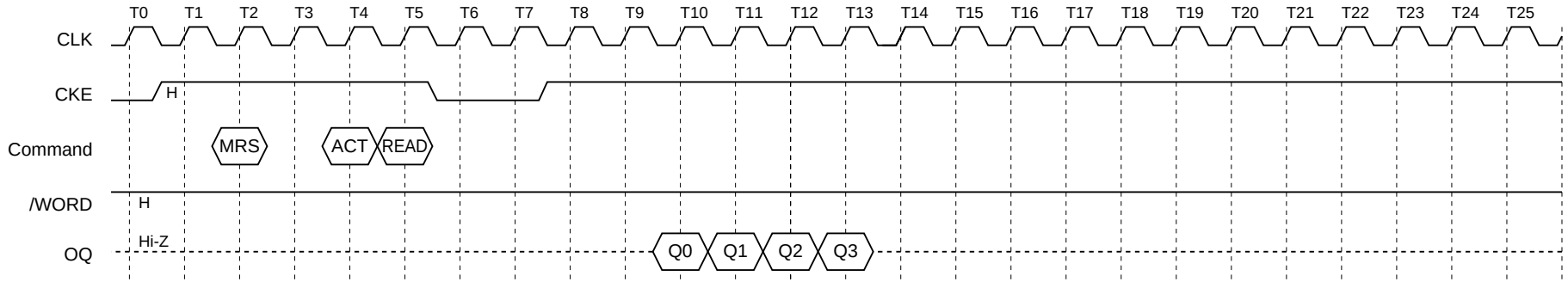
12.4.9 READ - READ (3)

/CAS latency = 3, Burst length = 4



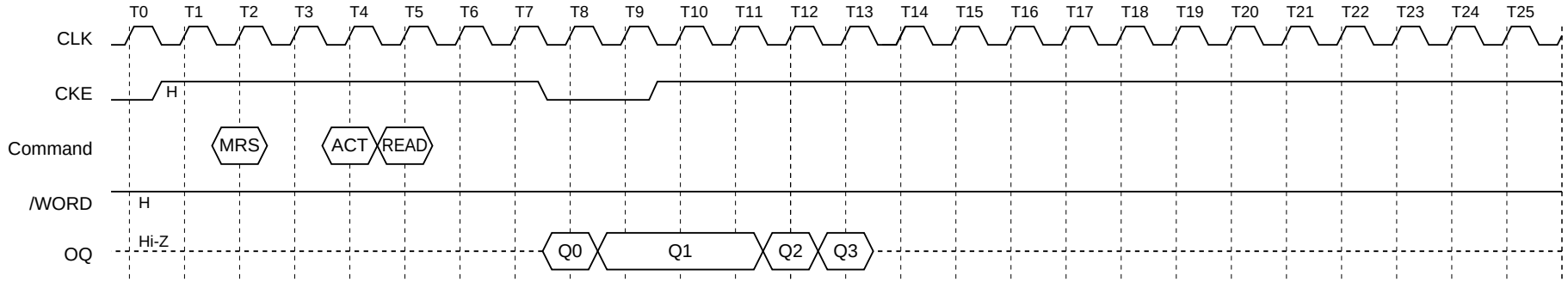
12.4.10 READ SUSPEND (1)

/CAS latency = 3, Burst length = 4



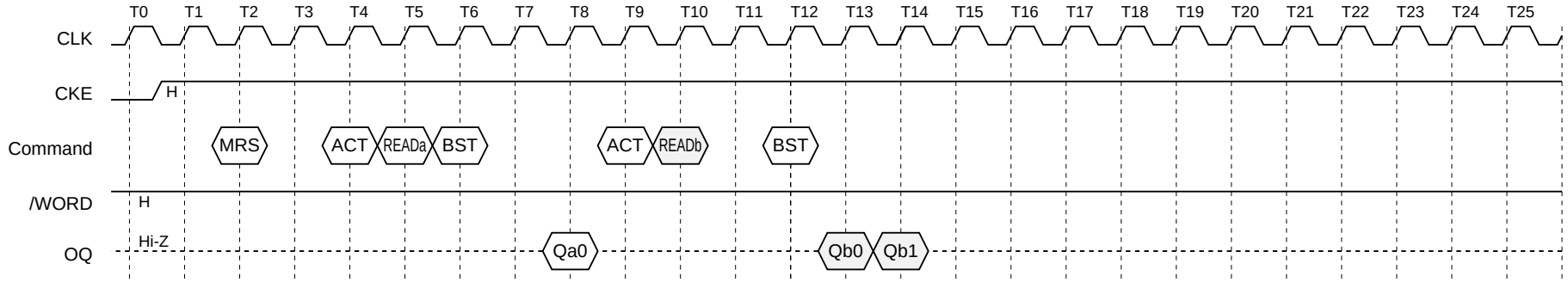
12.4.11 READ SUSPEND (2)

/CAS latency = 3, Burst length = 4



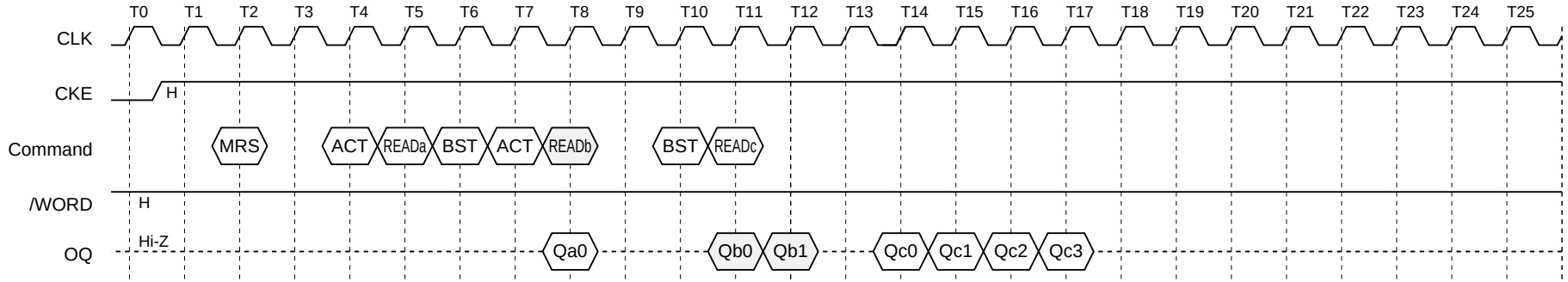
12.4.12 BURST STOP (1)

/CAS latency = 3, Burst length = 4



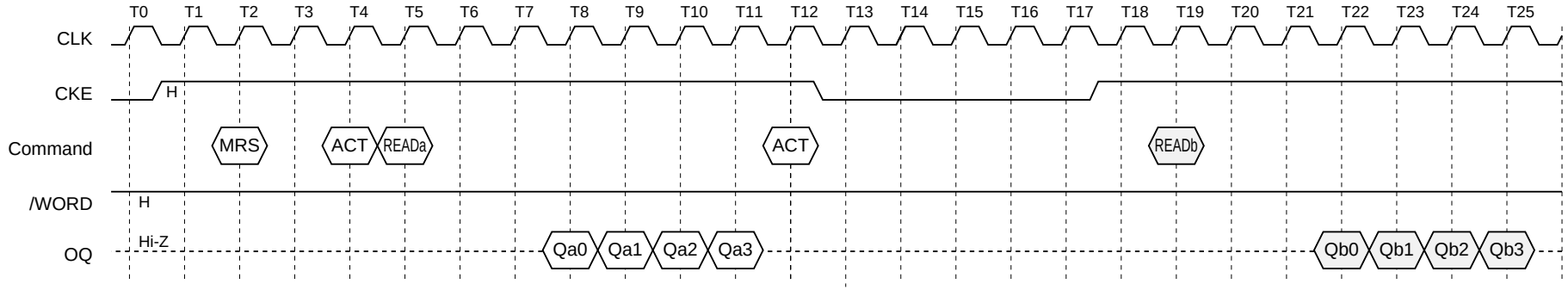
12.4.13 BURST STOP (2)

/CAS latency = 3, Burst length = 4



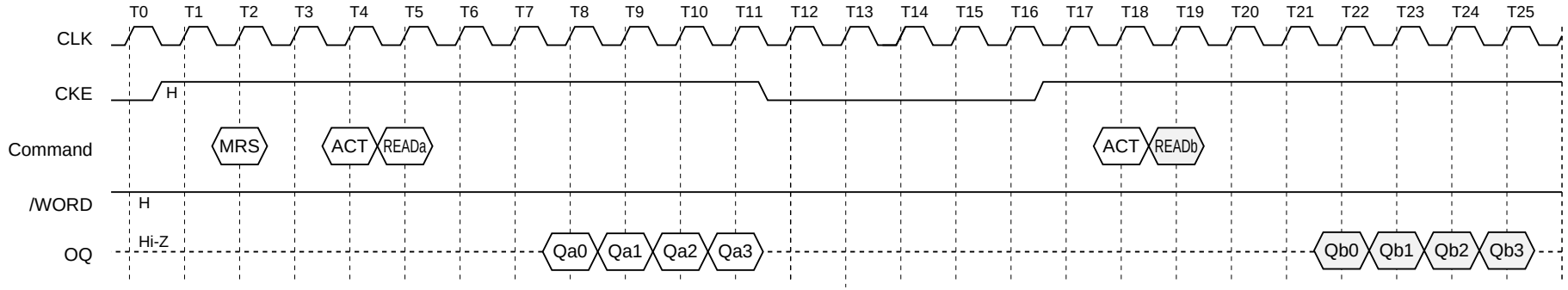
12.4.14 CLOCK SUSPEND

/CAS latency = 3, Burst length = 4



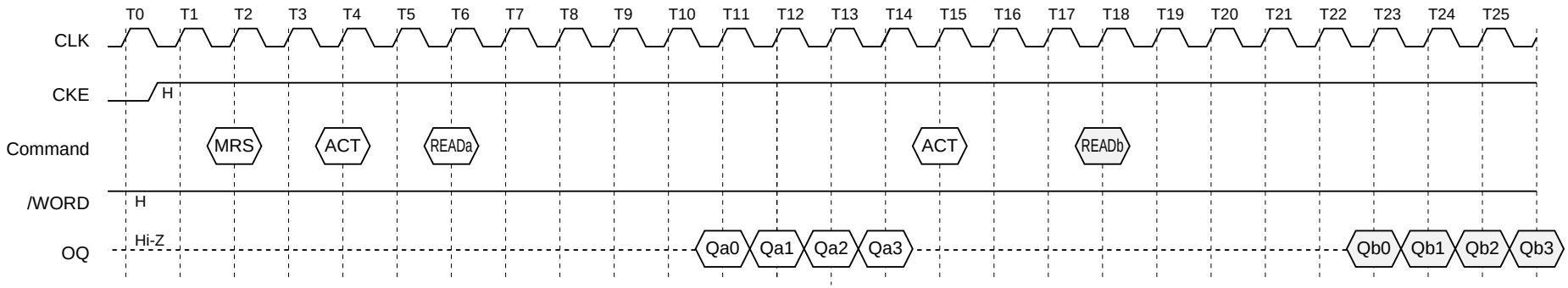
12.4.15 POWER DOWN

/CAS latency = 3, Burst length = 4



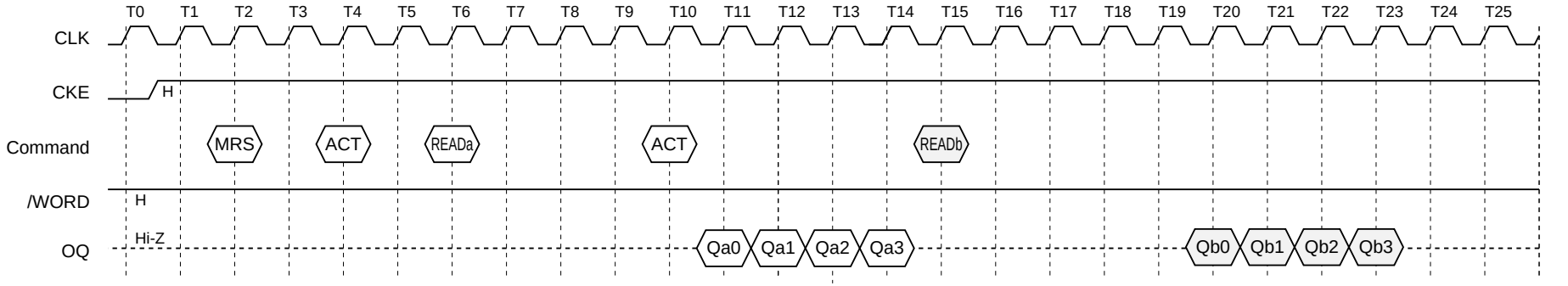
12.4.16 ROW ACTIVATE - READ (1)

/CAS latency = 5, Burst length = 4



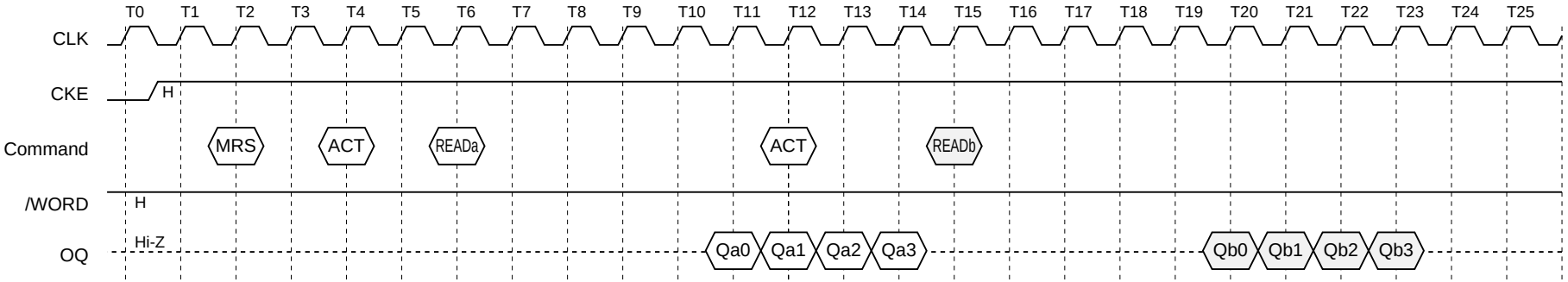
12.4.17 ROW ACTIVATE - READ (2)

/CAS latency = 5, Burst length = 4



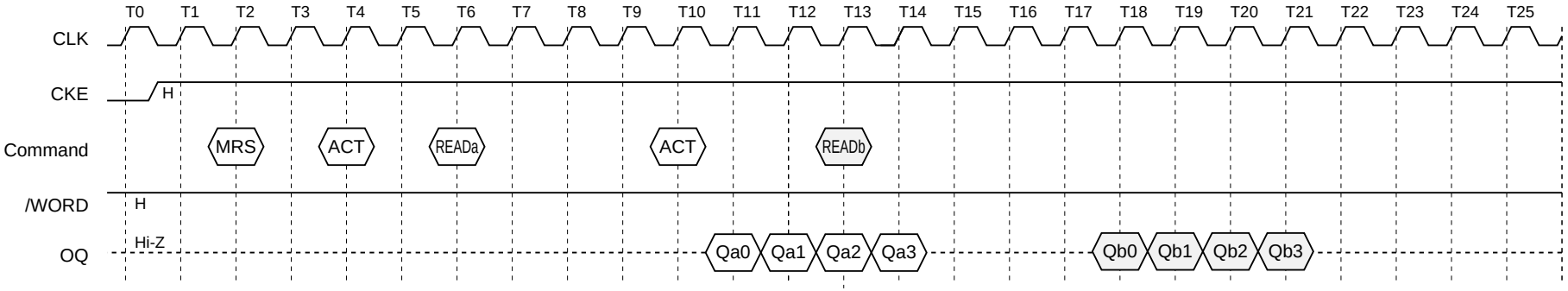
12.4.18 ROW ACTIVATE - READ (3)

/CAS latency = 5, Burst length = 4



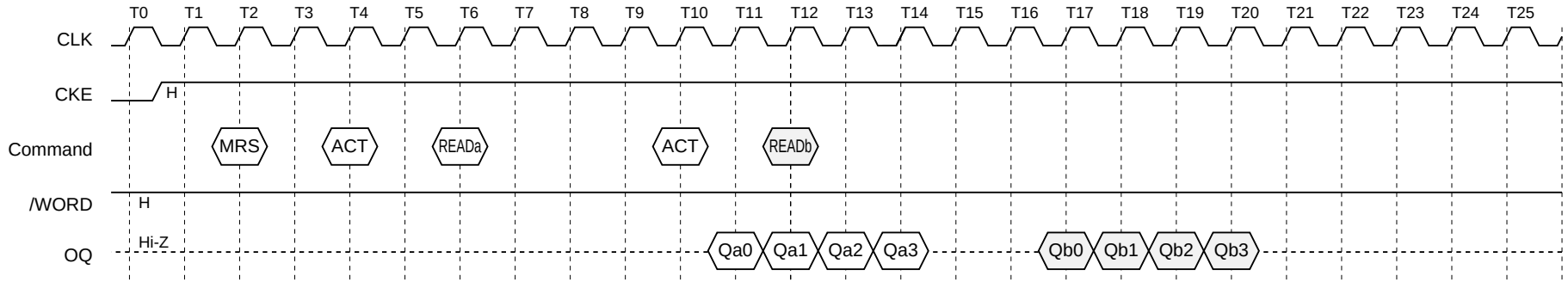
12.4.19 ROW ACTIVATE - READ (4)

/CAS latency = 5, Burst length = 4



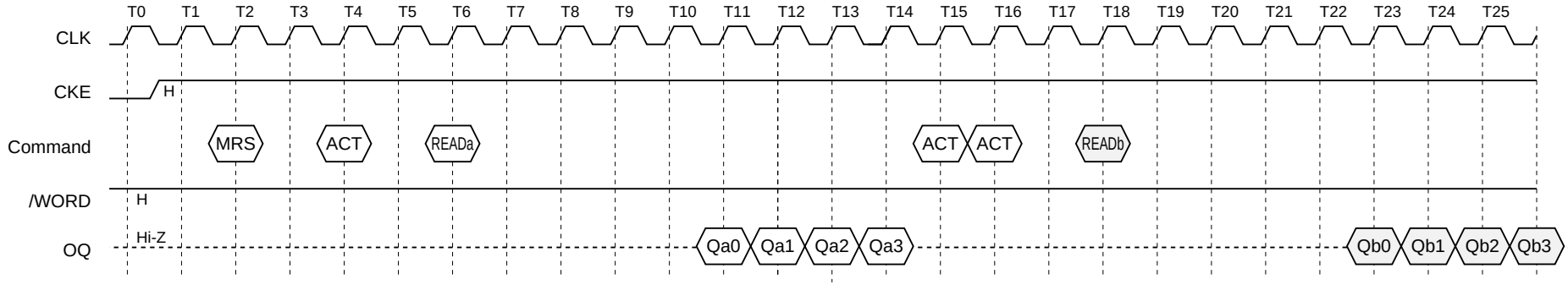
12.4.20 ROW ACTIVATE - READ (5)

/CAS latency = 5, Burst length = 4



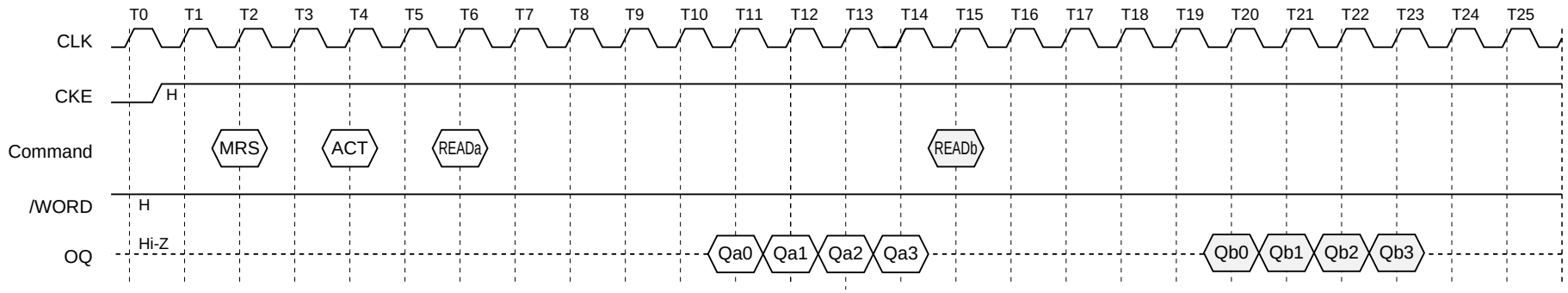
12.4.21 ROW ACTIVATE - ROW ACTIVATE

/CAS latency = 5, Burst length = 4



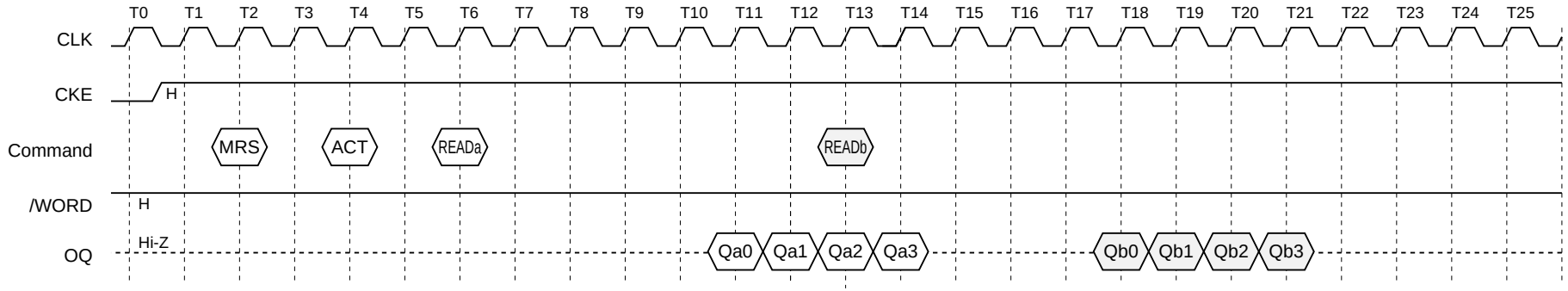
12.4.22 READ - READ (1)

/CAS latency = 5, Burst length = 4

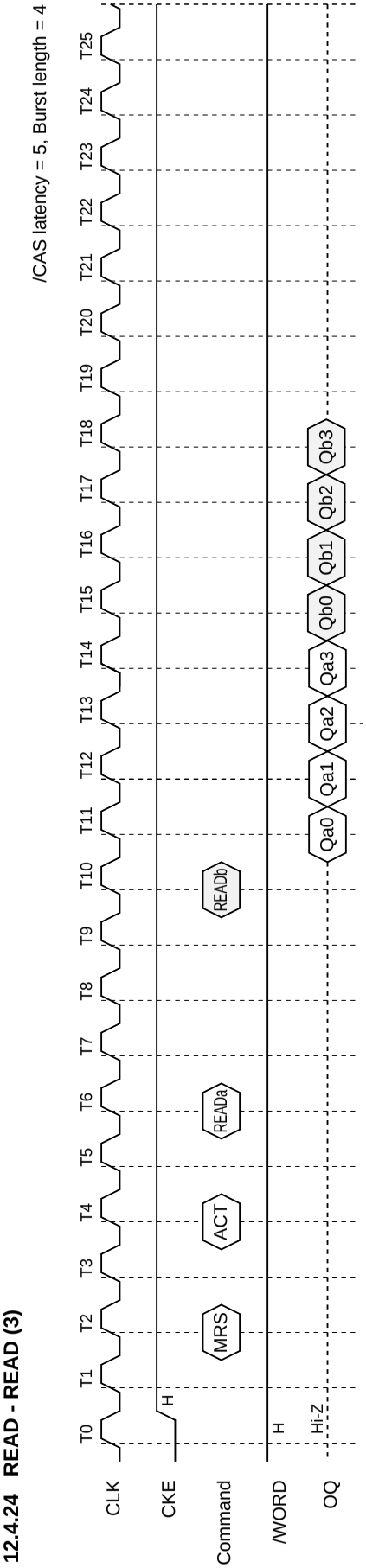


12.4.23 READ - READ (2)

/CAS latency = 5, Burst length = 4

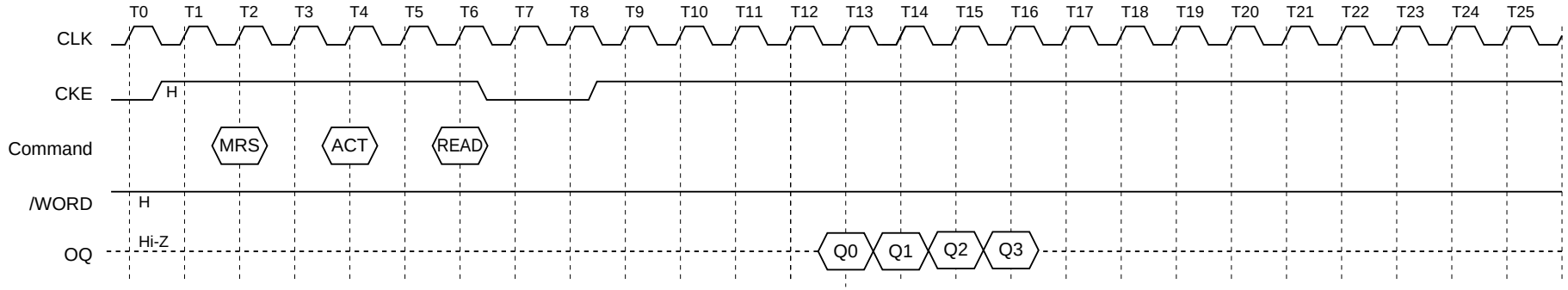


12.4.24 READ - READ (3)



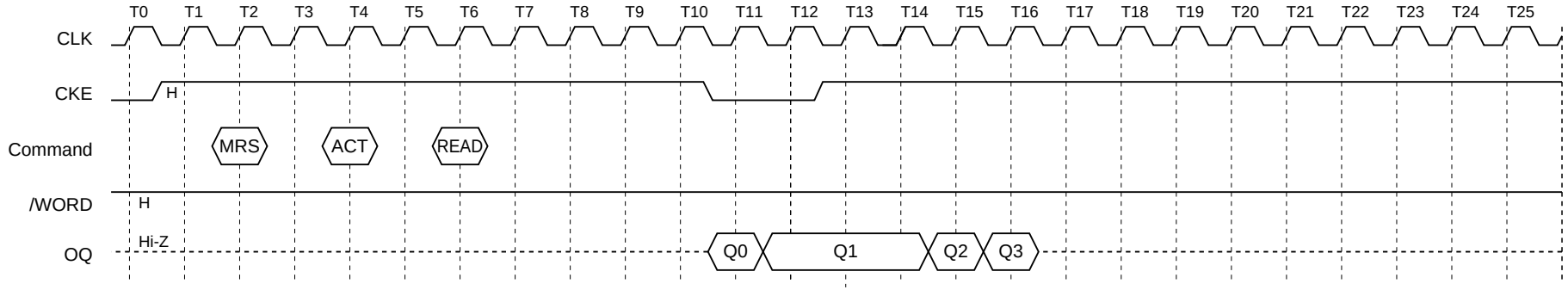
12.4.25 READ SUSPEND (1)

/CAS latency = 5, Burst length = 4



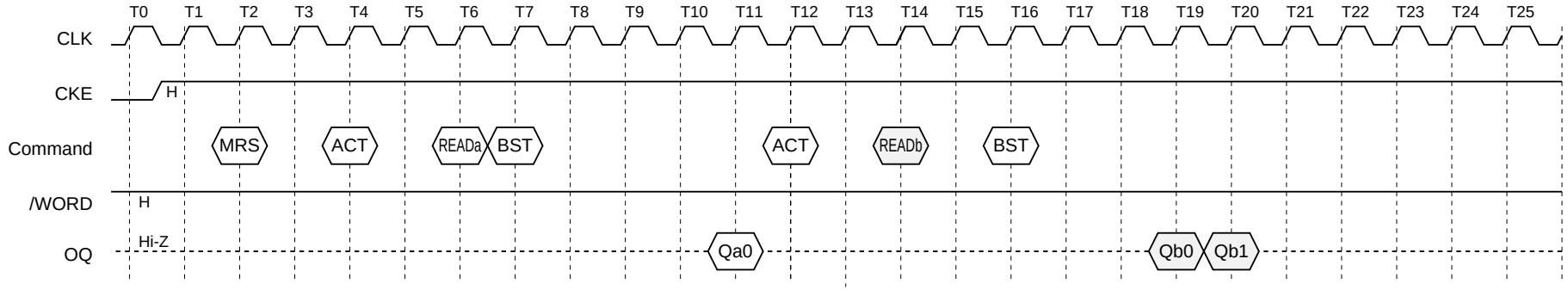
12.4.26 READ SUSPEND (2)

/CAS latency = 5, Burst length = 4



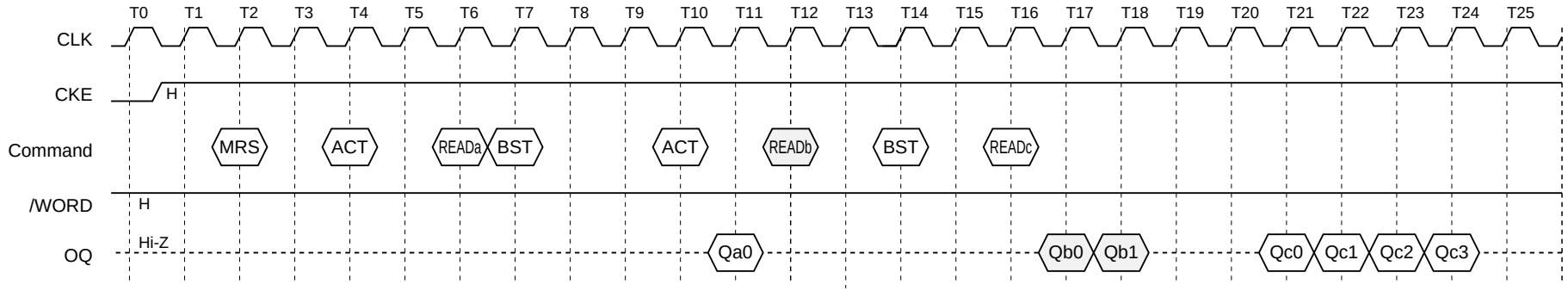
12.4.27 BURST STOP (1)

/CAS latency = 5, Burst length = 4



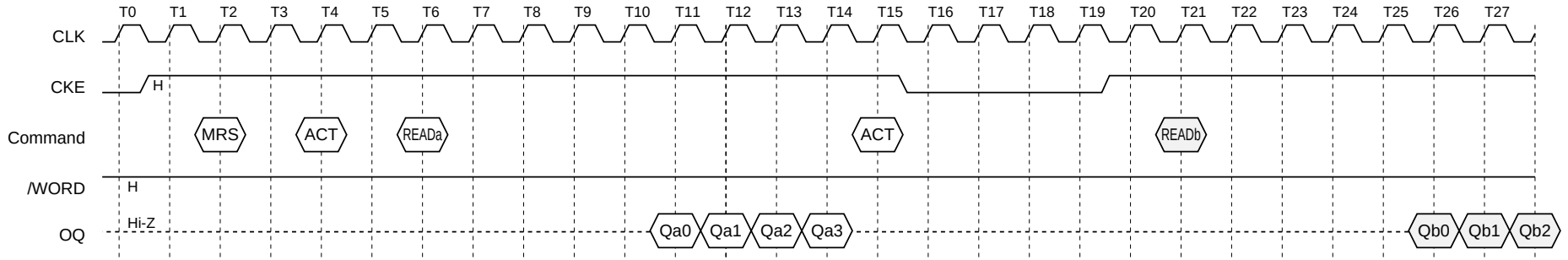
12.4.28 BURST STOP (2)

/CAS latency = 5, Burst length = 4



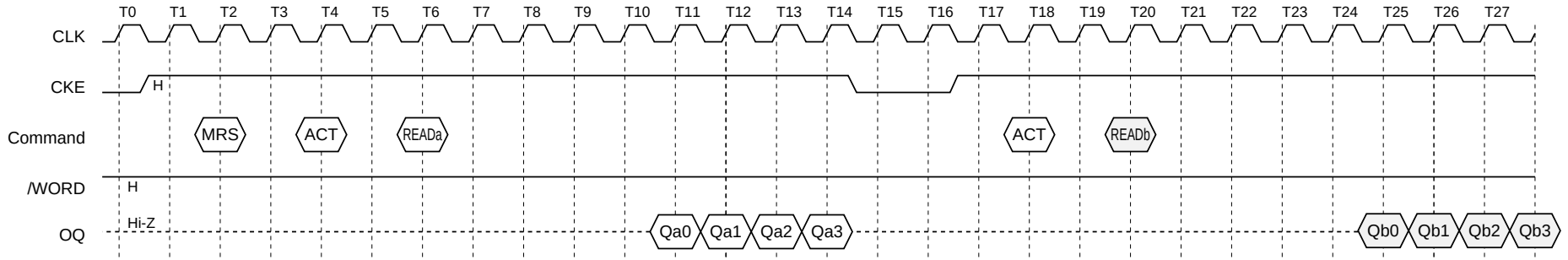
12.4.29 CLOCK SUSPEND

/CAS latency = 5, Burst length = 4



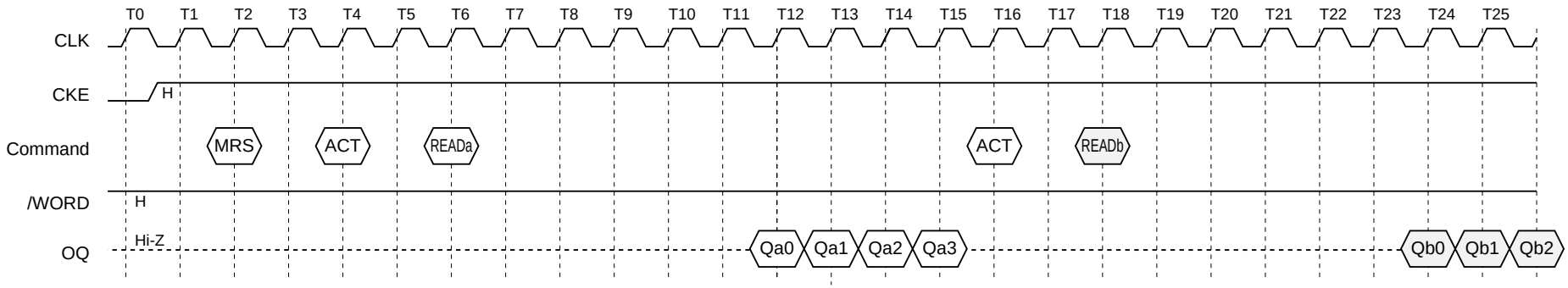
12.4.30 POWER DOWN

/CAS latency = 5, Burst length = 4



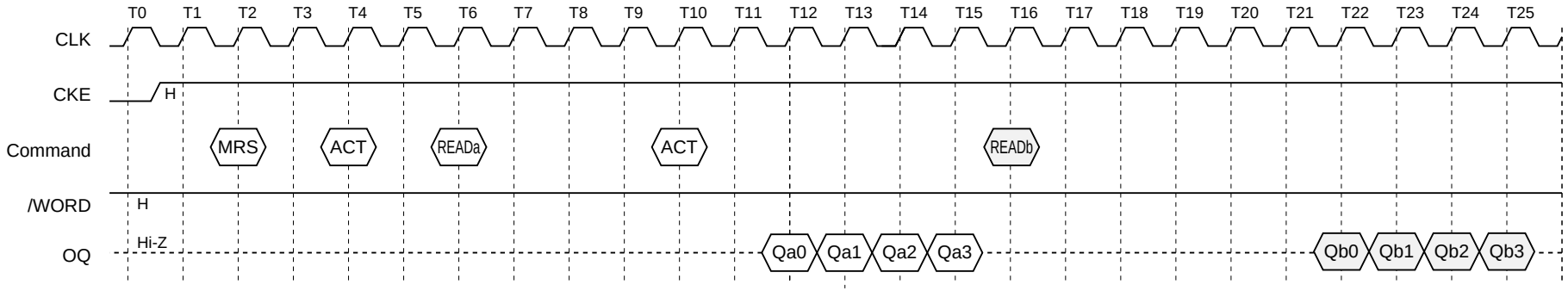
12.4.31 ROW ACTIVATE - READ (1)

/CAS latency = 6, Burst length = 4



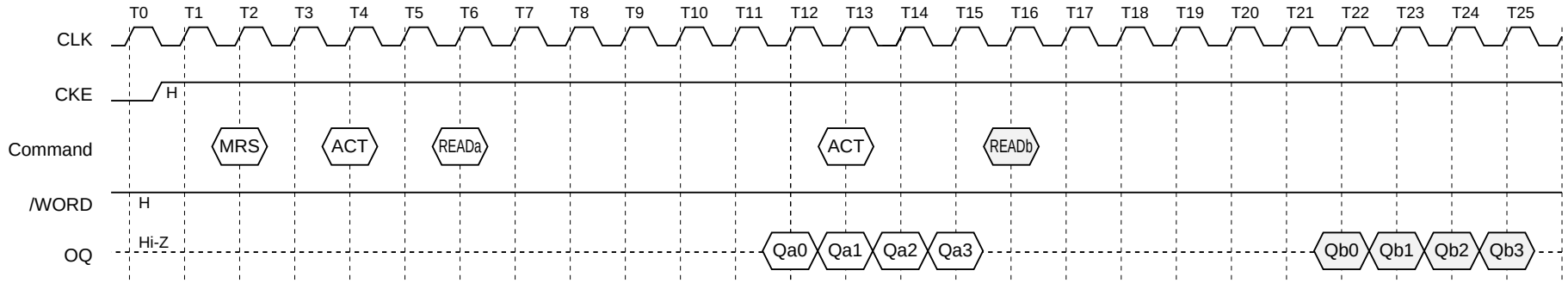
12.4.32 ROW ACTIVATE - READ (2)

/CAS latency = 6, Burst length = 4



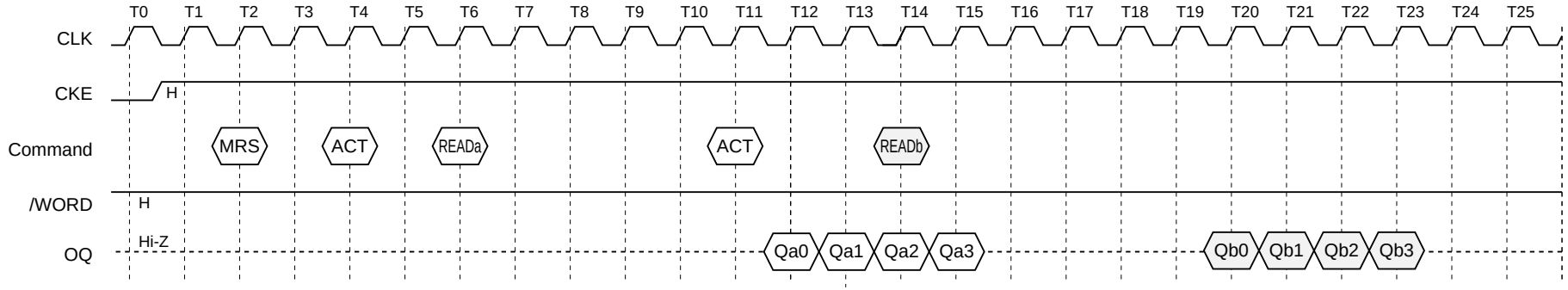
12.4.33 ROW ACTIVATE - READ (3)

/CAS latency = 6, Burst length = 4



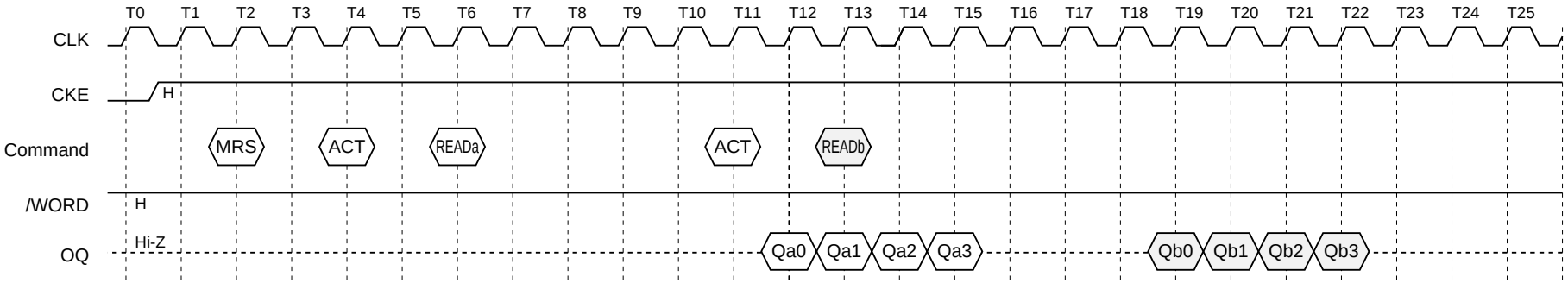
12.4.34 ROW ACTIVATE - READ (4)

/CAS latency = 6, Burst length = 4



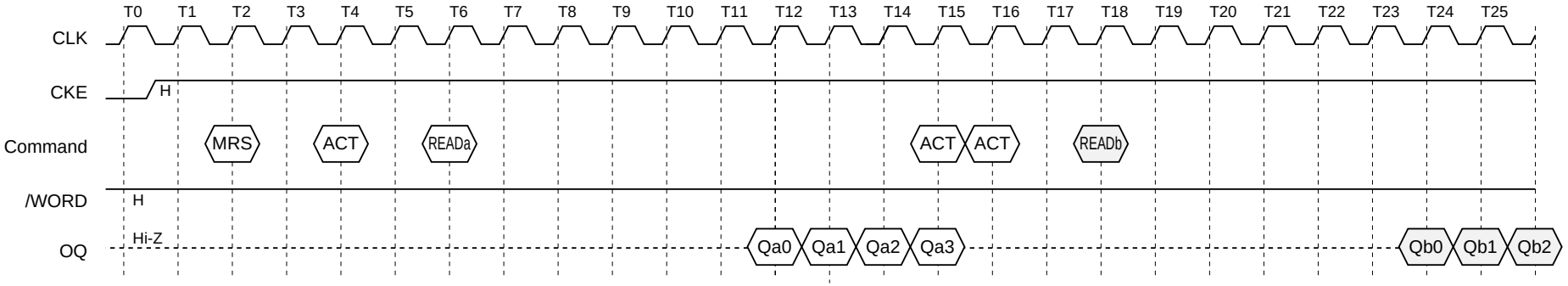
12.4.35 ROW ACTIVATE - READ (5)

/CAS latency = 6, Burst length = 4



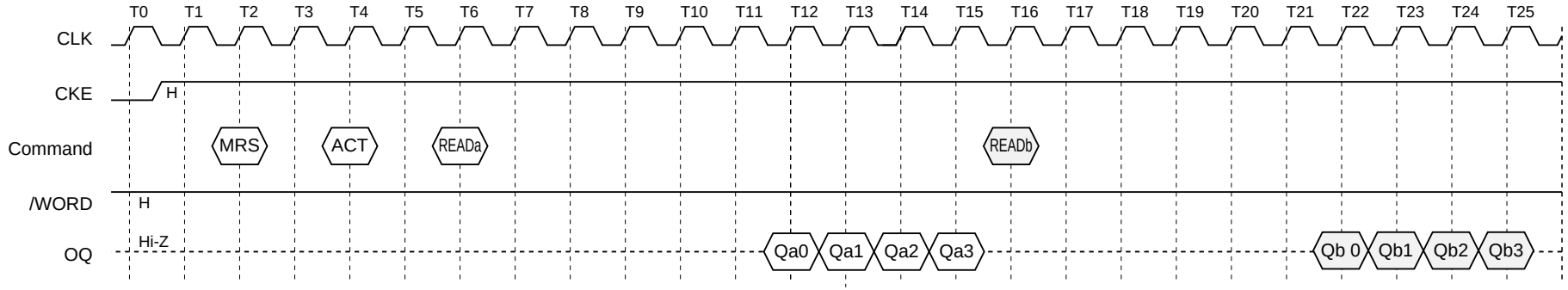
12.4.36 ROW ACTIVATE - ROW ACTIVATE

/CAS latency = 6, Burst length = 4



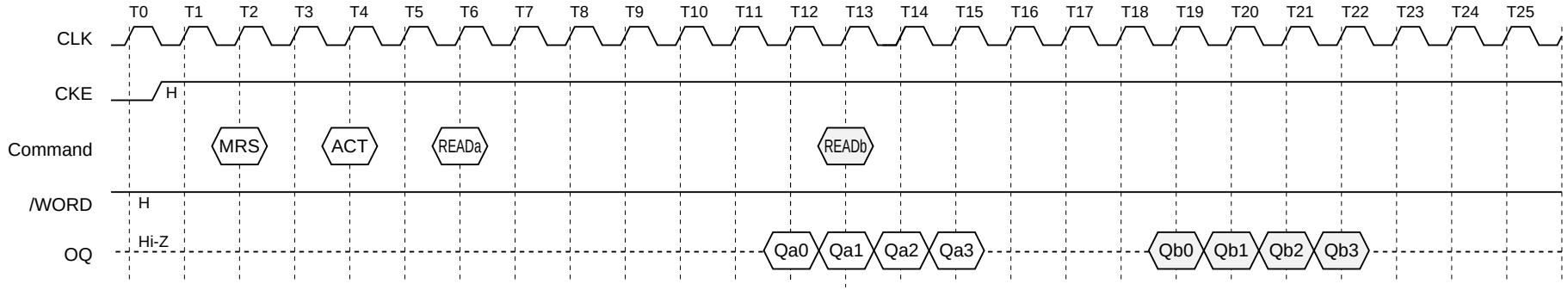
12.4.37 READ - READ (1)

/CAS latency = 6, Burst length = 4



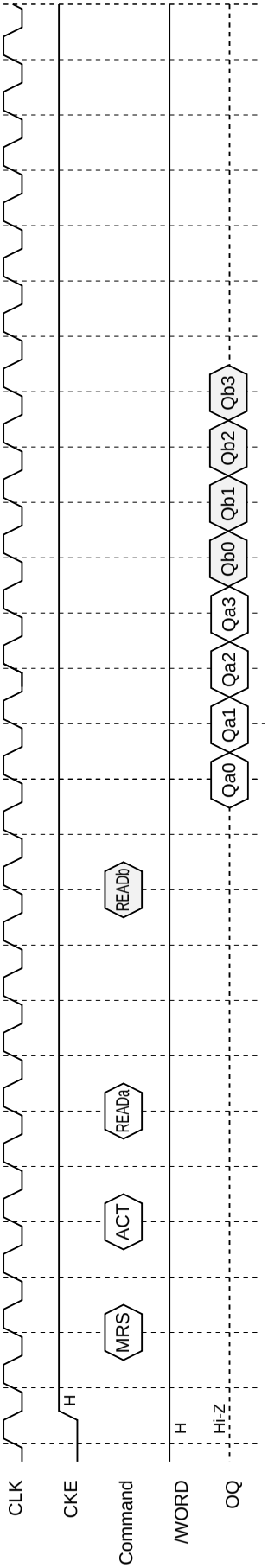
12.4.38 READ - READ (2)

/CAS latency = 6, Burst length = 4



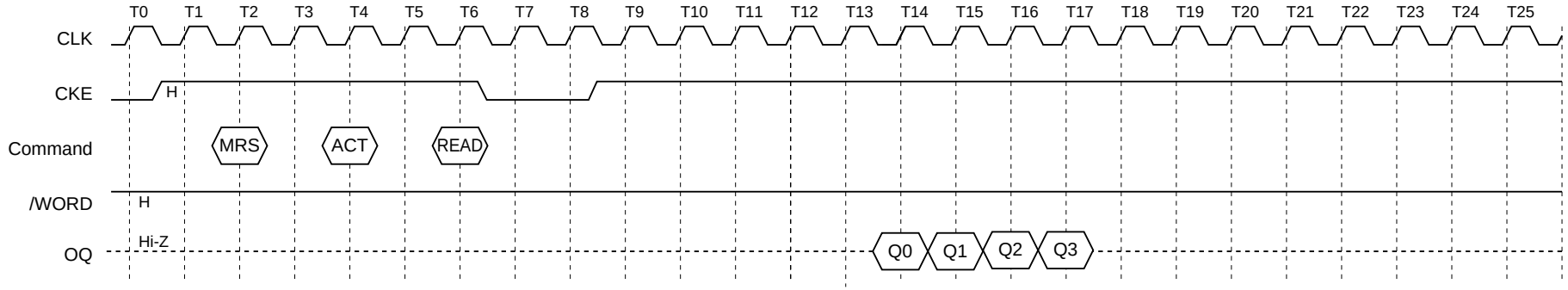
12.4.39 READ - READ (3)

/CAS latency = 6, Burst length = 4



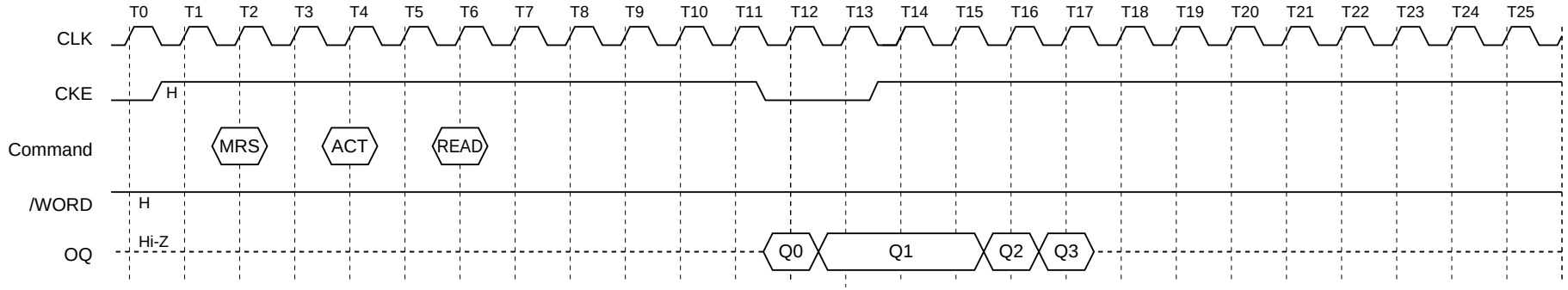
12.4.40 READ SUSPEND (1)

/CAS latency = 6, Burst length = 4



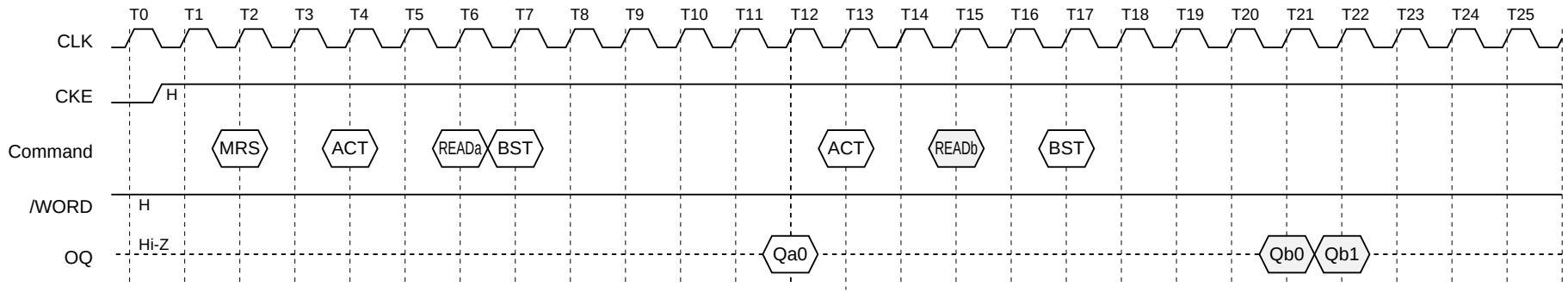
12.4.41 READ SUSPEND (2)

/CAS latency = 6, Burst length = 4



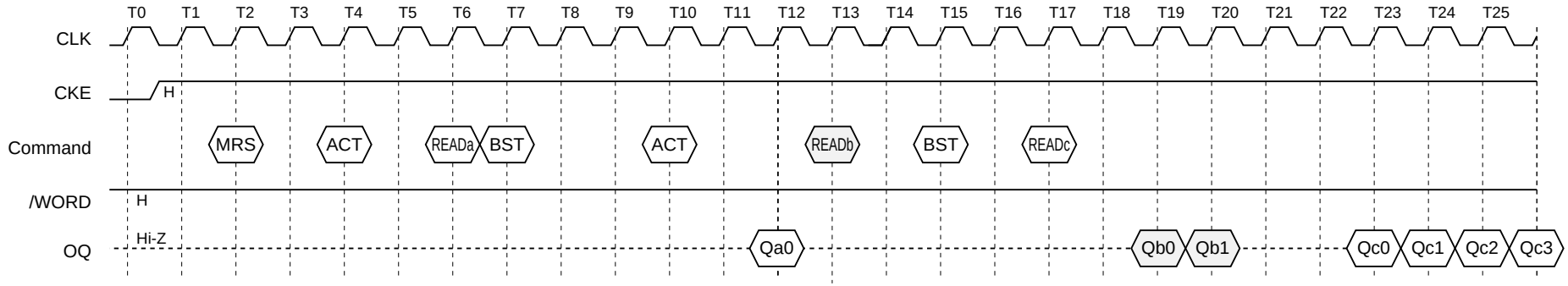
12.4.42 BURST STOP (1)

/CAS latency = 6, Burst length = 4



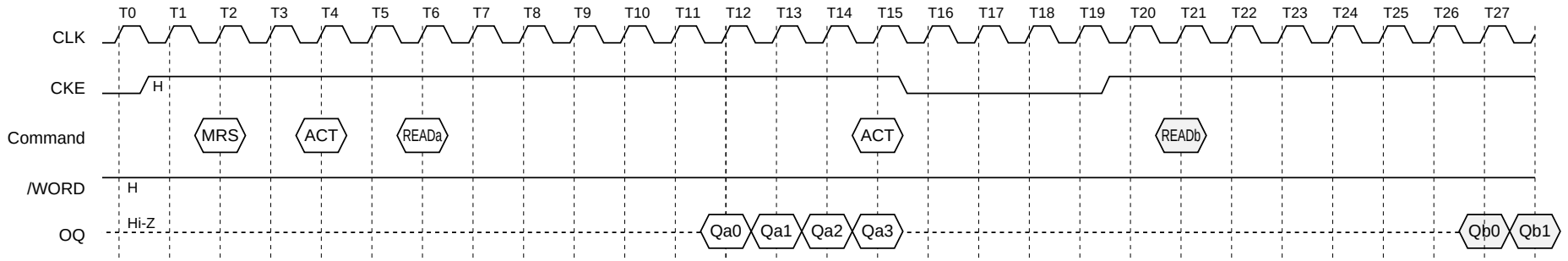
12.4.43 BURST STOP (2)

/CAS latency = 6, Burst length = 4



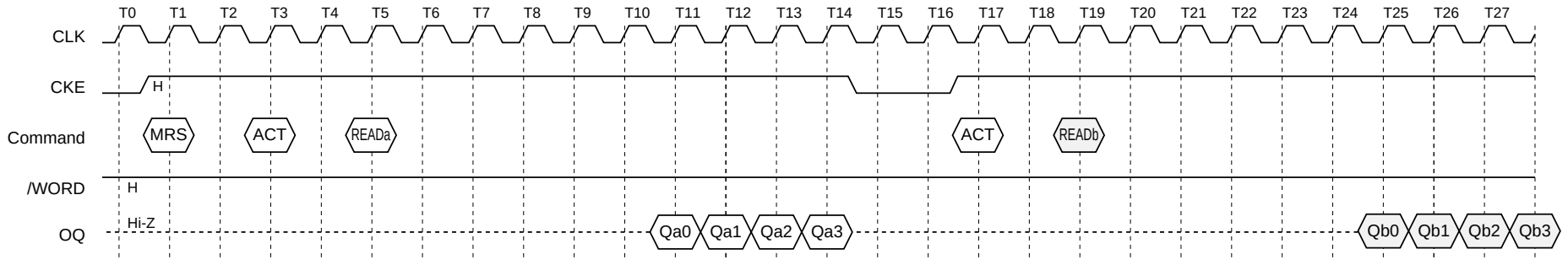
12.4.44 CLOCK SUSPEND

/CAS latency = 6, Burst length = 4



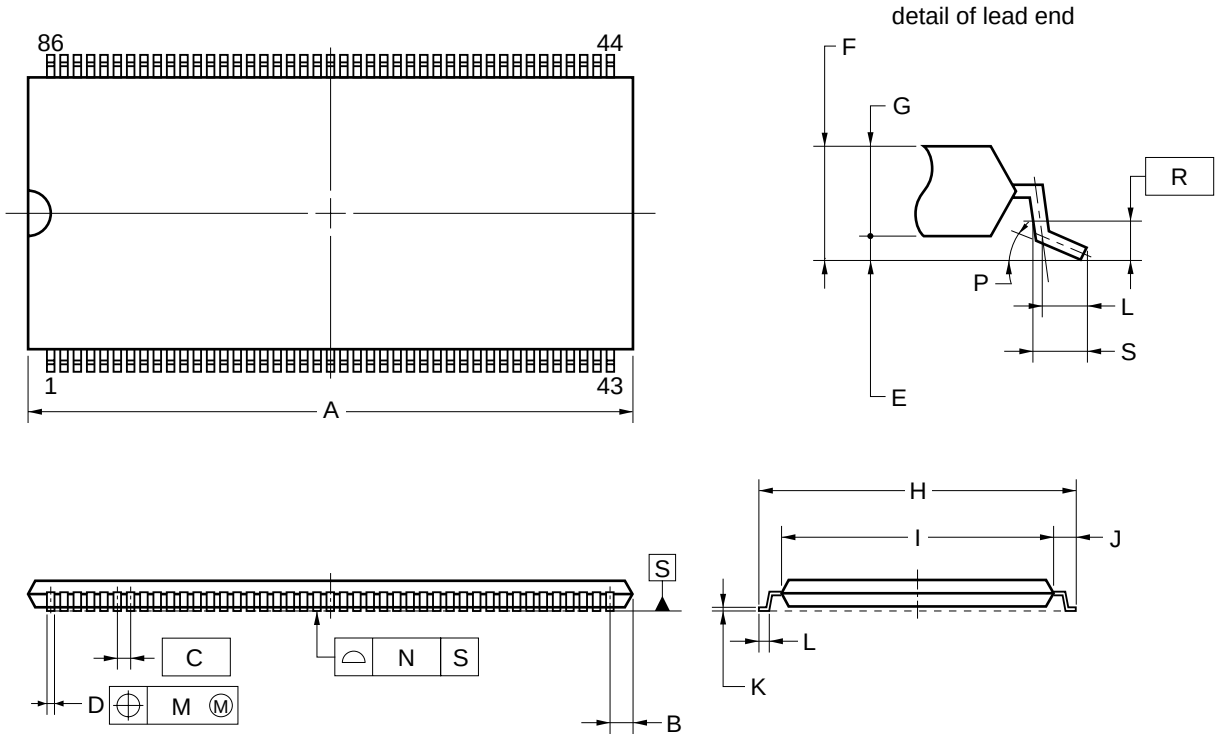
12.4.45 POWER DOWN

/CAS latency = 6, Burst length = 4



13. Package Drawing

86-PIN PLASTIC TSOP (II) (10.16 mm (400))



NOTES

1. Each lead centerline is located within 0.1 mm of its true position (T.P.) at maximum material condition.
2. Dimension "A" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.

ITEM	MILLIMETERS
A	22.22±0.05
B	0.765 MAX.
C	0.5 (T.P.)
D	$0.22^{+0.06}_{-0.04}$
E	0.10±0.05
F	1.1±0.1
G	1.00
H	11.76±0.20
I	10.16±0.10
J	0.80±0.20
K	$0.145^{+0.025}_{-0.015}$
L	0.50
M	0.1
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S86G5-50-9JH1-1

14. Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of the μPD23C64202L.

Type of Surface Mount Device

μPD23C64202LG5-9JH : 86-pin PLASTIC TSOP (II) (10.16 mm (400))

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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