

## TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

### 524,288-WORD BY 8-BIT CMOS STATIC RAM

#### DESCRIPTION

The TC55V8512J/FT is a 4,194,304-bit high-speed static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using CMOS technology and advanced circuit techniques to provide high speed, it operates from a single 3.3 V power supply. Chip enable ( $\overline{CE}$ ) can be used to place the device in a low-power mode, and output enable ( $\overline{OE}$ ) provides fast memory access. This device is well suited to cache memory applications where high-speed access and high-speed storage are required. All inputs and outputs are directly LVTTL compatible. The TC55V8512J/FT is available in plastic 36-pin SOJ and 44-pin TSOP with 400mil width for high density surface assembly.

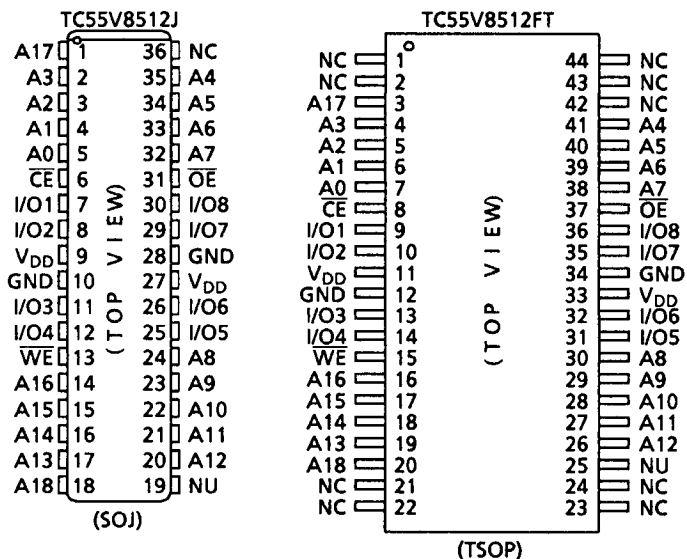
#### FEATURES

- Fast access time (the following are maximum values)
  - TC55V8512J/FT-12: 12 ns
  - TC55V8512J/FT-15: 15 ns
- Low-power dissipation (the following are maximum values)
 

|                 |     |     |     |     |    |
|-----------------|-----|-----|-----|-----|----|
| Cycle Time      | 12  | 15  | 20  | 25  | ns |
| Operation (max) | 170 | 140 | 130 | 110 | mA |
- Single power supply voltage of  $3.3V \pm 0.3V$
- Fully static operation
- All inputs and outputs are LVTTL compatible
- Output buffer control using  $\overline{OE}$
- Package:
  - SOJ36-P-400-1.27 (J) (Weight: 1.35g typ)
  - TSOP II 44-P-400-0.80 (FT) (Weight: 0.45g typ)

Standby: 4 mA (both devices)

#### PIN ASSIGNMENT



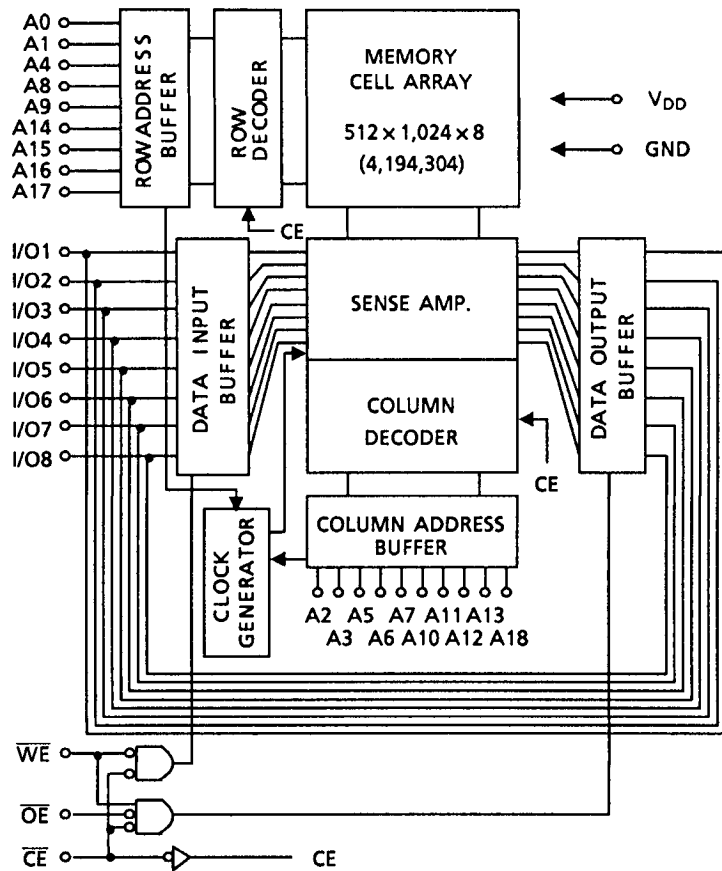
#### PIN NAMES

|                 |                     |
|-----------------|---------------------|
| A0 to A18       | Address Inputs      |
| I/O1 to I/O8    | Data Inputs/Outputs |
| $\overline{CE}$ | Chip Enable Input   |
| $\overline{WE}$ | Write Enable Input  |
| $\overline{OE}$ | Output Enable Input |
| V <sub>DD</sub> | Power (+ 3.3V)      |
| GND             | Ground              |
| NC              | No Connection       |
| NU              | Not Usable (Input)  |

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BLOCK DIAGRAM



MAXIMUM RATINGS

| SYMBOL              | RATING                        | VALUE                             | UNIT |
|---------------------|-------------------------------|-----------------------------------|------|
| V <sub>DD</sub>     | Power Supply Voltage          | - 0.5 to 4.6                      | V    |
| V <sub>IN</sub>     | Input Terminal Voltage        | - 0.5* to 4.6                     | V    |
| V <sub>I/O</sub>    | Input/Output Terminal Voltage | - 0.5* to V <sub>DD</sub> + 0.5** | V    |
| P <sub>D</sub>      | Power Dissipation             | 1.4                               | W    |
| T <sub>solder</sub> | Soldering Temperature (10s)   | 260                               | °C   |
| T <sub>strg</sub>   | Storage Temperature           | - 65 to 150                       | °C   |
| T <sub>opr</sub>    | Operating Temperature         | - 10 to 85                        | °C   |

\* : -1.5V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)  
 \*\* : V<sub>DD</sub>+1.5V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)

DC RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = 0° to 70°C)

| SYMBOL          | PARAMETER            | MIN    | TYP | MAX                     | UNIT |
|-----------------|----------------------|--------|-----|-------------------------|------|
| V <sub>DD</sub> | Power Supply Voltage | 3.0    | 3.3 | 3.6                     | V    |
| V <sub>IH</sub> | Input High Voltage   | 2.0    | -   | V <sub>DD</sub> + 0.3** | V    |
| V <sub>IL</sub> | Input Low Voltage    | - 0.3* | -   | 0.8                     | V    |

\* : -1.0V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)  
 \*\* : V<sub>DD</sub>+1.0V with a pulse width of 20% · t<sub>RC</sub> min (4ns max)

**DC CHARACTERISTICS** (Ta = 0° to 70°C, V<sub>DD</sub> = 3.3V ± 0.3V)

| SYMBOL             | PARAMETER                                | TEST CONDITION  | MIN                   | TYP | MAX | UNIT |    |
|--------------------|--|---|-----------------------|-----|-----|------|----|
| I <sub>IL</sub>    | Input Leakage Current<br>(Except NU pin) | V <sub>IN</sub> = 0 to V <sub>DD</sub>  | -1                    | -   | 1   | μA   |    |
| I <sub>LO</sub>    | Output Leakage Current                   | $\overline{CE} = V_{IH}$ or $\overline{WE} = V_{IL}$ or $\overline{OE} = V_{IH}$<br>V <sub>OUT</sub> = 0 to V <sub>DD</sub>       | -1                    | -   | 1   | μA   |    |
| I <sub>I(NU)</sub> | Input Current<br>(NU pin)                | V <sub>IN</sub> = 0 to 0.8V   | -1                    | -   | 20  | μA   |    |
|                    |  | V <sub>IN</sub> = 0 to 0.2V   | -1                    | -   | 1   |      |    |
| V <sub>OH</sub>    | Output High Voltage                      | I <sub>OH</sub> = -2mA  | 2.4                   | -   | -   | V    |    |
|                    |  | I <sub>OH</sub> = -100μA  | V <sub>DD</sub> - 0.2 | -   | -   |      |    |
| V <sub>OL</sub>    | Output Low Voltage                       | I <sub>OL</sub> = 2mA   | -                     | -   | 0.4 |      |    |
|                    |  | I <sub>OL</sub> = 100μA   | -                     | -   | 0.2 |      |    |
| I <sub>DDO</sub>   | Operating Current                        | $\overline{CE} = V_{IL}$ , I <sub>out</sub> = 0mA<br>$\overline{OE} = V_{IH}$<br>Other Inputs = V <sub>IH</sub> / V <sub>IL</sub> | tcycle = 12ns         | -   | -   | 170  | mA |
|                    |  |   | tcycle = 15ns         | -   | -   | 140  |    |
|                    |  |   | tcycle = 20ns         | -   | -   | 130  |    |
|                    |  |   | tcycle = 25ns         | -   | -   | 110  |    |
| I <sub>DDS1</sub>  | Standby Current                          | $\overline{CE} = V_{IH}$ , Other Inputs = V <sub>IH</sub> or V <sub>IL</sub>  | -                     | -   | 50  | mA   |    |
| I <sub>DDS2</sub>  |  | $\overline{CE} = V_{DD} - 0.2V$<br>Other Inputs = V <sub>DD</sub> - 0.2V or 0.2V  | -                     | -   | 4   |      |    |

**CAPACITANCE** (Ta = 25°C, f = 1.0 MHz)

| SYMBOL           | PARAMETER                | TEST CONDITION         | MAX | UNIT |
|------------------|--------------------------|------------------------|-----|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = GND  | 6   | pF   |
| C <sub>I/O</sub> | Input/Output Capacitance | V <sub>I/O</sub> = GND | 8   | pF   |

Note: This parameter is periodically sampled and is not 100% tested.

**OPERATING MODE**

| MODE            | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O1 to I/O8   | POWER            |
|-----------------|-----------------|-----------------|-----------------|----------------|------------------|
| Read            | L               | L               | H               | Output         | I <sub>DDO</sub> |
| Write           | L               | x               | L               | Input          | I <sub>DDO</sub> |
| Outputs Disable | L               | H               | H               | High Impedance | I <sub>DDO</sub> |
| Standby         | H               | x               | x               | High Impedance | I <sub>DDS</sub> |

x: Don't care

Note: The NU pin must be left unconnected or tied to GND or a voltage level of less than 0.8 V. You must not apply a voltage of more than 0.8 V to the NU.

**AC CHARACTERISTICS** ( $T_a = 0^\circ$  to  $70^\circ\text{C}$  (Note 1),  $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$ )

**READ CYCLE**

| SYMBOL    | PARAMETER                                 | TC55V8512J/FT-12 |     | TC55V8512J/FT-15 |     | UNIT |
|-----------|---|------------------|-----|------------------|-----|------|
|           |   | MIN              | MAX | MIN              | MAX |      |
| $t_{RC}$  | Read Cycle Time                           | 12               | -   | 15               | -   | ns   |
| $t_{ACC}$ | Address Access Time                       | -                | 12  | -                | 15  |      |
| $t_{CO}$  | Chip Enable Access Time                   | -                | 12  | -                | 15  |      |
| $t_{OE}$  | Output Enable Access Time                 | -                | 6   | -                | 8   |      |
| $t_{OH}$  | Output Data Hold Time from Address Change | 3                | -   | 4                | -   |      |
| $t_{COE}$ | Output Enable Time from Chip Enable       | 3                | -   | 4                | -   |      |
| $t_{OEE}$ | Output Enable Time from Output Enable     | 1                | -   | 1                | -   |      |
| $t_{COD}$ | Output Disable Time from Chip Enable      | -                | 7   | -                | 8   |      |
| $t_{ODO}$ | Output Disable Time from Output Enable    | -                | 7   | -                | 8   |      |

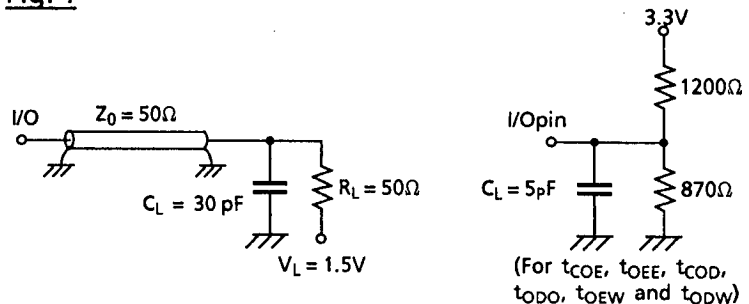
**WRITE CYCLE**

| SYMBOL    | PARAMETER                             | TC55V8512J/FT-12 |     | TC55V8512J/FT-15 |     | UNIT |
|-----------|---------------------------------------|------------------|-----|------------------|-----|------|
|           |                                       | MIN              | MAX | MIN              | MAX |      |
| $t_{WC}$  | Write Cycle Time                      | 12               | -   | 15               | -   | ns   |
| $t_{WP}$  | Write Pulse Width                     | 8                | -   | 9                | -   |      |
| $t_{CW}$  | Chip Enable to End of Write           | 10               | -   | 12               | -   |      |
| $t_{AW}$  | Address Valid to End of Write         | 10               | -   | 12               | -   |      |
| $t_{AS}$  | Address Setup Time                    | 0                | -   | 0                | -   |      |
| $t_{WR}$  | Write Recovery Time                   | 0                | -   | 0                | -   |      |
| $t_{DS}$  | Data Setup Time                       | 7                | -   | 8                | -   |      |
| $t_{DH}$  | Data Hold Time                        | 0                | -   | 0                | -   |      |
| $t_{OEW}$ | Output Enable Time from Write Enable  | 1                | -   | 1                | -   |      |
| $t_{ODW}$ | Output Disable Time from Write Enable | -                | 7   | -                | 8   |      |

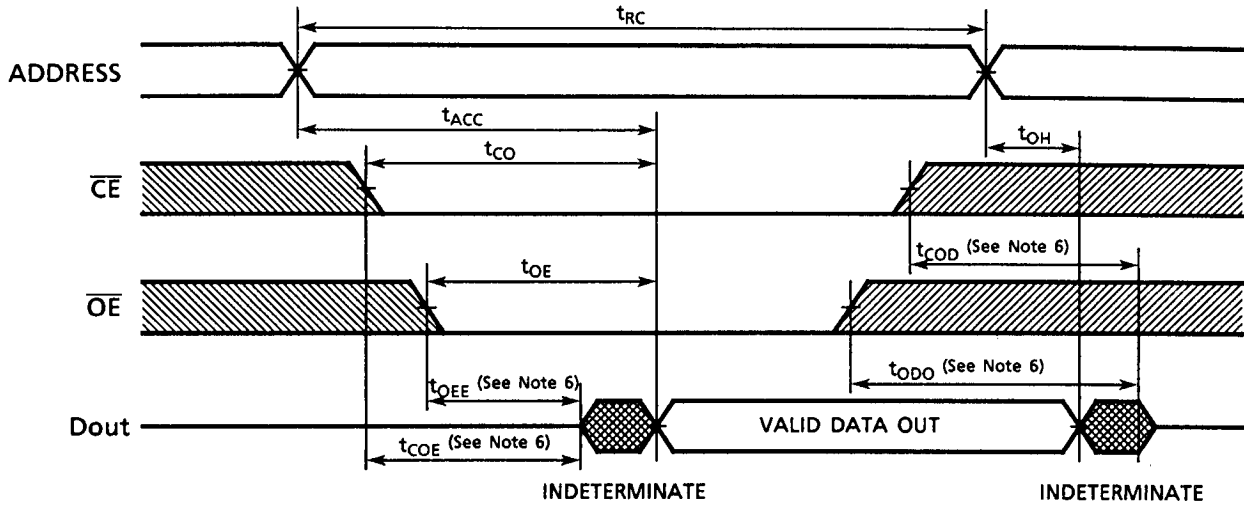
**AC TEST CONDITIONS**

|   |           |
|---|-----------|
| Input Pulse Level                         | 3.0V/0.0V |
| Input Pulse Rise and Fall Time            | 2ns       |
| Input Timing Measurement Reference Level  | 1.5V      |
| Output Timing Measurement Reference Level | 1.5V      |
| Output Load                               | Fig. 1    |

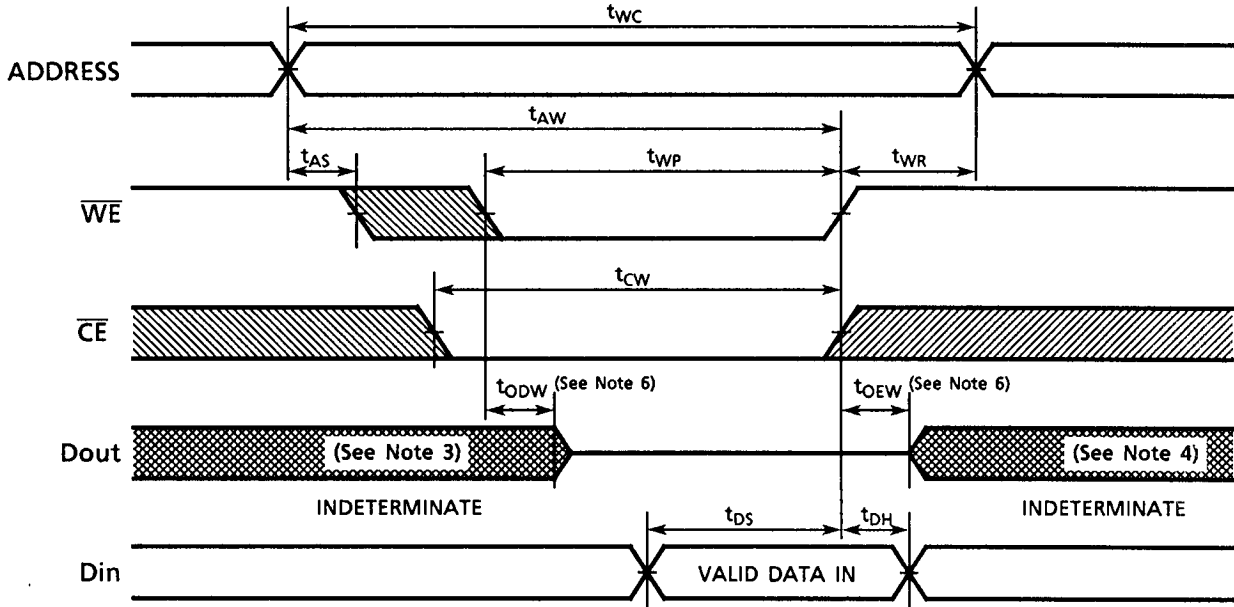
**Fig. 1**



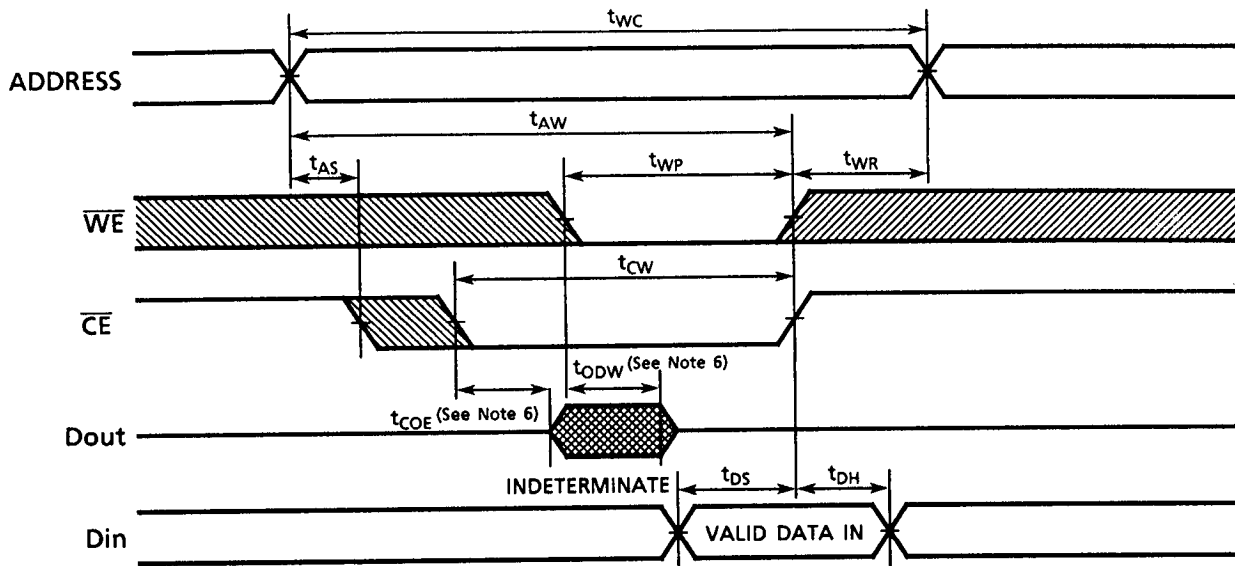
**TIMING DIAGRAMS**  
**READ CYCLE** (See Note 2)



**WRITE CYCLE 1 ( $\overline{WE}$  CONTROLLED)** (See Note 5)



WRITE CYCLE 2 ( $\overline{CE}$  CONTROLLED) (See Note 5)



Note: (1) Operating temperature ( $T_a$ ) is guaranteed for transverse air flow exceeding 400 linear feet per minute.

(2)  $\overline{WE}$  remains HIGH for the Read Cycle.

(3) If  $\overline{CE}$  goes LOW coincident with or after  $\overline{WE}$  goes LOW, the outputs will remain at high impedance.

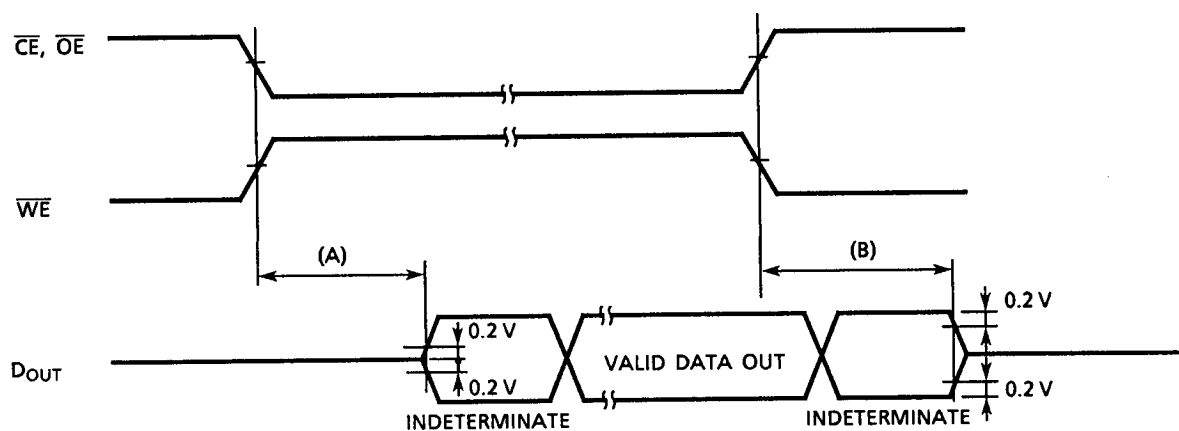
(4) If  $\overline{CE}$  goes HIGH coincident with or before  $\overline{WE}$  goes HIGH, the outputs will remain at high impedance.

(5) If  $\overline{OE}$  is HIGH during the write cycle, the outputs will remain at high impedance.

(6) The parameters specified below are measured using the load shown in Fig. 1.

(A)  $t_{COE}, t_{OEE}, t_{OEW}$  ..... Output Enable Time

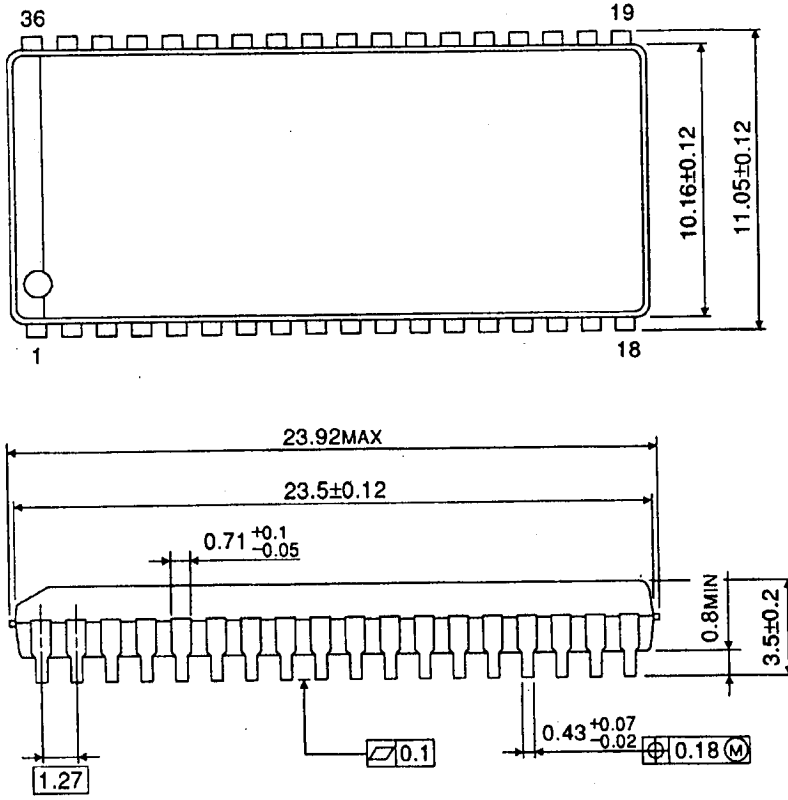
(B)  $t_{COD}, t_{ODO}, t_{ODW}$  ..... Output Disable Time



**PACKAGE DIMENSIONS**

Plastic SOJ (SOJ36-P-400-1.27)

Unit in mm



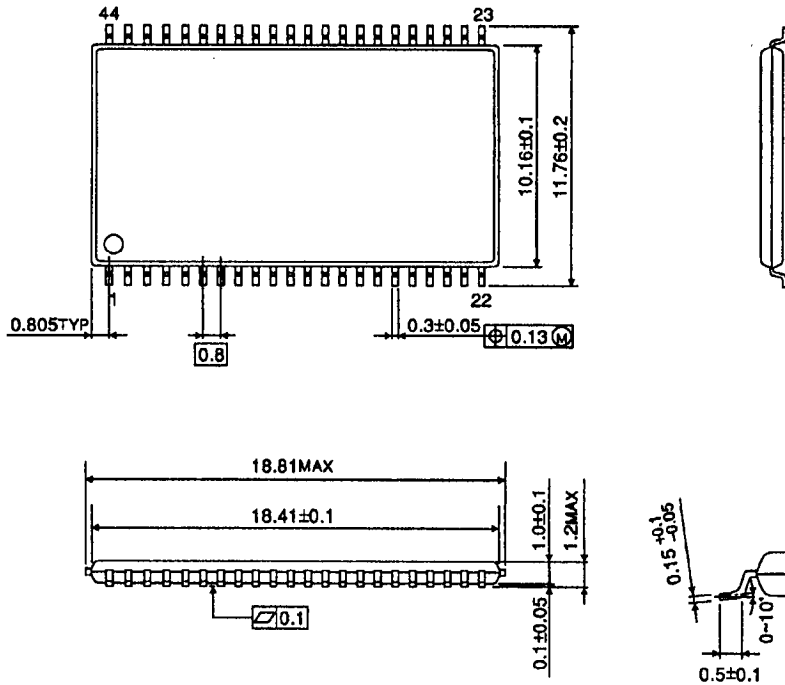
Weight : 1.35g (Typ)



PACKAGE DIMENSIONS

Plastic TSOP (TSOPII 44-P-400-0.80)

Unit in mm



Weight : 0.45g (Typ)