256K Static RAM 64K x 4-Bit with Separate I/O

Features

- High speed access times
  Com'l: 8, 10, 12, 15, 20 and 25 ns
  Ind'l: 10, 12, 15, 20, and 25 ns

- Low power operation
  - PDM41252SA, PDM41251SA
    Active: 400 mW (typ.)
    Standby: 150 mW (typ.)
  - PDM41252LA, PDM41251LA
    Active: 350 mW (typ.)
    Standby: 25 mW (typ.)

- Separate data input and output pins
- PDM41251: output track inputs during write mode
- PDM41252: high impedance outputs during write mode
- TTL compatible inputs and outputs
- Single +5V (±10%) power supply
- TTL compatible inputs and outputs
- Packages
  Plastic DIP (300 mil) - P
  Cerdip (300 mil) - D
  Plastic SOJ (300 mil) - SO
  Plastic TSOP - T

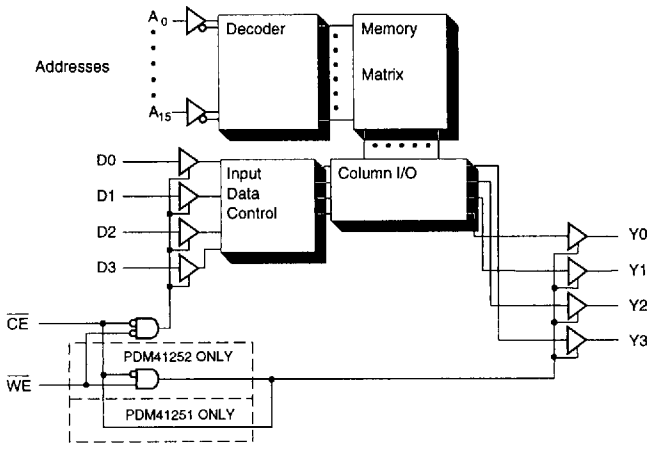
Description

The PDM41251 and PDM41252 are high-performance CMOS static RAMs organized as 65,536 x 4 bits. This product is produced in Paradigm's proprietary CMOS technology which offers the designer the highest speed parts. Writing to these devices is accomplished when the write enable ($\overline{WE}$) and the chip enable ($\overline{CE}$) inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW.

The PDM41251/2 operates from a single +5V power supply and all the inputs and outputs are fully TTL compatible. The PDM41251 and PDM41252 each come in two versions, the standard power version PDM41251SA and PDM41252SA and a low power version the PDM41251LA and PDM41252LA. The two versions are functionally the same and only differ in their power consumption.

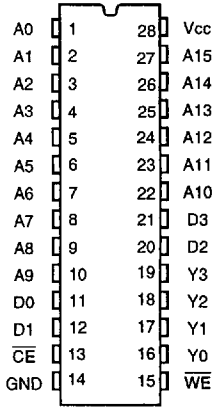
The PDM41251 and PDM41252 are available in a 28-pin 300 mil DIP. The PDM41251 and PDM41252 are also available in a 28-pin plastic TSOP and a 28-pin 300 mil SOJ for surface mount applications.

Functional Block Diagram



Pin Configuration

DIP
SOJ, TSOP



Truth Table

$\overline{WE}$	$\overline{CE}$	Output	MODE
X	H	Hi-Z	Standby
H	L	D_{OUT}	Read
L	L	D_{IN}	Write(2)
L	L	Hi-Z	Write(3)

NOTE: 1. H = V_{IH}, L = V_{IL}, X = DON'T CARE
2. For PDM41251 only.
3. For PDM41252 only.

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	-0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V±10%)

Symbol	Parameter	Test Conditions		PDM41251/2SA		PDM41251/2LA		Unit
				Min.	Max.	Min.	Max.	
I_{LI}	Input Leakage Current	V_{CC} = MAX., V_{IN} = GND to V_{CC}	Com'l/ Ind.	–5	5	–2	5	µA
I_{LO}	Output Leakage Current	V_{CC}= MAX., $\overline{CE}$ = V_{IH}, V_{OUT} = GND to V_{CC}	Com'l/ Ind.	–5	5	–2	5	µA
V_{IH}	Input High Voltage			2.2	6.0	2.2	6.0	V
V_{IL}	Input Low Voltage			–0.5(1)	0.8	–0.5(1)	0.8	V
V_{OL}	Output Low Voltage	I_{OL}=8 mA, V_{CC} = Min. I_{OL} = 10 mA, V_{CC} = Min.		— —	0.4 0.5	— —	0.4 0.5	V V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{CC} = Min.		2.4	—	2.4	—	V

NOTE: 1. V_{IL}(min) = –3.0V for pulse width less than 20 ns.

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Power Supply Characteristics

Symbol	Parameter	Power	-8	-10		-12		-15		-20		-25	
			Com'l.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.	Com'l	Ind.
I_{CC}	Operating Current $\overline{CE}$ = V_{IL}	SA	200	190	200	180	190	170	180	160	170	150	160
	f = f_{MAX} = 1/t_{RC} V_{CC} = Max I_{OUT} = 0 mA	LA	180	170	180	160	170	150	160	140	150	130	140
I_{SB}	Standby Current $\overline{CE}$ = V_{IH}	SA	80	70	70	60	60	50	50	40	40	35	35
	f = f_{MAX} = 1/t_{RC} V_{CC} = Max	LA	80	70	70	60	60	50	50	40	40	35	35
I_{SB1}	Full Standby Current $\overline{CE}$ ≥ V_{CC} – 0.2V	SA	20	20	20	20	20	10	20	10	20	10	20
	f = 0 V_{CC} = Max V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	LA	5	5	10	5	10	5	10	5	10	5	10

SHADED AREA = PRELIMINARY DATA.
NOTE: All Values are maximum guaranteed values.

Capacitance(1) (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	8	pF
C_{OUT}	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input rise and fall times	5 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See figures 1 and 2

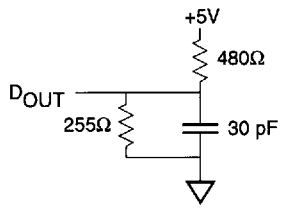


Figure 1. Output Load Equivalent

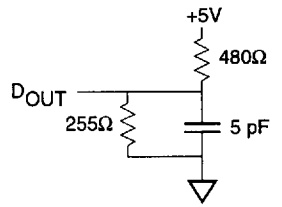
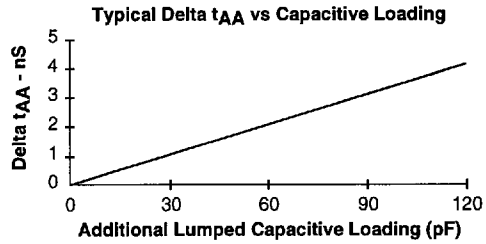
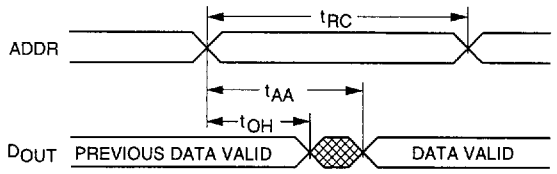


Figure 2. Output Load Equivalent
(for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE})



Read Cycle No. 1[1]



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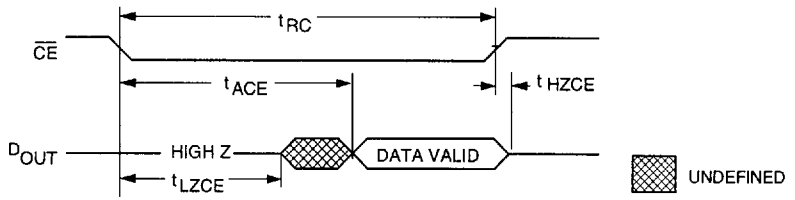
Read Cycle No. 2[2]

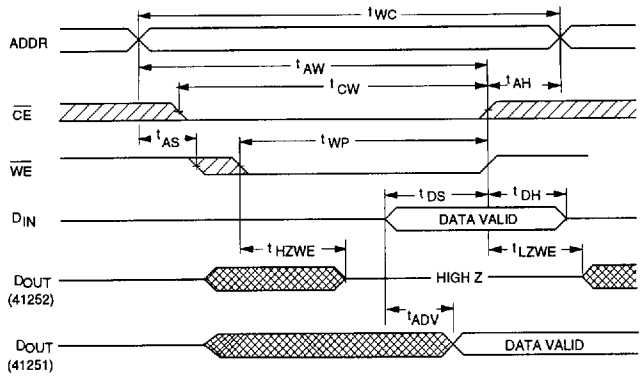


AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

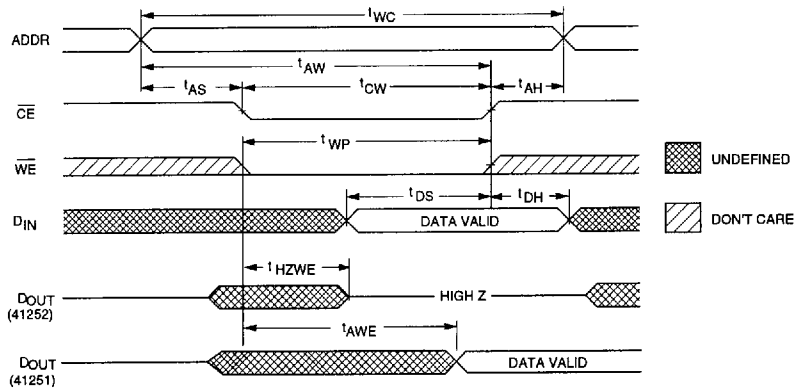
Description		-8[6]		-10[6]		-12		-15		-20		-25		
READ Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
READ cycle time	t_{RC}	8		10		12		15		20		25		ns
Address access time	t_{AA}		8		10		12		15		20		25	ns
Chip enable access time	t_{ACE}		8		10		12		15		20		25	ns
Output hold from address change	t_{OH}	3		3		3		3		3		3		ns
Chip enable to output in low Z[3, 4, 5]	t_{LZCE}	5		5		5		5		5		5		ns
Chip disable to output in high Z[3, 4, 5]	t_{HCZE}		5		10		10		10		15		15	ns
Chip enable to power up time[4]	t_{PU}	0		0		0		0		0		0		ns
Chip disable to power down time[4]	t_{PD}		8		10		12		15		20		25	ns

SHADED AREA = PRELIMINARY DATA.
Notes referenced are after Data Retention Table.

Write Cycle No. 1 (Write Enable Controlled)



Write Cycle No. 2 (Chip Enable Controlled)

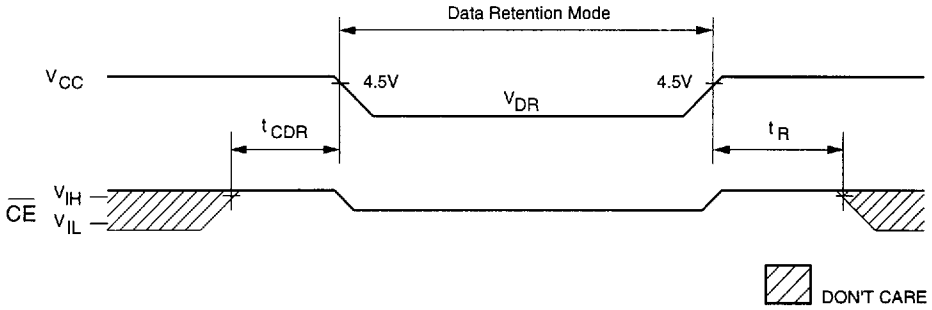


AC Electrical Characteristics (V_{CC} = 5V ± 10%, All Temperature Ranges)

Description		-8[6]		-10[6]		-12		-15		-20		-25		
WRITE Cycle	**Sym**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**
WRITE Cycle time	t_{WC}	8		10		12		15		20		25		ns
Chip enable access time	t_{CW}	8		10		10		12		13		15		ns
Address Valid to end of write	t_{AW}	8		10		10		12		13		15		ns
Address setup time	t_{AS}	0		0		0		0		0		0		ns
Address hold from end of write	t_{AH}	0		0		0		0		0		0		ns
Write pulse width	t_{WP}	8		10		10		11		12		15		ns
Data setup time	t_{DS}	7		7		7		8		9		10		ns
Write disable to output in low Z[4, 5]	t_{LZWE}	0		0		0		0		0		0		ns
Write enable to output in high Z[4, 5] (41252)	t_{HZWE}		3		3		3		3		3		5	ns
Write enable to data valid (41251)	t_{AWE}		8		10		12		15		20		20	ns
Data valid to output valid (41251)	t_{ADV}		8		10		12		15		20		20	ns
Data hold time	t_{DH}	0		0		0		0		0		0		ns

SHADED AREA = PRELIMINARY DATA.

Low V_{CC} Data Retention Waveform



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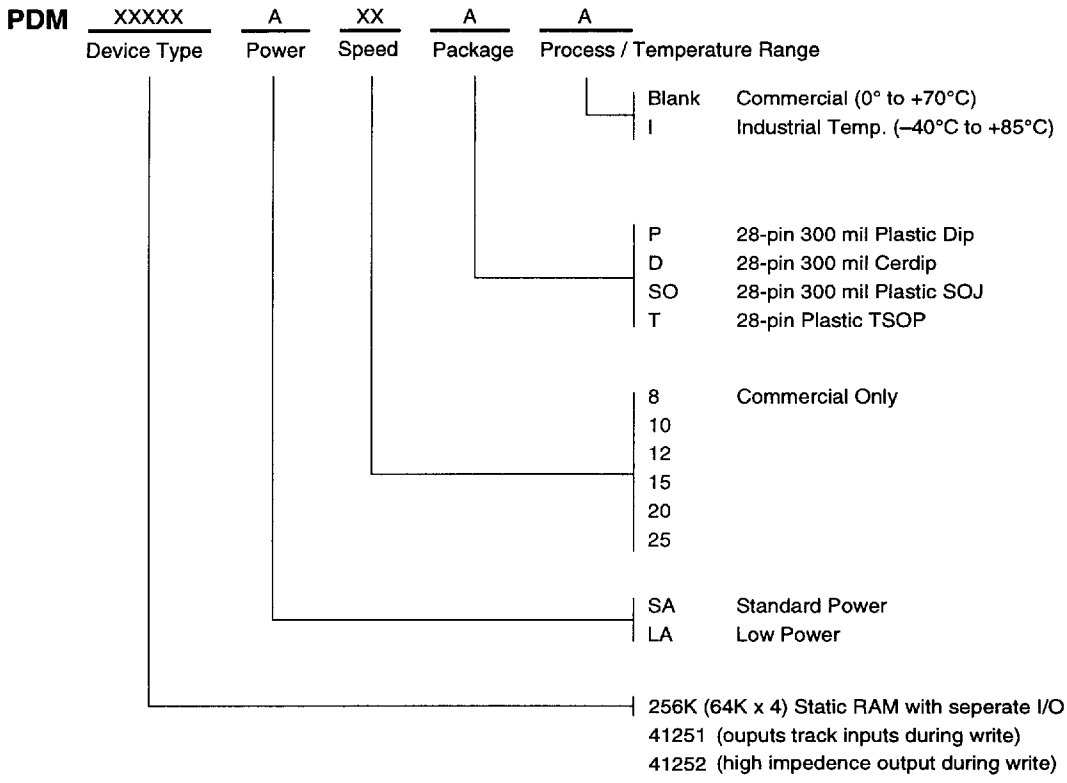
Data Retention Electrical Characteristics (LA Version Only)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
V_{DR}	V_{CC} for Retention Data			2	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$	—	95	500	µA
			$V_{CC} = 3V$	—	350	750	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[4]	Operation Recovery Time			t_{RC}	—	—	ns

NOTES: (For 3 previous Electrical Characteristics tables)

1. The device is continuously selected. All the Chip Enables are held in their active state.
2. The address is valid prior to or coincident with the latest occuring Chip Enable.
3. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}.
4. This parameter is sampled.
5. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage.
6. V_{CC} = 5V ± 5%.

Ordering Information



Chip	Package Type
PDM41251	28-pin Plastic DIP
	28-pin Cerdip
	28-pin Plastic SOJ
	28-pin Plastic TSOP