19-1227; Rev 1; 6/97

EVALUATION KIT AVAILABLE

MAXIM

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

General Description

The MAX1624/MAX1625 are ultra-high-performance, step-down DC-DC controllers for CPU power in high-end computer systems. Designed for demanding applications in which output voltage precision and good transient response are critical for proper operation, they deliver over 35A from 1.1V to 3.5V with ±1% total accuracy from a +5V ±10% supply. Excellent dynamic response corrects output transients caused by the latest dynamically clocked CPUs. These controllers achieve over 90% efficiency by using synchronous rectification. Flying-capacitor bootstrap circuitry drives inexpensive, external N-channel MOSFETs.

The switching frequency is resistor programmable from 100kHz to 1MHz. High switching frequencies allow the use of a small surface-mount inductor and decrease output filter capacitor requirements, reducing board area and system cost.

The MAX1624 is available in a 24-pin SSOP and offers additional features such as a digitally programmable output in 100mV increments; adjustable transient response; selectable 0.5%, 1%, or 2% AC load regulation; and gate drive for a current-boost MOSFET. The MAX1625 is resistor adjustable and comes in a 16-pin narrow SO package. Other features in both controllers include internal digital soft-start, a power-good output, and a 3.5V ±1% reference output. For a similar controller compatible with the latest Intel V_{RM}/V_{ID} specification, see the MAX1638* data sheet.

Applications

Pentium Pro™, Pentium II™, PowerPC™, Alpha™, and K6™ Systems

Desktop Computers

LAN Servers

Industrial Computers

GTL Bus Termination

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1624EAG	-40 ℃ to +85 ℃	24 SSOP
MAX1625ESE	-40 ℃ to +85 ℃	16 Narrow SO

Pin Configurations appear at end of data sheet.

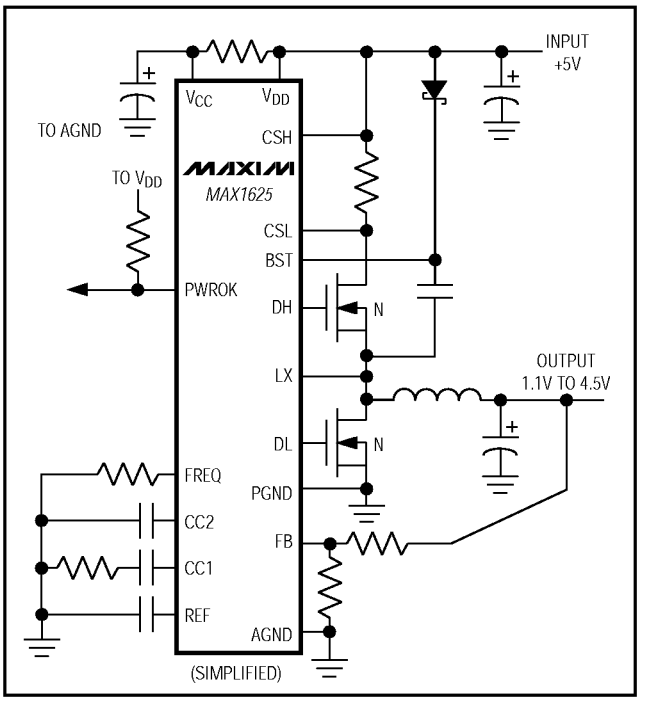
**Future product.*

Pentium Pro and Pentium II are trademarks of Intel Corp.
PowerPC is a trademark of IBM Corp.
Alpha is a trademark of Digital Equipment Corp.
K6 is a trademark of Advanced Micro Devices.
GlitchCatcher is a trademark of Maxim Integrated Products.

Features

- ♦ **Better than ±1% Output Accuracy Over Line and Load**
- ♦ **90% Efficiency**
- ♦ **Excellent Transient Response**
- ♦ **Resistor-Programmable Fixed Switching Frequency from 100kHz to 1MHz**
- ♦ **Over 35A Output Current**
- ♦ **Digitally Programmable Output from 1.1V to 3.5V in 100mV Increments (MAX1624)**
- ♦ **Resistor-Adjustable Output down to 1.1V (MAX1625)**
- ♦ **Remote Sensing**
- ♦ **Adjustable AC Loop Gain (MAX1624)**
- ♦ **GlitchCatcher™ Circuit for Fast Load-Transient Response (MAX1624)**
- ♦ **Power-Good (PWROK) Output**
- ♦ **Current-Mode Feedback**
- ♦ **Digital Soft-Start**
- ♦ **Strong 2A Gate Drivers**
- ♦ **Current-Limited Output**

Typical Operating Circuit



High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

ABSOLUTE MAXIMUM RATINGS

V_{DD}, V_{CC}, PWROK to AGND .....-0.3V to 6V
PGND to AGND .....±0.3V
CSH, CSL to AGND .....-0.3V to (V_{CC} + 0.3V)
NDRV, PDRV, DL to PGND.....-0.3V to (V_{DD} + 0.3V)
REF, CC1, CC2, LG, D0–D4, FREQ,
FB to AGND .....-0.3V to (V_{CC} + 0.3V)
BST to PGND .....-0.3V to 12V
BST to LX .....-0.3V to 6V
DH to LX.....(LX - 0.3V) to (BST + 0.3V)

Continuous Power Dissipation (T_A = ±70 °C)
24 Pin SSOP (derate 8.00mW/ °C above +70 °C) 640mW
16 Pin Narrow SO (derate 8.70mW/ °C above 70 °C).....696mW
Operating Temperature Range
MAX162_E_ _.....-40 °C to +85 °C
Storage Temperature Range .....-65 °C to +125 °C
Lead Temperature (soldering, 10sec) .....+300 °C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3 = 0V, R_{FREQ} = 33.3kΩ, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC} = V_{DD}			4.5		5.5	V
Input Undervoltage Lockout	V_{CC} rising edge, 1% hysteresis			4.0		4.2	V
V_{CC} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV	Operating mode				2.5	mA
		Standby mode				0.3	
V_{DD} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV, operating or standby mode					0.1	mA
Reference Voltage	No load			3.465	3.5	3.535	V
Reference Load Regulation	0µA < I_{LOAD} < 100µA					10	mV
Reference Undervoltage Lockout	Rising edge, 1% hysteresis			2.7		3.0	V
Reference Short-Circuit Current	V_{REF} = 0V			0.5		4.0	mA
FB Accuracy	MAX1624, over line and load (Note 1)	T_A = +25 °C to +85 °C				±1	%
		T_A = 0 °C to +85 °C				±1.5	
FB Set Voltage	MAX1625, over line and load (Note 2)	T_A = +25 °C to +85 °C				±1	%
		T_A = 0 °C to +85 °C				±1.5	
AC Load Regulation (Note 3)	CSH - CSL = 0mV to 80mV	MAX1624	LG = GND		0.5		%
			LG = REF		1		
			LG = V_{CC}		2		
		MAX1625			1		
DC Load Regulation (Note 3)	CSH - CSL = 0mV to 80mV	MAX1624	LG = GND		0.05		%
			LG = REF		0.1		
			LG = V_{CC}		0.2		
		MAX1625			0.1		
PWROK Trip Level	Rising FB, 1% hysteresis with respect to V_{REF}			-7.5	-6	-4.5	%
	Falling FB, 1% hysteresis with respect to V_{REF}			6.5	8	9.5	
PWROK Output Voltage Low	I_{SINK} = 2mA, V_{CC} = 4.5V					0.4	V
PWROK Output Current High	PWROK = 5.5V					1	µA
Switching Frequency	R_{FREQ} = 20kΩ			850	1000	1150	kHz
	R_{FREQ} = 33.3kΩ			540	600	660	
	R_{FREQ} = 200kΩ			85	100	115	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3 = 0V, R_{FREQ} = 33.3kΩ, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Duty Cycle	R_{FREQ} = 20kΩ		85	90		%
LG Input Voltage	LG = GND (low)				0.2	V
	LG = REF (mid)		3.3		3.7	
	LG = V_{CC} (high)		V_{CC} - 0.2			
Logic Input Voltage Low	D0–D4; V_{CC} = 5.5V				0.8	V
Logic Input Voltage High	D0–D4; V_{CC} = 4.5V		2.0			V
D0–D4 Input Current	D0–D4 = 0V, 5V				±1	µA
LG Input Current					4	µA
CSH, CSL Input Current	MAX1624, CSH = CSL = 1.3V, D0–D3 = 5V, D4 = 0V				50	µA
	MAX1625, CSH = CSL = 1.1V				50	
FB Input Current	FB = 1.1V				±0.1	µA
CC1 Output Resistance				10		kΩ
CC2 Transconductance				1		mmho
CC2 Clamp Voltage	Minimum		2.4		3.0	V
	Maximum		4		V_{CC}	
CC2 Source/Sink Current	100mV overdrive			100		µA
DH On-Resistance	BST - LX = 4.5V			0.7	2	Ω
DL On-Resistance	V_{DD} = 4.5V			0.7	2	Ω
DH, DL Source/Sink Current	DH = DL = 2.5V			2		A
DH, DL Dead Time			0	30		ns
PDRV Trip Level	With respect to V_{REF}, FB going low	T_A = +25°C	-2.75	-2	-1.25	%
		T_A = 0°C to +85°C	-3		-1	
NDRV Trip Level	With respect to V_{REF}, FB going high	T_A = +25°C	1.25	2	2.75	%
		T_A = 0°C to +85°C	1		3	
PDRV, NDRV Response Time	FB overdrive = 5%			75		ns
PDRV, NDRV On-Resistance	V_{DD} = 4.5V			2	5	Ω
PDRV, NDRV Source/Sink Current	PDRV = NDRV = 2.5V			0.5		A
PDRV, NDRV Minimum On-Time				100		ns
Current-Limit Trip Voltage			85	100	115	mV
Soft-Start Time	To full current limit			1536		1 / f_{OSC}
BST Leakage Current	BST = 12V, LX = 7V, REF = GND				50	µA

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

ELECTRICAL CHARACTERISTICS

(V_{DD} = V_{CC} = D4 = +5V, PGND = AGND = D0–D3= 0V, R_{FREQ} = 33.3kΩ, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC} = V_{DD}		4.5		5.5	V
Input Undervoltage Lockout	V_{CC} rising edge, 1% hysteresis		3.9		4.3	V
V_{CC} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV	Operating mode			3	mA
		Standby mode			0.4	
V_{DD} Supply Current	V_{CC} = V_{DD} = 5.5V, FB overdrive = 200mV, operating or standby mode				0.2	mA
Reference Voltage	No load		3.447	3.5	3.553	V
FB Accuracy	MAX1624, over line and load				±2.5	%
FB Set Voltage	MAX1625				±2.5	%
PWROK Trip Level	Rising FB, 1% hysteresis with respect to V_{REF}		-8	-6	-4	%
	Falling FB, 1% hysteresis with respect to V_{REF}		6	8	10	
Switching Frequency	R_{FREQ} = 20kΩ		800	1000	1200	kHz
	R_{FREQ} = 33.3kΩ		510	600	690	
	R_{FREQ} = 200kΩ		80	100	120	
Maximum Duty Cycle	R_{FREQ} = 20kΩ		84	90		%
DH On-Resistance	BST - LX = 4.5V			0.7	2	Ω
DL On-Resistance	V_{DD} = 4.5V			0.7	2	Ω
Current-Limit Trip Voltage			70	100	130	mV

Note 1: FB accuracy is 100% tested at FB = 3.5V (code 10000) with V_{CC} = V_{DD} = 4.5V to 5.5V and CSH - CSL = 0mV to 80mV. The other DAC codes are tested at the major transition points with V_{CC} = V_{DD} = 5V and CSH - CSL = 0. FB accuracy at other DAC codes over line and load is guaranteed by design.

Note 2: FB set voltage is 100% tested with V_{CC} = V_{DD} = 4.5V to 5.5V and CSH - CSL = 0mV to 80mV.

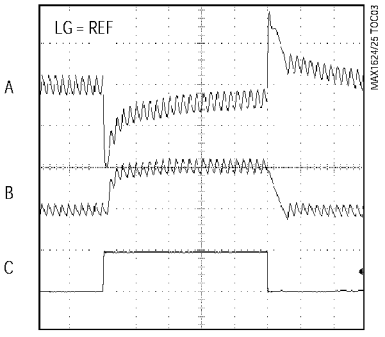
Note 3: AC load regulation sets the AC loop gain, to make tradeoffs between output filter capacitor size and transient response, and has only a slight effect on DC accuracy or DC load-regulation error.

Note 4: Specifications from 0 °C to -40 °C are not production tested.

Typical Operating Characteristics

(T_A = +25 °C, using the MAX1624 evaluation kit, unless otherwise noted.)

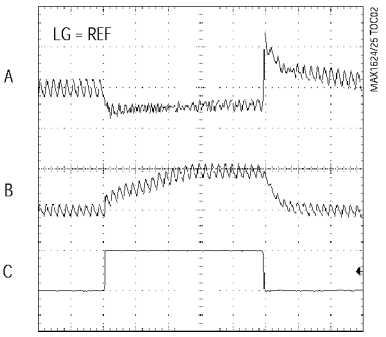
MAX1624
LOAD-TRANSIENT RESPONSE
(WITHOUT GLITCHCATCHER)
(1.1V)



10µs/div

A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

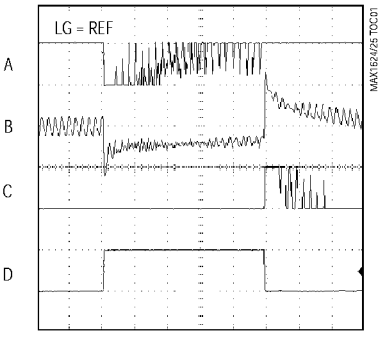
MAX1624
LOAD-TRANSIENT RESPONSE
(WITH GLITCHCATCHER)
(1.1V)



10µs/div

A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

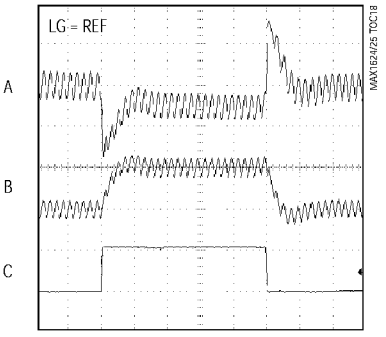
MAX1624
LOAD-TRANSIENT RESPONSE DETAIL
(WITH GLITCHCATCHER)
(1.1V)



10µs/div

A: PDRV, 5V/div
B: V_{OUT}, 50mV/div, AC COUPLED
C: NDRV, 5V/div
D: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

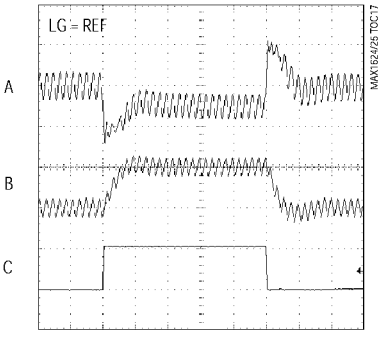
MAX1624
LOAD-TRANSIENT RESPONSE
(WITHOUT GLITCHCATCHER)
(2.5V)



10µs/div

A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

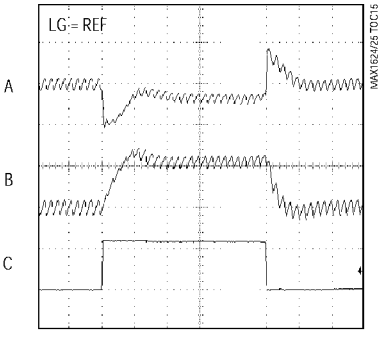
MAX1624
LOAD-TRANSIENT RESPONSE
(WITH GLITCHCATCHER)
(2.5V)



10µs/div

A: V_{OUT}, 50mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 10A, t_{RISE} = t_{FALL} = 100ns

MAX1624
LOAD-TRANSIENT RESPONSE
(WITHOUT GLITCHCATCHER)
(3.5V)



10µs/div

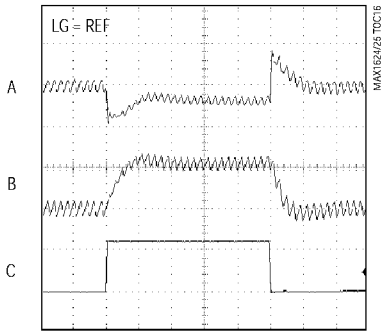
A: V_{OUT}, 100mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 11A, t_{RISE} = t_{FALL} = 100ns

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Typical Operating Characteristics (continued)

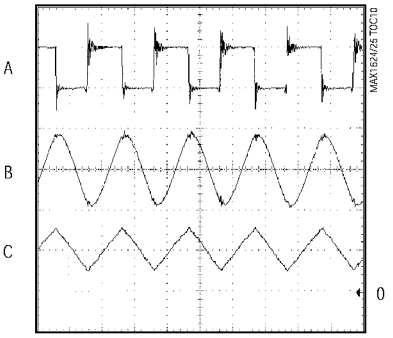
(T_A = +25°C, using the MAX1624 evaluation kit, unless otherwise noted.)

MAX1624
LOAD-TRANSIENT RESPONSE
(WITH GLITCHCATCHER)
(3.5V)



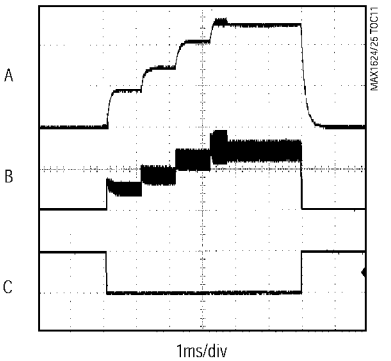
A: V_{OUT}, 100mV/div, AC COUPLED
B: INDUCTOR CURRENT, 10A/div
C: LOAD CURRENT, 0A TO 11A, t_{RISE} = t_{FALL} = 100ns

MAX1624
SWITCHING WAVEFORMS



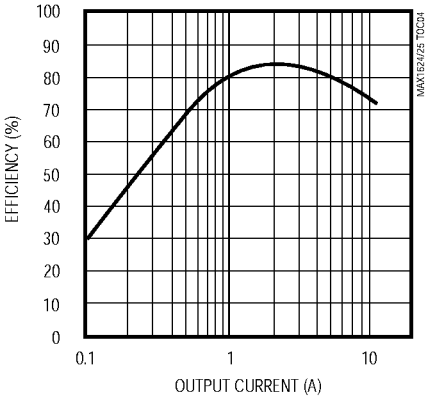
V_{IN} = 5V, V_{OUT} = 2.5V, LOAD = 5A
A: LX, 5V/div
B: V_{OUT}, 20mV/div, AC COUPLED
C: INDUCTOR CURRENT, 5A/div

MAX1624
STARTUP AND STANDBY RESPONSE

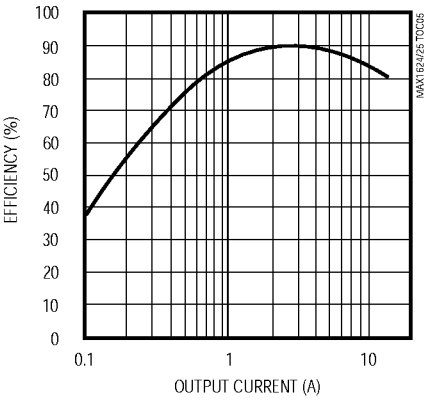


V_{IN} = 5V, V_{OUT} = 2.5V, LOAD = 13.8A
A: V_{OUT}, 1V/div
B: INDUCTOR CURRENT, 10A/div
C: STANDBY, D0–D4

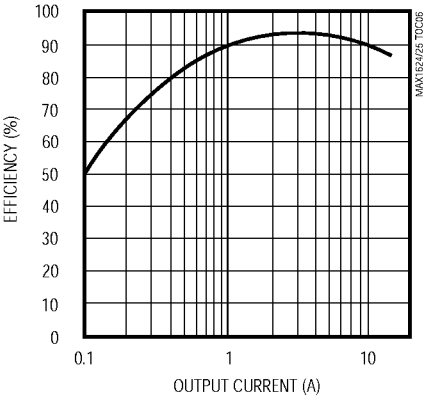
MAX1624
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 1.1V)



MAX1624
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 2.5V)



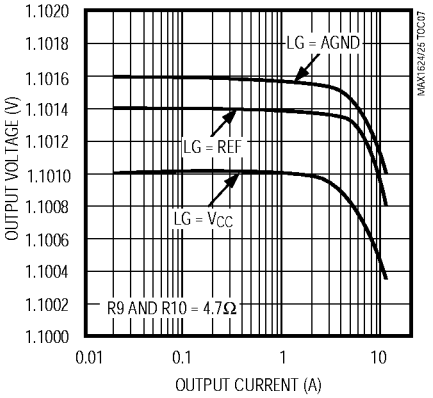
MAX1624
EFFICIENCY vs. OUTPUT CURRENT
(V_{OUT} = 3.5V)



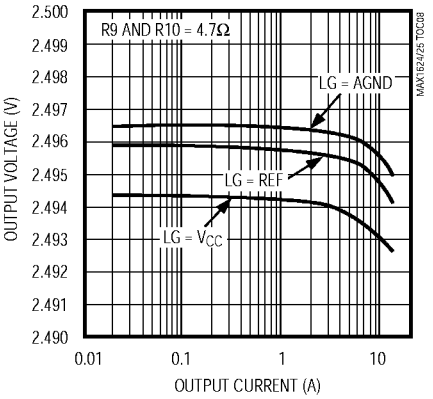
Typical Operating Characteristics (continued)

(T_A = +25 °C, using the MAX1624 evaluation kit, unless otherwise noted.)

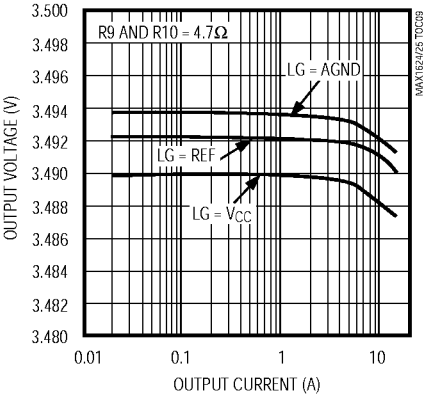
MAX1624
OUTPUT VOLTAGE vs. OUTPUT CURRENT
(V_{OUT} = 1.1V)



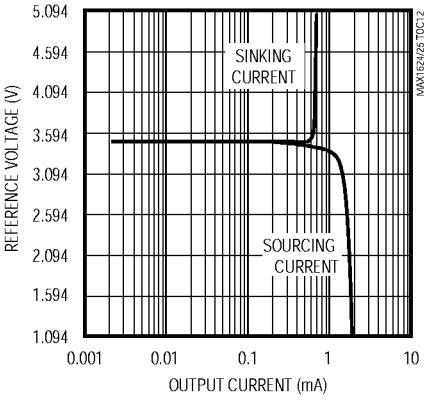
MAX1624
OUTPUT VOLTAGE vs. OUTPUT CURRENT
(V_{OUT} = 2.5V)



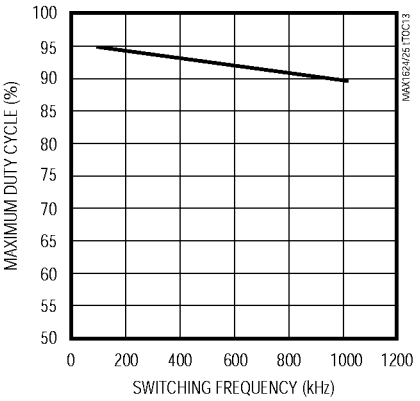
MAX1624
OUTPUT VOLTAGE vs. OUTPUT CURRENT
(V_{OUT} = 3.5V)



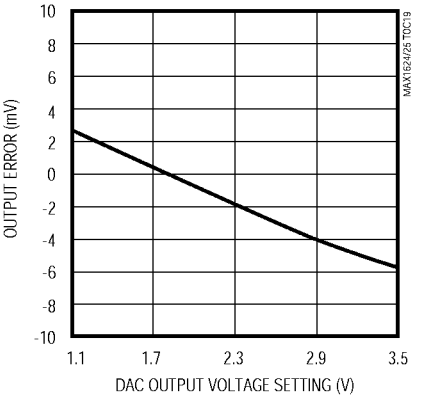
REFERENCE VOLTAGE
vs. OUTPUT CURRENT



MAXIMUM DUTY CYCLE
vs. SWITCHING FREQUENCY



MAX1624
OUTPUT ERROR vs.
DAC OUTPUT VOLTAGE SETTING



High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Pin Description

PIN		NAME	FUNCTION
MAX1624	MAX1625		
1	1	BST	Boost-Capacitor Bypass for High-Side MOSFET Gate Drive. Connect a 0.1µF capacitor and low-leakage Schottky diode as a bootstrapped charge-pump circuit to derive a 5V gate drive from V_{DD} for DH.
2	2	PWROK	Open-Drain Logic Output. PWROK is high when the voltage on FB is within +8% and -6% of its setpoint.
3	3	CSL	Current-Sense Amplifier's Inverting Input. Place the current-sense resistor very close to the controller IC, and use a Kelvin connection. Use an RC filter network at CSL (Figure 1).
4	4	CSH	Current-Sense Amplifier's Noninverting Input. Use an RC filter network at CSH (Figure 1).
5, 6, 7	—	D2, D1, D0	Digital Inputs for Programming the Output Voltage. D0–D4 are logic inputs that set the output to a voltage between 1.1V and 3.5V in 100mV increments.
8	—	LG	Loop Gain-Control Input. LG is a three-level input that is used to trade off loop gain vs. AC load-regulation and load-transient response. Connect LG to V_{CC}, REF, or AGND for 2%, 1%, or 0.5% AC load-regulation errors, respectively.
9	5	V_{CC}	Analog Supply Input, 5V. Use an RC filter network, as shown in Figure 1.
10	6	REF	Reference Output, 3.5V. Bypass REF to AGND with 0.1µF (min). Sources up to 100µA for external loads. Force REF below 2V to turn off the controller.
11	7	AGND	Analog Ground
12	8	FB	Voltage-Feedback Input. **MAX1624:** Connect FB to the CPU's remote voltage-sense point. The voltage at this input is regulated to a value determined by D0–D4. **MAX1625:** Connect a feedback resistor voltage divider close to FB from the output to AGND. FB is regulated to 1.1V.
13	9	CC1	Fast-Loop Compensation Capacitor Input. Connect a ceramic capacitor and resistor in series from CC1 to AGND. See the section *Compensating the Feedback Loop*.
14	10	CC2	Slow-Loop Compensation Capacitor Input. Connect a ceramic capacitor from CC2 to AGND. See the section *Compensating the Feedback Loop*.
15	11	FREQ	Frequency-Programming Input. Attach a resistor within 0.2 in. (5mm) of FREQ to AGND to set the switching frequency between 100kHz and 1MHz. The FREQ pin is normally 2V DC.
16, 17	—	D4, D3	Digital Inputs for Programming the Output Voltage
18	—	NDRV	GlitchCatcher N-Channel MOSFET Driver Output. NDRV swings between V_{DD} and PGND.
19	—	PDRV	GlitchCatcher P-Channel MOSFET Driver Output. PDRV swings between V_{DD} and PGND.
20	12	V_{DD}	5V Power Input for MOSFET Drivers. Bypass V_{DD} to PGND within 0.2 in. (5mm) of the V_{DD} pin using a 0.1µF capacitor and 4.7µF capacitor connected in parallel.
21	13	DL	Low-Side Synchronous Rectifier Gate-Drive Output. DL swings between PGND and V_{DD}. See the section *BST High-Side Gate-Driver Supply and MOSFET Drivers*.
22	14	PGND	Power Ground
23	15	LX	Switching Node. Connect LX to the high-side MOSFET source and inductor.
24	16	DH	High-Side Main MOSFET Switch Gate-Drive Output. DH is a floating driver output that swings from LX to BST, riding on the LX switching-node voltage. See the section *BST High-Side Gate-Driver Supply and MOSFET Drivers*.

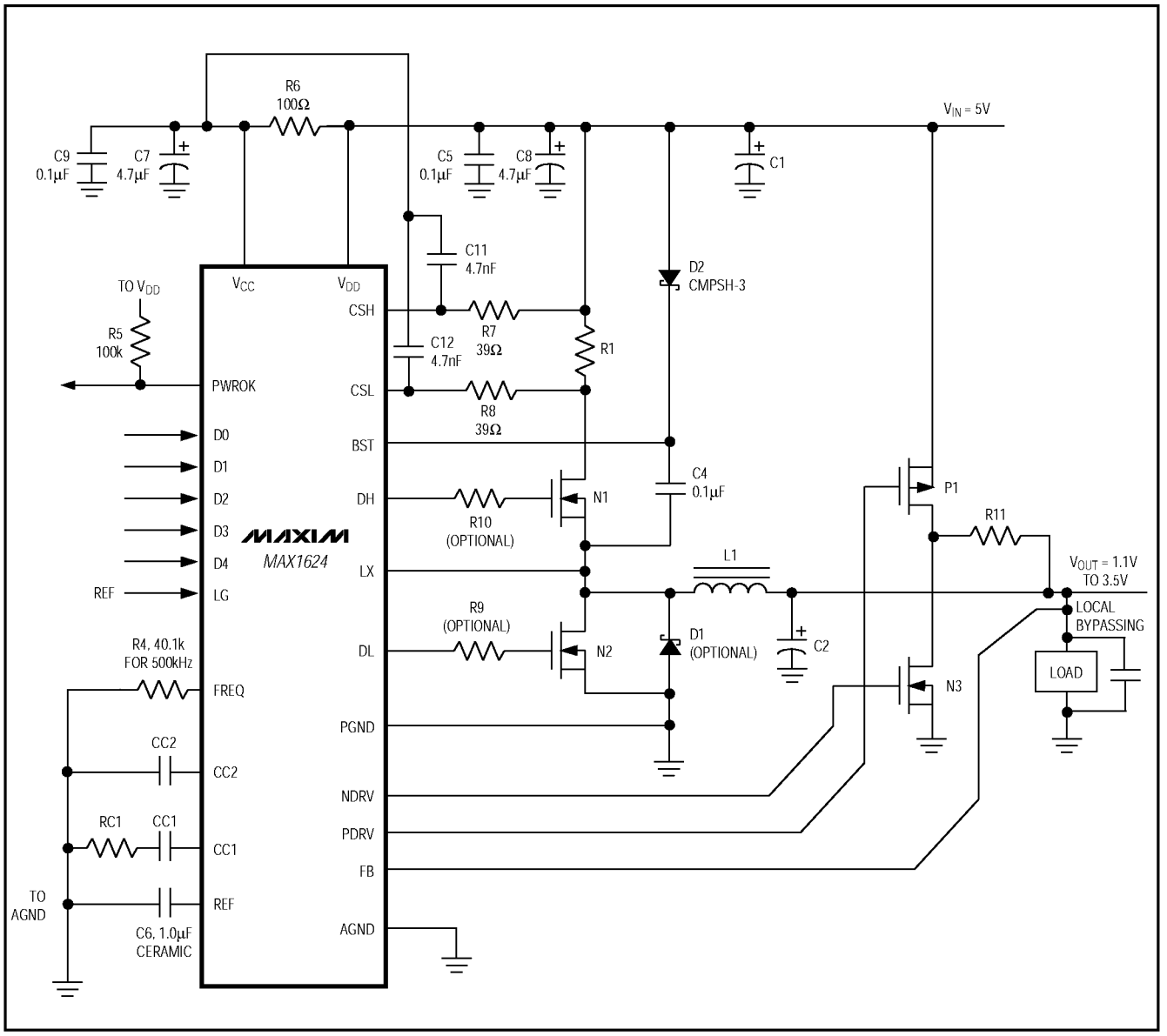


Figure 1. MAX1624 Standard Application Circuit

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

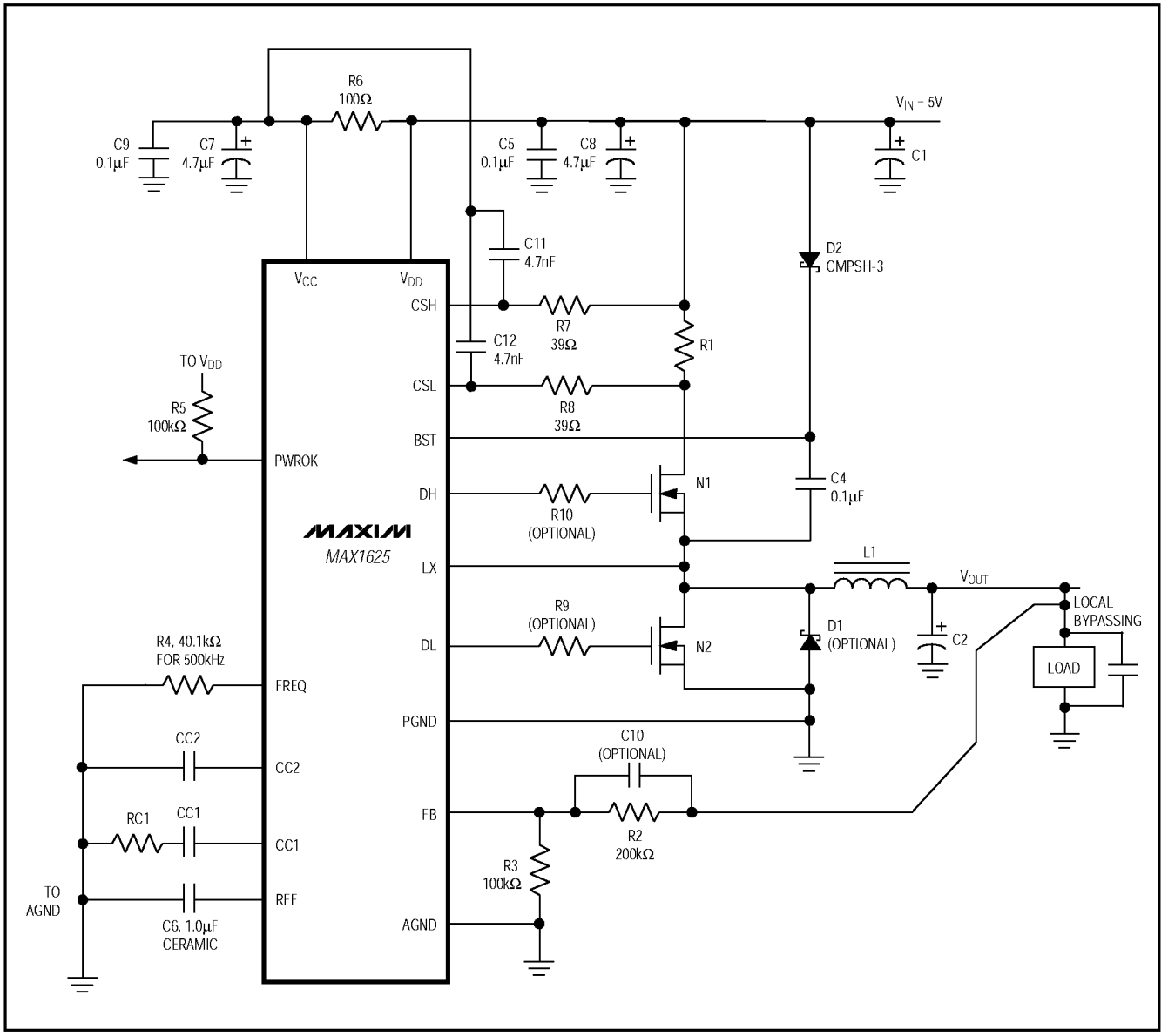


Figure 2. MAX1625 Standard Application Circuit

Table 1. Component List for Standard 3.3V Applications by Load Current* (Output Voltage = 3.3V, Frequency = 500kHz)

COMPONENT	DESCRIPTION BY LOAD CURRENT		
	6A	12A	11A (LOW-COST V_{RM})
Application Equipment	Power PC/Pentium/GTL bus termination	Pentium Pro	Pentium Pro
C1 Input Capacitor	100µF, 10V Sanyo OS-CON 10SL100M	3 x 100µF, 10V Sanyo OS-CON 10SL100M	3 x 2700µF, 6.3V aluminum electrolytic, Sanyo 6MV2700GX
C2 Output Capacitor	2 x 220µF, 4V Sanyo OS-CON 4SP220M	3 x 220µF, 4V Sanyo OS-CON 4SP220M	4 x 2700µF, 6.3V aluminum electrolytic, Sanyo 6MV2700GX
C10 Capacitor	Optional (see text)		
CC1 Capacitor	680pF ceramic	1000pF ceramic	1000pF ceramic
CC2 Capacitor	0.056µF ceramic	0.056µF ceramic	0.056µF ceramic
D1 Rectifier	Optional Schottky, Nihon NSQ03A02	Optional Schottky, Nihon NSQ03A02	Optional Schottky, Nihon NSQ03A02
D2 Rectifier	Central Semiconductor CMPSH-3	Central Semiconductor CMPSH-3	Central Semiconductor CMPSH-3
L1 Inductor	1.5µH, 8A Coiltronics UP2-1R5	0.5µH, 17A Coilcraft DO5022P-501HC	0.5µH Coiltronics UP4-R47, Coilcraft DO5022P-501HC
N1 High-Side MOSFET	International Rectifier IRF7413	International Rectifier IRL3103S, D^2PAK	International Rectifier IRF7413 x 2
N2 Low-Side MOSFET	International Rectifier IRF7413	International Rectifier IRL3103S, D^2PAK	International Rectifier IRF7413 x 2
N3/P1 (MAX1624)		International Rectifier IRF7107	
R1 Resistor	12mΩ Dale WSL-2512-R012-F	2 x 12mΩ in parallel, Dale WSL-2512-R012-F	2 x 12mΩ in parallel Dale WSL-2512-R012-F
R2 Resistor	200kΩ, 1% resistor	N/A	N/A
R3 Resistor	100kΩ, 1% resistor	N/A	N/A
R11 Resistor (MAX1624)		500mΩ Dale WSL-2512-R500	N/A
RC1 Resistor	1kΩ, 5% resistor	1kΩ, 5% resistor	1kΩ, 5% resistor

**MAX1624: LG = REF, D4–D0 = 10010.*

Table 2. Component Suppliers

SUPPLIER	USA PHONE	FACTORY FAX
AVX	(803) 946-0690	(803) 626-3123
Central Semiconductor	(516) 435-1110	(516) 435-1824
Coilcraft	(847) 639-6400	(847) 639-1469
Coiltronics	(561) 241-7876	(561) 241-9339
Dale Inductors	(605) 668-4131	(605) 665-1627
International Rectifier	(310) 322-3331	(310) 322-3332
IRC	(512) 992-7900	(512) 992-3377
Matsuo	(714) 969-2491	(714) 960-6492
Motorola	(602) 303-5454	(602) 994-6430
Murata-Erie	(814) 237-1431	(814) 238-0490
Nichicon	(847) 843-7500	(847) 843-2798
NIEC	(805) 867-2555*	[81] 3-3494-7414
Sanyo	(619) 661-6835	[81] 7-2070-1174
Siliconix	(408) 988-8000	(408) 970-3950
Sprague	(603) 224-1961	(603) 224-1430
Sumida	(847) 956-0666	[81] 3-3607-5144

**Distributor*

Table 3. MAX1624 Output Voltage Adjustment Settings (Abbreviated†)

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)	COMPATIBILITY
1	0	0	0	0	3.5	Intel-compatible codes
1	0	0	0	1	3.4	
1	—	—	—	—	Decreases in 100mV increments	
1	1	1	1	0	2.1	
1	1	1	1	1	No CPU (OFF)	
0	0	0	0	0	1.9	Non-Intel compatible codes
0	0	0	0	1	1.8	
0	0	—	—	—	Decreases in 100mV increments	
0	0	1	1	1	1.2	
0	1	0	0	0	1.1	
0	1	—	—	—	1.1	
0	1	1	1	0	1.1	
0	1	1	1	1	No CPU (OFF)	

†See Table 4 for a complete listing.

Standard Application Circuits

The predesigned MAX1624/MAX1625 circuits shown in Figures 1 and 2 meet a wide range of applications with output currents up to 12A and higher. Use Table 1 to select components appropriate for the desired output current range, and adapt the evaluation kit PC board layout as necessary. Table 2 lists suggested vendors. These circuits represent a good set of trade-offs between cost, size, and efficiency while staying within the worst-case specification limits for stress-related parameters, such as capacitor ripple current.

These MAX1624/MAX1625 circuits were designed for the specified frequencies. Do not change the switching frequency without first recalculating component values—particularly the inductance, output filter capacitance, and RC1 resistance values. Recalculate the voltage-feedback resistor and compensation-capacitor values (CC1 and CC2) as necessary to reconfigure them for different output voltages. Table 3 lists voltage adjustment DAC codes for the MAX1624.

Detailed Description

The MAX1624/MAX1625 are BiCMOS switch-mode, power-supply controllers designed for buck-topology regulators. They are optimized for powering the latest high-performance CPUs—demanding applications where output voltage precision, good transient response, and high efficiency are critical for proper operation. With appropriate external components, the MAX1624/MAX1625 deliver over 15A between 1.1V and 3.5V with ±1% accuracy. The MAX1625 offers 1% typical transient-load regulation from a +5V supply, while the MAX1624 offers a selectable transient-load regulation of 0.5%, 1%, or 2%. Remote output sensing ensures voltage precision by eliminating errors caused by PC board trace impedance. These controllers achieve 90% efficiency by using synchronous rectification.

A typical application circuit consists of two N-channel MOSFETs, a rectifier, and an LC output filter (Figure 1). At each of the internal oscillator's rising edges, the high-side MOSFET switch (N1) is turned on and allows current to ramp up through the inductor to the output filter capacitor and load, storing energy in a magnetic field. The current is monitored by reading the voltage

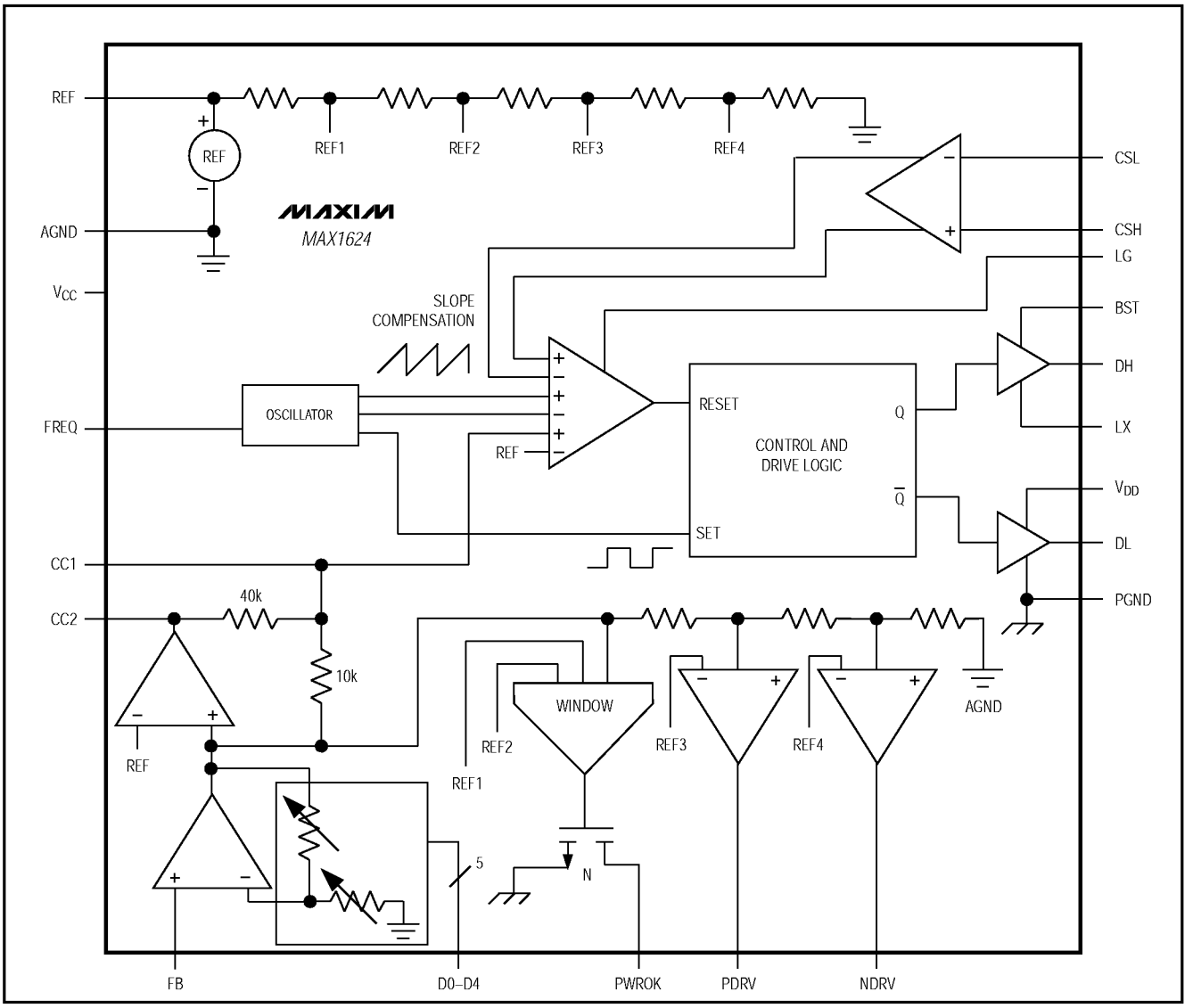


Figure 3. MAX1624 Simplified Block Diagram

across the current-sense resistor (R1). When the inductor current ramps up to the current-sense threshold, the MOSFET turns off and interrupts the flow of current from the supply. This causes the magnetic field in the inductor to collapse, resulting in a voltage surge that forces the rectifier diode (D1) or MOSFET body diode (N2) on and keeps the inductor current flowing in the same amplitude and direction. At this point, the synchronous rectifier MOSFET turns on until the end of the cycle to reduce conduction losses across the rectifier diode. The current through the inductor ramps back down, transferring the stored energy to the output filter capacitor and load. The output filter capacitor stores energy when inductor current is high and releases it when inductor current is low, smoothing the voltage delivered to the load.

The MAX1624/MAX1625 use a current-mode pulse-width-modulation (PWM) control scheme (Figures 3 and 4). The output voltage is regulated by switching at a constant frequency and then modulating the peak inductor current to change the energy transferred per pulse and to adjust to changes in the load. The output

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

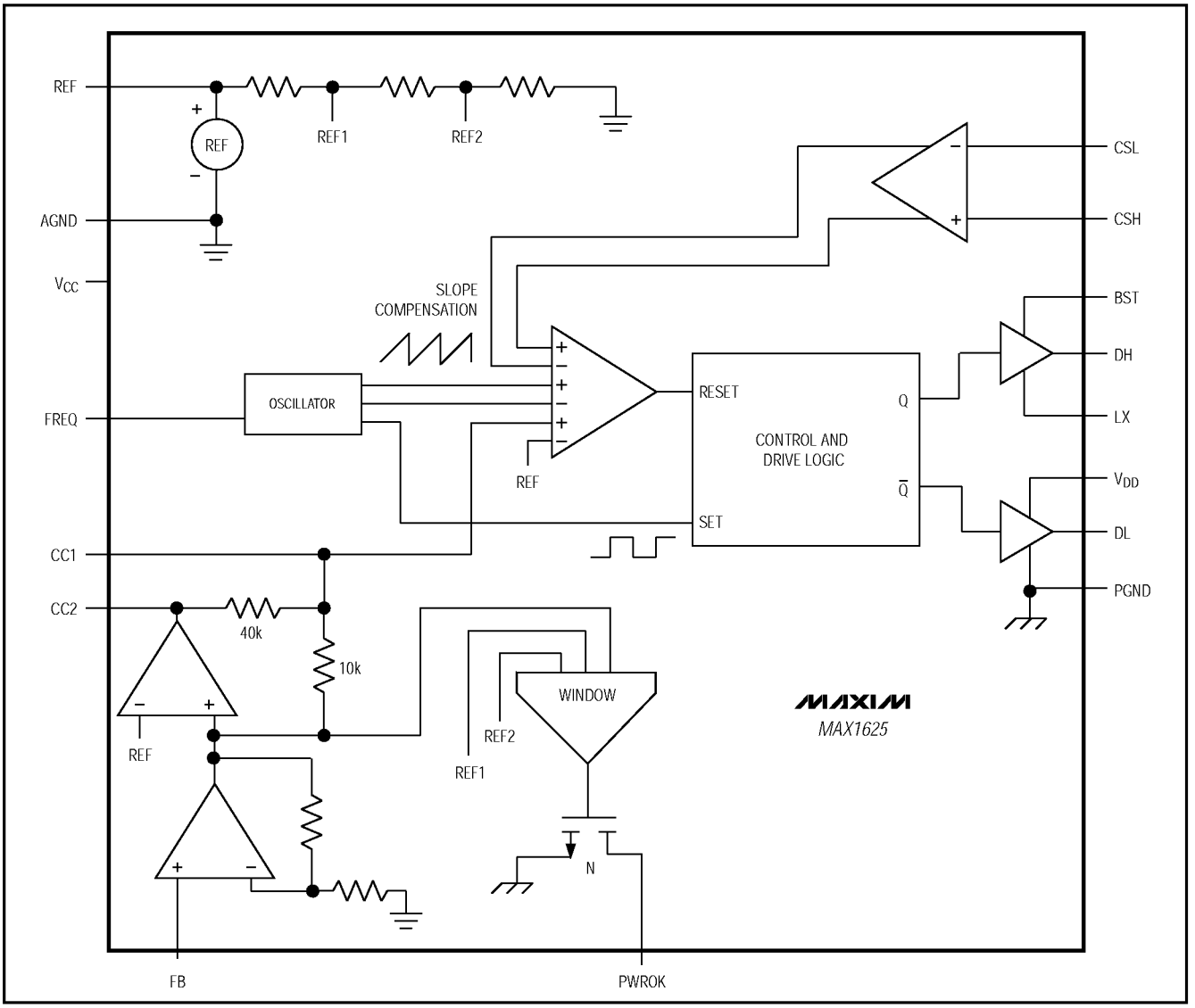


Figure 4. MAX1625 Simplified Block Diagram

voltage is the average of the AC voltage at the switching node, which is adjusted and regulated by changing the duty cycle of the MOSFET switches. Slope compensation is necessary to stabilize current-mode feedback controllers with a duty cycle greater than 50%. Maximum duty cycle is greater than 85% (see *Typical Operating Characteristics*).

PWM Controller Block and Integrator

The heart of the current-mode PWM controller is a multi-input open-loop comparator that sums three signals: the buffered feedback signal, the current-sense signal, and the slope-compensation ramp. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage. The output voltage error signal is generated by an error amplifier that compares the amplified feedback voltage to an internal reference.

Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch for a period determined by the duty factor (approximately V_{OUT} / V_{IN}). The current-mode feedback system regulates the peak inductor current as a function of the output voltage

error signal. Since average inductor current is nearly the same as peak current (assuming the inductor value is set relatively high to minimize ripple current), the circuit acts as a switch-mode transconductance amplifier. It pushes the second output LC filter pole, normally found in a duty-factor-controlled (voltage-mode) PWM, to a higher frequency. To preserve inner-loop stability and eliminate regenerative inductor current staircasing, a slope-compensation ramp is summed into the main PWM comparator. As the high-side switch turns off, the synchronous rectifier latch is set. The low-side switch turns on 30ns later and stays on until the beginning of the next clock cycle. Under fault conditions where the inductor current exceeds the maximum current-limit threshold, the high-side latch resets, and the high-side switch turns off.

Internal Reference

The internal 3.5V reference (REF) is accurate to ±1% from 0 ℃ to +85 ℃, making REF useful as a system reference. Bypass REF to AGND with a 0.1µF (min) ceramic capacitor. A larger value (such as 1µF) is recommended for high-current applications. Load regulation is 10mV for loads up to 100µA. Loading REF reduces the main output voltage slightly, according to the reference-voltage load-regulation error (see *Typical Operating Characteristics*). Reference undervoltage lockout is between 2.7V and 3V. Short-circuit current is less than 4mA.

Synchronous-Rectifier Driver

Synchronous rectification reduces conduction losses in the rectifier by shunting the normal Schottky diode or MOSFET body diode with a low-on-resistance MOSFET switch. The synchronous rectifier also ensures proper start-up by precharging the boost-charge pump used for the high-side switch gate-drive circuit. Thus, if you must omit the synchronous power MOSFET for cost or other reasons, replace it with a small-signal MOSFET, such as a 2N7002.

The DL drive waveform is simply the complement of the DH high-side drive waveform (with typical controlled dead time of 30ns to prevent cross-conduction or shoot-through). The DL output's on-resistance is 0.7Ω (typ) and 2Ω (max).

BST High-Side Gate-Driver Supply and MOSFET Drivers

Gate-drive voltage for the high-side N-channel switch is generated using a flying-capacitor boost circuit (Figure 5). The capacitor is alternately charged from the +5V supply and placed in parallel with the high-side MOSFET's gate and source terminals.

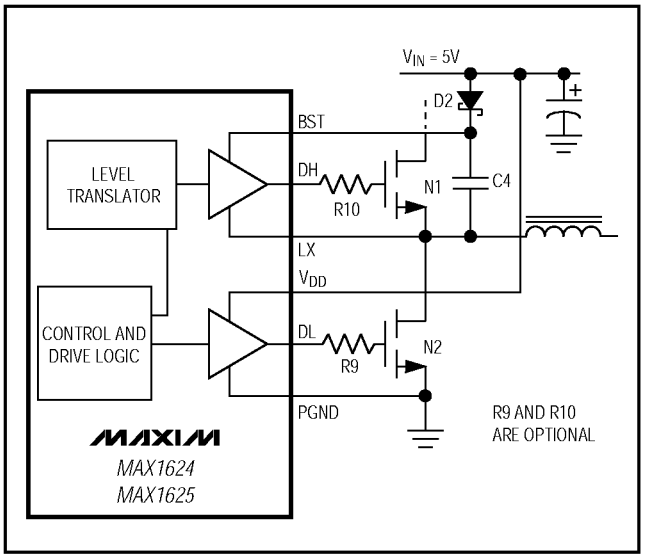


Figure 5. Boost Supply for Gate Drivers

On start-up, the synchronous rectifier (low-side MOSFET) forces LX to 0V and precharges the BST capacitor (C4) to 5V through a diode (D2). This provides the necessary enhancement voltage to turn on the high-side switch. On the next half-cycle, the PWM control logic turns on the high-side MOSFET by closing an internal switch between BST and DH. As the MOSFET turns on, the LX node rises to the input voltage, an action that boosts the 5V gate-drive signal above the +5V supply. DH on-resistance is 0.7Ω (typical) and 2Ω (max). Do not bias D2 with voltages greater than 5.5V, as this will destroy the DH gate driver.

A 0.1µF minimum ceramic capacitor is recommended for the boost supply. Use a low-power, SOT23 Schottky diode to minimize reduction of the gate drive from the diode's forward voltage. Use a low-leakage Schottky diode, such as a CMPSH-3 from Central Semiconductor or a 1N4148, to prevent reverse leakage from discharging the BST capacitor when the ambient temperature is high. Place the BST capacitor and diode within 0.4 in. (10mm) of the BST pin.

Gate-drive resistors (R9 and R10) can often be useful to reduce jitter in the switching waveforms by slowing down the fast-slewing LX node and reducing ground bounce at the controller IC. Low-valued resistors from around 1Ω to 5Ω are sufficient for many applications.

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GlitchCatcher Current-Boost Driver (MAX1624)

Drivers for an optional current-boost circuit are included in the MAX1624 to improve transient response. Some dynamically clocked CPUs switch computational blocks on and off as needed to reduce power consumption, and can generate load steps of several amperes in a few tens of nanoseconds. The current-boost circuit is intended to improve transient response to such load steps by bypassing the inductor's lowpass filter operation. When the output drops out of regulation by more than ±1.5% to ±2.5%, the P-channel or N-channel switches turn on and force the output back into regulation. The MOSFET drivers' response time is typically 75ns, and their minimum on-time is typically 100ns.

Current Sense and Overload Current Limiting

The current-sense circuit resets the main PWM latch and turns off the high-side MOSFET switch whenever the voltage difference between CSH and CSL from current through the sense resistor (R1) exceeds the peak current limit (100mV typical).

Current-mode control offers a practical level of overload protection in response to many fault conditions. During normal operation, maximum output current is enforced by the peak current limit. If the output is shorted directly to GND through a low-resistance path, the current-sense comparator may be unable to enforce a current limit. Under such conditions, circuit parasitics such as MOSFET $R_{DS(ON)}$ typically limit the short-circuit current to a value around the peak-current-limit setting.

Attach a lowpass-filter network between the current-sense pins and resistor to reduce high-frequency common-mode noise (Figure 6). The filter should be designed with a time constant of around 200ns. Resistors in the 20Ω to 100Ω range are recommended for R7 and R8. Connect the filter capacitors C11 and C12 from V_{CC} to CSH and CSL, respectively.

Values of 39Ω and 4.7nF are suitable for many designs. Place the current-sense filter network close to the IC, within 0.1 in. (2.5mm) of the CSH and CSL pins.

Internal Soft-Start

Soft-start allows a gradual increase of the internal current limit at start-up to reduce input surge currents. In the MAX1624/MAX1625, an internal DAC raises the current-limit threshold from 0V to 100mV in four steps (25mV, 50mV, 75mV, and 100mV) over the span of 1536 oscillator cycles.

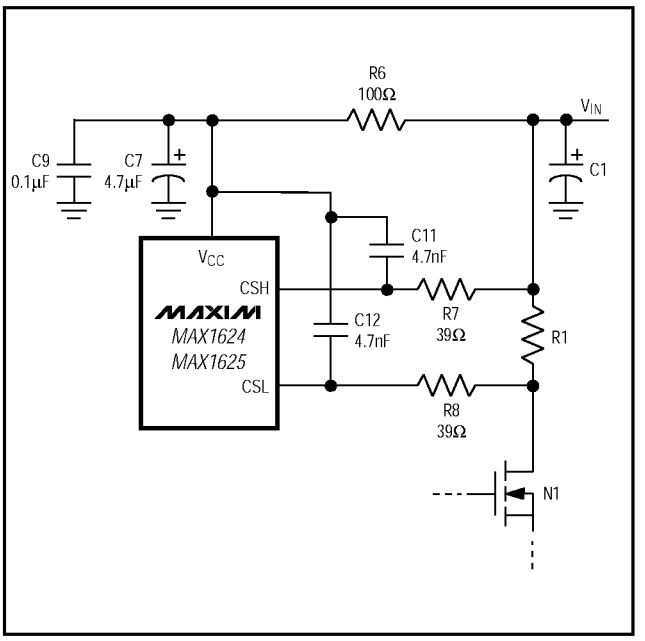

Figure 6. Current-Sense Filter

Design Procedure

Setting the Output Voltage

MAX1624

Select the output voltage using the D0–D4 pins. The MAX1624 uses an internal 5-bit DAC as a feedback-resistor voltage divider. The output voltage can be digitally set in 100mV increments from 1.1V to 3.5V using the D0–D4 inputs (Table 4).

D0–D4 are logic inputs and accept both TTL and CMOS voltage levels. The MAX1624 has both FB and AGND inputs, allowing a Kelvin connection for remote voltage and ground sensing to eliminate the effects of trace resistance on the feedback voltage. (See *PC Board Layout Considerations* for further details.) FB input current is 0.1µA (max).

The MAX1624 DAC codes were designed for compatibility with Intel specifications for output voltages between 3.5V and 2.1V. Codes 10000 through 11110 are compatible with Intel specifications, while codes 00000 through 01111 are not. Codes 11111 and 01111 turn off the buck controller, placing the IC in a low-current mode (0.2mA typical). For compatibility with Intel codes for output voltages below 2.1V, see the MAX1638/MAX1639 data sheet.

Table 4. Output Voltage-Adjustment Settings

D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)	COMPATIBILITY
1	0	0	0	0	3.5	Intel-compatible DAC codes
1	0	0	0	1	3.4	
1	0	0	1	0	3.3	
1	0	0	1	1	3.2	
1	0	1	0	0	3.1	
1	0	1	0	1	3.0	
1	0	1	1	0	2.9	
1	0	1	1	1	2.8	
1	1	0	0	0	2.7	
1	1	0	0	1	2.6	
1	1	0	1	0	2.5	
1	1	0	1	1	2.4	
1	1	1	0	0	2.3	
1	1	1	0	1	2.2	
1	1	1	1	0	2.1	
1	1	1	1	1	No CPU (off)	
0	0	0	0	0	1.9	Non-Intel-compatible DAC codes
0	0	0	0	1	1.8	
0	0	0	1	0	1.7	
0	0	0	1	1	1.6	
0	0	1	0	0	1.5	
0	0	1	0	1	1.4	
0	0	1	1	0	1.3	
0	0	1	1	1	1.2	
0	1	0	0	0	1.1	
0	1	0	0	1	1.1	
0	1	—	—	—	1.1	
0	1	1	1	0	1.1	
0	1	1	1	1	No CPU (off)	

MAX1625

Set the output voltage by connecting R2 and R3 (Figure 7) to the FB pin from the output to AGND. R2 is given by the following equation:

$$R2 = R3 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

where V_{FB} = 1.1V. Since the input bias current at FB has a maximum value of ±0.1µA, values up to 100kΩ can be used for R3 with no significant accuracy loss. Values under 1kΩ are recommended to improve noise immunity and minimize parasitic capacitance at the FB node. Place R2 and R3 very close to the MAX1625, within 0.2 in. (5mm) of the FB pin.

Selecting the Oscillator Frequency

Set the switching frequency between 100kHz and 1MHz by connecting a resistor from FREQ to AGND. Select the resistor according to the following equation:

$$R4 = \frac{2 \times 10^{10}}{f_{OSC}}$$

Low-frequency operation reduces controller IC quiescent current and improves efficiency. High-frequency operation reduces cost and PC board area by allowing the use of smaller inductors and fewer and smaller output capacitors. Inductor energy-storage requirements and output capacitor requirements at 1MHz are one-third those at 300kHz.

Choosing the Error-Amplifier Gain (MAX1624)

Set the error-amplifier gain to match the voltage-precision requirements of the CPU used. The MAX1624's loop-gain control input (LG) allows trade-offs in DC/AC voltage accuracy versus output filter capacitor requirements. AC load regulation can be set to 0.5%, 1%, or 2% by connecting LG as shown in Table 5. The MAX1625's default AC regulation is 1%.

DC load regulation is typically 10 times better than AC load regulation, and is determined by the gain set by the LG pin.

Table 5. LG Pin Adjustment Settings

LG CONNECTED TO	AC LOAD-REGULATION ERROR (%)	DC LOAD-REGULATION ERROR (%)	TYPICAL A_E (V_{GAIN}/I_{GAIN})
V_{CC}	2	0.2	2
REF	1	0.1	4
GND	0.5	0.05	8

Specifying the Inductor

Three key inductor parameters must be specified: inductance value (L), peak current (I_{PEAK}), and DC resistance (R_{DC}). The following equation includes a constant LIR, which is the ratio of inductor peak-to-peak AC current to DC load current. A higher LIR value allows for smaller inductors and better transient response, but results in higher losses and output ripple.

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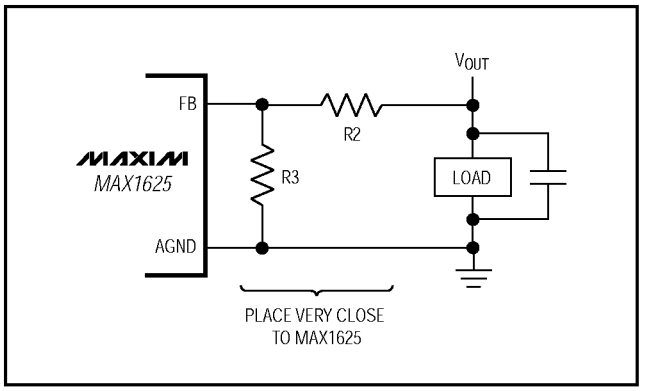


Figure 7. MAX1625 Adjustable Output Operation

A good compromise between size and loss is a 45% ripple current to load current ratio (LIR = 0.45), which corresponds to a peak inductor current 1.23 times higher than the DC load current.

$$L = \frac{V_{OUT}\left(V_{IN(MAX)} - V_{OUT}\right)}{V_{IN(MAX)} \times f_{OSC} \times I_{OUT} \times LIR}$$

where f is the switching frequency, between 100kHz and 1MHz; I_{OUT} is the maximum DC load current; and LIR is the ratio of AC to DC inductor current (typically 0.45). The exact inductor value is not critical and can be adjusted to make trade-offs among size, transient response, cost, and efficiency. Although lower inductor values minimize size and cost, they also reduce efficiency due to higher peak currents. In general, higher inductor values increase efficiency, but at some point resistive losses due to extra turns of wire exceed the benefit gained from lower AC current levels. Load-transient response can be adversely affected by high inductor values, especially at low (V_{IN} - V_{OUT}) differentials.

The peak inductor current at full load is 1.23 x I_{OUT} if the previous equation is used; otherwise, the peak current can be calculated using the following equation:

$$I_{PEAK} = I_{OUT} + \frac{V_{OUT}\left(V_{IN(MAX)} - V_{OUT}\right)}{2f_{OSC} \times L \times V_{IN(MAX)}}$$

The inductor's DC resistance is a key parameter for efficient performance, and should be less than the current-sense resistor value.

Calculating the Current-Sense Resistor Value

Calculate the current-sense resistor value according to the worst-case minimum current-limit threshold voltage (from the *Electrical Characteristics*) and the peak inductor current required to service the maximum load. Use I_{PEAK} from the equation in the section *Specifying the Inductor*.

$$R_{SENSE} = \frac{85mV}{I_{PEAK}}$$

The high inductance of standard wire-wound resistors can degrade performance. Low-inductance resistors, such as surface-mount power metal-strip resistors, are preferred. The current-sense resistor's power rating should be higher than the following:

$$R_{POWER\ RATING} = \frac{(115mV)^2}{R_{SENSE}}$$

In high-current applications, connect several resistors in parallel as necessary, to obtain the desired resistance and power rating.

Selecting the Output Filter Capacitor

Output filter capacitor values are generally determined by effective series resistance (ESR) and voltage-rating requirements, rather than by the actual capacitance value required for loop stability. Due to the high switching currents and demanding regulation requirements in a typical MAX1624/MAX1625 application, use only specialized low-ESR capacitors intended for switching-regulator applications, such as AVX TPS, Sprague 595D, Sanyo OS-CON, or Nichicon PL series. Do not use standard aluminum-electrolytic capacitors, which can cause high output ripple and instability due to high ESR. The output voltage ripple is usually dominated by the filter capacitor's ESR, and can be approximated as I_{RIPPLE} x R_{ESR}. To ensure stability, the capacitor must meet *both* minimum capacitance and maximum ESR values as given in the following equations:

$$C_{OUT} > \frac{V_{REF}\left(1 + \frac{V_{OUT}}{V_{IN(MIN)}}\right)}{V_{OUT} \times R_{SENSE} \times f_{OSC}}$$

$$R_{ESR} < R_{SENSE}$$

Compensating the Feedback Loop

The feedback loop needs proper compensation to prevent excessive output ripple and poor efficiency caused by instability. Compensation cancels unwanted poles and zeros in the DC-DC converter's transfer function that are due to the power-switching and filter elements with corresponding zeros and poles in the feedback network. These compensation zeros and poles are set by the compensation components CC1, CC2, and RC1. The objective of compensation is to ensure stability by ensuring that the DC-DC converter's phase shift is less than 180 ° by a safe margin, at the frequency where the loop gain falls below unity.

One simple method for ensuring adequate phase margin is to place pole-zero pairs to approximate a single-pole response with a -20dB/decade slope all the way to unity-gain crossover (Figure 8). (Other compensation schemes are possible.) The order of undesired poles and zeros may differ from that shown in Figure 8, depending on the characteristics of the load, output filter capacitor, switching frequency, and inductor. These procedures are guidelines only, and empirical experimentation is needed to select the compensation components' final values.

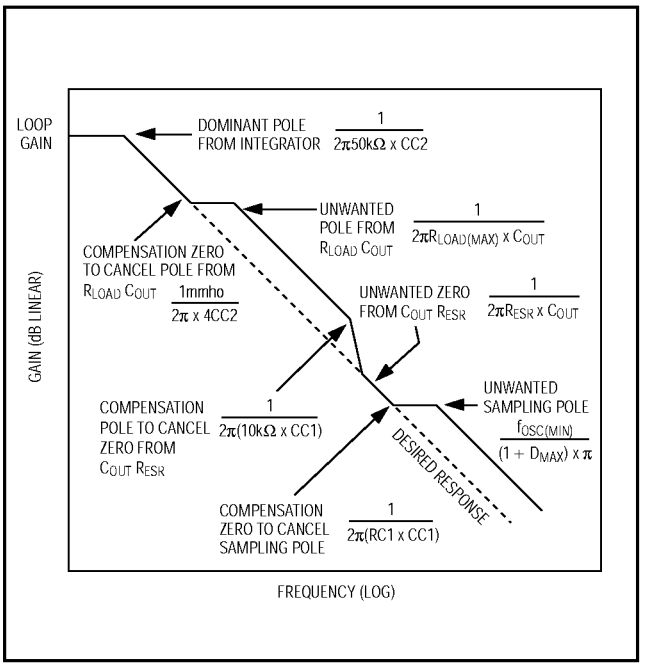


Figure 8. MAX1624/MAX1625 Bode Plot with Compensation Poles and Zeros

Canceling the Sampling Pole and Output Filter ESR Zero

Compensate the fast-voltage feedback loop by connecting a resistor and a capacitor in series from the CC1 pin to AGND. The pole from CC1 can be set to cancel the zero from the filter-capacitor ESR. Thus the capacitor at CC1 should be as follows:

$$CC1 = \frac{C_{OUT} \times R_{ESR}}{10k\Omega}$$

Resistor RC1 sets a zero that can be used to compensate for the sampling pole generated by the switching frequency. Set RC1 to the following:

$$RC1 = \frac{\left(1 + \frac{V_{OUT}}{V_{IN}}\right)}{2f_{OSC} \times CC1}$$

The CC1 pin's output resistance is 10kΩ. In the sampling pole equation (Figure 8), D_{MAX} is the maximum duty cycle, or $V_{OUT} / V_{IN(MIN)}$.

Setting the Dominant Pole and Canceling the Load and Output Filter Pole

Compensate the slow-voltage feedback loop by adding a ceramic capacitor from the CC2 pin to AGND. This is an integrator loop used to cancel out the DC load-regulation error. Selection of capacitor CC2 sets the dominant pole and a compensation zero. The zero is typically used to cancel the unwanted pole generated by the load and output filter capacitor at the maximum load current. Select CC2 to place the zero close to or slightly lower than the frequency of the unwanted pole, as follows:

$$CC2 = \frac{1mmho \times C_{OUT}}{4} \times \frac{V_{OUT}}{I_{OUT(MAX)}}$$

The transconductance of the integrator amplifier at CC2 is 1mmho. The voltage swing at CC2 is internally clamped around 2.4V to 3V minimum and 4V to V_{CC} maximum to improve transient response times. CC2 can source and sink up to 100µA.

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Calculating the Loop Gain (Optional)

The loop gain is an important parameter in alternative compensation schemes:

$$\text{Loop Gain (dB)} = 20\text{Log}\left(A_E \frac{V_{REF}}{V_{OUT}} \times \frac{R_{LOAD}}{R_{CS}} \times A_I\right)$$

$$= 20\text{Log}\left(A_E \frac{V_{REF}}{85mV} \times 10\right)$$

where A_E is the error-comparator relative gain, and A_I = 10 is the integrator gain. A_E is 4 for the MAX1625, but it is 2, 4, or 8 for LG pin settings of V_{CC}, REF, or AGND, respectively, for the MAX1624.

Feed-Forward Compensation (MAX1625)

An optional compensation capacitor, typically 220pF, may be needed across the upper feedback resistor to counter the effects of stray capacitance on the FB pin, and to help ensure stable operation when high-value feedback resistors are used (Figure 9). Empirically adjust the feed-forward capacitor as needed.

Choosing the MOSFET Switches

The two high-current N-channel MOSFETs must be logic-level types with guaranteed on-resistance specifications at V_{GS} = 4.5V. Lower gate-threshold specs are better (i.e., 2V max rather than 3V max). Gate charge should be less than 100nC to minimize switching losses and reduce power dissipation.

I^2R losses are the greatest heat contributor to MOSFET power dissipation and are distributed between the high- and low-side MOSFETs according to duty factor, as follows:

$$P_D \text{ (high side)} = I_{LOAD}^2 \times R_{DS(ON)} \times \frac{V_{OUT}}{V_{IN}}$$

$$P_D \text{ (low side)} = I_{LOAD}^2 \times R_{DS(ON)} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

$$P_D \text{ (low side, shorted)} = I_{LIMIT}^2 \times R_{DS(ON)}$$

where $I_{LIMIT} = 115mV / R_{SENSE}$.

Switching losses affect the upper MOSFET only, and are insignificant at 5V input voltages. Gate-charge losses are dissipated in the IC, and do not heat the MOSFETs. Ensure that both MOSFETs are at a safe junction temperature by calculating the temperature rise according to package thermal-resistance specifications. The high-side MOSFET's worst-case dissipation occurs at the maximum output voltage and minimum input voltage. For the low-side MOSFET, the worst case is at the maximum input voltage when the output is short-circuited (consider the duty factor to be 100%).

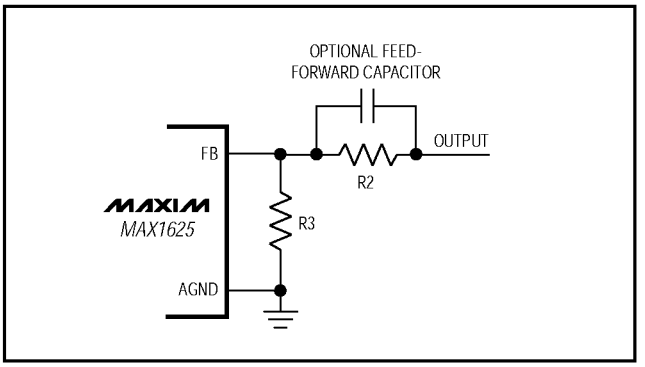


Figure 9. MAX1625 Optional Feed-Forward Compensation Capacitors

Selecting the Rectifier Diode

The rectifier diode D1 is a clamp that catches the negative inductor swing during the 30ns typical dead time between turning off the high-side MOSFET and turning on the low-side MOSFET synchronous rectifier. D1 must be a Schottky diode, to prevent the MOSFET body diode from conducting. It is acceptable to omit D1 and let the body diode clamp the negative inductor swing, but efficiency will drop 1% or 2% as a result. Use a 1N5819 diode for loads up to 3A, or a 1N5822 for loads up to 10A.

Adding the BST Supply Diode and Capacitor

A signal diode, such as a 1N4148, works well for D2 in most applications, although a low-leakage Schottky diode provides slightly improved efficiency. Do not use large power diodes, such as the 1N4001 or 1N5817. Exercise caution in the selection of Schottky diodes, since some types exhibit high reverse leakage at high operating temperatures. Bypass BST to LX using a 0.1µF capacitor.

Selecting the Input Capacitors

Place a 0.1µF ceramic capacitor and 4.7µF capacitor between V_{CC} and AGND, as well as between V_{DD} and PGND, within 0.2 in. (5mm) of the V_{CC} and V_{DD} pins.

Select low-ESR input filter capacitors with a ripple-current rating exceeding the RMS input ripple current, connecting several capacitors in parallel if necessary. RMS input ripple current is determined by the input voltage and load current, with the worst-possible case occurring at V_{IN} = 2 x V_{OUT}:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}\,(V_{IN} - V_{OUT})}}{V_{IN}}$$

$$I_{RMS} = I_{OUT} / 2 \text{ when } V_{IN} = 2V_{OUT}$$

Bypassing the Internal Reference

Bypass the internal 3.5V reference at the REF pin by connecting a 0.1µF capacitor to AGND. Use a larger value, such as 1µF, for high-current applications.

Choosing the GlitchCatcher MOSFETs

P-channel and N-channel switches and a series resistor are required for the current-boost circuit (Figure 10). Current through the MOSFETs and current-limiting resistors must be sufficient to supply the load current, with enough extra for prompt output regulation without excessive overshoot. Design for boost-current values 1.5 times the maximum load current, and choose MOSFETs and current-limiting resistors such that:

$$R_{DSON,P(MAX)} + R_{LIMIT} \approx \frac{V_{IN} - V_{OUT}}{1.5\ I_{OUT(MAX)}}$$

and

$$R_{DSON,N(MAX)} + R_{LIMIT} \approx \frac{V_{OUT}}{1.5\ I_{OUT(MAX)}}$$

Applications Information

Efficiency Considerations

Refer to the MAX796–MAX799 data sheet for information on calculating losses and improving efficiency.

PC Board Layout Considerations

Good PC board layout and routing are *required* in high-current, high-frequency switching power supplies to achieve good regulation, high efficiency, and stability. The PC board layout artist must be provided with explicit instructions concerning the placement of power-switching components and high-current routing.

It is strongly recommended that the evaluation kit PC board layouts be followed as closely as possible. Contact Maxim's Applications Department concerning the availability of PC board examples for higher-current circuits.

In most applications, the circuit is on a multilayer board, and full use of the four or more copper layers is recommended. Use the top layer for high-current power and ground connections. Leave the extra copper on the board as a pseudo-ground plane. Use the bottom layer for quiet connections (REF, FB, AGND), and the inner layers for an uninterrupted ground plane. A ground plane and pseudo-ground plane are essential for reducing ground bounce and switching noise.

Follow these steps:

1) Place the high-power components (C1, R1, N1, D1, N2, L1, and C2 in Figure 1) as close together as possible, following these priorities:

- **Minimize ground-trace lengths** in high-current paths. The surface-mount power components should be butted up to one another with their ground terminals almost touching. Connect their ground terminals using a wide, filled zone of top-layer copper (the pseudo-ground plane), rather than through the internal ground plane. At the output terminal, use vias to connect the top-layer pseudo-ground plane to the normal inner-layer ground plane at the output filter capacitor ground terminals. This minimizes interference from IR drops and ground noise, and ensures that the IC's AGND is sensing at the supply's output terminals.

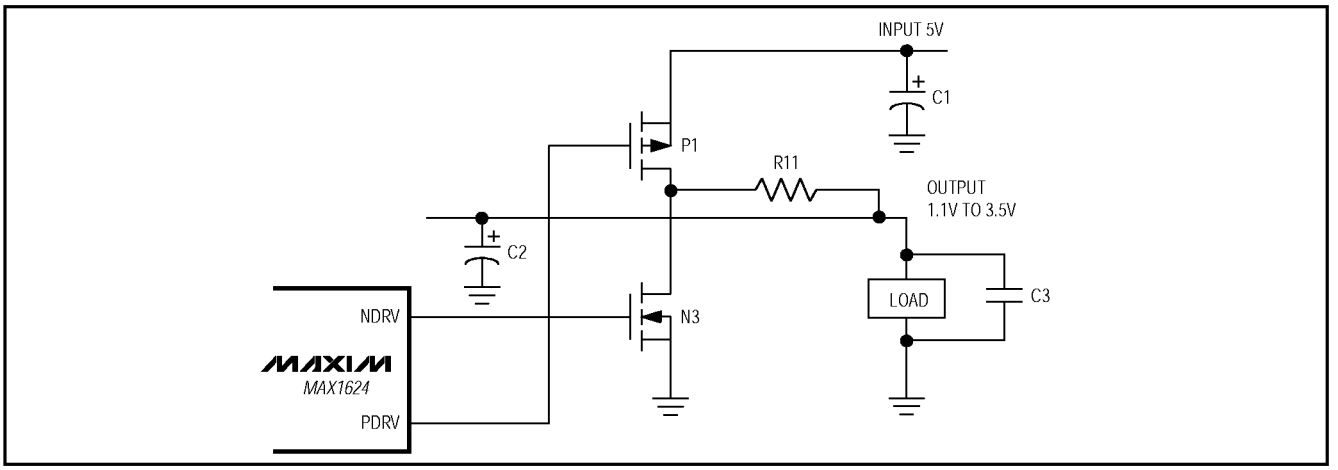


Figure 10. GlitchCatcher Circuit

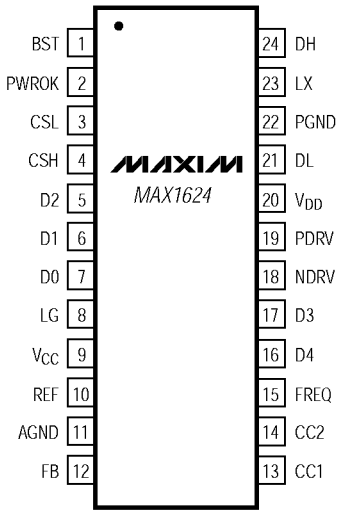
- **Minimize high-current path trace lengths.** Use very short and wide traces. From C1 to N1: 0.4 in. (10mm) max length; D1 cathode to N2: 0.2 in. (5mm) max length; LX node (N1 source, N2 drain, D1 cathode, inductor L1): 0.6 in. (15mm) max length.

2) Place the MAX1624/MAX1625 and supporting components following these rules:

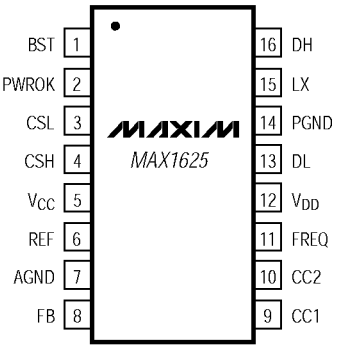
- **Minimize trace lengths to the current-sense resistor.** The IC must be no farther than 0.4 in. (10mm) from the current-sense resistor. Use a Kelvin connection.
- **Minimize ground trace lengths between the MAX1624/MAX1625 and supporting components.** Connect components for the REF, CC1, CC2, and FREQ pin directly to AGND. Connect AGND and PGND at the IC.
- **Keep noisy nodes and components away from sensitive analog nodes,** such as the current-sense, voltage-feedback, REF, CC1, CC2, and FREQ pins. Placing the IC and analog components on the opposite side of the board from the power-switching node is desirable. Noisy nodes include the main switching node (LX), inductor, and gate-drive outputs.
- **Place components for the FREQ, REF, CC1, and CC2 pins as close to the IC as possible,** within 0.2 in. (5mm).
- Keep the gate-drive traces (DH, DL, and BST) shorter than 20mm, and route them away from CSH, CSL, REF, FB, etc.
- Filter the V_{CC} supply input to the IC. Bypass the IC directly from V_{DD} to PGND using a 0.1µF ceramic capacitor and 4.7µF electrolytic capacitor placed within 0.2 in. (5mm) of the IC.
- Place the voltage-feedback components close to the FB pin of the MAX1625, within 0.2 in. (5mm). Connect the voltage-feedback trace directly to the CPU's power input and route it to avoid noisy traces.

Pin Configurations

TOP VIEW



SSOP



SO

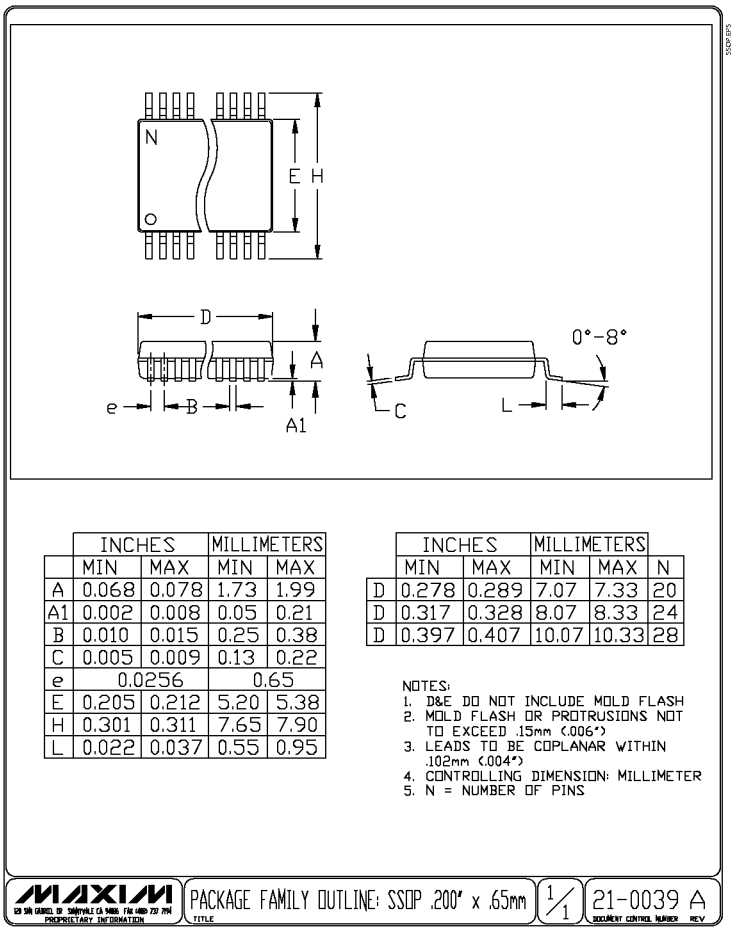
Chip Information

TRANSISTOR COUNT: 2472

SUBSTRATE CONNECTED TO AGND

High-Speed Step-Down Controllers with Synchronous Rectification for CPU Power

Package Information



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.068	0.078	1.73	1.99
A1	0.002	0.008	0.05	0.21
B	0.010	0.015	0.25	0.38
C	0.005	0.009	0.13	0.22
e	0.0256		0.65	
E	0.205	0.212	5.20	5.38
H	0.301	0.311	7.65	7.90
L	0.022	0.037	0.55	0.95

	INCHES		MILLIMETERS		
	MIN	MAX	MIN	MAX	N
D	0.278	0.289	7.07	7.33	20
D	0.317	0.328	8.07	8.33	24
D	0.397	0.407	10.07	10.33	28

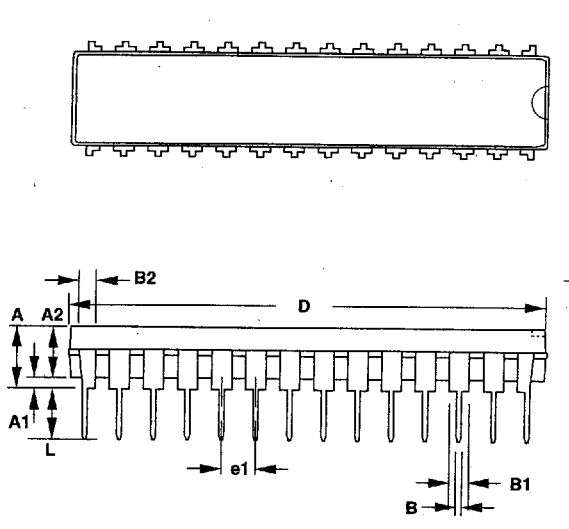
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX 408/737 7194 PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SSOP .200" x .65mm (TITLE)

1/1

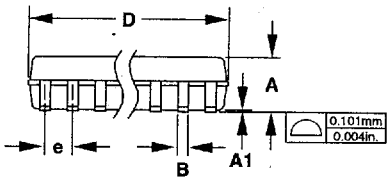
21-0039 A (DOCUMENT CONTROL NUMBER) (REV)

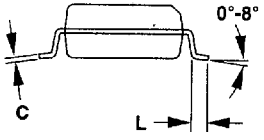


DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.180	–	4.572
A1	0.020	–	0.508	–
A2	0.125	0.150	3.175	3.810
B	0.015	0.022	0.381	0.559
B1	0.045	0.060	1.143	1.524
B2	0.035	0.045	0.889	1.143
C	0.008	0.012	0.203	0.305
D	1.350	1.380	34.290	35.052
E	0.300	0.325	7.620	8.255
E1	0.275	0.295	6.985	7.493
e1	0.100 BSC		2.54 BSC	
eA	0.300 BSC		7.62 BSC	
L	0.115	0.150	2.921	3.810
α	0°	15°	0°	15°

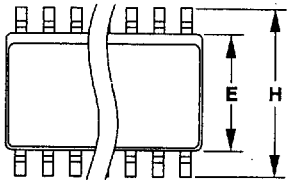
21-0400A

Narrow Plastic DIP
28-PIN PLASTIC
DUAL-IN-LINE
PACKAGE
(0.300 in.)





DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
E	0.150	0.157	3.80	4.00
e	0.050		1.27	
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27



Narrow SO
SMALL-OUTLINE
PACKAGE
(0.150 in.)

DIM	PINS	INCHES		MILLIMETERS	
		MIN	MAX	MIN	MAX
D	8	0.189	0.197	4.80	5.00
D	14	0.337	0.344	8.55	8.75
D	16	0.386	0.394	9.80	10.00

21-0041A