DESCRIPTION

The HYM5V64124A is a 1M x 64-bit EDO mode CMOS DRAM module consisting of four HY51V18164B in 42/42 pin SOJ or 44/50 pin TSOP-II and one 2048 bit EEPROM on a 168 pin glass-epoxy printed circuit board. 0.1μF and 0.01μF decoupling capacitors are mounted for each DRAM. The HYM5V64124ARG/ATRG/ASLRG/ASLTRG is Gold plated socket type Dual In-line Memory Modules suitable for easy interchange and addition of 8M byte memory.

FEATURES

- **Low power dissipation**
  Max. self-refresh 5.0mW (SL-part)
  Max. battery back-up 6.5mW (SL-part)
  Max. CMOS standby 2.9mW (SL-part)
  14.4mW
  Max. TTL standby 28.8mW
  Max. operating

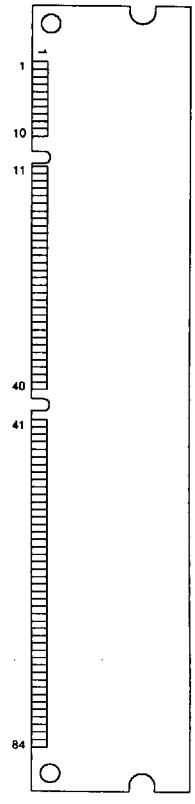
Speed	Power
60	2.45W
70	2.16W
80	1.87W

- **Single power supply of 3.3V± 10%**
- **TTL compatible inputs and outputs**
- **Fast access time**

Speed	tRAC	tCAC	tHPC
60	60ns	15ns	25ns
70	70ns	20ns	30ns
80	80ns	20ns	35ns

- **EDO mode operation**
- **$\overline{CAS}$-before-$\overline{RAS}$, $\overline{RAS}$-only, Hidden refresh and Self-refresh**
- **1024 refresh cycles / 256ms (SL-part)**
  1024 refresh cycles / 16ms
- **Serial Presence Detect**

PIN CONNECTION



PIN DESCRIPTION

$\overline{RAS0}$,$\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS7}$	Column Address Strobe
$\overline{WE0}$,$\overline{WE2}$	Write Enable
$\overline{OE0}$,$\overline{OE2}$	Output Enable
A0-A9	Address Input
DQ0-DQ63	Data Input/Output
SLC	Serial PD Clock Input
SDA	Serial PD Data Input/Output
SA0-SA2	Serial PD Device Add. Input
Vcc	Power (+ 5V)
Vss	Ground

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PIN NAME

#	NAME	#	NAME	#	NAME	#	NAME
1	Vss	43	Vss	85	Vss	127	Vss
2	DQ0	44	$\overline{OE2}$	86	DQ32	128	NC
3	DQ1	45	$\overline{RAS2}$	87	DQ33	129	NC
4	DQ2	46	$\overline{CAS2}$	88	DQ34	130	$\overline{CAS6}$
5	DQ3	47	$\overline{CAS3}$	89	DQ35	131	$\overline{CAS7}$
6	Vcc	48	$\overline{WE2}$	90	Vcc	132	NC
7	DQ4	49	Vcc	91	DQ36	133	Vcc
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	NC	94	DQ39	136	NC
11	DQ8	53	NC	95	DQ40	137	NC
12	Vss	54	Vss	96	Vss	138	Vss
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	Vcc	101	DQ45	143	Vcc
18	Vcc	60	DQ20	102	Vcc	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	NC	63	NC	105	NC	147	NC
22	NC	64	Vss	106	NC	148	Vss
23	Vss	65	DQ21	107	Vss	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	Vcc	68	Vss	110	Vcc	152	Vss
27	$\overline{WE0}$	69	DQ24	111	NC	153	DQ56
28	$\overline{CAS0}$	70	DQ25	112	$\overline{CAS4}$	154	DQ57
29	$\overline{CAS1}$	71	DQ26	113	$\overline{CAS5}$	155	DQ58
30	$\overline{RAS0}$	72	DQ27	114	NC	156	DQ59
31	$\overline{OE0}$	73	Vcc	115	NC	157	Vcc
32	Vss	74	DQ28	116	Vss	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	Vss	120	A7	162	Vss
37	A8	79	NC	121	A9	163	NC
38	NC	80	NC	122	NC	164	NC
39	NC	81	NC	123	NC	165	SA0
40	Vcc	82	SDA	124	Vcc	166	SA1
41	Vcc	83	SCL	125	NC	167	SA2
42	NC	84	Vcc	126	NC	168	Vcc

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SERIAL PD BYTE DEFINITION

BYTE NUMBER	FUNCTION DESCRIBED	FUNCTION	VALUE
Byte 0	Number of Byte written during module production	15 Bytes	0Fh
Byte 1	Total Byte of Serial Presence Detect Device	256 Bytes	08h
Byte 2	Memory Type	EDO	02h
Byte 3	Number of ROW Addresses	10	0Ah
Byte 4	Number of COLUMN Addresses	10	0Ah
Byte 5	Number of Banks	1 Bank	01h
Byte 6	Module Data Width	64bit	40h
Byte 7	Module Data Width(Continued)	Not Used	00h
Byte 8	Module Interface Levels	LVTTL	01h
Byte 9	tRAC	60ns 70ns 80ns	3Ch 46h 50h
Byte 10	tCAC	17ns 20ns 20ns	11h 14h 14h
Byte 11	Module Configuration Type	None	00h
Byte 12	Refresh Rate/Type	Normal(15.6μs) SL-Part(250μs)	00h 86h
Byte 13	Primary DRAM Width	x16	10h
Byte 14	Error Checking DRAM width	None	00h
Byte 15 - 255	Undefined	Undefined	Undefined

NOTE:
1. Serial PD interface is standard IIC architecture.
2. Pull-up resistors(4.7K typical value) are required on all open collector bus devices (SCL and SDA).
3. Current sink capability on SCL and SDA (I_{OL} max) must be at least 3ma to maintain a valid low level.

IIC BUS INTERFACE

SYMBOL	RATING	NOTE
C_{MAX}	400pF	1
f_{MAX}	80 KHz(3.3V) 100 KHz(5.0V)	2
I_{OL} MAX	3mA	

NOTE:
1. The maximum number of devices connected on the IIC bus is controlled by the maximum allowable capacitance which is 400pF per line.
2. The maximum IIC system clock frequency depends on V_{CC}.

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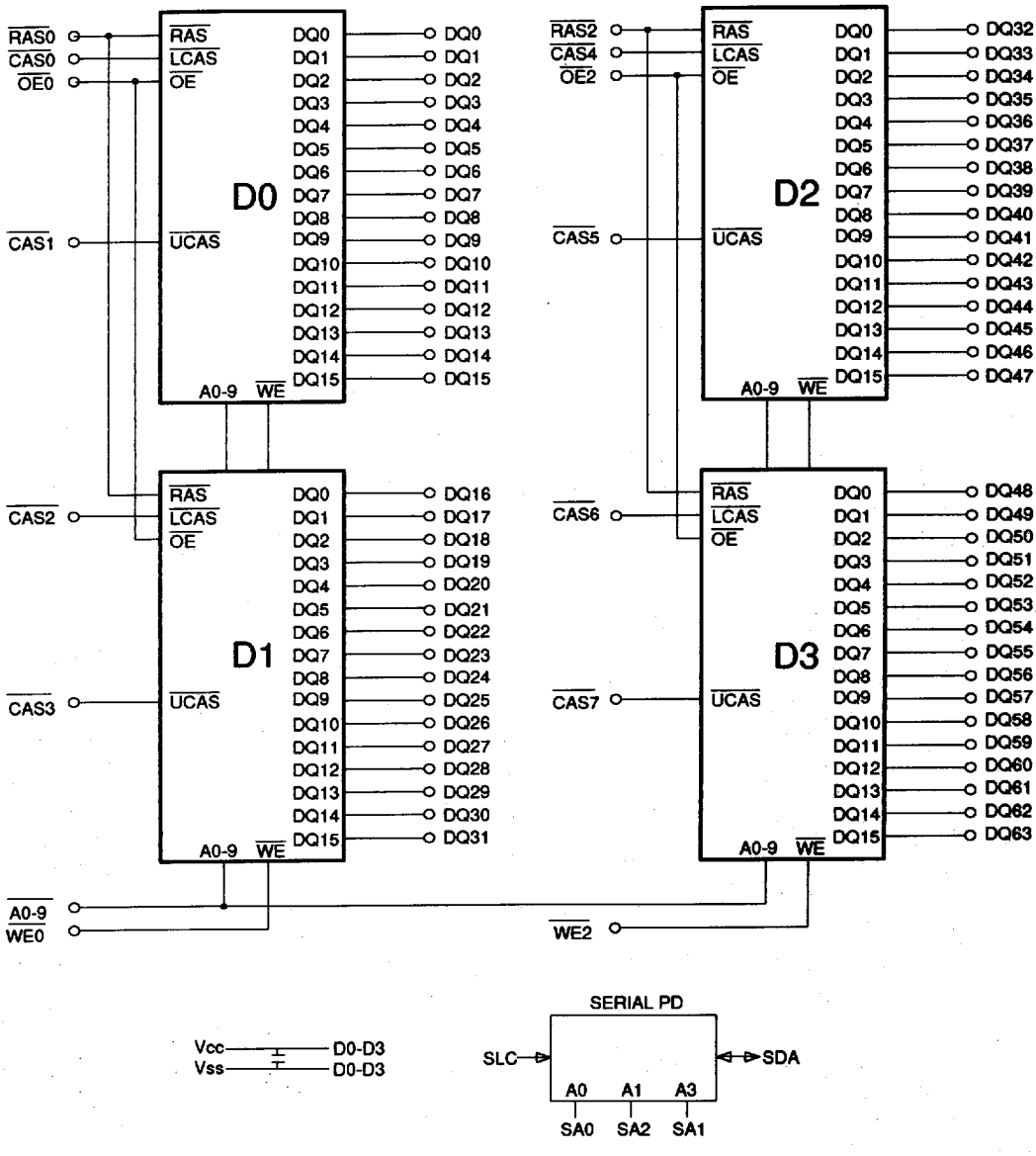
BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	–55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	–1.0 to 4.6	V
V_{CC}	Voltage on V_{CC} Relative to V_{SS}	–1.0 to 4.6	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	2.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.0	-	V_{CC}+ 0.3	V
V_{IL}	Input Low Voltage	–0.3	-	0.8	V

NOTE : All voltages are referenced to V_{SS}.

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DC CHARACTERISTICS

(T_A= 0°C to 70°C, V_{CC}= 3.3V± 10%, V_{SS}= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pin)	$V_{SS} \le V_{IN} \le V_{CC}$+ 1.0, other pins not under test= V_{SS}		-40	40	µA	
I_{LO}	Output Leakage Current (High Impedance State)	$V_{SS} \le V_{OUT} \le V_{CC}$, $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	V_{CC} Supply Current, Operating	t_{RC}= t_{RC} (min.)	60 70 80	- - -	680 600 520	mA	1,2,3
I_{CC2}	V_{CC} Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH}, other inputs≥ V_{SS}		-	8	mA	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-only refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	680 600 520	mA	1,3
I_{CC4}	V_{CC} Supply Current, EDO mode	t_{HPC}= t_{HPC} (min.)	60 70 80	- - -	560 480 440	mA	1,2,3
I_{CC5}	V_{CC} Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS}$ ≥ V_{CC}–0.2V	 SL-part	- -	4 0.8	mA	
I_{CC6}	V_{CC} Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	t_{RC}= t_{RC} (min.)	60 70 80	- - -	680 600 520	mA	1,3
I_{CC7}	V_{CC} Supply Current, Battery Back Up (SL-part only)	t_{RC}= 250µs $\overline{CAS}$= CBR cycling or 0.2V $\overline{WE}$= V_{CC}-0.2V, A0-A9= V_{CC} - 0.2V or 0.2V DQ0-DQ63= V_{CC} - 0.2V, 0.2V or open	$t_{RAS} \le$ 300ns $t_{RAS} \le$ 1µs	- -	1.4 1.8	mA	1,4,5
I_{CC8}	V_{CC} Supply Current, Self Refresh (SL-part)	$\overline{RAS}$ & $\overline{CAS}$= V_{IL} OE & WE & A0-A9= V_{CC} - 0.2V or 0.2V DQ0-DQ63= V_{CC} - 0.2V, 0.2 or open		-	1.4	mA	5
V_{OL}	Output Low Voltage	I_{OL}= 2.0mA		-	0.4	V	
V_{OH}	Output High Voltage	I_{OH}= –2.0mA		2.4	-	V	

NOTE :
1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} and I_{CC7} depend on cycle rate.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on output loading. Specified values are obtained with the output open.
3. I_{CC} is specified as average current. for I_{CC1}, I_{CC3}, and I_{CC6}, address can be changed maximum two times while $\overline{RAS}$= V_{IL}. for I_{CC4}, address can be changed maximum once while $\overline{CAS}$= V_{IH}.
4. Only tRAS(max.)= 1µs is applied to refresh of battery backup but tRAS(max.)= 10µs is applied to normal functional operation.
5. I_{CC5}(max.)= 0.8mA, I_{CC7} and I_{CC8} are applied to SL-part (HYM5V64124ASLRG/ASLTRG).

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AC CHARACTERISTICS

(TA= 0°C to 70°C, Vcc= 3.3V± 10%, Vss = 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HYM5V64124A R-Series						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	105	-	125	-	145	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	142	-	167	-	187	-	ns	
3	tHPC	EDO Mode Cycle Time	25	-	30	-	35	-	ns	
4	tHPRWC	EDO Mode Read-Modify-Write Cycle Time	73	-	85	-	100	-	ns	
5	tRAC	Access Time from $\overline{RAS}$	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from $\overline{CAS}$	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from $\overline{CAS}$ Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	$\overline{CAS}$ to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tCEZ	Output Buffer Turn-off Delay	0	15	0	15	0	15	ns	5
11	tT	Transition Time (Rise and Fall)	2.5	50	2.5	50	2.5	50	ns	3
12	tRP	$\overline{RAS}$ Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	$\overline{RAS}$ Pulse Width (EDO Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	$\overline{RAS}$ Hold Time	13	-	15	-	20	-	ns	
16	tCSH	$\overline{CAS}$ Hold Time	40	-	50	-	60	-	ns	
17	tCAS	$\overline{CAS}$ Pulse Width	13	10K	15	10K	20	10K	ns	
18	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	9
19	tRAD	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	-	5	-	5	-	ns	
21	tCP	$\overline{CAS}$ Precharge Time	7	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	10	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from $\overline{RAS}$	30	-	35	-	35	-	ns	
27	tRAL	Column Address to $\overline{RAS}$ Lead Time	30	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to $\overline{CAS}$	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to $\overline{RAS}$	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from $\overline{RAS}$	30	-	35	-	35	-	ns	
33	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
34	tRWL	Write Command to $\overline{RAS}$ Lead Time	15	-	15	-	15	-	ns	
35	tCWL	Write Command to $\overline{CAS}$ Lead Time	13	-	15	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	10	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to $\overline{RAS}$	30	-	35	-	35	-	ns	
39	tREF	Refresh Period (1024 cycles) SL-part	- -	16 256	- -	16 256	- -	16 256	ms ms	 12
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

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AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HYM5V64124A R-Series						UNIT	NOTE
			-60		-70		-80			
			MIN	MAX	MIN	MAX	MIN	MAX		
41	tCWD	$\overline{CAS}$ to $\overline{WE}$ Delay Time	37	-	45	-	45	-	ns	8
42	tRWD	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	-	95	-	105	-	ns	8
43	tAWD	Column Address to $\overline{WE}$ Delay Time	50	-	60	-	65	-	ns	8
44	tCSR	$\overline{CAS}$ Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	$\overline{CAS}$ Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5	-	5	-	5	-	ns	
47	tCPT	$\overline{CAS}$ Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	
48	tROH	$\overline{RAS}$ Hold Time Reference to $\overline{OE}$	10	-	10	-	10	-	ns	
49	tOEA	$\overline{OE}$ Access Time	-	17	-	20	-	20	ns	
50	tOED	$\overline{OE}$ to Data Delay	15	-	20	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	15	0	15	0	15	ns	5
52	tOEH	$\overline{OE}$ Command Hold Time	15	-	20	-	20	-	ns	
53	tCPWD	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	55	-	65	-	75	-	ns	8
54	tRHCP	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	40	-	40	-	50	-	ns	
55	tWRP	$\overline{WE}$ to $\overline{RAS}$ Precharge Time (CBR Cycle)	10	-	10	-	10	-	ns	

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NOTE :

1. An initial pause of 200μs is required after power-up followed by 8 $\overline{RAS}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initilization cycles instead of 8 $\overline{RAS}$-only refresh cycles are required. The device should be carefully initialized to be prevented from being entered into multi bit test mode.
2. If $\overline{RAS}$= Vss during power-up, the HYM5V64124A could begin an active cycle. This condition results in higher power-up current than necessary demands from the power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.
3. Refer to the HY51V18164B data sheet for detailed information.
4. Measured with a load equivalent to 2 TTL loads and 100pF. (V_{OH}= 2.0V,V_{OL}= 0.8V)
5. t_{CEZ}(max.) $t_{OEZ(MAX)}$, $t_{REZ(MAX)}$ and $t_{WEZ(MAX)}$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in late write or read-modify-write cycles.
8. t_{WCS} is not a restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle.
9. Operation within the $t_{RCD(max.)}$ limit insures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
10. Operation within the $t_{RAD(max.)}$ limit insures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA}.
11. Measured with the specified current load and 100pF.
12. A burst of 1024 $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles must be executed within 16ms after exiting self refresh (for SL-part).
13. If $t_{CWD} \geq t_{WCS(MIN.)}$, $t_{RWD} \geq t_{RWD(MIN.)}$, $t_{AWD} \geq t_{AWD(MIN.)}$ and $t_{CPWD} \geq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes bach to V_{IH}) is indeterminated.
14. In $\overline{CAS}$ before $\overline{RAS}$ self refresh mode.
    In case of using distributed $\overline{CAS}$ before $\overline{RAS}$ refresh, refresh 1024 times during a 256ms after reset
    In case of using burst $\overline{CAS}$ before $\overline{RAS}$ refresh, refresh 1024 times during a 16ms after reset
    In case of using $\overline{RAS}$ only refresh, refresh against all refresh address during a 16ms after reset
15. If $\overline{RAS}$ goes to high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes to high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.

CAPACITANCE

(T_A= 25°C, V_{CC}= 3.3V± 10%, V_{SS}= 0V, f= 1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C_{IN1}	Input Capacitance (A0-A9)	-	30	pF
C_{IN2}	Input Capacitance ($\overline{WE0}$,$\overline{WE2}$,$\overline{OE0}$,$\overline{OE2}$)	-	24	pF
C_{IN3}	Input Capacitance ($\overline{RAS0}$, $\overline{RAS2}$)	-	24	pF
C_{IN4}	Input Capacitance ($\overline{CAS0}$-$\overline{CAS7}$)	-	17	pF
C_{DQ}	Data Input/output Capacitance (DQ0-DQ63)	-	17	pF

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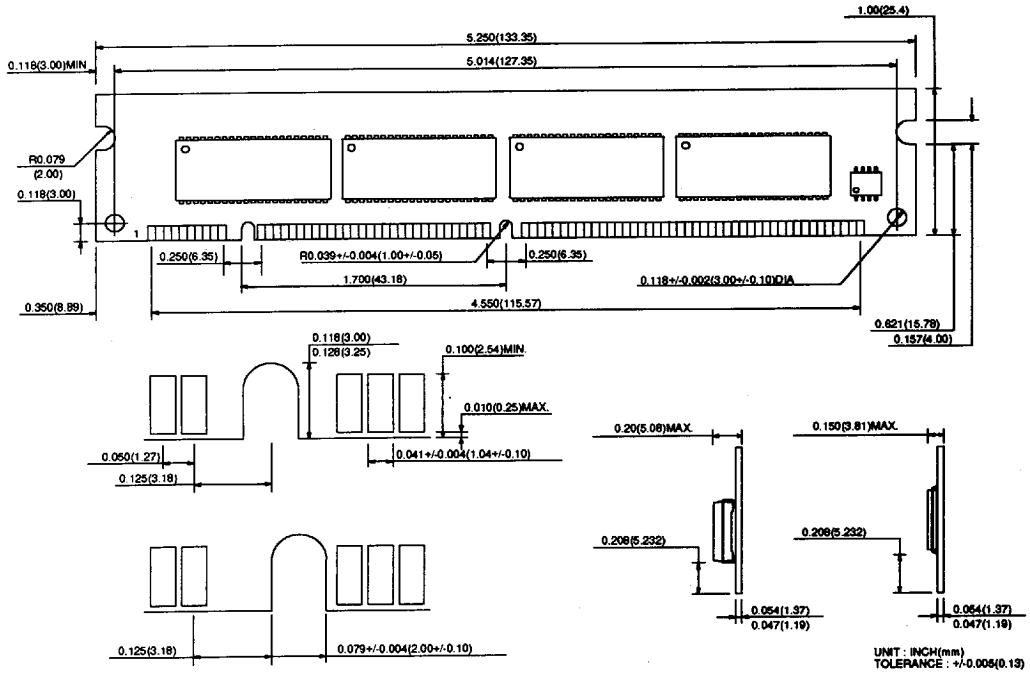
PACKAGE INFORMATION

168 pin Dual In-line Memory Module (RG ; Gold plated)



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ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE	PLATING
HYM5V64124ARG	60/70/80		DIMM	Gold
HYM5V64124ASLRG	60/70/80	SL-part	DIMM	Gold
HYM5V64124ATRG	60/70/80		DIMM	Gold
HYM5V64124ASLTRG	60/70/80	SL-part	DIMM	Gold

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