140 – 155 Mbit/s CMI Encoder/ Decoder GD16367B/GD16368B

Preliminary

General Description

The GD16367B and GD16368B is a chip- set intended for use in SDH STM-1/ SONET OC-3 and PDH E4 systems, where electrical CMI coded interface is needed.

The chip set is designed to take care of all processing above 78 MHz in an STM-1/OC-3/E4 interface, accommodating both electrical (CMI) and optical (NRZ) data format. Hence the same board may be configured as STM-1o, STM-1e, E4o, or E4e at system integration level.

The Encoder - GD16367B

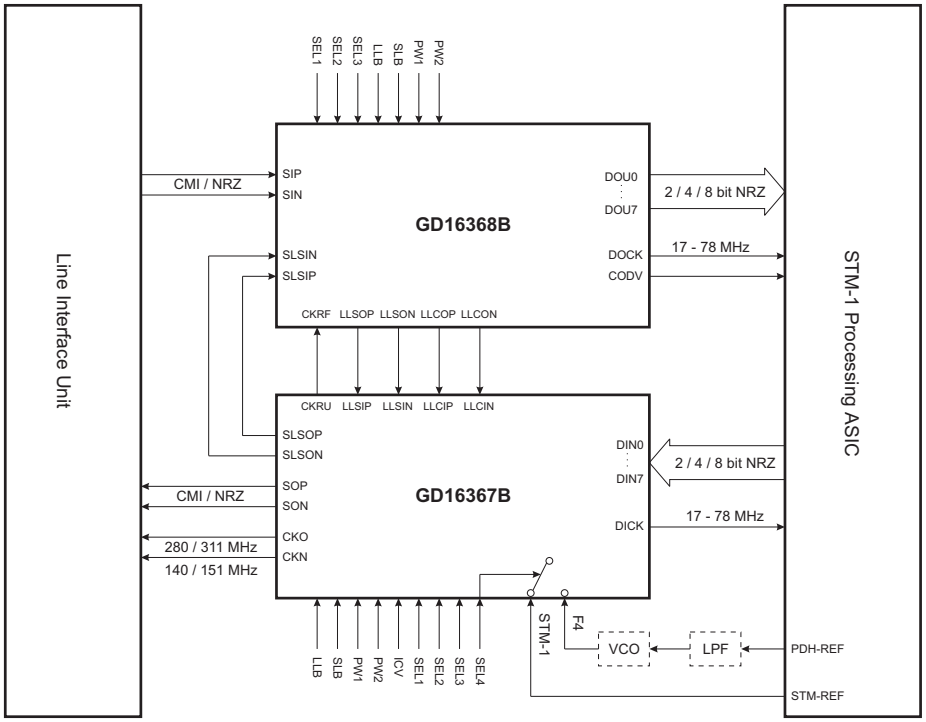
The MUX/Encoder device generates the CMI coded data signal and associated clock at 280/311 MHz. The reference input clock for the clock synthesis may be selected from two individual inputs, 70/ 78 MHz or 17/19 MHz allowing for programmable selection between reference inputs for E4 or STM-1/OC-3. The CMI encoder may be switched off when the interface is optical.

The Decoder - GD16368B

The DeMUX/Decoder device provides clock and data recovery extracting the 280/311 MHz clock of the incoming CMI signal and a decoder that turns CMI to NRZ. CMI code violations are detected and signaled by the CODV output. The CMI decoder may be switched off when the interface is optical

Both devices provide selectable 2, 4 or 8 bit parallel interface to the processing device for maximum flexibility.

The phase relation between parallel data and clock is selectable in four phases (0°, 90°, 180°, 270°) providing flexible timing between the system and the devices.



Features

- Integrates all high-speed signal processing above 78 MHz.
- ITU-T G.703 CMI encoding/decoding for STM-1 and E4 electrical interfaces.
- Meet G.751, G.823 and G.825 for jitter tolerance and jitter generation.
- Remote and local loops available.
- CMI disable function for board level configuration for optical interface.
- Selectable 2, 4 or 8 bit parallel interface for maximum flexibility.
- Selectable 0°, 90°, 180°, 270° phase relation for parallel data I/O.
- 3.3 V LVPECL High speed I/O's.
- CMOS Interface to system ASIC.
- Power consumption typical:
  - 400 mW for GD16367B
  - 600 mW for GD16368B
- 3.3 V supply; 5 V for VCO.
- Designed for low cost and volume production.
- High-speed BiCMOS technology.
- Package 52 pin PQFP (10 x 10 mm).

Applications

- Tele Communication:
  - SDH STM-1
  - SONET OC-3
  - PDH E4

Functional Details, Both Devices

General

The GD16367B/GD16368B chip set provides transmission of 140 Mbit/s (E4) and 155 Mbit/s (STM-1/OC-3).

Both Optical NRZ signal transmission and Electrical CMI-coded signal transmission are supported by the internal selectable CMI-Encoding/Decoding circuitry.

Selectable 2/4/8 bit system interface is provided.

140/155 Mbit/s and NRZ/CMI Clock Frequencies

The VCO tuning range covers the clock frequencies of 280 MHz to 311 MHz. The actual clock frequency is determined by reference clocks and received data.

The 280/311 MHz are used for CMI-operation. When operating in NRZ-mode the VCO clock is divided by 2.

NRZ/CMI and Parallel Width Selection

The devices can operate in different line and system modes; selected by SEL1, PW2, and PW1 (See Table 1).

The bit order at the system site is defined with bit 0 as the first bit transferred (DIN0 for the transmitter and DOU0 for the receiver).

Line/System Loop Back

Connecting the differential Line Loop signals and clocks (LLxxx) from GD16368B to GD16367B allows loop-back of the received and recovered line signal, when LLB is high on both devices. The Line Loop back is also called remote loop back.

Connecting the differential System Loop signals (SLxxx) from GD16367B to GD16368B allows system loop back, when SLB is high on both devices. The System Loop back is also called a local loop back.

Loop Filters

Both circuits comprise fully integrated PLL functions for re-timing data at the transmit site, and for clock and data recovery at the receive site.

A passive loop filter consisting of a resistor and a capacitor is used for each device. The external loop filters are terminated to VEEA as shown in Figure 1 (for the transmitter) and Figure 4 (for the receiver).

The loop filter values are optimised at the evaluation board GD90367/368. The optimal values depend on the actual application. The suggested values in Figures 1 and 4 can be used as starting point for the optimisation.

Mode	SEL1	PW2	PW1	Line Clock [Frequency/MHz]	System Clock [Frequency/MHz]	Used Bits
CMI, 2 bit	0	0	0	280/311	70/78	0 & 1
CMI, 4 bit	0	0	1	280/311	35/39	0...3
CMI, 8 bit	0	1	0	280/311	17/19	0...8
Not valid	0	1	1	-	-	-
NRZ, 2 bit	1	0	0	140/155	70/78	0 & 1
NRZ, 4 bit	1	0	1	140/155	35/39	0...3
NRZ, 8 bit	1	1	0	140/155	17/19	0...8
Not valid	1	1	1	-	-	-

Table 1 NRZ/CMI and parallel width selection. This table is common for both devices.

The GD16367B is the encoder/transmitter (see Figure 1) with:

- Multiplexer (2/4/8:1)
- Selectable CMI-Encoding
- NRZ/CMI data and clock differential outputs
- Selectable System Loop Back data differential output
- Selectable Line Loop Back data and clock differential inputs

Multiplexer

The parallel input data (DIN0...DIN7) are received by the multiplexer. This is done synchronously with the DICK output clock, which is used when counter clocking. Counter clocking allows 2:1, 4:1 , and 8:1 multiplexing. Forward clocking is only possible when operating in the 2:1 mode.

A low noise reference clock is recommended, as the clock noise within the PLL loop bandwidth is transmitted as jitter on the serial outputs. The 70/78 MHz clock input (CKR0) is selected when SEL4 is low. The 17/19 MHz clock input (CKR1) is selected when SEL4 is high. For PDH system rates 17 or 70 MHz is used. For SDH system rates 19 or 78 MHz is used.

Counter Clocking

The output clock (DICK) is used for clocking out the parallel system data into the MUX. The frequency of DICK depends on the reference clock and the multiplexing mode (See Table 1 on page 2). Four phases timing relation between DINx and DICK are provided by the SEL2 and SEL3 (See AC Characteristics on page 11, and Pin List on page 7).

Forward Clocking

When operated in 2:1 multiplexing mode, a forward clocking scheme can be used:

- Set PW1=PW2=SEL4=0
- Connect the forwarded 70/78 MHz clock to CKR0.

The control inputs (SEL2 and SEL3) control the timing relation between DINx and CKR0, see pin list on page 7.

CMI-Encoder

When the CMI-encoding is enabled (SEL1=0), every bit of the 140/155 Mbit/s output from the multiplexer is encoded to a 2-bit CMI-word, resulting in a 280/311 Mbit/s output of the CMI-encoder; and a 280/311 MHz clock (CKO/CKN) from the CMI-encoder. See the CMI-coding in Table 2.

NRZ:	CMI:	Note:
0	01	consecutive NRZ zeros “0000..” gives “01010101...” as CMI-output
1	00/11	consecutive NRZ ones “1111...” gives “00110011...” as CMI-output

Table 2 CMI Coding.

When the CMI-encoding is disabled (SEL1=1), the 140/155 Mbit/s output from the multiplexer is passed through the CMI-encoder; and a 140/155 MHz clock (CKO/CKN) is generated from the CMI-encoder.

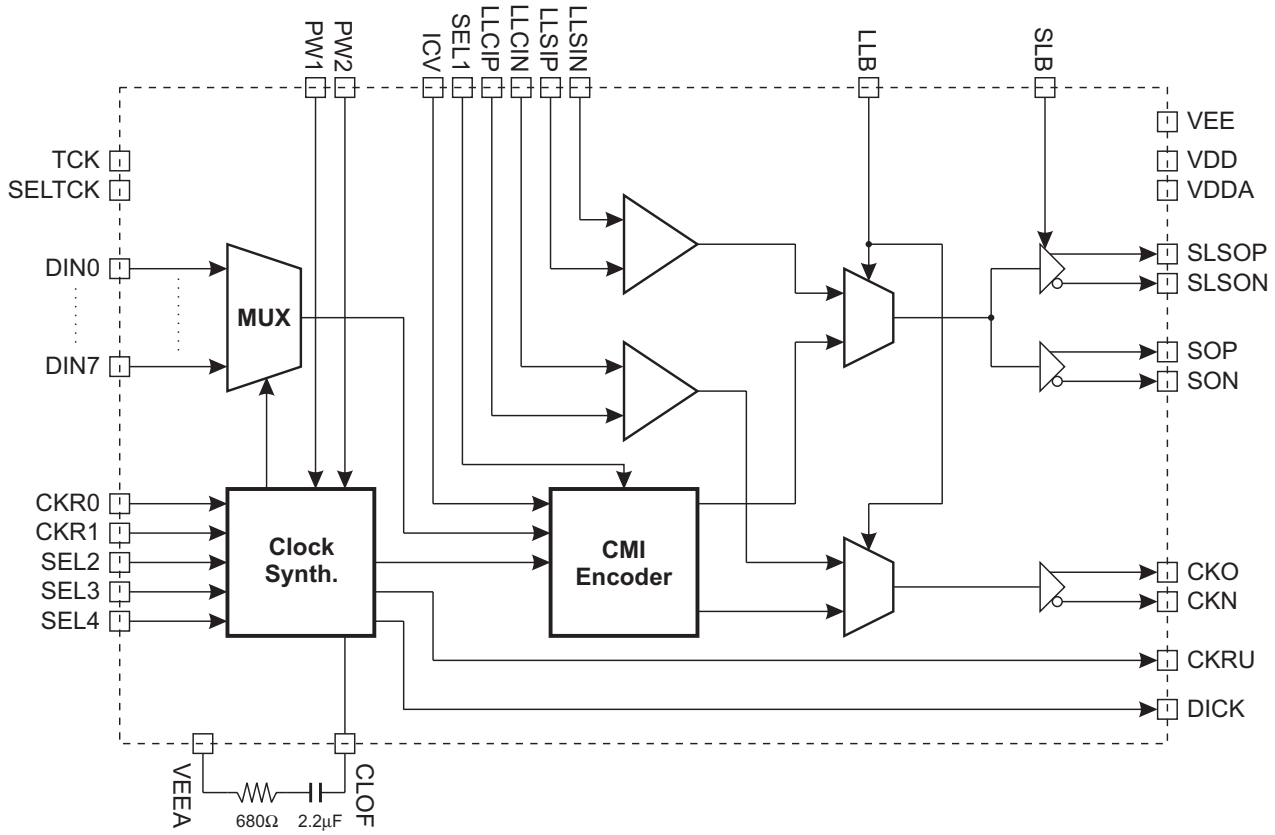


Figure 1. *Block Diagram - GD16367B*

Outputs

The outputs from the multiplexer are fed to the LVPECL output stages. See Figures 2 and 3 for output termination.

The serial data output (SOP/SON) is accompanied by a differential clock output (CKO/CKN). See AC Characteristics on page 11.

SLSOP/SLSON is enabled when SLB is high. When SLB is low SLSOP=0 and SLSON=1; thus avoiding noise injection at normal operation.

The clock output (CKRU) provides a 70/78 MHz clock suitable for driving the GD16368B receiver (connect to CKRF input).

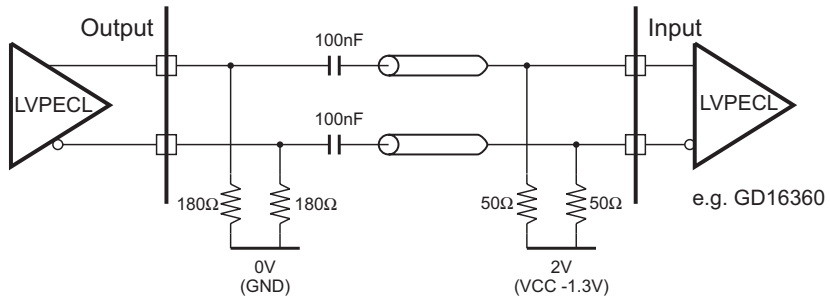


Figure 2. *LVPECL Output Termination, AC-coupled.*

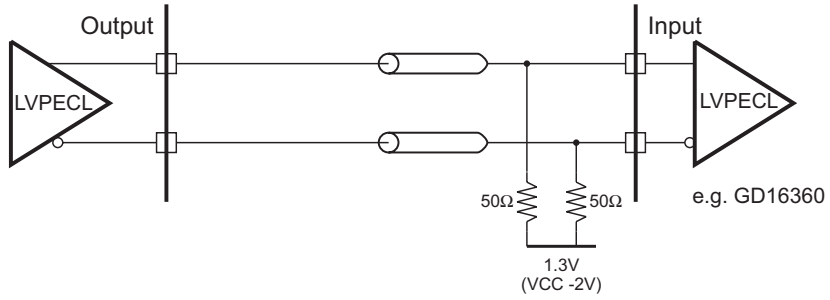


Figure 3. *LVPECL Output Termination, DC-coupled.*

The GD16368B is the receiver (see Figure 4) with:

- Clock&Data Recovery (CDR)
- Selectable CMI-Decoding
- Demultiplexer (1:2/4/8)
- Selectable System Loop Back data differential input
- Selectable Line Loop Back / 1:1 CDR data and clock outputs

Inputs

The serial input is selected by SLB. For normal operation, SIP/SIN is selected when SLB is low. For system loop back operation, SLSIP/SLSIN is selected when SLB is high.

The selected serial input data is the input of the CDR, where the clock and data is recovered.

The PLL constantly attempts to lock to the incoming data stream. In case the incoming data signal is lost, the VCO will drift away from the CKRF reference frequency. The VCO is monitored by a built-in lock detector. When it drifts more than 500 ppm (or 2000 ppm, selectable) away from the reference frequency, it is “kicked back” to the reference frequency and starts hunting for incoming data again.

CKRF does not have any part in the jitter performance (as long as the incoming data frequency is within 500 ppm of the required 70/78 MHz).

CMI-Decoder

When the CMI-decoding is enabled (SEL1=0), 280/311 Mbit/s is decoded as 2-bits CMI-words into 1-bit NRZ 140/155 Mbit/s. The internal 140/155 MHz clock is aligned to the CMI-words. See Table 2 on page 3 for the CMI-coding.

When the CMI-decoding is disabled (SEL1=1), the 140/155 Mbit/s data signal is passed unchanged through the CMI-decoder.

Outputs

The 140/155 Mbit/s recovered (and decoded) data is de-multiplexed into 2, 4, or 8 parallel data bits (DOU0...DOU7) selected by PW1 and PW2 (see Table 1 on page 2).

DOCK is the output clock synchronous to the parallel data (See AC Characteristics on page 11).

The phase can be adjusted with SEL2 and SEL3 (0°/90°/180°/270°, see pin list).

If the incoming data stream is lost, DOCK will be floating within a +/-500(2000) ppm window around the CKRF frequency (divided by 1, 2, or 4 depending of the parallel bit rate). In CMI-mode, the CODV output will be signalling errors if the signal is lost.

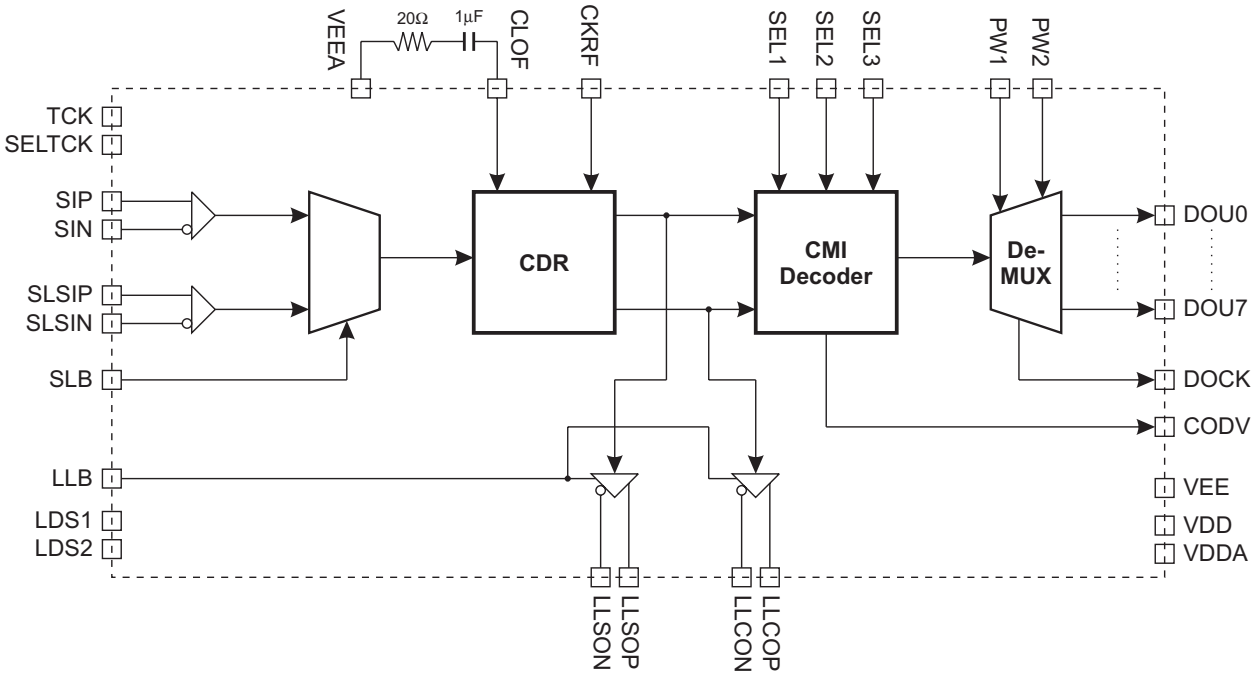


Figure 4. *Block Diagram - GD16368B*

Practical Considerations

General

The PCB should be multilayer in order to optimise high-speed signal performance. Our evaluation board GD90367/368 uses a standard FR4 PCB.

Use shortest possible conductors for the signals to the line interfaces. The high-speed serial data lines should be designed as transmission lines with constant trace width to ensure constant impedance along the transmission line. Any coupling capacitors should have foot print width matching the trace width. Special attention must be paid to the layout where the signal trace meets connectors in/out of the board, The solder pads for e.g. SMA connectors must be kept very small to ensure good impedance match.

De-coupling capacitors should be applied to each power supply pin. Care should be taken to reduce ground bounce.

The line loop signal and clock must be terminated close to the transmitter device (GD16367B).

The Decoder/DeMux has no internal input termination. Hence the input lines (SIP/SIN) should be terminated to a decoupled +2 V DC point close to the GD16368B device.

The system loop signal and clock must be terminated close to the receiver device (GD16368B).

Transmission Cable Connection

The high-speed differential LVPECL line interface of the GD16367B/368B devices can easily be interfaced with an E4 or STM-1 transmission cable. A cable receiver/equalizer is required at the receiver site, while a cable driver is required at the transmitter site.

GIGA provides an integrated device (GD16360) which provides cable equalizer, cable driver, and additionally a LOS detector – for two channels.

Pin List, GD16367B

Mnemonic:	Pin No.:	Pin Type:	Description:
SOP, SON	6, 7	LVPECL-OUT	Serial differential data output.
CKO, CKN	9, 10	LVPECL-OUT	Differential 140/155 or 280/311 MHz clock out, selected by SEL1.
DIN0, DIN1, DIN2, DIN3, DIN4, DIN5, DIN6, DIN7	38, 37, 36, 34, 33, 31, 30, 29	CMOS-IN	2, 4 or 8-bit wide data input. DIN0 is transferred as the first bit, followed by DIN1, ...
DICK	41	CMOS-OUT	70/78, 34/39 or 17/19 MHz clock output selected by PW1 and PW2.
CKR0, CKR1	20, 21	CMOS-IN	Reference clock inputs for the clock synthesis. CKR0: 70/78 MHz, CKR1: 17/19 MHz. CKR0 can be used for forward clocking (70/78 MHz) in 2-bit mode.
SEL1	45	CMOS-IN	When low the CMI encoder is enabled and CKO/CKN is 280/311 MHz. When high, data is passed unchanged (NRZ mode) and CKO/CKN is 140/155 MHz.
SEL4	25	CMOS-IN	When high CKR1 is used as reference for the PLL. When low CKR0 is used.
SEL2, SEL3	23, 24	CMOS-IN	DINx input phase versus DICK/CKRx select: SEL3 SEL2 0 0 T_{DEL} = 0 ° 1 1 T_{DEL} = 90 ° 1 0 T_{DEL} = 180 ° 0 1 T_{DEL} = 270 °
CKRU	42	CMOS-OUT	70/78 MHz clock output. May be used as input to the GD16368B CKRF pin.
CLOF	18	ANL	Ext. Loop filter pin. Connect 2.2 µF in series with 680 Ω from this pin to the VEEA pin.
LLSIP, LLSIN	48, 47	LVPECL-IN	Line loop-back serial differential data, 140/155 MHz. To be connected from LLSOP/LLSON of the GD16368B.
LLCIP, LLCIN	51, 50	LVPECL-IN	Line loop-back serial differential clock, 140/155 Mbit/s. To be connected from LLCOP/LLCON of the GD16368B.
LLB	49	CMOS-IN	When high, Line loop-back is enabled.
SLSOP, SLSON	4, 3	LVPECL-OUT	Switch loop-back serial differential data, 140/155 Mbit/s. To be connected to SLSIP/SLSIN of the GD16368B.
SLB	2	CMOS-IN	When high, switch loop-back is enabled.
PW1, PW2	44, 43	CMOS-IN	Parallel port width / parallel clock rate: PW2 PW1 0 0 2 bit, DIN0..DIN1 - DICK = 70/78 MHz 0 1 4 bit, DIN0..DIN3 - DICK = 35/38 MHz 1 0 8 bit, DIN0..DIN7 - DICK = 17/19 MHz 1 1 Not valid
ICV	28	CMOS-IN	Insert Code Violation. When shifted high, one violation is inserted (“1" level toggled).
TCK	12	ANL-IN	Test clock input - for test purpose only. Connect to VEEA for normal operation.
SELTCK	14	ANL-IN	Test clock enable - for test purpose only. Connect to VDD for normal operation.
VDD	5, 8, 11, 22, 26, 32, 35, 40, 46, 52	PWR	3.3 V power.
VDDA	16, 19	PWR	5 V power for VCO.
VEE	1, 13, 27, 39	PWR	0 V power.
VEEA	15	PWR	0 V power for VCO.
NC	17		No Connected.

Pin List, GD16368B

Mnemonic:	Pin No.:	Pin Type:	Description:
SIP, SIN	4, 5	LVPECL-IN	Differential serial data input.
DOU0, DOU1, DOU2, DOU3, DOU4, DOU5, DOU6, DOU7	38, 37, 35, 34, 32, 31, 29, 28	CMOS-OUT	2, 4 or 8-bit wide data output. DOU0 is the first received bit, followed by DOU1, ...
DOCK	24	CMOS-OUT	70/78, 34/39 or 17/19 MHz clock output selected by PW1 and PW2.
CODV	25	CMOS-OUT	Code violation output. High for one 70/78 MHz clock period if error detected, otherwise low. Disabled (low) in NRZ-mode.
SEL1	44	CMOS-IN	When low the CMI decoder is enabled. When high, data is passed unchanged (NRZ mode).
SEL2, SEL3	43, 42	CMOS-IN	DOUx output phase versus DOCK select: SEL3 SEL2 0 0 T_{DEL} = 0° 1 1 T_{DEL} = 90° 1 0 T_{DEL} = 180° 0 1 T_{DEL} = 270°
CKRF	41	CMOS-IN	70/78 MHz reference clock input for the CDR block. Used to ensure fast acquisition to incoming data and to ensure stable DOCK output clock in absence of data.
CLOF	48	ANL	Ext. loop filter pin. Connect 1 µF in series with 20 Ω from this pin to the neighbour VEEA pin.
LLSOP, LLSON	19, 20	LVPECL-OUT	Line loop-back serial differential data, 140/155 MHz, CMI or NRZ according to SEL1. To be connected to LLSIP/LLSIN of the GD16367B.
LLCOP, LLCON	16, 17	LVPECL-OUT	Line loop-back serial differential clock, 140/155 MHz or 280/311 MHz according to SEL1. To be connected to LLCIP/LLCIN of the GD16367B.
LLB	18	CMOS-IN	When high, line loop-back is enabled.
SLSIP, SLSIN	8, 7	LVPECL_IN	Switch loop-back serial differential data, 140/155 MHz. To be connected to SLSOP/SLSON of the GD16367B.
SLB	10	CMOS-IN	When high, switch loop-back is enabled.
PW1, PW2	22, 23	CMOS-IN	Parallel port width / parallel clock rate: PW1 PW2 0 0 2 bit, DOU0..DOU1 – DOCK = 70/78 MHz 1 0 4 bit, DOU0..DOU3 – DOCK = 35/38 MHz 0 1 8 bit, DOU0..DOU7 – DOCK = 17/19 MHz 1 1 Not valid
TCK	2	ANL-IN	Test clock input, for test purpose only. Connect to VEE.
SELTCK	52	ANL-IN	Test clock select, for test purpose only. Connect to VDD.
LDS1, LDS2	12, 46	CMOS-IN	Lock Detect Selection: LDS1 LDS2 Lock mode 1 1 Auto 2000 ppm (default) 1 0 Auto 500 ppm 0 1 Manual select BB 0 0 Manual select PFC
VDD	3, 6, 9,11,15,21,26, 30, 33, 36, 40, 45	PWR	3.3 V power.
VDDA	47, 50	PWR	5 V power for VCO.
VEE	1, 13, 14, 27, 39	PWR	0 V power.
VEEA	51	PWR	0 V power for VCO.
NC	49	NC	No Connected.

Package Pinout

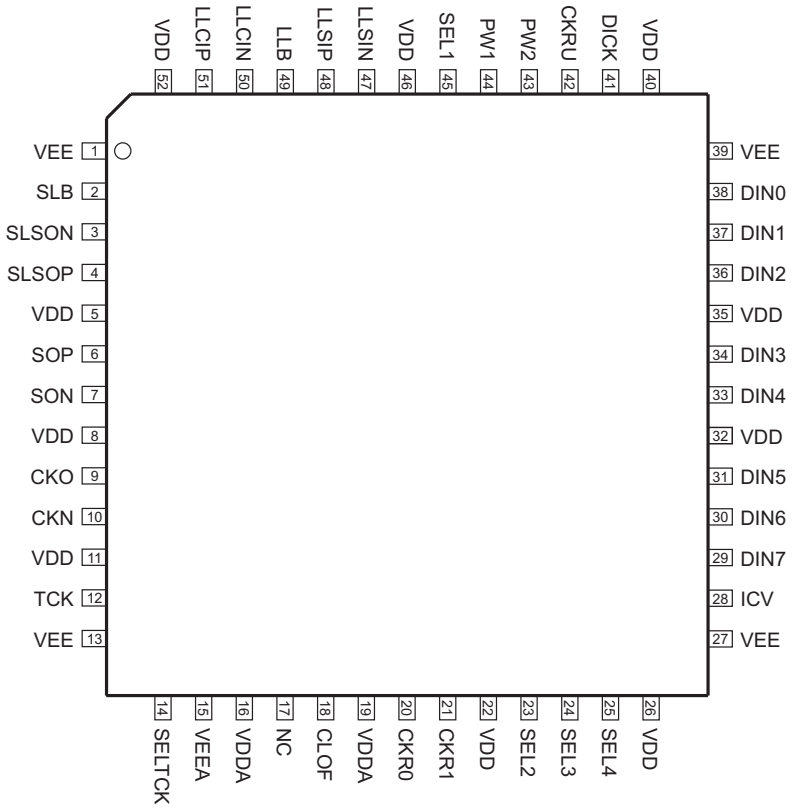


Figure 5. *GD16367B, 52 pin PQFP - Top View*

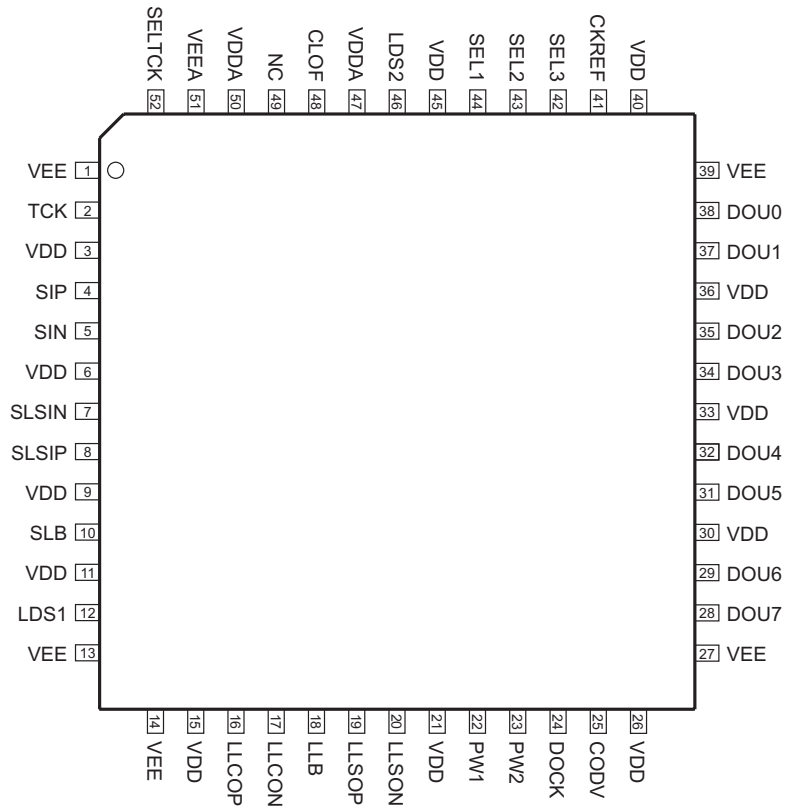


Figure 6. *GD16368B, 52 pin PQFP - Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages are referenced to VEE unless otherwise noted.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD} , V_{DDA}	Supply Voltage		0		6	V
$V_{O\ max}$	Output Voltage	LVPECL/CMOS	-0.5		V_{DD} + 0.5	V
$I_{O,LVPECL\ max}$	Output Current	LVPECL			40	mA
$I_{O,CMOS\ max}$	Output Current	CMOS	-10		10	mA
$V_{I\ max}$	Input Voltage	LVPECL/CMOS	-0.5		V_{DD} + 0.5	V
$I_{I\ max}$	Input Current	LVPECL/CMOS	-1.0		1.0	mA
T_O	Operating Temperature	Junction	-55		+150	°C
T_S	Storage Temperature	Junction	-65		+175	°C

DC Characteristics

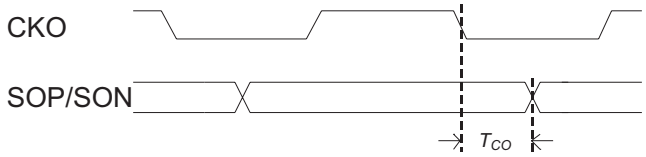
$T_{AMBIENT}$ = 0 °C to 75 °C.
θ_{ja} = 55 °C/W, still air, (GD16367B).
θ_{ja} = 50 °C/W, still air, (GD16368B)
All voltages in table are referred to VEE unless otherwise noted.

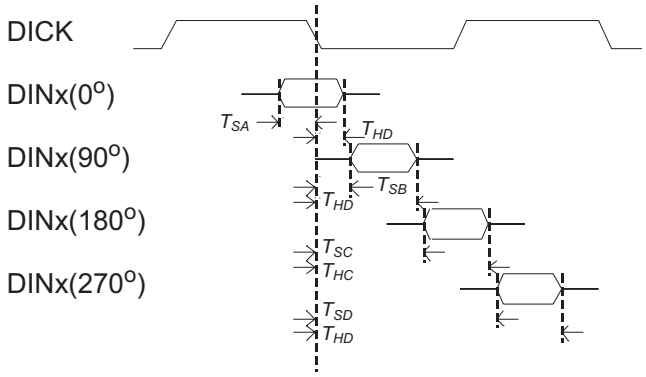
Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}	Supply Voltage	Note 1	3.15	3.30	3.60	V
V_{DDA}	Supply Voltage, VCO		4.7	5.00	5.25	V
$I_{DD,GD16368B}$	Supply Current, GD16368B	Note 2		140	210	mA
$I_{DDA,GD16368B}$	Supply Current, GD16368B	Note 2		10	20	mA
$I_{DD,GD16367B}$	Supply Current, GD16367B	Note 2		95	125	mA
$I_{DDA,GD16367B}$	Supply Current, GD16367B	Note 2		10	20	mA
$V_{IH,LVPECL}$	LVPECL Differential Input HI Voltage	Note 3	V_{DD} -1.75		V_{DD} -0.45	V
$V_{IL,LVPECL}$	LVPECL Differential Input LO Voltage	Note 3	V_{DD} -2.00		V_{DD} -0.70	V
$V_{IDIFF,LVPECL}$	LVPECL Differential Input Voltage	Note 3	0.250	0.500	1.400	V
$I_{IH,LVPECL}$	LVPECL Input HI Current	$V_{IH\ LVPECL,\ max}$			100	µA
$I_{IL,LVPECL}$	LVPECL Input LO Current	$V_{IL\ LVPECL,\ min}$	-100			µA
$V_{OH,LVPECL}$	LVPECL Output HI Voltage	Note 4	V_{DD}-1.11		V_{DD} -0.67	V
$V_{OL,LVPECL}$	LVPECL Output LO Voltage	Note 4	V_{DD}-2.00		V_{DD} -1.50	V
$V_{ODIFF,LVPECL}$	LVPECL Output Differential Voltage	Note 4	0.390		1.330	V
$V_{IH,CMOS}$	CMOS Input HI Voltage	Note 5	V_{DD} x0.8		V_{DD}	V
$V_{IL,CMOS}$	CMOS Input LO Voltage	Note 5	0		V_{DD} x0.2	V
$I_{IH\ CMOS}$	CMOS Input HI Current	$V_{IH\ CMOS,\ max}$			100	µA
$I_{IL\ CMOS}$	CMOS Input LO Current	$V_{IL\ CMOS,\ min}$	-100			µA
$V_{OH\ CMOS}$	CMOS Output HI Voltage	I_{OH}= 1mA	V_{DD} - 0.2		V_{DD}	V
$V_{OL\ CMOS}$	CMOS Output LO Voltage	I_{OL}= -1mA	0		0.2	V

Note 1: Supply voltage difference limits: 0.7 V ≤ V_{DDA} - V_{DD} ≤ 1.8 V.
Note 2: Supply currents are measured without loads on the (LVPECL/CMOS) outputs.
Note 3: Although $V_{IDIFF,LVPECL}$ may vary within $V_{IH,MAX}$ and $V_{IL,MIN}$, it must not exceed $V_{IDIFF,MAX}$.
Note 4: 50 Ω termination to V_{DD} -2.0 V.
Note 5: If not connected, the input is pulled high (approximately 2.6 V) by internal pull-up resistor (48k ±20 %).

AC Characteristics

GD16367B

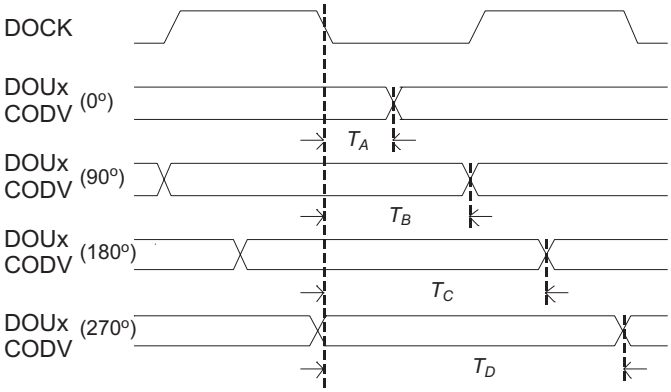


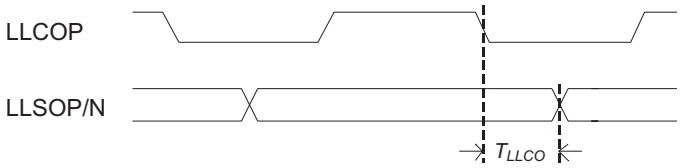


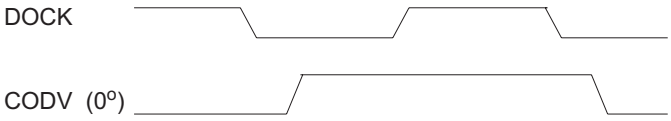
GD16367B	Frequency Range:	Jitter: [UIp-p]	Period: [s]	Specification:
E4	200 Hz - 3.5 MHz	0.05	10	ITU-T G.751
STM-1(CMI)	500 Hz - 1.3 MHz 65 kHz - 1.3 MHz	0.5 0.075	60 60	DE/TM-3017-4
STM-1(opt)	500 Hz - 1.3 MHz 65 kHz - 1.3 MHz	0.5 0.1	60 60	ITU-T G.813
OC3	12 kHz - 1.3 MHz	0.1	60	

The GD16367B will meet the above specifications for jitter generation when tested in appropriate mode with a jitter free input reference clock applied.

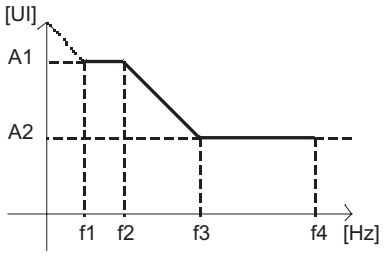
GD16368B







Jitter tolerance according to G.823 and G.825



GD16368B	f1 [Hz]	f2 [Hz]	f3 [Hz]	f4 [Hz]	A1 [UI_{p-p}]	A2 [UI_{p-p}]	Specification:
E4	200	500	10k	3.5M	1.5	0.075	ITU-T G.823
STM-1 (CMI)	500	3.25k	65k	1.3M	1.5	0.075	DE/TM-03067
STM-1 (opt)	500	6.5k	65k	1.3M	1.5	0.15	ITU-T G.825
OC3	300	6.5k	65k		1.5	0.15	

The GD16368B will meet the above specifications for jitter tolerance when tested in the appropriate mode.

General

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
T_A	DOCK to DOUx Valid			1		ns
T_B	DOCK to DOUx Valid	Note 1		T/4 + 1		ns
T_C	DOCK to DOUx Valid	Note 1		T/2 + 1		ns
T_D	DOCK to DOUx Valid	Note 1		3*T/4 + 1		ns
T_{CO}	CKO to SOP/SON Valid	Note 2		0.5		ns
T_{LLCO}	LLCOP to LLSOP/N Valid			0.3		ns
T_{SA}	Set-up Time before DICK			1		ns
T_{SB}	Set-up Time after DICK	Note 3		T/4 - 1		ns
T_{SC}	Set-up Time after DICK	Note 3		T/2 - 1		ns
T_{SD}	Set-up Time after DICK	Note 3		3*T/4 - 1		ns
T_{HA}	Hold Time after DICK			1		ns
T_{HB}	Hold Time after DICK	Note 3		T/4 + 1		ns
T_{HC}	Hold Time after DICK	Note 3		T/2 + 1		ns
T_{HD}	Hold Time after DICK	Note 3		3*T/4 + 1		ns
R_{Duty}	Duty Cycle, CKR0/1, CKRF	Note 4	40/60		60/40	%
D_{CKRF}	CRKF Frequency Deviation from Nominal Line Frequency		-200		+200	ppm
F_{VCO}	VCO Frequency Range		136		158	MHz
$T_{Acq\text{-}PU}$	Acquisition Time, GD16367B/368B	Power up			100	µs
$T_{Acq\text{-}INT}$	Acquisition Time, GD16368B	Inp. Interrupt			10	µs
L_{CID}	Number of Consecutive Identical Digits, GD16368B		>120			Units
$T_{R\text{-}LVPECL}$	LVPECL Rise Time	Note 5			800	ps
$T_{F\text{-}LVPECL}$	LVPECL Fall Time	Note 5			800	ps
$T_{R\text{-}CMOS}$	CMOS Rise Time	Note 6			5	ns
$T_{F\text{-}CMOS}$	CMOS Fall Time	Note 6			3	ns

Note 1: T equals the period time of DOCK (one bit period).
Note 2: Also valid for LLB operation. The typical LLB data & clock delay difference for the GD16367B ($T_{LLSIP \rightarrow SOP/N}$ - $T_{LLCOP/N \rightarrow CKO/N}$) is 0.2 ns. As the T_{LLCO} of the GD16368B (LLCOP to LLSOP/N) is 0.3 ns (typ.), the resulting T_{CO} in LLB mode mode is 0.5 ns = 0.3 ns (GD16367B) + 0.2 ns (GD16368B).
Note 3: T equals the period time of DICK (one bit period).
Note 4: Duty cycle measured at V_{TH} = 1.4 V
Note 5: 20 - 80 %, 50 Ω to V_{DD} -2.0 V
Note 6: 20 - 80 %, 10 pF and 100 µA load. Typically, T_R = 0.5 ns + C x 0.4 ns/pF; T_F = 1 ns + C x 0.16 ns/pF.

Package Outline

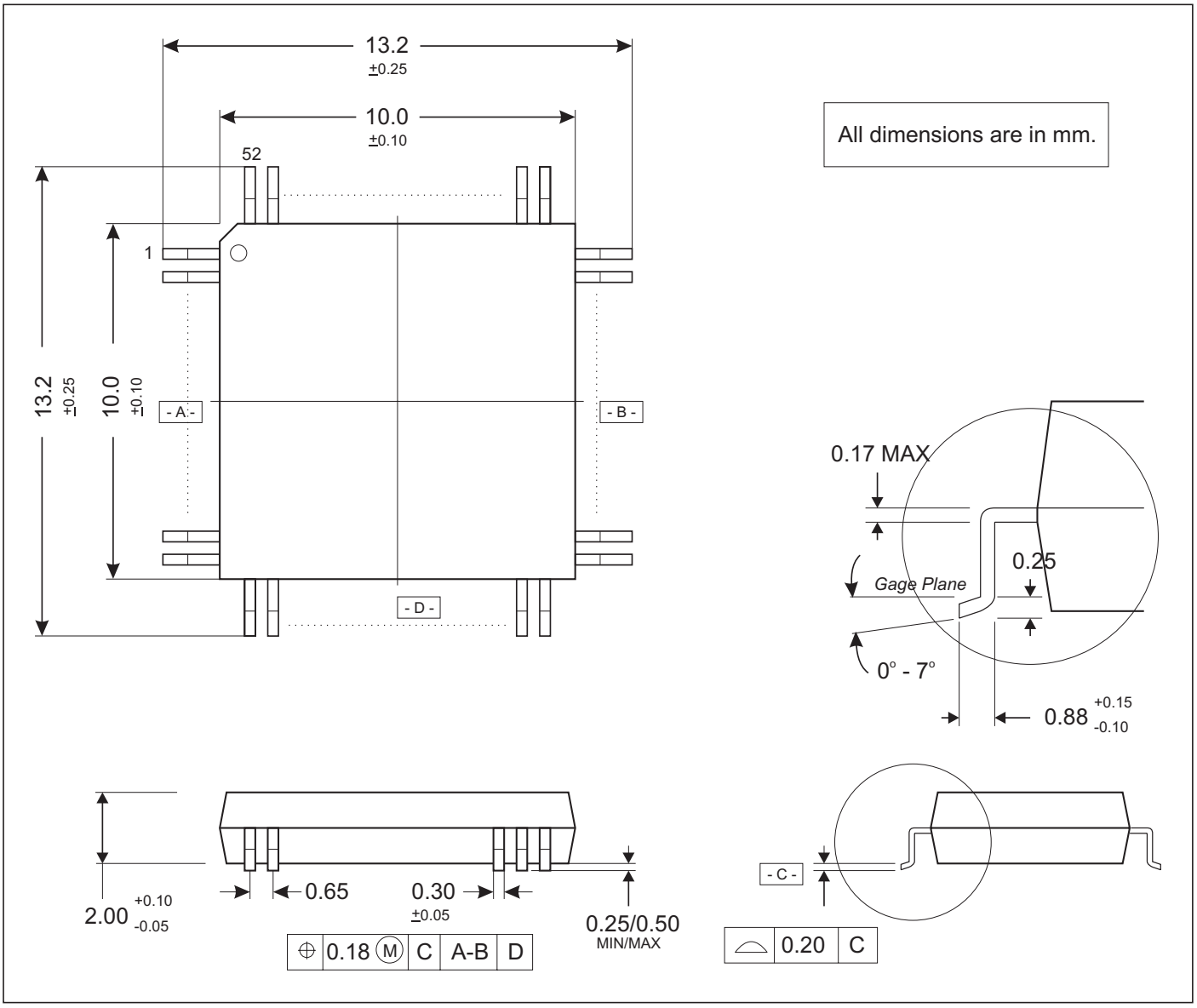


Figure 7. *Package 52 pin PQFP*

External References

GD90367/368	: Data sheet for the evaluation board for the GD16367B and GD16368B chip set (latest revision).
ITU-T G.751 (11/88)	: Digital multiplex equipments operating at the third order bit rate of 34368 kbit/s.
ITU-T G.813 (8/96)	: Timing characteristics of SDH equipment slave clocks.
ITU-T G.823 (3/93)	: The control of jitter and wander within digital networks based on the 2048 kbit/s hierarchy.
ITU-T G.825 (3/93)	: The control of jitter and wander within digital networks based on SDH.
DE/TM-3017-4 (Draft)	: Transmission and multiplexing; generic requirements for synchronisation networks.
DE/TM-03067 (Draft)	: Transmission and multiplexing; the control of jitter and wander in transport networks.

Device Marking

Figure 8. *Device Marking - Top View*

Ordering Information

To order, please specify as shown below:

Product Name:	Type:	Package Type:	Temperature Range:
GD16367B-52BA	Encoder	52 pin PQFP	0..75 °C
GD16368B-52BA	Decoder	52 pin PQFP	0..75 °C

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Distributor: