**DENSE-PAC**
MICROSYSTEMS

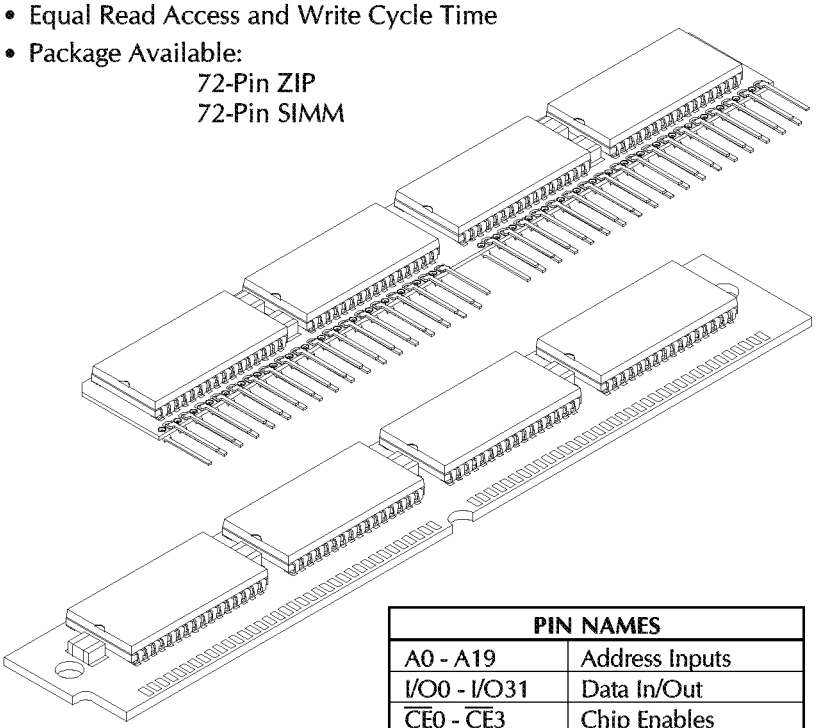
# 32 Megabit CMOS SRAM

## DESCRIPTION:

The DPS1MX32ML/DPS1MX32MW is a 1 Meg x 32 high density, high-speed Static Random Access Memory (SRAM) module, intended for high performance computers and digital signal processing applications. The DPS1MX32ML/DPS1MX32MW is comprised of eight 1 Meg x 4 devices surface mounted on an epoxy laminate substrate.

## FEATURES:

- 1 Meg x 32, 2 Meg x 16 or 4 Meg x 8 Configuration
- High Speed: 15, 17, 20, 25, 35ns
- All Inputs and Ouputs TTL Compatible
- Fully Static Operation; No Clock or Refresh Required
- Equal Read Access and Write Cycle Time
- Package Available:
  - 72-Pin ZIP
  - 72-Pin SIMM



PD0 = $V_{SS}$
PD1 = N.C.
PD2 = $V_{SS}$
PD3 = N.C.

| PIN NAMES | |
|---|---|
| A0 - A19 | Address Inputs |
| I/O0 - I/O31 | Data In/Out |
| $\overline{CE}$0 - $\overline{CE}$3 | Chip Enables |
| PD0 - PD3 | Density I.D. Pins [1] |
| $\overline{OE}$ | Output Enable |
| $\overline{WE}$ | Write Enable |
| $V_{DD}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| N.C. | No Connect |

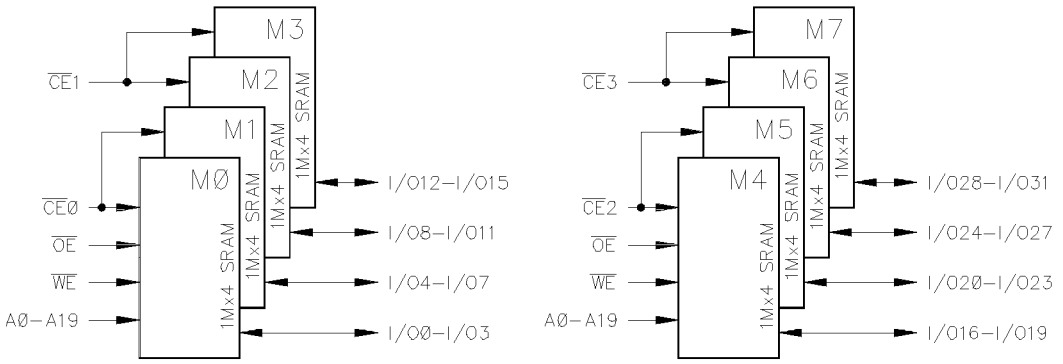
**PIN-OUT DIAGRAM**

TOP VIEW

| | | | | | |
|---|---|---|---|---|---|
| * INDEX → | | | 1 | N.C. |
| N.C. | 2 | | 3 | PD2 |
| PD3 | 4 | | 5 | VSS |
| PD0 | 6 | | 7 | PD1 |
| I/O0 | 8 | | 9 | I/O8 |
| I/O1 | 10 | | 11 | I/O9 |
| I/O2 | 12 | | 13 | I/O10 |
| I/O3 | 14 | | 15 | I/O11 |
| VDD | 16 | | 17 | A0 |
| A7 | 18 | | 19 | A1 |
| A8 | 20 | | 21 | A2 |
| A9 | 22 | | 23 | I/O12 |
| I/O4 | 24 | | 25 | I/O13 |
| I/O5 | 26 | | 27 | I/O14 |
| I/O6 | 28 | | 29 | I/O15 |
| I/O7 | 30 | | 31 | VSS |
| $\overline{WE}$ | 32 | | 33 | A15 |
| A14 | 34 | | 35 | $\overline{CE}$1 |
| $\overline{CE}$0 | 36 | | | |
| | | | 37 | $\overline{CE}$3 |
| $\overline{CE}$2 | 38 | | 39 | A17 |
| A16 | 40 | | 41 | $\overline{OE}$ |
| VSS | 42 | | 43 | I/O24 |
| I/O16 | 44 | | 45 | I/O25 |
| I/O17 | 46 | | 47 | I/O26 |
| I/O18 | 48 | | 49 | I/O27 |
| I/O19 | 50 | | 51 | A3 |
| A10 | 52 | | 53 | A4 |
| A11 | 54 | | 55 | A5 |
| A12 | 56 | | 57 | VDD |
| A13 | 58 | | 59 | A6 |
| I/O20 | 60 | | 61 | I/O28 |
| I/O21 | 62 | | 63 | I/O29 |
| I/O22 | 64 | | 65 | I/O30 |
| I/O23 | 66 | | 67 | I/O31 |
| VSS | 68 | | 69 | A18 |
| A19 | 70 | | 71 | NC |
| NC | 72 | | | |

* Index SIMM = Notch
ZIP = Chamfer

## FUNCTIONAL BLOCK DIAGRAM




### TRUTH TABLE

| Mode | $\overline{CE}$n | $\overline{WE}$ | $\overline{OE}$ | I/O Pin | Supply Current |
|---|---|---|---|---|---|
| Not Selected | H | X | X | HIGH-Z | Standby |
| $D_{OUT}$ Disable | L | H | H | HIGH-Z | Active |
| Read | L | H | L | $D_{OUT}$ | Active |
| Write | L | L | X | $D_{IN}$ | Active |

H = HIGH L = LOW X = Don't Care

### CAPACITANCE [5]: $T_A$ = 25°C, F = 1.0MHz

| Symbol | Parameter | Max. | Unit | Condition |
|---|---|---|---|---|
| $C_{ADR}$ | Address Input | 60 | pF | $V_{IN}$ = 0V |
| $C_{CE}$ | Chip Enable | 25 | | |
| $C_{WE}$ | Write Enable | 80 | | |
| $C_{OE}$ | Output Enable | 80 | | |
| $C_{I/O}$ | Data Input/Output | 15 | | |

### RECOMMENDED OPERATING RANGE [2]

| Symbol | Characteristic | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input HIGH Voltage | 2.2 | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input LOW Voltage | -0.5[3] | | 0.8 | V |
| $T_A$ | Operating Temp. | 0 | +25 | +70 | °C |

### DC OUTPUT CHARACTERISTICS

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | HIGH Voltage | $I_{OH}$ = -4.0mA | 2.4 | - | V |
| $V_{IL}$ | LOW Voltage | $I_{OL}$ = 8.0mA | | 0.4 | V |

### ABSOLUTE MAXIMUM RATINGS [4]

| Symbol | Parameter | Max. | Unit |
|---|---|---|---|
| $T_{STC}$ | Storage Temperature | -55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -10 to + 85 | °C |
| $V_{DD}$ | Supply Voltage [2] | -0.5 to + 7.0 | V |
| $V_{ID}$ | Input/Output Voltage [2] | -0.5 to $V_{DD}$ +0.5 | V |

### DC OPERATING CHARACTERISTICS: Over operating ranges

| Symbol | Characteristics | Test Conditions | COMMERCIAL | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| $I_{IN}$ | Input Leakage Current | $V_{IN}$ = 0V to $V_{DD}$ | -16 | +16 | µA |
| $I_{OUT}$ | Output Leakage Current | $V_{I/O}$ = 0V to $V_{DD}$, $\overline{CE}$n = $V_{IH}$ | -10 | +10 | µA |
| $I_{CC}$ | Operating Supply Current | $\overline{CE}$n = $V_{IL}$, f = max., $I_{OUT}$ = 0mA | | 1520 | mA |
| $I_{SB1}$ | Full Standby Supply Current | $V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V, $\overline{CE}$n ≥ $V_{DD}$ -0.2, f = 0mHz | | 120 | mA |
| $I_{SB2}$ | Standby Current | $\overline{CE}$n = $V_{IH}$, f = max. | | 480 | mA |
| $V_{OL}$ | Output Low Voltage | $I_{OUT}$ = 8.0mA | | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $I_{OUT}$ = -4.0mA | 2.4 | | V |

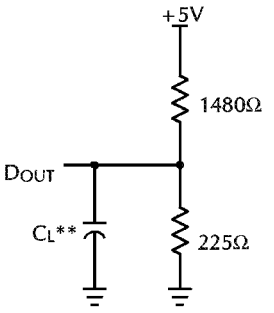
| AC TEST CONDITIONS | |
|---|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Pulse Rise and Fall Times | 5ns * |
| Input and Output Timing Reference Levels | 1.5V |

* Transition measured between 0.8V and 2.2V.

| Output Load | | |
|---|---|---|
| Load | $C_L$ | Parameters Measured |
| 1 | 30pF | except $t_{CLZ}$, $t_{CHZ}$, $t_{WHZ}$, $t_{OW}$, $t_{OLZ}$ and $t_{OHZ}$ |
| 2 | 5pF | $t_{CLZ}$, $t_{CHZ}$, $t_{WHZ}$, $t_{OW}$ |

Figure 1. Output Load

** Including Probe and Jig Capacitance.

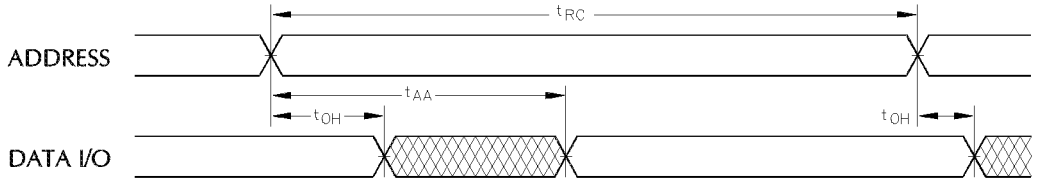



| AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | Symbol | Parameter | 15ns | | 17ns | | 20ns | | 25ns | | 35ns | | Unit |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | $t_{RC}$ | Read Cycle Time | 15 | | 17 | | 20 | | 25 | | 35 | | ns |
| 2 | $t_{AA}$ | Address Access Time | | 15 | | 17 | | 20 | | 25 | | 35 | ns |
| 3 | $t_{ACS}$ | Chip Enable Access Time | | 15 | | 17 | | 20 | | 25 | | 35 | ns |
| 4 | $t_{CLZ}$ | Chip Enable to Output in LOW-Z [5, 7] | 5 | | 5 | | 5 | | 5 | | 5 | | ns |
| 5 | $t_{OE}$ | Output Enable to Output Valid | | 8 | | 8 | | 10 | | 12 | | 12 | ns |
| 6 | $t_{OLZ}$ | Output Enable to Output in LOW-Z [5, 7] | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| 7 | $t_{CHZ}$ | Chip Enable to Output in HIGH-Z [5, 7] | 0 | 7 | 0 | 7 | 0 | 9 | 0 | 10 | 0 | 12 | ns |
| 8 | $t_{OHZ}$ | Output Enable to Output in HIGH-Z [5, 7] | 0 | 7 | 0 | 7 | 0 | 9 | 0 | 10 | 0 | 12 | ns |
| 9 | $t_{OH}$ | Output Hold from Address Change | 5 | | 5 | | 5 | | 5 | | 5 | | ns |

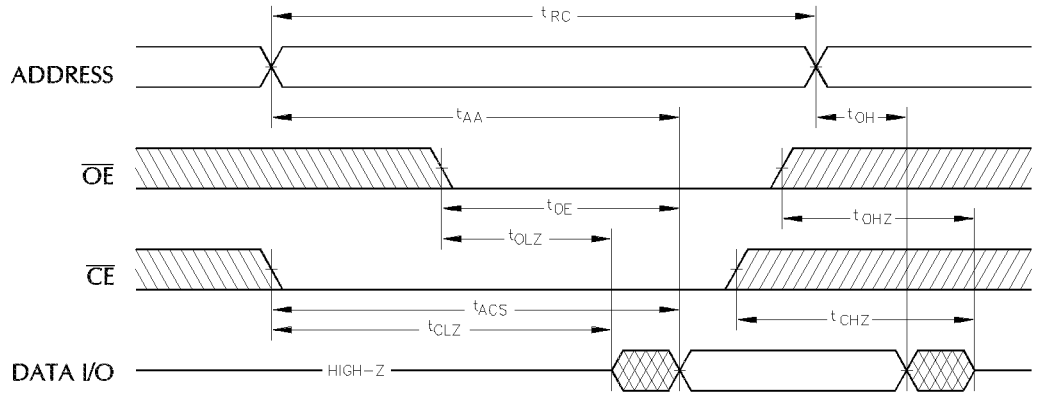
| AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [8] | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | Symbol | Parameter | 15ns | | 17ns | | 20ns | | 25ns | | 35ns | | Unit |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 10 | $t_{WC}$ | Write Cycle Time | 15 | | 17 | | 20 | | 25 | | 35 | | ns |
| 12 | $t_{CW}$ | Chip Enable to End of Write | 12 | | 12 | | 15 | | 17 | | 20 | | ns |
| 11 | $t_{AW}$ | Address Valid to End of Write | 12 | | 12 | | 15 | | 17 | | 20 | | ns |
| 13 | $t_{AS}$ | Address Set-up Time *** | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| 14 | $t_{WP}$ | Write Pulse Width | 12 | | 12 | | 15 | | 17 | | 20 | | ns |
| 15 | $t_{WR}$ | Write Recovery Time | 3 | | 3 | | 3 | | 3 | | 3 | | ns |
| 16 | $t_{WHZ}$ | Write Enable to Output in HIGH-Z [5, 7] | 0 | 7 | 0 | 8 | 0 | 9 | 0 | 10 | 0 | 15 | ns |
| 17 | $t_{DW}$ | Data to Write Time Overlap | 8 | | 8 | | 10 | | 12 | | 15 | | ns |
| 18 | $t_{DH}$ | Data Hold Time from Write Time | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| 19 | $t_{OW}$ | Output Active from End of Write [5, 7] | 3 | | 5 | | 5 | | 5 | | 5 | | ns |

*** Valid for both Read and Write Cycles.

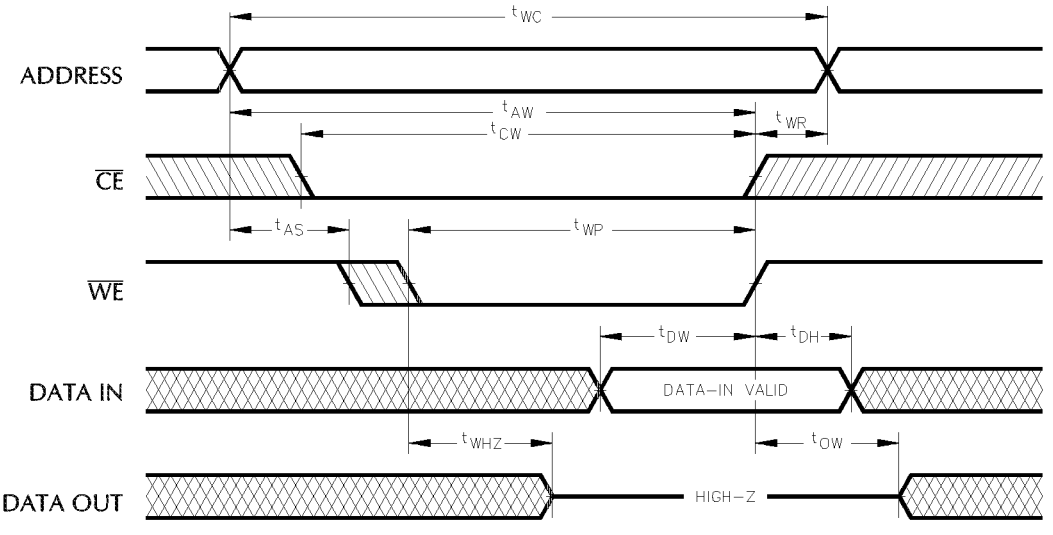
**READ CYCLE 1:** Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



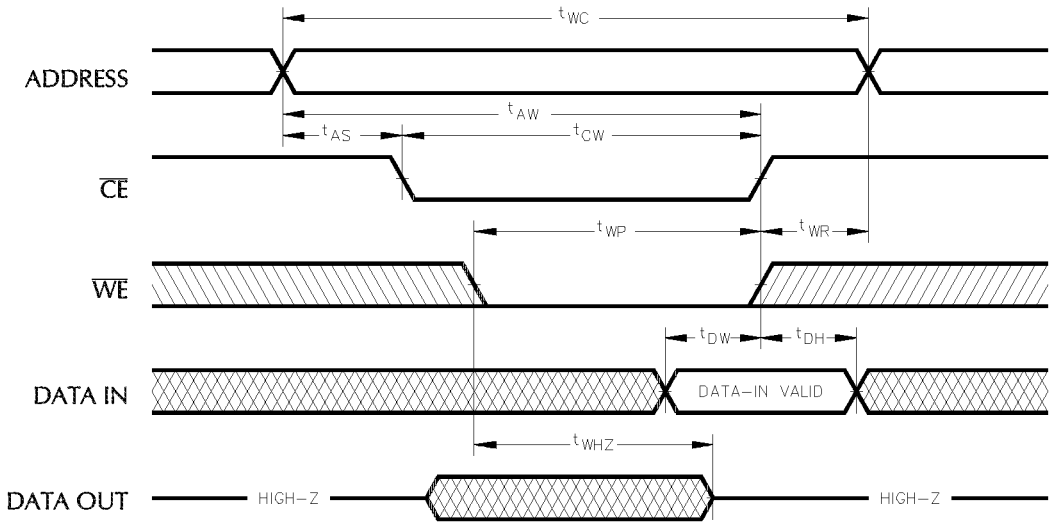

**READ CYCLE 2:** $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.




**WRITE CYCLE 1:** $\overline{WE}$ Controlled.. [8]



**WRITE CYCLE 2: $\overline{CE}$ Controlled.**




**NOTES:**

1. The PD0 - PD3 pins are used to identify memory density when other density versions of the JEDEC STD module can be installed in the same socket.
2. All voltages are with respect to $V_{SS}$.
3. -2.0V min. for pulse width less than 20ns ($V_{IL}$ min. = -0.5V at DC level).
4. Stresses greater than those under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. This parameter is guaranteed and not 100% tested.
6. Transition is measured at the point of ± 500mV from steady state voltage.
7. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
8. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

**WAVEFORM KEY**

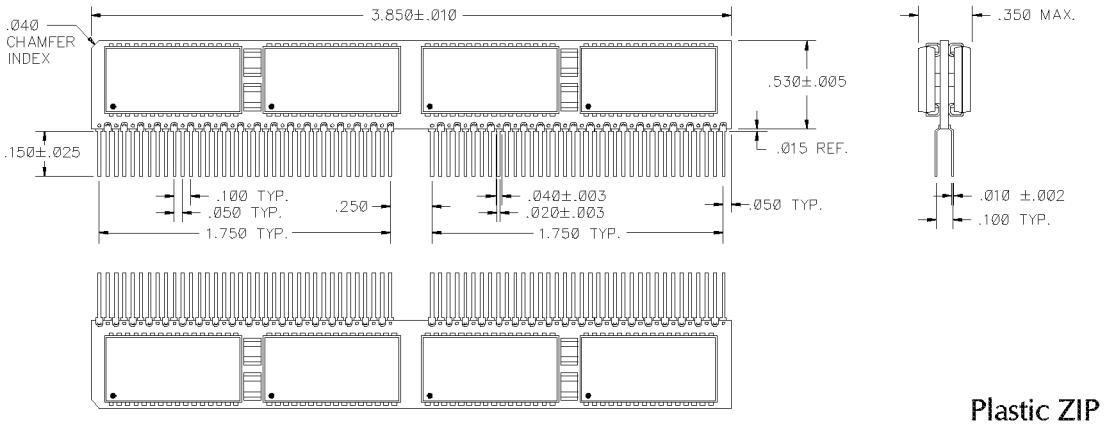
| Data Valid | Transition from HIGH to LOW | Transition from LOW to HIGH | Data Undefined or Don't Care |
|---|---|---|---|

## ORDERING INFORMATION

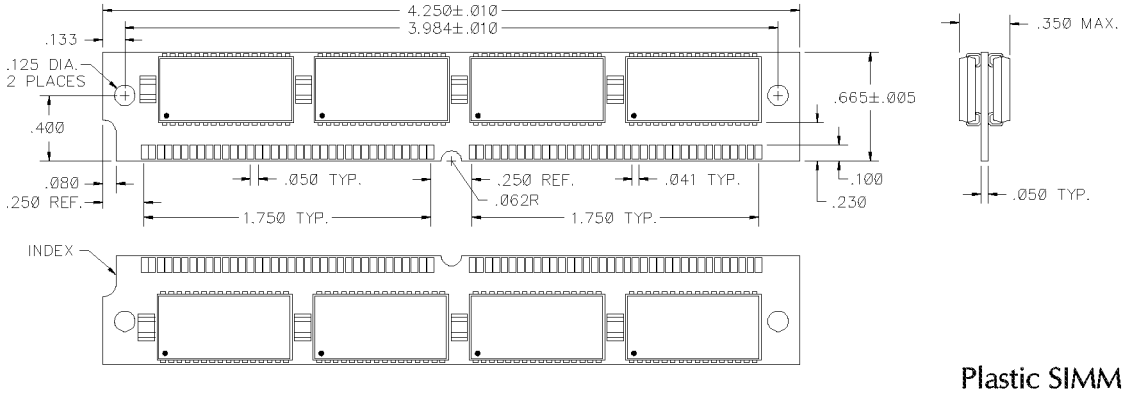
| DP | S | 1M | X | 32 | M | X | – XX | C |
|---|---|---|---|---|---|---|---|---|
| PREFIX | TYPE | MEMORY DEPTH | DESIG | MEMORY WIDTH | DESIG | PACKAGE | SPEED | GRADE |

- GRADE: C COMMERCIAL 0°C to +70°C
- SPEED: 15 15ns; 17 17ns; 20 20ns; 25 25ns; 35 35ns
- PACKAGE: L PLASTIC ZIP (LEADED); W PLASTIC SIMM (LEADLESS)
- MEMORY DESIG: 4 MEGABIT BASED DEVICES
- MEMORY WIDTH: 32
- DESIG: MEMORY MODULE WITHOUT SUPPORT LOGIC
- TYPE: CMOS SRAM

## MECHANICAL DRAWINGS




Plastic ZIP




Plastic SIMM

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