CY2XP41

Crystal to LVPECL Clock Generator

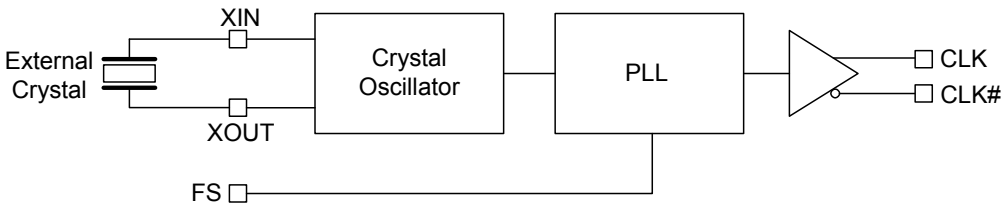
Features

- One LVPECL output pair
- External crystal frequency: 25.0 MHz
- Selectable Output Frequency: 62.5 MHz or 75 MHz
- Low RMS phase jitter at 75 MHz, using 25 MHz crystal (1.5 MHz–10 MHz): 0.27 ps (typical)
- Low RMS phase jitter at 62.5 MHz, using 25 MHz crystal (1.5 MHz–10 MHz): 0.38 ps (typical)
- Pb-free 8-Pin TSSOP package
- Supply voltage: 3.3V
- Commercial Temperature Range

Functional Description

The CY2XP41 is a PLL (Phase Locked Loop) based high performance clock generator. It is optimized to generate high performance clock frequencies for DVD-R applications. It uses Cypress's low noise VCO technology to achieve less than 1 ps typical RMS phase jitter, that meets application jitter requirements. The CY2XP41 has a crystal oscillator interface input and one LVPECL output pair.

Logic Block Diagram



Pinouts

Figure 1. Pin Diagram - 8 Pin TSSOP

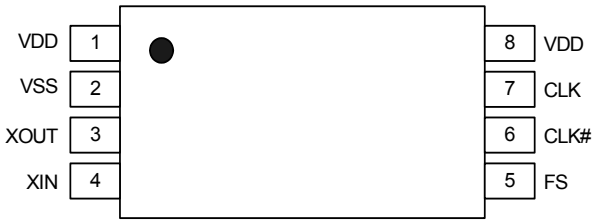


Table 1. Pin Definitions - 8 Pin TSSOP

Pin	Name	Type	Description
1, 8	VDD	Power	3.3V power supply. All supply current flows through pin 1
2	VSS	Power	Ground
3, 4	XOUT, XIN	XTAL output and input	Parallel resonant crystal interface
5	FS	LVCMOS/LVTTL input	Frequency Select Input, See “Frequency Table” on page 3
6,7	CLK#, CLK	LVPECL output	Differential Clock Output

Frequency Table

Input		Output Frequency (MHz)
Input Xtal Frequency (MHz)	FS	
25	0	62.5
25	1	75.0

Absolute Maximum Conditions

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.4	V
V_{IN}[1.]	Input Voltage, DC	Relative to VSS	–0.5	V_{DD} + 0.5	V
T_S	Temperature, Storage	Non Functional	–65	150	°C
T_J	Temperature, Junction			135	°C
ESD_{HBM}	ESD Protection (Human Body Model)	JEDEC STD 22-A114-B	2000		V
UL–94	Flammability Rating	At 1/8 in.	V–0		
Θ_{JA}[2]	Thermal Resistance, Junction to Ambient	0 m/s airflow	100		°C/W
		1 m/s airflow	91		
		2.5 m/s airflow	87		

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DD}	3.3V Supply Voltage	3.135	3.465	V
T_A	Ambient Temperature, Commercial	0	70	°C
T_{PU}	Power up time for all V_{DD} to reach minimum specified voltage (ensure power ramps are monotonic)	0.05	500	ms

Electrical Characteristics for Input

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–	–	$0.3*V_{DD}$	V
V_{IH}	Input High Voltage		$0.7*V_{DD}$	–	–	V
I_{IL}	Input Low Current	FS = V_{SS}	–50	–	–	µA
I_{IH}	Input High Current	FS = V_{DD}	–	–	115	µA
C_{IN}	Input Capacitance			15		pF

DC Electrical Characteristics for Power Supplies

Parameter	Description	Min	Typ	Max	Unit
I_{DD}[3]	Power Supply Current with output terminated	–	–	180	mA

Note
1. The voltage on any input or IO pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
2. Simulated using Apache Sentinel TI software. The board is derived from the JEDEC multilayer standard. It measures 76 x 114 x 1.6 mm and has 4-layers of copper (2/1/1/2 oz.). The internal layers are 100% copper planes, while the top and bottom layers have 50% metallization. No vias are included in the model.
3. I_{DD} includes ~16 mA of current that is dissipated externally in the output termination resistors.

DC Electrical Characteristics for LVPECL Output

Parameter	Description	Min	Typ	Max	Unit
V_{CM}	Common-Mode Voltage (CLK + CLK#) / 2, defined in Figure 5 on page 5, using Figure 2 on page 5 circuit.	175	–	2000	mV
V_{PP}	Differential Peak Output Voltage, defined in Figure 5 on page 5, using Figure 2 on page 5 circuit.	350	780	850	mV

Crystal Characteristics

Parameter	Description	Min	Typ	Max	Unit
	Mode of Oscillation		Fundamental		
F	Frequency	–	25	–	MHz
ESR	Equivalent Series Resistance	–	–	50	Ω
C_L	Crystal Load Capacitance	–	10	–	pF
C_S	Shunt Capacitance	–	–	7	pF
DL	Crystal Drive Level	–	–	300	µW

AC Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
F_{OUT}	Output Frequency		62.5	–	75.0	MHz
T_R/T_F	Output Rise/Fall time	Defined in Figure 5 on page 5	–	350	–	ps
$T_{Jitter(\phi)}$	RMS Phase Jitter (Random)	75 MHz, (1.5 MHz - 10 MHz filter), 3.3V	–	0.27	–	ps
		62.5 MHz, (1.5 MHz - 10 MHz filter), 3.3V	–	0.38	–	ps
T_{DC}	Duty Cycle	Defined in Figure 4 on page 5	45	–	55	%

Measurement Definitions

Figure 2. Output Load AC Test Circuit

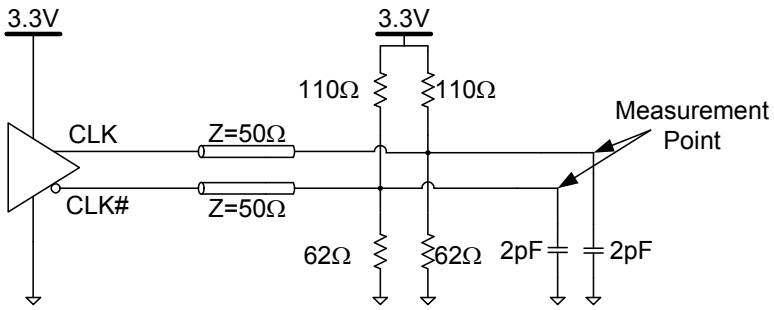


Figure 3. RMS Phase Jitter

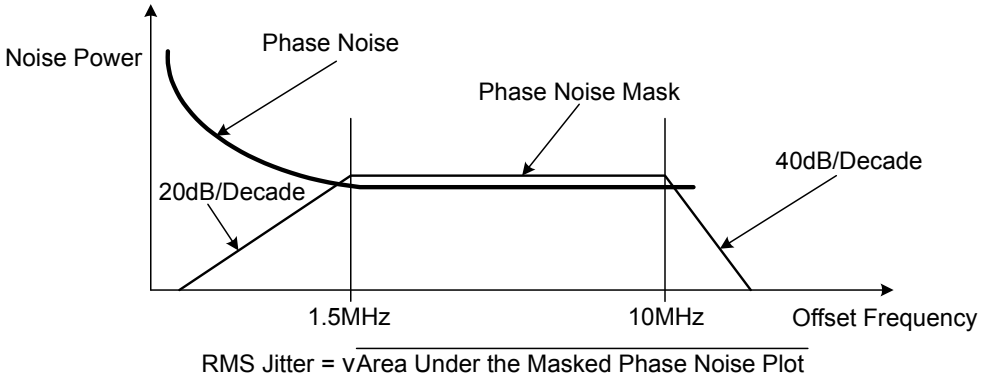


Figure 4. Output Duty Cycle

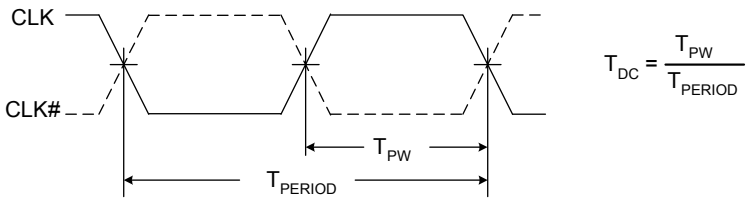
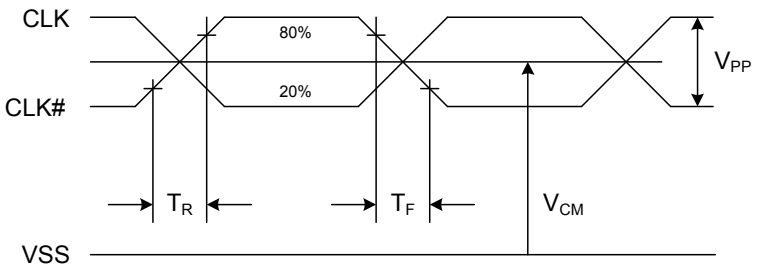


Figure 5. Output Rise and Fall Time and Peak-Peak Voltage Swing

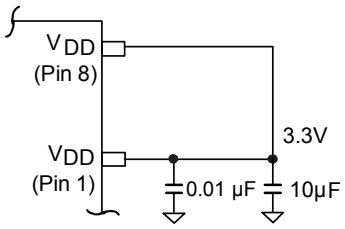


Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, noise at the power supply pins degrades performance. To achieve optimum jitter performance, good power supply isolation practices are advised. Figure 6. shows a typical filtering scheme. Since all of the current flows through pin 1, the resistance and inductance between this pin and the supply is minimized. A 0.01 or 0.1 µF ceramic chip capacitor is also located close to this pin to provide a short and low impedance AC path to ground. A ~5 to 10 µF tantalum capacitor is also located in the vicinity of this device.

Figure 6. Power Supply Filtering



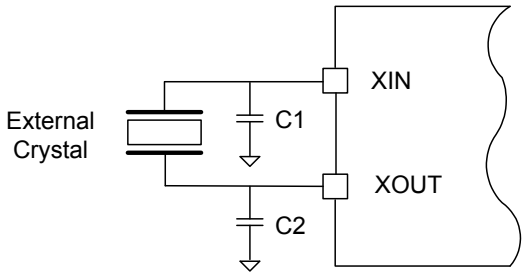
Termination for 3.3V LVPECL Output

CLK and CLK# are pull up drivers that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources are used for functionality. Matched impedance techniques are used to maximize operating frequency and minimize signal distortion. Figure 2 on page 5 shows a termination scheme that is recommended as a guideline. Other suitable clock layouts exist and it is recommended that the board designers simulate to guarantee compatibility across all printed circuit and process variations. **Cypress recommends the following RU and RD values: RU=110Ω and RD=62Ω.** This is a 40Ω load, which is used to achieve the specified common mode and peak-to-peak voltage swing. For optimal signal integrity, 40Ω traces are recommended.

Crystal Input Interface

The CY2XP41 is characterized with 10 pF parallel resonant crystals. The capacitor values shown in Figure 7. are determined using a 25 MHz 10 pF parallel resonant crystal and are chosen to minimize the ppm error. **Cypress recommends the following C1 and C2 values: C1 = C2 = 6.8pF.**

Figure 7. Crystal Input Interface

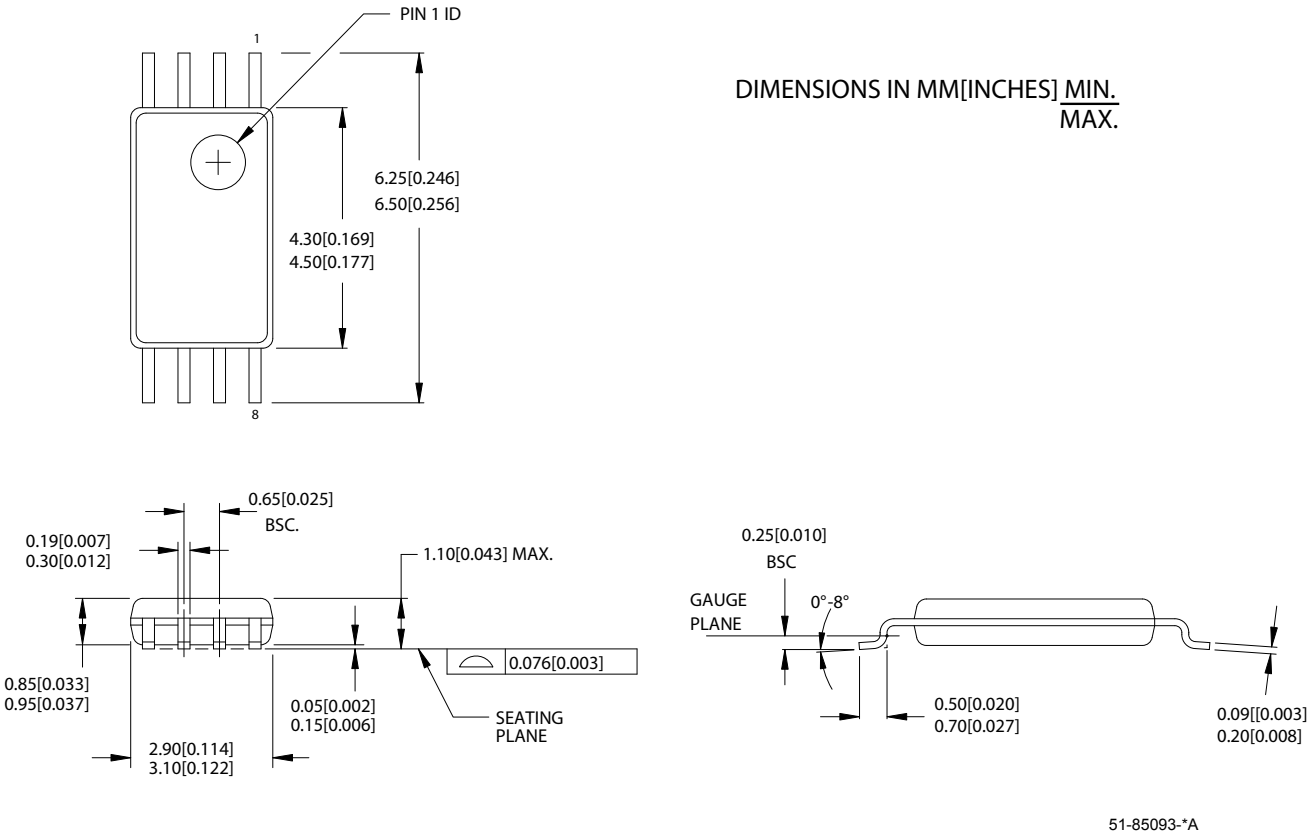


Ordering Information

Part Number	Package Type	Product Flow
CY2XP41ZXC	8-Pin TSSOP	Commercial, 0°C to 70°C
CY2XP41ZXCT	8-Pin TSSOP–Tape and Reel	Commercial, 0°C to 70°C

Package Drawing and Dimensions

Figure 8. 8-Pin Thin Shrunk Small Outline Package (4.40mm Body) Z8



Document History Page

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REV.	**ECN NO.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2669117	03/05/09	XHT/CXQ/ KVM	New data sheet
*A	2718433	06/12/09	WWZ/HMT	No change. Submit to ECN for product launch.

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