CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX7131/CMX7141

Digital PMR Processor

dPMR

D/7131/41_FI-1.0/7 October 2009

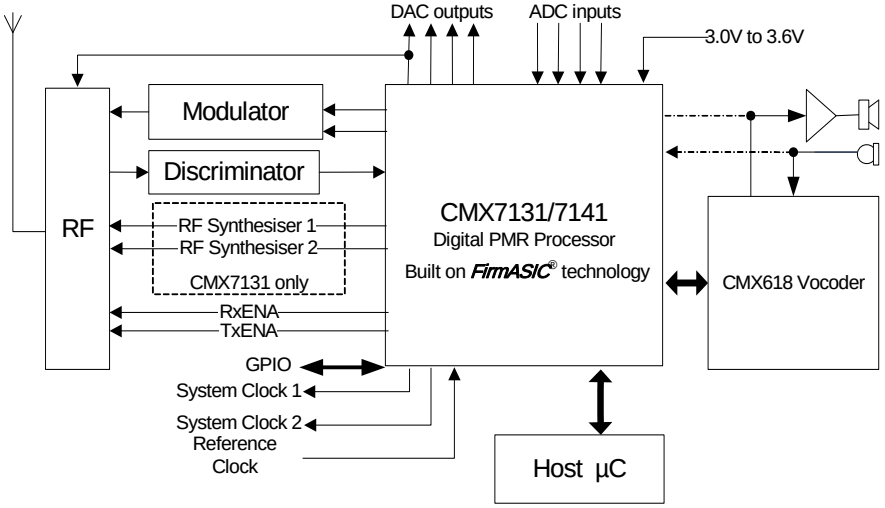
DATASHEET

Advance Information

7131/7141FI-1.x: dPMR Baseband Data Processor with Auxiliary System Clocks, ADCs and DACs

Features

- Digital PMR
- dPMR (ETSI TS 102 490) Compliant
- Air Interface Physical Layer (Layer 1)
- Air Interface Data Link Layer (Layer 2)
- 4FSK Modem
- 4.8 and 9.6 kbps Data Rates
- Soft-decision Data Output Option
- AFSD (Automated Frame Sync Detection)
- Raw Data Mode
- Vocoder Connectivity
- Vocoder Management and Control
- Vocoder Data Transport
- 2 Auxiliary ADCs (4 Multiplexed Inputs)
- 4 Auxiliary DACs
- 2 Auxiliary System Clock Outputs
- Tx Outputs for Two Point or I/Q Modulation
- Flexible Powersave Modes
- Available in Small LQFP or VQFN Packages
- Low-power (3.3V) Operation
- C-BUS Serial Interface to Host µController
- Two RF Synthesisers (CMX7131 only)



This document contains:

1 Brief Description

The 7131/7141FI-1.x Function Image™ (FI) implements a half-duplex 4FSK modem and a large proportion of the dPMR Air Interface, Data Link and Call Control layers. In conjunction with a suitable host and a limiter/discriminator based RF transceiver, a compact, low cost, low power digital PMR radio conforming to ETSI's dPMR standard TS 102 490 can be realised. Dual mode, analogue/digital PMR operation can also be achieved with the CMX7131/CMX7141. Both ISF and CSF configurations are supported, including built-in support for BCD addressing modes.

The embedded functionality of the CMX7131/CMX7141, managing voice and data systems autonomously including CMX6x8 Vocoder control (via the Auxiliary SPI/C-BUS interface), minimises host microcontroller interactions enabling the lowest operating power and therefore the longest battery life for a dPMR radio.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external EEPROM or host µController over the built-in C-BUS serial interface. The device's functions and features may be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades. This document refers specifically to the features provided by Function Image™ 1.x.

Other features include two auxiliary ADCs with four selectable inputs and four auxiliary DAC interfaces (with an optional RAMDAC on the first DAC output, to facilitate transmitter power ramping). Additionally the CMX7131 features two on-chip RF synthesisers, with easy Rx/Tx frequency changeover.

The CMX7141 is identical in functionality to the CMX7131 with the exception that the two on-chip RF Synthesisers have been deleted, which enables it to be supplied in a smaller package. This document refers to both parts, unless otherwise stated.

The device has flexible powersaving modes and is available in both LQFP and VQFN packages.

Note that text shown in pale grey indicates features that will be supported in future versions of the Function Image™.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained by registering your interest in this product with your local CML representative.

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Figure Page

Information in this data sheet should not be relied upon for final product design. It is always recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
7	• 3.1 added • 6.2 (Device Control) revised • 6.3 (dPMR description) revised • 7.3 Company standard text and diagrams used • 7.4 6x8 supported modes clarified • 7.5.6 PRBS pattern conforms to EN 300 113 • 7.6.4 Addition of “silence” payload at Vocoder start-up • 7.11 references to RF “channel” replaced by RF “Synthesiser”	06.10.09
6	• CMX7131 features added • Modulation Diagram updated to latest (fig 9) • Note added that 9600bps mode does not support automated CMX6x8 operation (6.3) • C-BUS timing diagram updated to latest (fig 23) • RAMDAC timing updated to latest • GPIO1&2 defined as Rx and Tx Enable • C-BUS signal names standardised • Contact details updated • Document style normalised	21.4.09 8.5.09 29.6.09
5	• Slow data support for Type 1 and Type 2 data modes • BCD wildcard reporting added • Additional Binary Group call ID’s added • FS detect flow chart and text added (Normal and Late Entry Calls) • Internal processing block diagram added • Slow Data IRQ added • Parametric specifications clarified	10.11.08
4	• Slow Data in voice mode added • Corrected AuxADC conversion time • Extended xtal f_{low} to 3MHz • Fine Input Attenuation removed	22.07.08

3	• Removal of C11 to ensure DC coupling of DISC input for 4-level FSK (4FSK) modulation • Updated Function Image™ software release list	25.06.08
2	• First released document, prepared for first beta release of software	19.11.07
1	• Original document, prepared for internal use	mid 2007

This is Advance Information; changes and additions may be made to this specification. Parameters marked TBD or left blank will be included in later issues. Items that are highlighted or greyed out should be ignored. These will be clarified in later issues of this document.
Information in this datasheet should not be relied upon for final product design.

2 Block Diagram

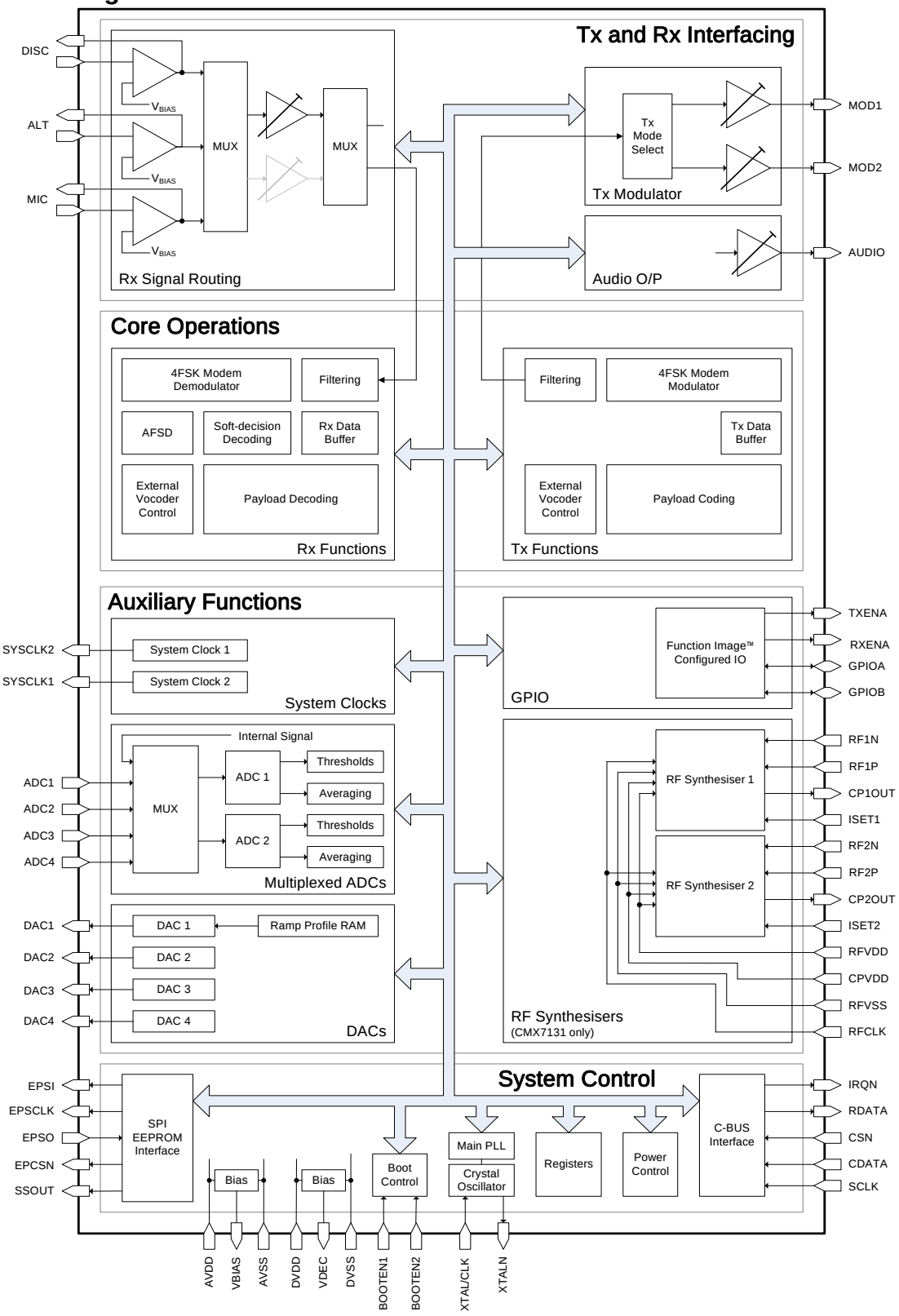


Figure 1 Block Diagram

3 Signal List

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Signal Name	Type	Description
1	**8**	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to DV_{SS} when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
2	-	RF1N	IP	RF Synthesiser #1 Negative Input
3	-	RF1P	IP	RF Synthesiser #1 Positive Input
4	-	RFVSS	PWR	RFV_{SS}: The negative supply rail (ground) for the 1st RF synthesiser
5	-	CP1OUT	OP	1st Charge Pump output
6	-	ISET1	IP	1st Charge Pump Current Set input
7	-	RFVDD	PWR	RFV_{DD} : The 2.5V positive supply rail for the RF synthesisers. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
8	-	RF2N	IP	RF Synthesiser #2 Negative Input
9	-	RF2P	IP	RF Synthesiser #2 Positive Input
10	-	RFVSS	PWR	RFV_{SS}: The negative supply rail (ground) for the 2nd RF synthesiser.
11	-	CP2OUT	OP	2nd Charge Pump output
12	-	ISET2	IP	2nd Charge Pump Current Set input
13	-	CPVDD	PWR	The 3.3V positive supply rail for the RF charge pumps. This should be decoupled to RFV_{SS} by a capacitor mounted close to the device pins.
14	-	RFCLK	IP	RF Clock Input (common to both synthesisers)[1]
15	-	GPIOA	OP	General Purpose I/O pin (7131 only)
16	-	GPIOB	OP	General Purpose I/O pin (7131 only)
17	-	-	NC	*reserved*– do not connect this pin
18	**9**	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFV_{DD}.
19	**10**	RXENA	OP	Rx Enable – active low when in Rx mode ($C1:b0 = 1)
-	**11**	GPIOA	OP	General Purpose I/O pin (7141 only)
-	**12**	GPIOB	OP	General Purpose I/O pin (7141 only)
20	**13**	SYSCLK1	OP	Synthesised Digital System Clock Output 1
21	**14**	DVSS	PWR	DV_{SS} Digital Ground
22	-	-	NC	*reserved* – do not connect this pin
23	**15**	TXENA	OP	Tx Enable – active low when in Tx mode ($C1:b1 = 1)

[1] To minimise crosstalk, this signal should be connected to the same clock source as XTAL / CLOCK input.

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Signal Name	Type	Description	
24	**16**	DISC	IP	Channel 1 inverting input	
25	**17**	DISCFB	OP	Channel 1 input amplifier feedback	
26	**18**	ALT	IP	Channel 2 inverting input	
27	**19**	ALTFB	OP	Channel 2 input amplifier feedback	
28	**20**	MICFB	OP	Channel 3 input amplifier feedback	
29	**21**	MIC	IP	Channel 3 inverting input	
30	**22**	AVSS	PWR	AV_{SS} Analogue Ground	
31	**23**	MOD1	OP	Modulator 1 output	
32	**24**	MOD2	OP	Modulator 2 output	
33	**25**	VBIAS	OP	Internally generated bias voltage of about $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins. No other connections allowed.	
34	**26**	AUDIO	OP	*reserved for future use*[2]	
35	**27**	ADC1	IP	Auxiliary ADC input 1	Each of the two ADC blocks can select its input signal from any one of these input pins, or from the MIC, ALT or DISC input pins. See section 10.1.3 for details.
36	**28**	ADC2	IP	Auxiliary ADC input 2	
37	**29**	ADC3	IP	Auxiliary ADC input 3	
38	**30**	ADC4	IP	Auxiliary ADC input 4	
39	**31**	AVDD	PWR	AV_{DD}: Analogue +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AV_{SS} by capacitors mounted close to the device pins.	
40	**32**	DAC1	OP	Auxiliary DAC output 1/RAMDAC	
41	**33**	DAC2	OP	Auxiliary DAC output 2	
42	**34**	AVSS	PWR	AV_{SS}: Analogue Ground	
43	**35**	DAC3	OP	Auxiliary DAC output 3	
44	**36**	DAC4	OP	Auxiliary DAC output 4	
-	**37**	DVSS	PWR	DV_{SS}: Digital Ground	
45	**38**	VDEC	PWR	V_{DEC}: Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFV_{DD}.	
46	**39**	XTAL/CLK	IP	Input from the external clock source or Xtal	
47	**40**	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external clock used.	
48	**41**	DVDD	PWR	DV_{DD}: Digital +3.3V supply rail. This pin should be decoupled to DV_{SS} by capacitors mounted close to the device pins.	

[2] The AUDIO OUT pin is not currently used in this FI, however it has been included here for compatibility with future products.

CMX7131 64-pin Q1/L9	CMX7141 48-pin Q3/L4	Signal Name	Type	Description
49	**42**	CDATA	IP	C-BUS Command Data: Serial data input from the µC
50	**43**	RDATA	TS OP	C-BUS Reply Data: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
51	**44**	SSOUT	OP	SPI bus Chip Select/Frame Sync (used for CMX6x8)
52	**45**	DVSS	PWR	DV_{SS} :Digital Ground
53	-	-	NC	*reserved* – do not connect this pin
54	**46**	SCLK	IP	C-BUS Serial Clock: The C-BUS serial clock input from the µC.
55	**47**	SYSCLK2	OP	Synthesised Digital System Clock Output 2
56	**48**	CSN	IP	C-BUS Chip Select: The C-BUS chip select input from the µC - there is no internal pullup on this input
57	-	-	NC	*reserved* – do not connect this pin
58	**1**	EPSI	OP	EEPROM Serial Interface: SPI bus Output
59	**2**	EPSCLK	OP	EEPROM Serial Interface: SPI bus Clock
60	**3**	EPSO	IP+PD	EEPROM Serial Interface: SPI bus Input
61	**4**	EPSCSN	OP	EEPROM Serial Interface: SPI bus ChipSelect
62	**5**	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
63	**6**	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
64	**7**	DVSS	PWR	DV_{SS} :Digital Ground
EXPOSED METAL PAD	EXPOSED METAL PAD	SUBSTRATE	~	On this device, the central metal pad (which is exposed on Q1 and Q3 packages only) may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connection is permitted.**

Notes: IP = Input (+ PU/PD = internal pullup/pulldown resistor)
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal.

3.1 Signal Definitions

Table 1 Definition of Power Supply and Reference Voltages

Signal Name	Pins	Usage
AV_{DD}	AVDD	Power supply for analogue circuits
DV_{DD}	DVDD	Power supply for digital circuits
V_{DEC}	VDEC	Power supply for core logic, derived from DV_{DD} by on-chip regulator
V_{BIAS}	VBIAS	Internal analogue reference level, derived from AV_{DD}
AV_{SS}	AVSS	Ground for all analogue circuits
DV_{SS}	DVSS	Ground for all digital circuits

4 External Components

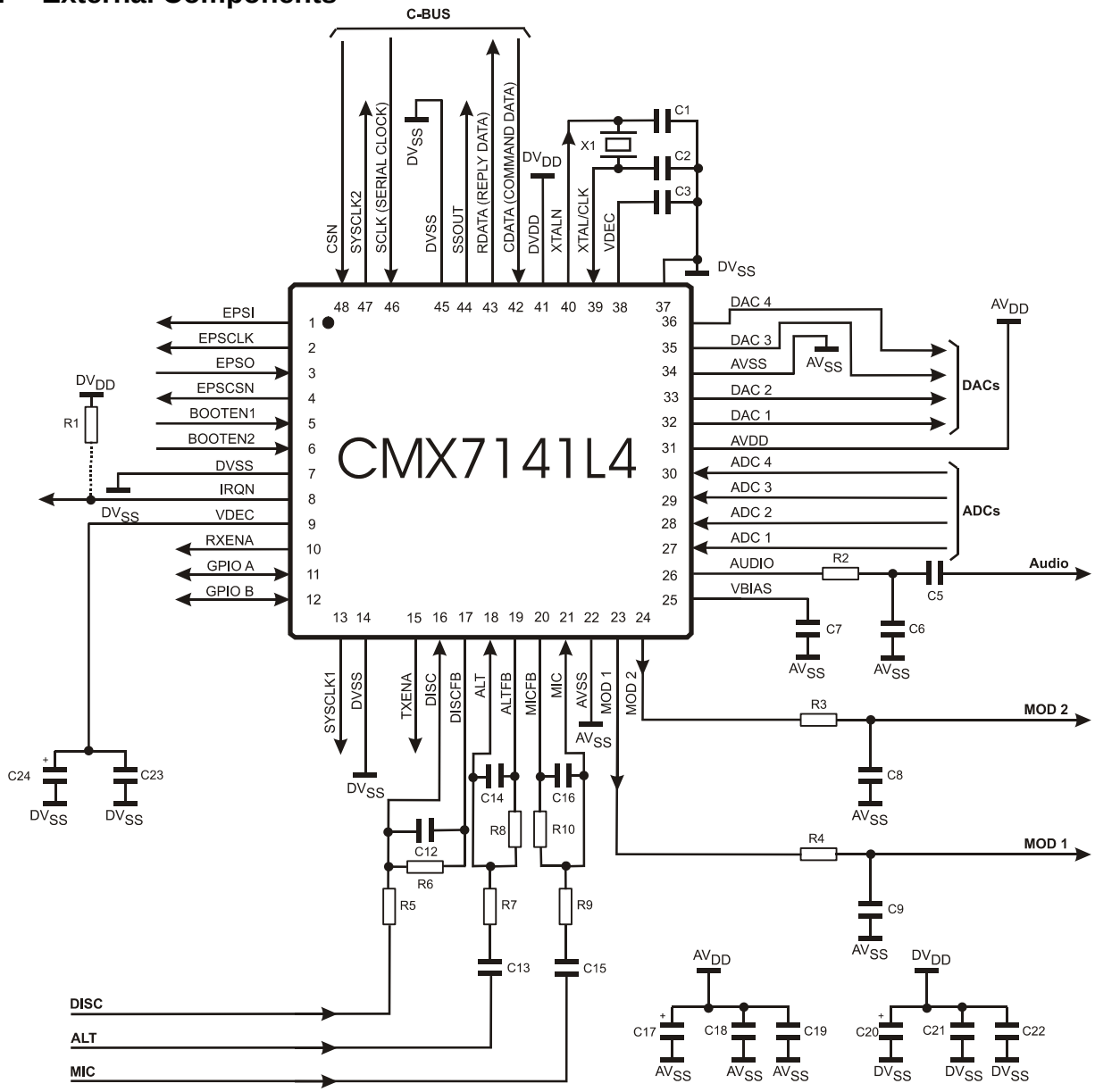


Figure 2 CMX7141 Recommended External Components

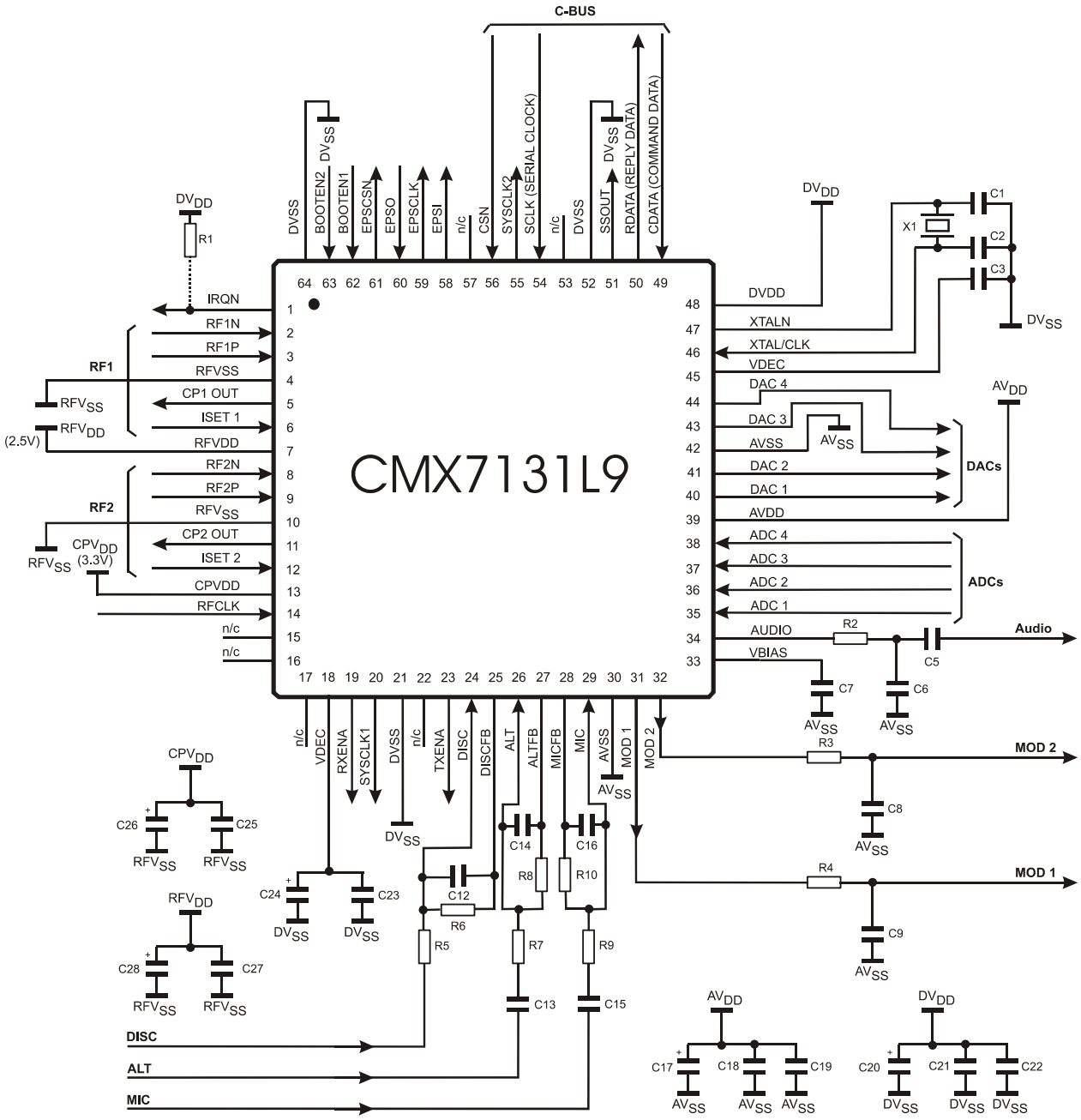


Figure 3 CMX7131 Recommended External Components

4.1 Recommended External Components

R1	100kΩ	C1	18pF	C11	*not used*	C21	10nF
R2	100kΩ	C2	18pF	C12	100pF	C22	10nF
R3	100kΩ	C3	10nF	C13	See note 5	C23	10nF
R4	100kΩ	C4	*not used*	C14	100pF	C24	10µF
R5	See note 2	C5	1nF	C15	See note 5		
R6	100kΩ	C6	100pF	C16	200pF		
R7	See note 3	C7	100nF	C17	10µF		
R8	100kΩ	C8	100pF	C18	10nF	X1	6.144MHz
R9	See note 4	C9	100pF	C19	10nF		See note 1
R10	100kΩ	C10	*not used*	C20	10µF		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, a 19.2MHz oscillator is assumed (in which case C1 and C2 are not required), other values could be used if the various internal clock dividers are set to appropriate values.

2. R5 should be selected to provide the desired dc gain of the discriminator input, as follows:

$$|GAIN_{DISC}| = 100k\Omega / R5$$

   The gain should be such that the resultant output at the DISCFB pin is within the DISC input signal range specified in 7.13.2. For 4FSK modulation, this signal should be dc coupled from the Limiter/ Discriminator output.

3. R7 should be selected to provide the desired dc gain (assuming C13 is not present) of the alternative input as follows:

$$|GAIN_{ALT}| = 100k\Omega / R7$$

   The gain should be such that the resultant output at the ALTFB pin is within the alternative input signal range specified in 7.13.

4. R9 should be selected to provide the desired dc gain (assuming C15 is not present) of the microphone input as follows:

$$|GAIN_{MIC}| = 100k\Omega / R9$$

   The gain should be such that the resultant output at the MICFB pin is within the microphone input signal range specified in 7.13.1. For optimum performance with low signal microphones, an additional external gain stage may be required.

5. C13 and C15 should be selected to maintain the lower frequency roll-off of the MIC and ALT inputs as follows:

$$C13 \geq 1.0\mu F \times |GAIN_{ALT}|$$
$$C15 \geq 30nF \times |GAIN_{MIC}|$$

6. ALT and ALTFB connections allow the user to have a second discriminator or microphone input. Component connections and values are as for the respective DISC and MIC networks. If this input is not required, the ALT pin should be connected to AV_{SS}.

7. C5 (AUDIO) should be increased to 1.0µF if frequencies below 300Hz need to be used on this pin.

8. A single 10µF electrolytic capacitor (C24, fitted as shown) may be used for smoothing the power supply to both VDEC pins, providing they are connected together on the pcb with an adequate width power supply trace. Alternatively, separate smoothing capacitors should be connected to each VDEC pin. High frequency decoupling capacitors (C3 and C23) must always be fitted as close as possible to both VDEC pins.

5 PCB Layout Guidelines and Power Supply Decoupling

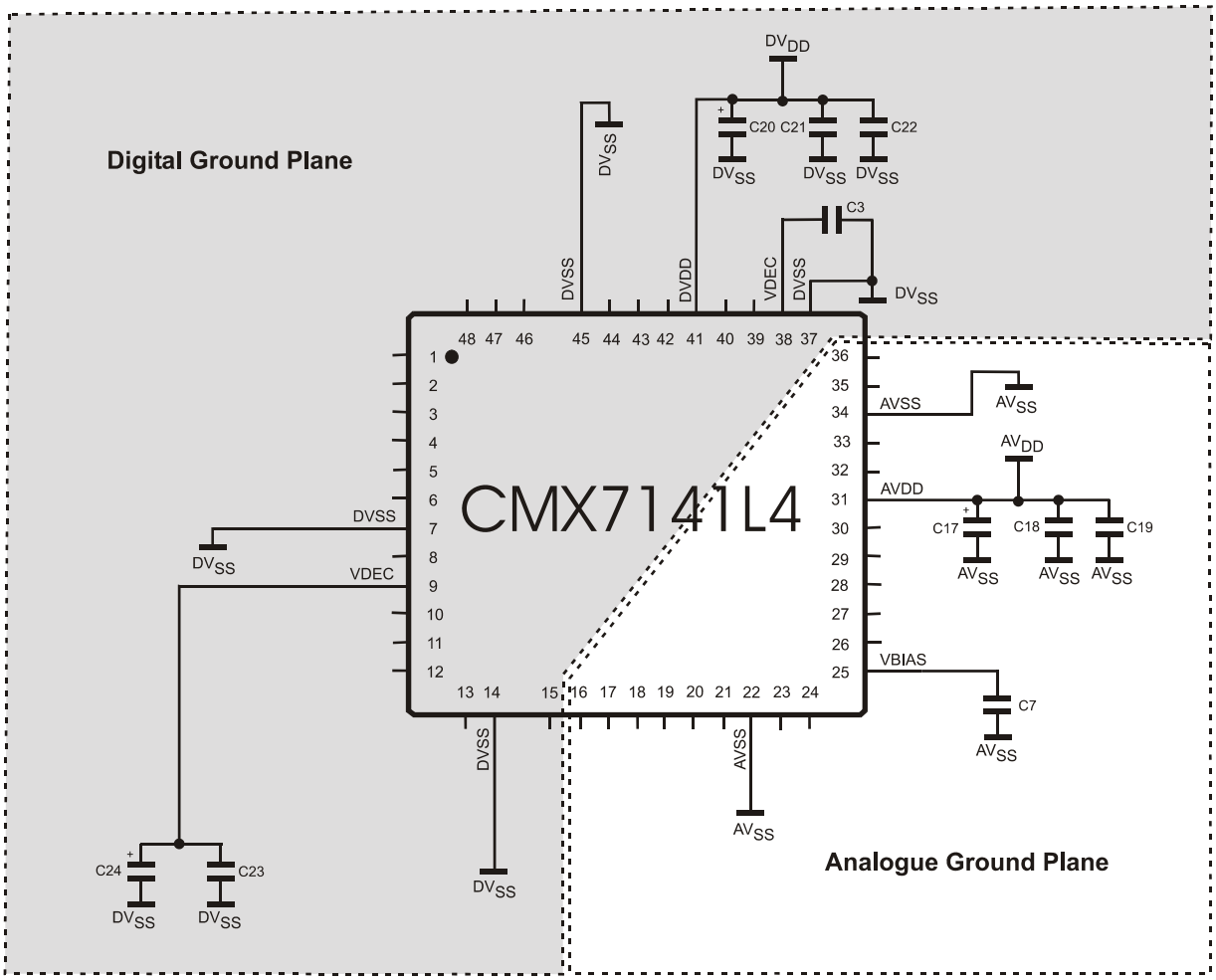


Figure 4 CMX7141 Power Supply and De-coupling

Component Values as per Figure 2

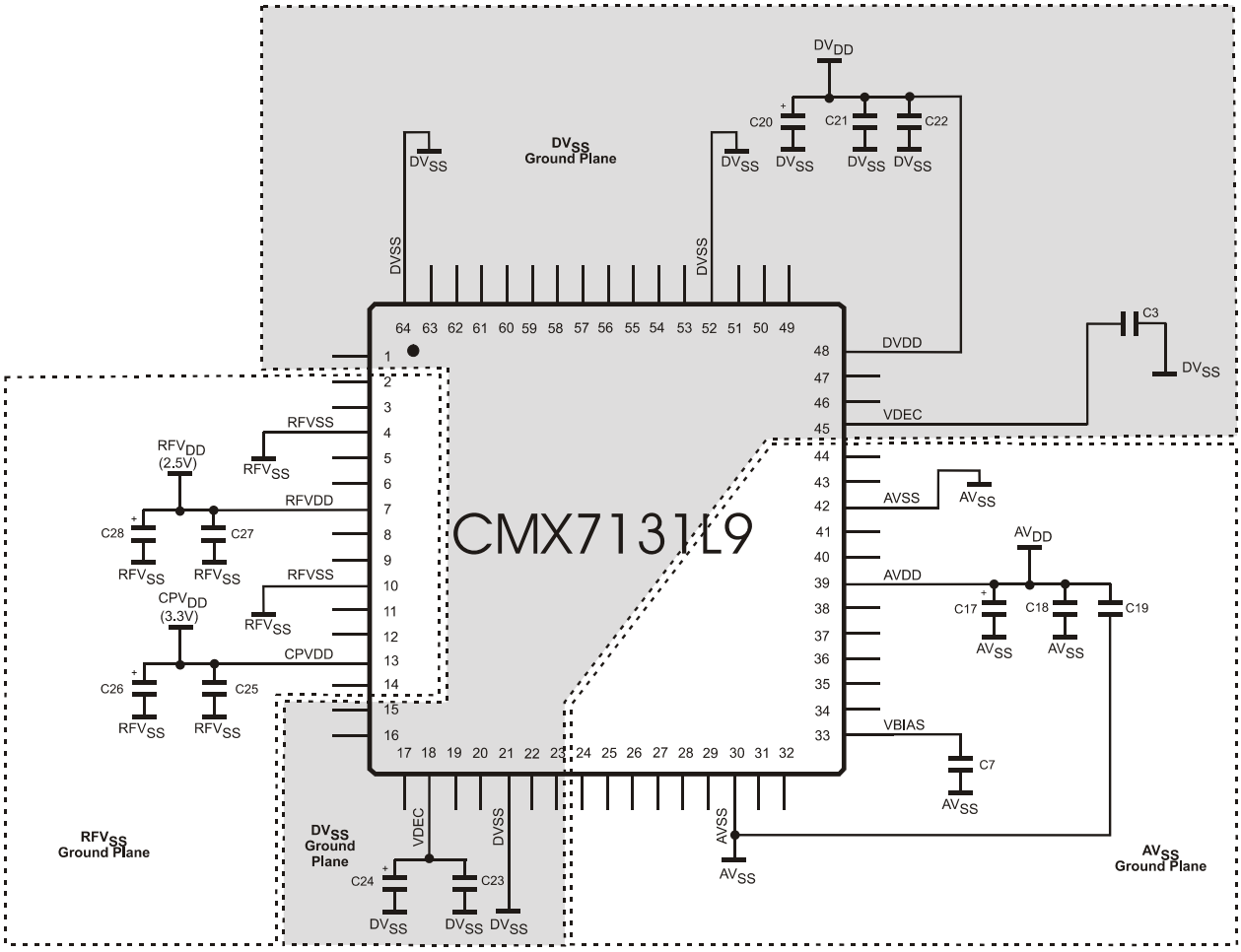


Figure 5 CMX7131 Power Supply and De-coupling

Component Values as per Figure 3

Notes:

It is important to protect the analogue pins from extraneous inband noise and to minimise the impedance between the CMX7131/CMX7141 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22 and C24 should be as close as possible to the CMX7131/CMX7141. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7131/CMX7141, with provision to make links between them, close to the CMX7131/CMX7141. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it should be buffered with a high input impedance buffer.

The single ended microphone input and audio output must be ac coupled (as shown), so that their return paths can be connected to AV_{SS} without introducing dc offsets. Further buffering of the audio output is advised.

The crystal, X1, may be replaced with an external clock source.

6 General Description

6.1 7131/7141 FI-1.x Features

The 7131/7141 FI-1.x Function Image™ is intended for use in half duplex digital PMR equipment using 4FSK modulation at 4800 or 9600 bps suitable for 6.25kHz and 12.5kHz channel systems.

Much of the dPMR ETSI TS 102 490 standard Air Interface protocol is embedded in the 7131/7141FI-1.x Function Image™ operation namely:

Air Interface Physical Layer 1

- 4FSK modulation and demodulation
- Bit and symbol definition
- Frequency and symbol synchronisation
- Transmission burst building and splitting

Air Interface Data Link Layer 2

- Channel coding (FEC, CRC)
- Interleaving, de-interleaving and bit ordering
- Frame and superframe building and synchronising
- Burst and parameter definition
- Link addressing (source and destination)
- Interfacing of voice applications (voice data) with the Physical Layer
- Data bearer services
- Exchanging signalling and/or user data with the Call Control Layer
- Automatic Own-ID and Group-ID detection

A flexible power control facility allows the device to be placed in its optimum powersave mode when not actively processing signals.

The device includes a crystal clock generator, with buffered output, to provide a common system clock if required.

A block diagram of the device is shown in Figure 1.

The signal processing blocks can be routed from any of the three DISC/ALT/MIC input pins.

Other Functions Include:

- Automatic Tx sequencer simplifies host control
- RAMDAC operation
- TXENA and RXENA hardware signals
- Two-point or I/Q modulation outputs
- Hard or Soft data output options

Analogue PMR functionality:

- Complete audio processing
- CTCSS/DCS signalling

Auxiliary Functions:

- Two programmable system clock outputs
- Two auxiliary ADCs with four selectable external input paths

- Four auxiliary DACs, one with built-in programmable RAMDAC
- Two RF PLLs (CMX7131 only)

Interface:

- Optimised C-BUS (4 wire high speed synchronous serial command/data bus) interface to host for control and data transfer
- Open drain IRQ to host
- Auxiliary SPI/C-BUS interface to CMX618/CMX608 with pass-through mode from host
- Two GPIO pins
- EEPROM boot mode
- C-BUS (host) boot mode

6.2 System Design

Figure 6 shows one possible implementation of the CMX7141 combined with a CMX618, a host µController and suitable RF sections to provide a digital PMR radio. The bold lines show the active signal paths in Rx and Tx respectively.

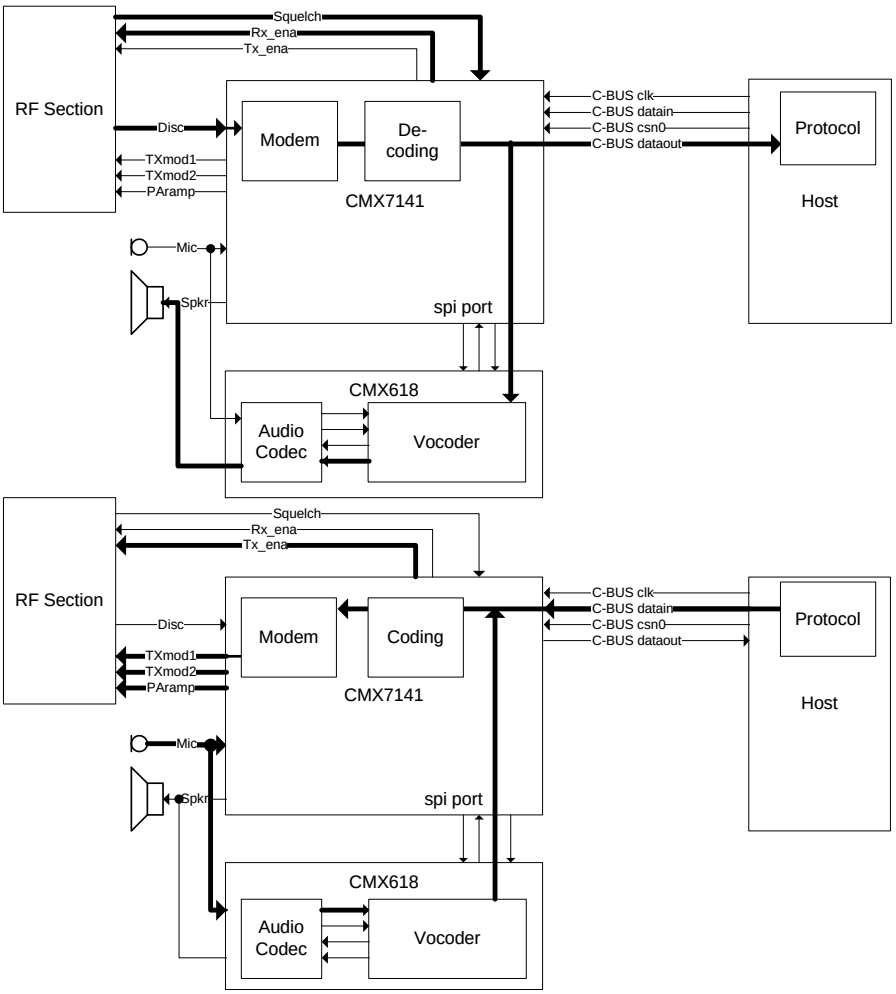


Figure 6 Digital Voice Rx and Tx Blocks

The paralleling of the microphone and speaker connections between the CMX618 and the CMX7131/CMX7141 is only required if the CMX7131/CMX7141 is also to provide analogue PMR functionality (implemented using 7031/7041 FI1.x). Otherwise, the microphone and speaker should be connected to the CMX618 only. The CMX618 RALCWI Vocoder provides an on-chip Audio and Voice Codec, but alternatively a CMX608 device could be used along with an external Audio Codec. Voice payload data is transferred directly from and to the CMX618 by the CMX7131/CMX7141, but if a third-party vocoder is used, all data will need to be transferred over the main C-BUS through the host.

The AuxADC provided by the CMX7131/CMX7141 can be used to detect the Squelch or RSSI signal from the RF section while the device is in Rx or Idle modes. This allows a significant degree of powersaving within the CMX7131/CMX7141 and avoids the need to wake the host up unnecessarily. The host programmable AuxADC thresholds allow for user selection of squelch threshold settings.

When transmitting, an initial block of payload or control channel data will need to be loaded from the host into the C-BUS TxData registers. The CMX7131/CMX7141 can then format and transmit that data while at the same time loading in the following data blocks from the host or CMX618.

When receiving, the host needs to understand that when a signal is received over the air there will be a processing delay while the CMX7131/CMX7141 filters, demodulates and decodes the output data before presenting it to the host or CMX618. For best performance voice payload data can be output in soft-decision (4-bit log-likelihood ratio) format compatible with the CMX618/CMX608 and other third-party vocoders, although this mode increases the data transfer rate over C-BUS by a factor of four.

6.3 Introduction

This modem can run at either 4800bps or 9600bps, occupying a 6.25kHz or a 12.5kHz bandwidth RF channel respectively. It has been designed such that, when combined with suitable RF, host controller, CMX618/CMX608 Vocoder and appropriate control software, it meets the requirements of the EN 301 166 or EN 300 113 standards as appropriate. See www.etsi.org for details of these standards.

TS 102 490 is available on the ETSI web site (www.etsi.org) which describes a 6.25kHz channel spacing FDMA dPMR system. This standard uses a 4FSK modulation scheme with an over-air bit rate of 4800bps (ie. 2400 symbols per second). With respect to dPMR formatted modes of operation, this document should be read in conjunction with the ETSI standard.

The dPMR standard does not specify a voice coding algorithm, but the CMX618 or CMX608 (also available from CML) are both suitable devices for this purpose. In the rest of this document these two devices are referred to generically as the CMX6x8, as the only significant difference between them is the inclusion of an on-chip audio codec in the CMX618 while the CMX608 requires an external Audio Codec.

Note that the TS 102 490 (dPMR) standard is NOT compatible with the TS 102 362 (DMR) 12.5kHz/9600baud TDMA system.

The 9600bps option is made available for customer-specific applications only – this mode does not support automated control of the CMX6x8 – in which case all data should be routed via the host.

6.3.1 Modulation

The dPMR 4FSK modulation scheme operates in a 6.25kHz channel bandwidth with a deviation index of 0.29 and has an over-air bit rate of 4800bps (2400 symbols per second). RRC filters are implemented in both Tx and Rx with a filter “alpha” of 0.2. The maximum frequency error is +/-625Hz and the CMX7131/CMX7141 can adapt to the maximum time-base clock drift of 2ppm over the duration of a 180-second burst. Figure 9 shows the basic parameters of the 4FSK modulation, symbol mapping and filtering requirements.

The 9600bps mode provided by the CMX7131/CMX7141 is essentially the same as the 4800bps mode, but with all timings modified by a factor of two.

Figure 7 and Figure 8 show a transmitted PRBS waveform, as recorded on a spectrum analyser in 36k span and zero-span mode, having been 2-point modulated using a suitable RF transmitter.

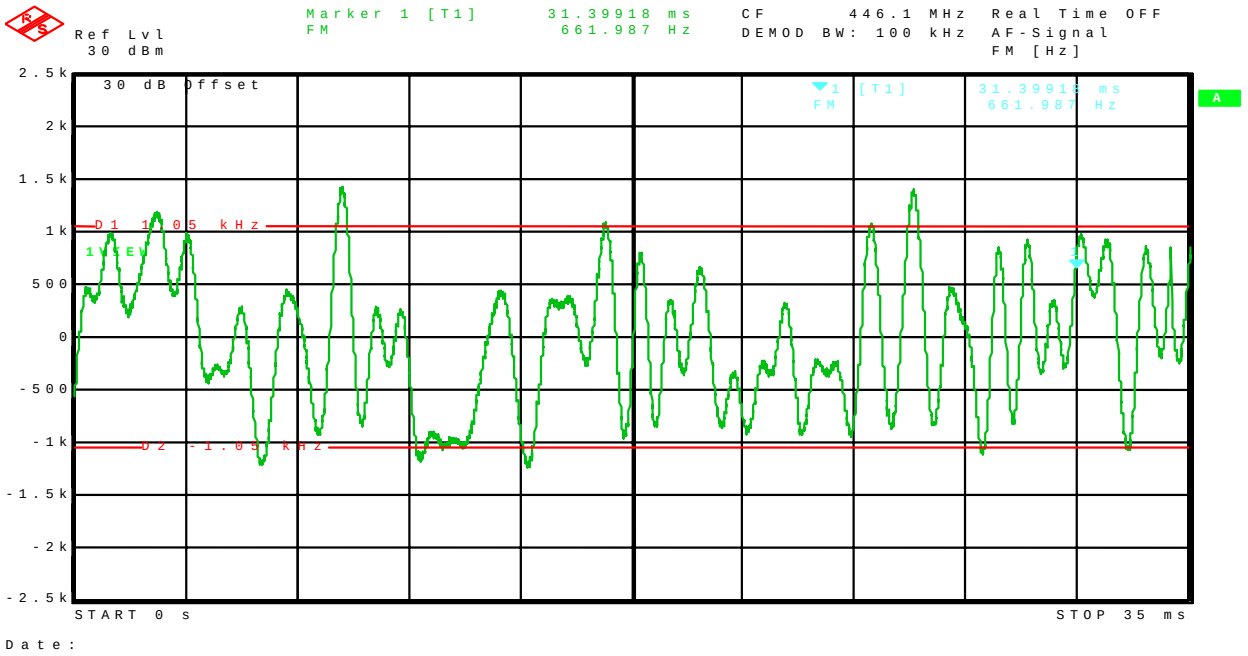


Figure 7 4FSK PRBS Waveform - Modulation

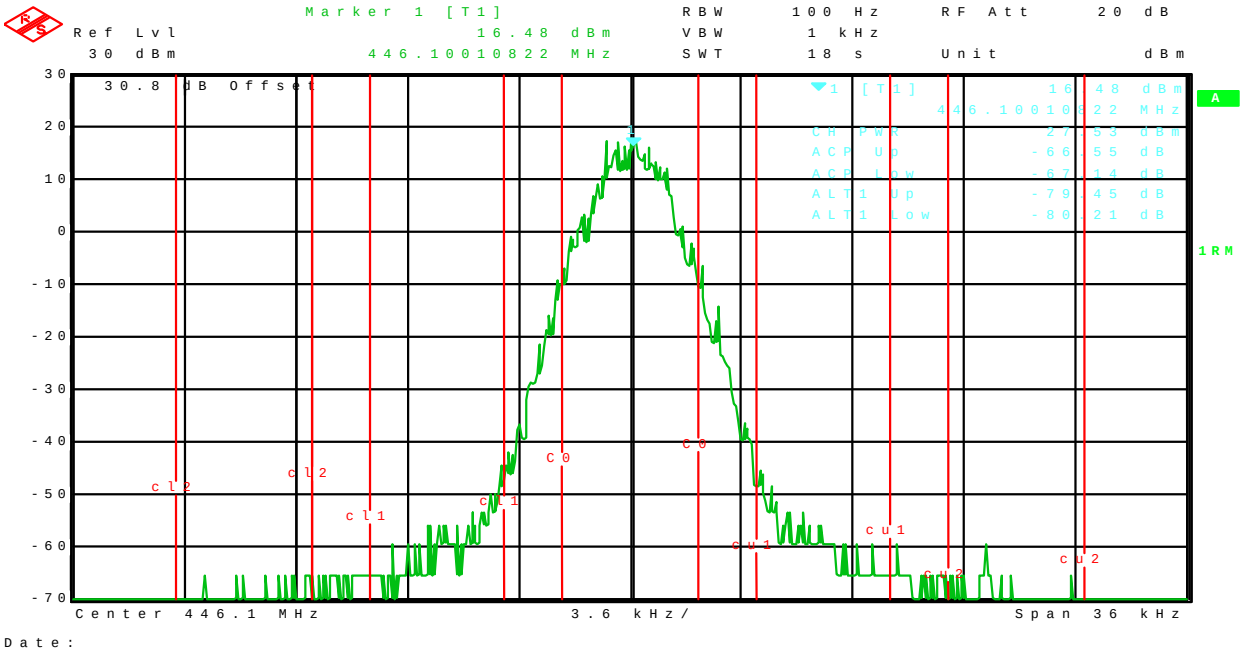
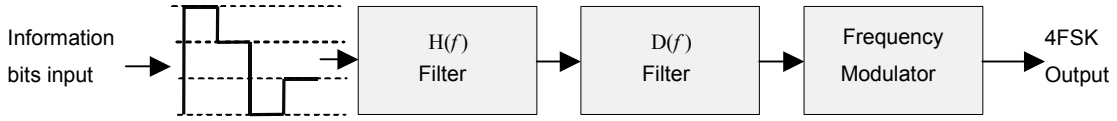


Figure 8 4FSK PRBS Waveform - Spectrum

Tx Baseband Filter



$$|H(f)| = \begin{cases} 1 & , \quad 0 = |f| < (1-\alpha)/2T \\ \cos[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T] & , \quad (1-\alpha)/ = |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/ = |f| \end{cases}$$

$\alpha = 0.2 \quad T = 1/2400$

$$|D(f)| = \frac{\sin(\pi f T)}{\pi f T}$$

4 FSK Deviation		
Di-bit	Symbol	Deviation
01_2	+3	+1 050Hz
00_2	+1	+350Hz
10_2	-1	-350Hz
11_2	-3	-1050Hz

Rx Baseband Filter

$$|H(f)| = \begin{cases} 1 & , \quad 0 = |f| < (1-\alpha)/2T \\ \cos[(T/4\alpha)(2\pi|f| - \pi(1-\alpha)/T] & , \quad (1-\alpha)/ = |f| < (1+\alpha)/2T \\ 0 & , \quad (1+\alpha)/ = |f| \end{cases}$$

$\alpha = 0.2 \quad T = 1/2400$

$$|D(f)| = \frac{\pi f T}{\sin(\pi f T)}$$

Figure 9 dPMR Modulation Characteristics

6.3.2 Internal Data Processing

The CMX7131/CMX7141 operates as a half-duplex device, either receiving signals from the RF circuits in Rx mode, or sourcing signals to the RF circuits in Tx mode. It also has a low power Idle mode to support battery saving protocols. The internal data processing blocks for Tx and Rx modes are illustrated in Figure 10.

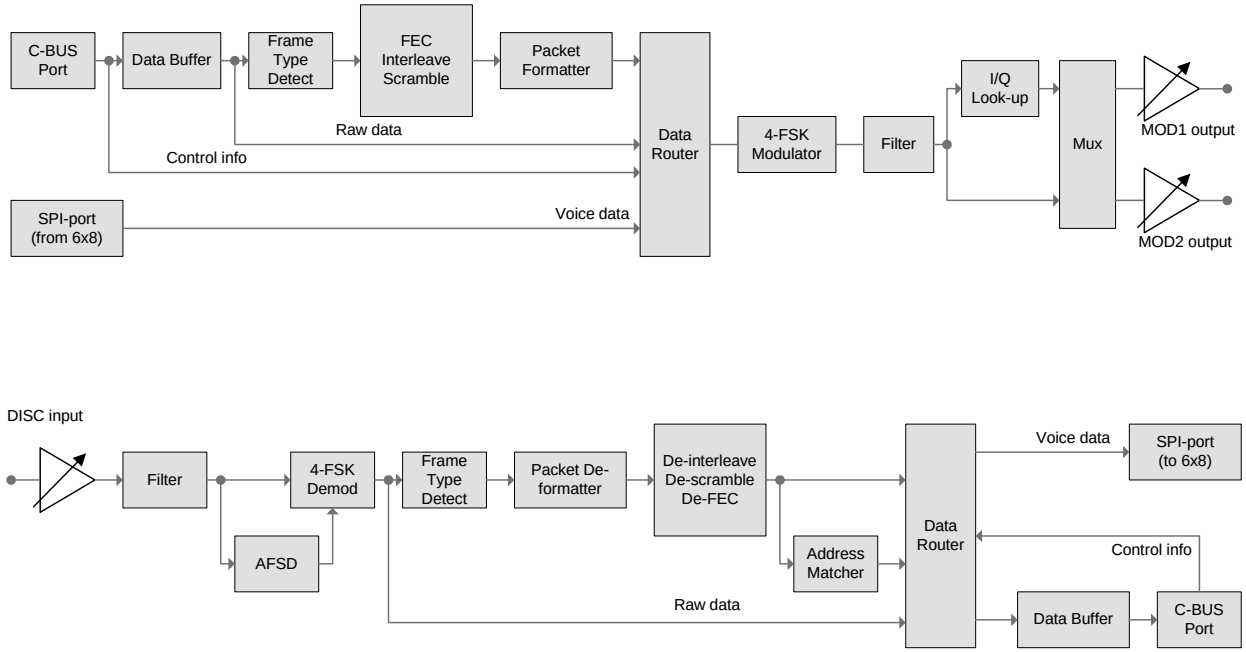


Figure 10 Internal Data Processing Blocks

6.3.3 Frame Sync Detection and Demodulation

The analogue signal from the limiter/discriminator of the external RF section should be applied to one of the CMX7131/CMX7141 inputs (normally the DISC input) where it can be adjusted to the correct level either by selection of the feedback resistor or using the CMX7131/CMX7141 Input Gain settings. The signal is filtered using a Root-Raised Cosine filter and Inverse Rx Sinc filter matching the filters applied in the transmitter, then passed to the AFSD (Automated Frame Sync Detector) block which extracts symbol and frame synchronisation. During this process the 4FSK demodulator and the following data-processing sections are dormant to minimise power consumption. When frame synchronisation has been achieved the AFSD section is powered down, and timing and symbol-level information is passed to the 4FSK demodulator which starts decoding the subsequent data bits. In Raw mode the demodulator will continue operating until the host switches it off, but in dPMR Formatted mode the CMX7131/CMX7141 can detect the end of a call by scanning the received control channel fields and will automatically disable the demodulator and restart frame sync search when required without host intervention.

A dPMR call begins with a 72-bit or longer preamble sequence followed by an 80ms Header Frame, which contains a 48-bit frame sync (FS1 or FS4). Subsequent payload frames contain either a 24-bit frame sync (FS2) or a 24-bit Colour Code. The CMX7131/CMX7141 can scan for all dPMR frame syncs concurrently. It uses FS1 to detect the start of a transmission, and this is reported to the host by setting the FS1 Detect bit in the IRQ Status register. It can also optionally use FS2 to perform “late entry” into an existing call, reported by setting the FS2 Detect bit. The short length of FS2 gives a high probability of false detections, so by default the CMX7131/CMX7141 will only generate an FS2 Detect if two successive FS2 frame syncs are detected at the correct frame spacing in the received signal.

In Raw mode operation, 24-bit frame sync detection is disabled but both the preamble and the 48-bit frame sync sequences are user-programmable (see User Manual sections 10.2.1). In dPMR Formatted mode, the frame syncs and Preamble defined in TS 102 490 are always used regardless of the programmed Raw mode frame syncs. In both cases, when frame synchronisation has been achieved and the 4FSK demodulator is enabled, frame sync detection is switched off and any subsequent frame sync sequences embedded in the received data are not reported to the host.

Table 2 dPMR Frame Format - Call set-up, no ACK

bit no.		24	48	72	96	120	144	168	192	216	240	264	288	312	336	360	384
		press PTT															
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
	Tx	repeat frames 1 to 4 until PTT released….															
End	Tx	FS3	End Flag														

Table 3 dPMR Frame Format - Call set-up with ACK

bit no.		24	48	72	96	120	144	168	192	216	240	264	288	312	336	360	384
		press PTT															
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
End	Tx	FS3	End Flag														
Ack	Rx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Header	Tx	Preamble			FS1		Header Info 0					CC	Header Info 1				
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 1	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 2	Tx	CC	CCH			Payload			Payload			Payload			Payload		
Frame 3	Tx	FS2	CCH			Payload			Payload			Payload			Payload		
Frame 4	Tx	CC	CCH			Payload			Payload			Payload			Payload		
	Tx	repeat frames 1 to 4 until PTT released….															
End	Tx	FS3	End Flag														

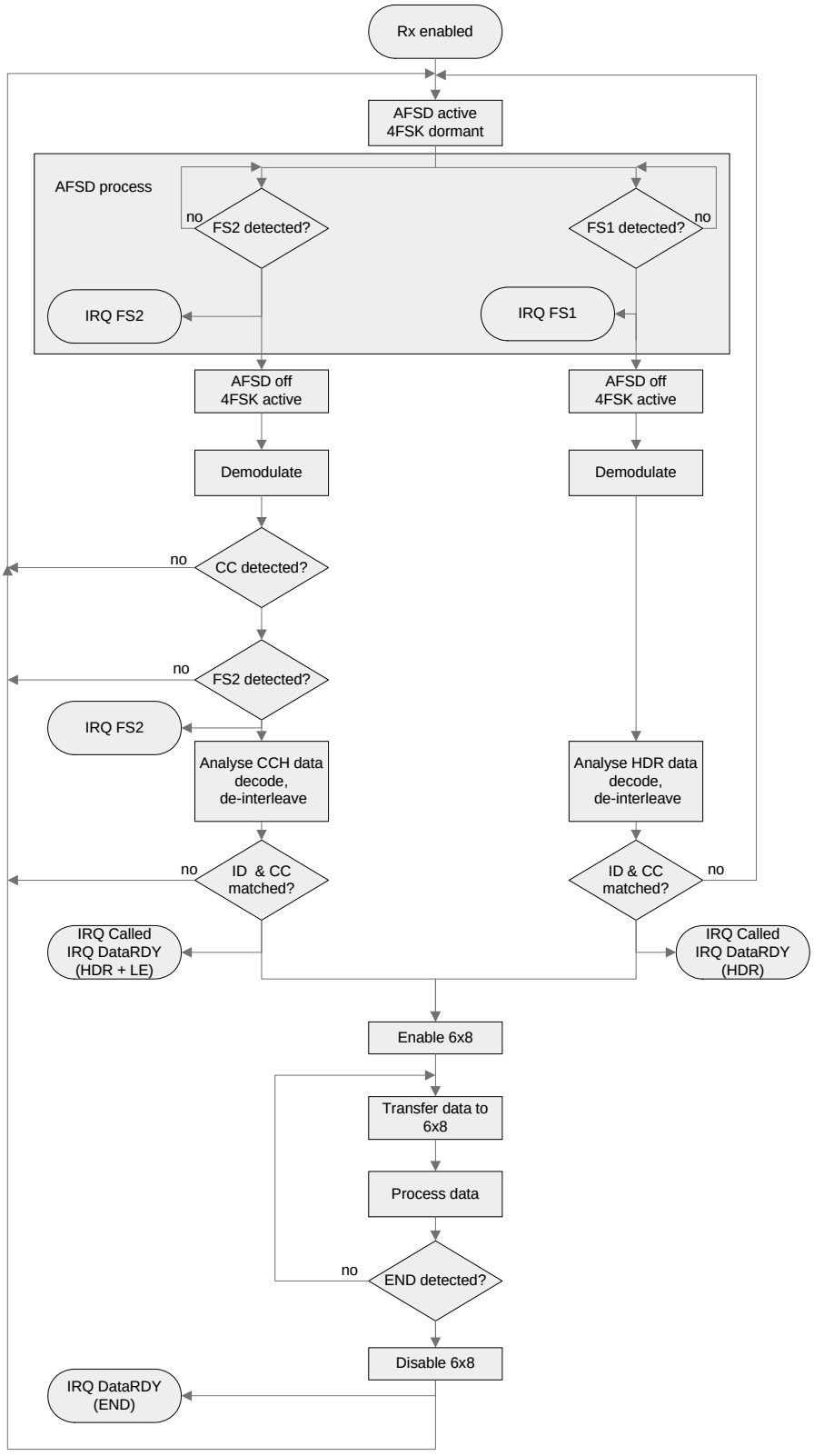


Figure 11 FS Detection

6.3.4 FEC and Coding

In Raw mode the CMX7131/CMX7141 does not implement any FEC processing.

In dPMR Formatted mode the CMX7131/CMX7141 implements all CRCs, Hamming codes, interleaving and scrambling required by the dPMR standard. CRC failures in control channel fields and coded data blocks are indicated to the host by issuing an "Event" IRQ with a corresponding error code in the Modem Status register, $C9. This relieves the host of a substantial processing load and has the added advantage of reducing the complexity and timing constraints of interfacing between the host, vocoder and CMX7131/CMX7141.

The dPMR Header Frame format contains duplicate copies of all control channel fields (in the HI0 and HI1 Header Information blocks) but only one decoded copy of each field will be presented back to the host. On receiving a Header Frame the CMX7131/CMX7141 decodes both HI blocks, checks CRCs and can accept the call if either block is valid (the other HI block is discarded).

6.3.5 Voice Coding

A CML CMX618 or CMX608 RALCWI vocoder can be used under the control of the CMX7131/CMX7141. The CMX7131/CMX7141 provides an auxiliary SPI/C-BUS port (shared with the boot EEPROM) which is used to issue control commands and transfer voice payload data directly to the CMX6x8 vocoder, minimising the loading on the host controller during voice calls.

Alternatively, the CMX7131/CMX7141 can support any third-party vocoder by routing voice payload data over the main C-BUS interface and through the host. In this mode, all vocoder control and data transfers must be managed by the host.

Voice data transferred to the CMX6x8 in Rx mode always uses soft decision (4-bit log-likelihood ratio) format. This option is also available for voice payload data routed to the host, although it increases the required data transfer rate over C-BUS by a factor of four.

6.3.6 Radio Performance Requirements

The CMX7131/CMX7141 demodulator is designed to process a 4FSK signal from a limiter/discriminator source. For optimum performance the signal should not be significantly degraded by filters that are excessively narrow and/or cause significant group delay distortion. Care should be taken in interfacing the device to the radio circuits to maintain the frequency and phase response (both low and high end), in order to achieve optimum performance. Test modes are provided to assist in both the initial design and production set-up procedures.

Further information and application notes can be found at http://www.cmlmicro.com .

7 Detailed Descriptions

7.1 Xtal Frequency

The CMX7131/CMX7141 is designed to work with an external frequency source of 19.2MHz. If this default configuration is not used, then Program Register Block 3 must be loaded with the correct values to ensure that the device will work to specification with the user selected clock frequency. A table of common values can be found in Table 4. Note the maximum Xtal frequency is 12.288MHz, although an external clock source of up to 24MHz can be used.

The register values in Table 1 are shown in hex, the default settings are shown in bold, and the settings which do not give an exact setting (but are within acceptable limits) are in italics. The new P3.2-3 settings take effect following the write to P3.3 (the settings in P3.4-7 are implemented on a change to Rx or Tx mode).

Table 4 Xtal/Clock Frequency Settings for Program Block 3

Program Register			External Frequency Source (MHz)							
			3.579	6.144	9.216	12.0	12.8	16.368	16.8	**19.2**
P3.2	Idle	GP timer	*$017*	$018	$018	$019	$019	*$018*	$019	**$018**
P3.3		VCO output and AUX clk divide	*$085*	$088	$08C	*$10F*	*$110*	*$095*	*$115*	**$099**
P3.4	Rx or Tx	Ref clk divide	*$043*	$040	$060	$07D	$0C8	$155	$15E	**$0C8**
P3.5		PLL clk divide	*$398*	$200	$200	$200	$300	$400	$400	**$200**
P3.6		VCO output and AUX clk divide	*$140*	$140	$140	$140	$140	$140	$140	**$140**
P3.7		Internal ADC/DAC clk divide	*$008*	$008	$008	$008	$008	$008	$008	**$008**

7.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7131/CMX7141 and the host µC; this interface is compatible with microwire and SPI. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set. See section 7.5.2.

The CMX7131/CMX7141 will monitor the state of the C-BUS registers that the host has written-to every 250µs (the C-BUS latency period) hence it is not advisable for the host to make successive writes to the same C-BUS register within this period.

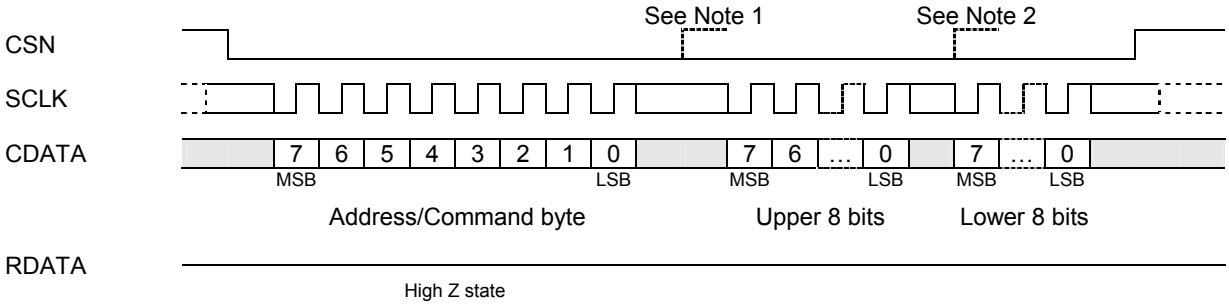
7.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7131/CMX7141's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single address byte sent from the µC which may be followed by one or more data byte(s) sent from the µC to be written into one of the CMX7131/CMX7141's Write Only Registers, or one or more data byte(s) read out from one of the CMX7131/CMX7141's Read Only Registers, as shown in Figure 12.

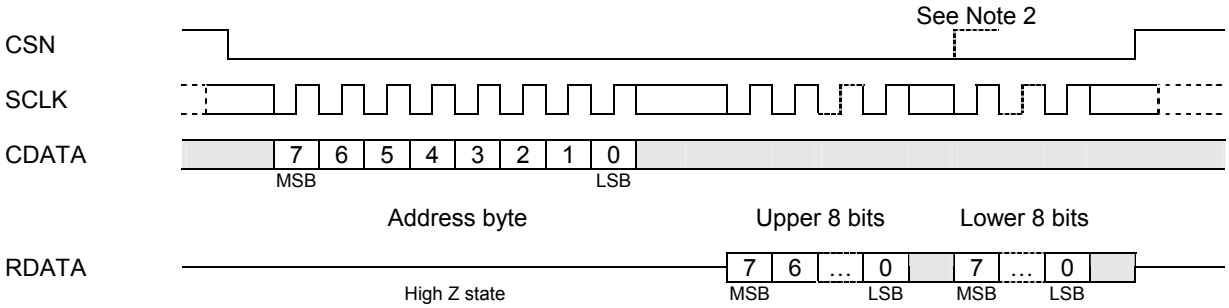
Data sent from the µC on the CDATA (Command Data) line is clocked into the CMX7131/CMX7141 on the rising edge of the SCLK (Serial Clock) input. RDATA (Reply Data) sent from the CMX7131/CMX7141 to the µC is valid when the SCLK is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine.

The number of data bytes following an address byte is dependent on the value of the Address byte. The most significant bit of the address or data is sent first. For detailed timings see section 8.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:



Data value unimportant

Repeated cycles

Either logic level valid (and may change)

Either logic level valid (but must not change from low to high)

Figure 12 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CDATA and RDATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The SCLK input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CDATA and RDATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

7.3 Function Image™ Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external EEPROM or Flash memory. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7131/CMX7141 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low current pull-down devices.

For C-BUS load operation, both pins should be pulled high by connecting them to DV_{DD} either directly or via a 47k resistor (see Figure 13).

For Flash/EEPROM load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the EEPROM or Flash memory in-situ from the host, either a jumper to DV_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Figure 14).

Once the FI has been loaded, the CMX7131/CMX7141 performs these actions:-

(1) The product identification code ($7141 or $7131) is reported in C-BUS register $C5
(2) The FI version code is reported in C-BUS register $C9
(3) The two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) The device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) Once activated, the device initialises fully, enters idle mode and becomes ready for use.

The checksums can be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and must be power cycled before an attempt is made to re-load the FI and re-activate.

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 5 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
Flash/EEPROM load	0	1
No FI load	0	0

Note: In the rare event that a General Reset needs to be issued without the requirement to re-load the FI, the BOOTEN pins must both be cleared to '0' before the command is issued. The Checksum values will be reported and the Device Activation code will need to be sent in a similar manner as that shown in Figure 14. There will not be any FI loading delay. This assumes that a valid FI has been previously loaded and that V_{DD} has been maintained throughout the reset to preserve the data.

7.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7131/CMX7141 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7131/CMX7141 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX7131/CMX7141.

If the host detects a brownout, the BOOTEN state should be set to re-load the FI. A General Reset should then be issued and the appropriate FI load procedure followed.
Each time the Programming register, $C8, is written, it is necessary to wait for the PRG flag (IRQ Status register ($C6) b0) to go high before another write to $C8. The PRG flag going high confirms the write to

the Programming register has been accepted. The PRG flag state can be determined by polling the IRQ Status register or by unmasking the interrupt (Interrupt Mask register, $CE, b0).

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

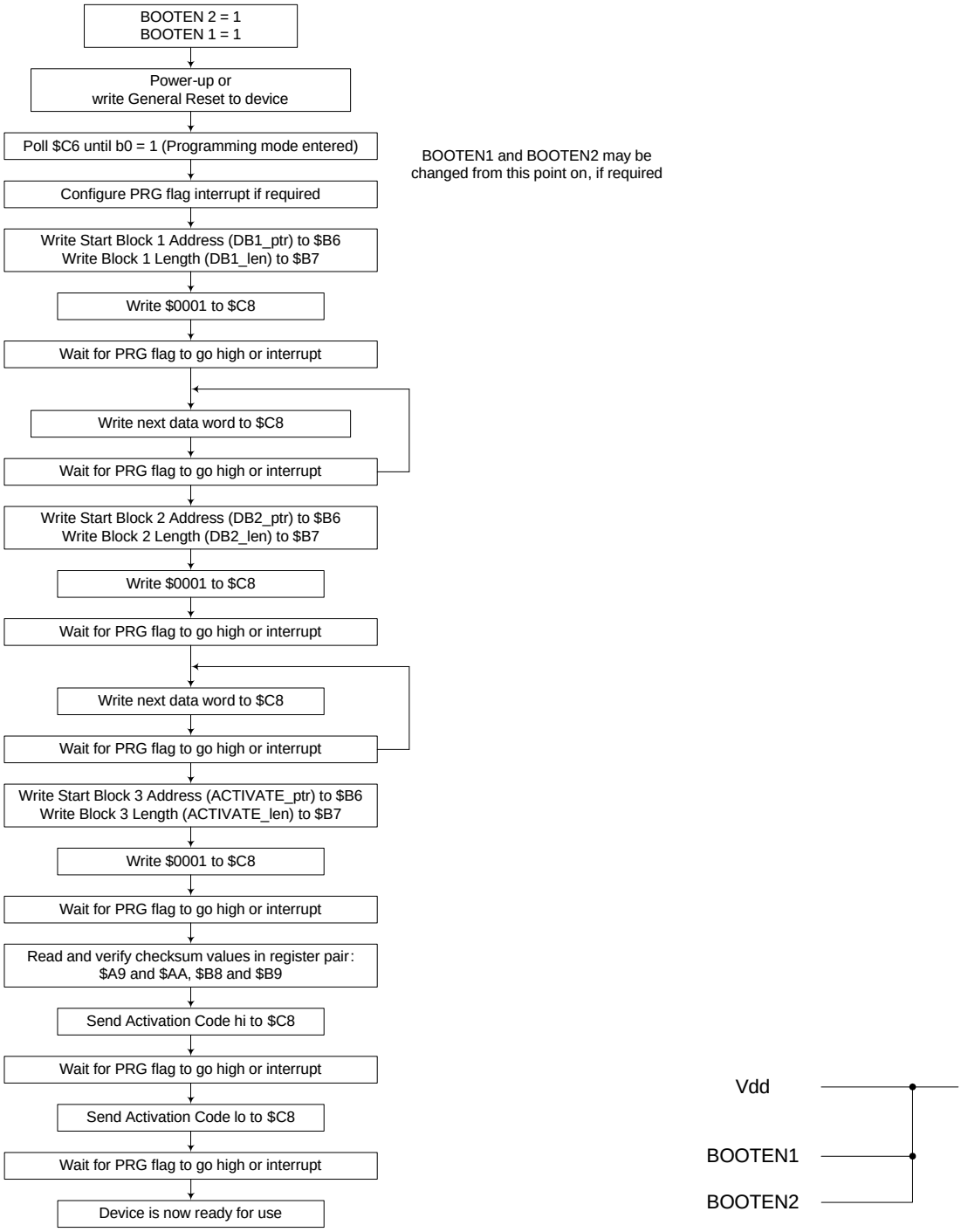


Figure 13 FI Loading from Host

7.3.2 FI Loading from Flash/EEPROM

The FI must be converted into a format for the Flash/EEPROM programmer (normally Intel Hex) and loaded into the EEPROM or Flash memory either by the host or an external programmer. The CMX7131/CMX7141 needs to have the BOOTEN pins set to Flash/EEPROM load, and then on power-on, or following a C-BUS General Reset, the CMX7131/CMX7141 will automatically load the data from the EEPROM or Flash memory without intervention from the host controller.

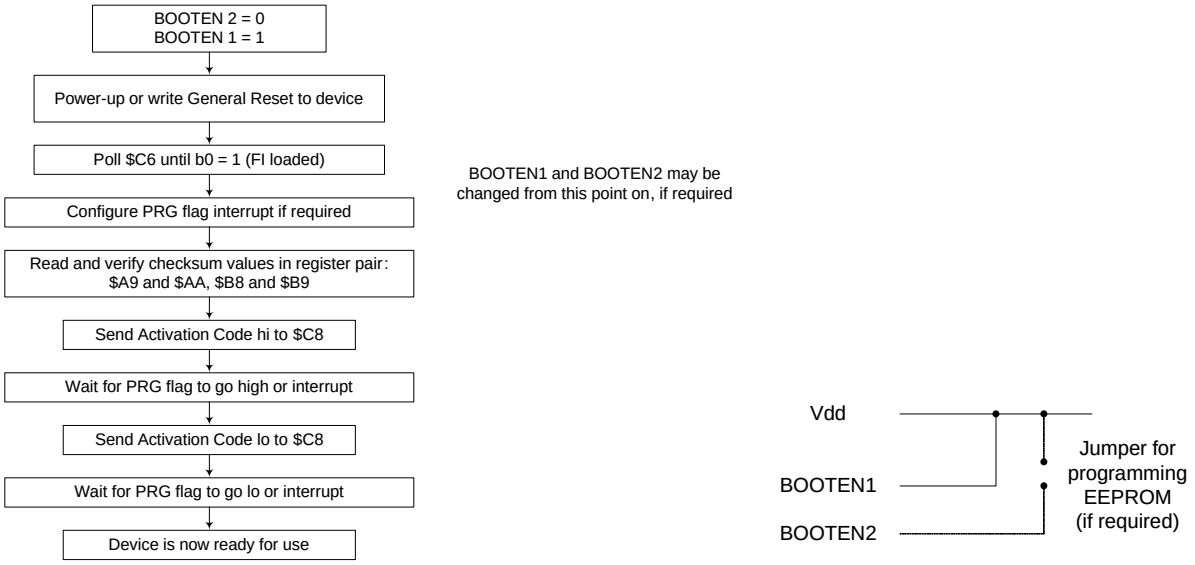


Figure 14 FI Loading from EEPROM

The CMX7131/CMX7141 has been designed to function with Atmel AT25HP512 serial EEPROM and the AT25F512 Flash EEPROM devices[3], however other manufacturers parts may also be suitable. The time taken to load the FI is dependant on the Xtal frequency, with a 19.2MHz Xtal, it should load in less than 1 second.

[3] Note that these two devices have slightly different addressing schemes. CMX7131/CMX7141 is compatible with both schemes, whereas previous FI 's were only compatible with the AT25HP512 addressing scheme.

7.4 CMX618/CMX608 Interface

An auxiliary SPI/C-BUS interface is provided which allows the CMX6x8 to be directly controlled by the CMX7131/CMX7141 without the need for the host to intervene. This is accomplished by re-using the EEPROM SPI interface with an additional Chip Select pin (SSOUT). The EEPROM Data Out pin MUST NOT drive the signal line when the chip is not enabled, otherwise the CMX6x8 will not be able to return its data to the CMX7131/CMX7141. The CMX7131/CMX7141 SPI serial bus should be connected to the C-BUS interface on the CMX6x8 using the SSOUT pin as the CSN signal for the CMX6x8.

The initialisation and operational settings of the CMX6x8 should be programmed by the host into the CMX7131/CMX7141 Program Block 1 on power-up. These values will be written to the defined registers in the CMX6x8 at:

- Initialisation
- Idle mode
- Rx mode
- Tx mode

Mic Gain and Speaker Gain commands may be sent to the CMX6x8 whenever the CMX7131/CMX7141 is in Rx or Tx mode.

The DTX and VAD modes of the CMX6x8 are not supported in FI-1. DTMF Mode 1 (transparent) is supported.
The default settings for the CMX6x8 are:

- 4 frame packet (80ms) with FEC no STD, no DTMF
- 2400bps with FEC
- Internal Sync
- Throttle = 1
- Internal Codec
- IRQ disabled
- Soft Coded data bits

7.5 Device Control

The CMX7131/CMX7141 can be set into the relevant mode to suit its environment. These modes are described in the following sections and are programmed over the C-BUS: either directly to operational registers or, for parameters that are not likely to change during operation, via the Programming register ($C8).

For basic operation:

(1) Enable the relevant hardware sections via the Power Down Control register

(2) Set the appropriate mode registers to the desired state

(3) Select the required Signal Routing and Gain

(4) Use the Mode Control register to place the device into Rx or Tx mode

To conserve power when the device is not actively processing a signal, place the device into Idle mode. This will also command the CMX6x8 to enter powersaving mode as well. Additional powersaving can be achieved by disabling any unused hardware blocks, however, care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the Input or Output blocks to function.

See:

- Power Down Control - $C0 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write

7.5.1 General Notes

In normal operation, the most significant registers, in addition to the TxData and RxData blocks, are:

- Modem Control - $C1 write
- IRQ Status - $C6 read
- Analogue Output Gain - $B0 write
- Input Gain and Signal Routing - $B1 write
- AuxData Write - $C2 write
- CMX6x8 Analogue Gain- $C3 write

Setting the Mode register to either Rx or Tx will automatically increase the internal clock speed to its operational speed and bring the CMX6x8 out of its powersave mode, whilst setting the Mode register to Idle will automatically return the internal clock to a lower (powersaving) speed. To access the Program Blocks (through the Programming register, $C8) the device MUST be in Idle mode.

Under normal circumstances the CMX7131/CMX7141 manages the Main Clock Control automatically, using the default values loaded in Program Block 3.

7.5.2 Interrupt Operation

The CMX7131/CMX7141 will issue an interrupt on the IRQN line when the IRQ bit (bit 15) of the IRQ Status register and the IRQ Mask bit (bit 15) are both set to 1. The IRQ bit is set when the state of the interrupt flag bits in the IRQ Status register change from a 0 to 1 and the corresponding mask bit(s) in the Interrupt Mask register is(are) set. Enabling an interrupt by setting a mask bit (0→1) after the corresponding IRQ Status register bit has already been set to 1 will also cause the IRQ bit to be set.

All interrupt flag bits in the IRQ Status register, except the Programming Flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the IRQ Status register. The Programming Flag bit is set to 1 only when it is permissible to write a new word to the Programming register.

See:

- IRQ Status - $C6 read
- Interrupt Mask - $CE write

7.5.3 Signal Routing

The CMX7131/CMX7141 offers a flexible routing architecture, with three signal inputs, a choice of two modulator configurations (to suit 2-point modulation or I/Q schemes) and a single audio output.

See:

- Input Gain and Signal Routing - $B1 write
- Modem Control - $C1 write
- Modem Configuration - $C7 write

The analogue gain/attenuation of each input and output can be set individually, with additional Fine Attenuation control available via the Programming registers in the CMX7131/CMX7141. The Mic. and Speaker gains are set by the CMX6x8, which is controlled through the CMX6x8 Analogue Gain- $C3 write of the CMX7131/CMX7141.

See:

- Analogue Output Gain - $B0 write (Tx MOD1 and 2)
- Input Gain and Signal Routing - $B1 write (Rx DISC input, Tx MOD1 and 2)
- CMX6x8 Analogue Gain- $C3 write (CMX6x8 Mic. and Speaker)

In common with other FIs developed for the CMX7131/CMX7141, this device is equipped with two signal processing paths. However, in this implementation of the FI, Input 2 is not currently used and so should not be enabled. Input 1 should be routed to either of the three input sources (ALT, DISC or MIC) which should be connected to the radio's discriminator output. The internal signals Output 1 and Output 2 are

used to provide either 2-point or I/Q signals and should be routed to the MOD1 and MOD2 pins as required.

In dPMR Formatted modes the microphone and speaker paths are automatically re-routed to the CMX6x8 Vocoder when appropriate. This routing is controlled by the data field in the Header Block which indicates whether the payload data is Voice or Data and the enable bit in the Modem Control register, $C1.

7.5.4 Modem Control

The CMX7131/CMX7141 operates in one of these operational modes:

- Idle
- Rx
- Tx
- CMX6x8 pass-through

At power-on or following a Reset, the device will automatically enter Idle mode, which allows maximum powersaving whilst still retaining the capability of monitoring the AuxADC inputs (if enabled). It is only possible to write to the Programming register whilst in Idle mode.
See:

- Modem Control - $C1 write

GPIO1 and GPIO2 pins (RXENA and TXENA) reflect bits 0 and 1 of the Modem Control register, as shown in Table 6. These can be used to drive external hardware without the host having to intervene. There are also two additional GPIO pins that are programmable under host control.

Table 6 Modem Mode Selection

Modem Control ($C1) b0-3	Modem Mode	GPIO2 - TXENA	GPIO1 - RXENA
0000	Idle – Low Power Mode	1	1
0001	Rx	1	0
0010	Tx	0	1
0011	*reserved*	x	x
0100	CMX6x8 Pass-through	1	1
0101	*reserved*	x	x
0110	*reserved*	x	x
0111	*reserved*	x	x
1xxx	*reserved*	x	x

The CMX6x8 pass-through mode is used to control and monitor the CMX6x8 directly. This cannot be accessed if the CMX7131/CMX7141 is in Rx or Tx modes. This mode will transfer data to/from the TxData0/RxData0 register to the CMX6x8 C-BUS register address specified in the Programming register ($C8). See section 7.5.10. The Modem Control bits are ignored in this mode.

Table 7 Modem Control Selection

4FSK Modem Control ($C1) b7-4	Rx	Tx
0000	Rx Idle	Tx Idle
0001	Rx 4FSK Formatted	Tx 4FSK Formatted
0010	Rx 4FSK Raw	Tx 4FSK Raw
0011	Rx 4FSK EYE	Tx 4FSK PRBS
0100	*reserved*	Tx 4FSK Preamble
0101	*reserved*	Tx 4FSK Mod Set-up
0110	Sync	Test
0111	Reset/Abort	Reset/Abort
1xxx	*reserved*	*reserved*

The Modem Mode bits and the Modem Control bits should be set together in the same C-BUS write.

In Tx mode, the CMX7131/CMX7141 can operate as a Raw mode data pump or in dPMR Formatted mode. In both cases the first block of control channel or payload data should be loaded into the C-BUS TxData registers before executing the mode change. A "DataReady" IRQ will be issued when the registers have been read by the CMX7131/CMX7141 and the host can then supply further blocks of payload data. When all payload has been transmitted the CMX7131/CMX7141 will issue a "TxDone" IRQ and the host can then reset the Mode bits to either Rx or Idle as required.

In Rx mode the received signal should be routed through Input1 (DISC). In Raw and dPMR Formatted modes the CMX7131/CMX7141 will first search for frame synchronisation, and when this has been achieved the following data is demodulated and supplied to the host through the RxData registers. A "DataReady" IRQ indicates when each new block becomes available. In Raw mode the CMX7131/CMX7141 will continue demodulating the input signal until the host resets the Mode bits to Tx or Idle, but in dPMR Formatted mode the modem can detect the end of a call and restart frame sync search automatically.

7.5.5 Tx Mode (Raw)

In Raw mode Tx operation ($C1, Modem Control = $0022), the preamble and frame sync are transmitted automatically (default values for Raw mode may be changed by use of the Program registers) and data from the TxData Block is then transmitted directly until the mode is changed to Rx, Pass-through or Idle. The first block of data should be loaded into the TxData registers before executing the Modem Mode change to Tx. Data is transmitted msb (most significant bit) first.

The host should write the initial data to the C-BUS TxData registers and then set the Modem Mode to TxRaw and the Mode bits to Tx. As soon as the data block has been read from the C-BUS TxData registers, the DataRDY IRQ will be asserted and the next block of data may be loaded.

When the host stops loading data into the device a Data Underflow condition will eventually occur. After the last data bit has left the modulator a "TxDone" IRQ will be issued. At this point it is now safe for the host to change the Modem Control and Modem Mode to Idle ($C1, Modem Control = $0000) and turn the RF transmitter off.

7.5.6 Tx Mode (PRBS)

In PRBS mode Tx operation ($C1, Modem Control = $0023) the preamble and frame sync are transmitted automatically followed by a PRBS pattern conforming to ITU-T O.153 (para 2.1) giving a 511-bit repeating sequence.

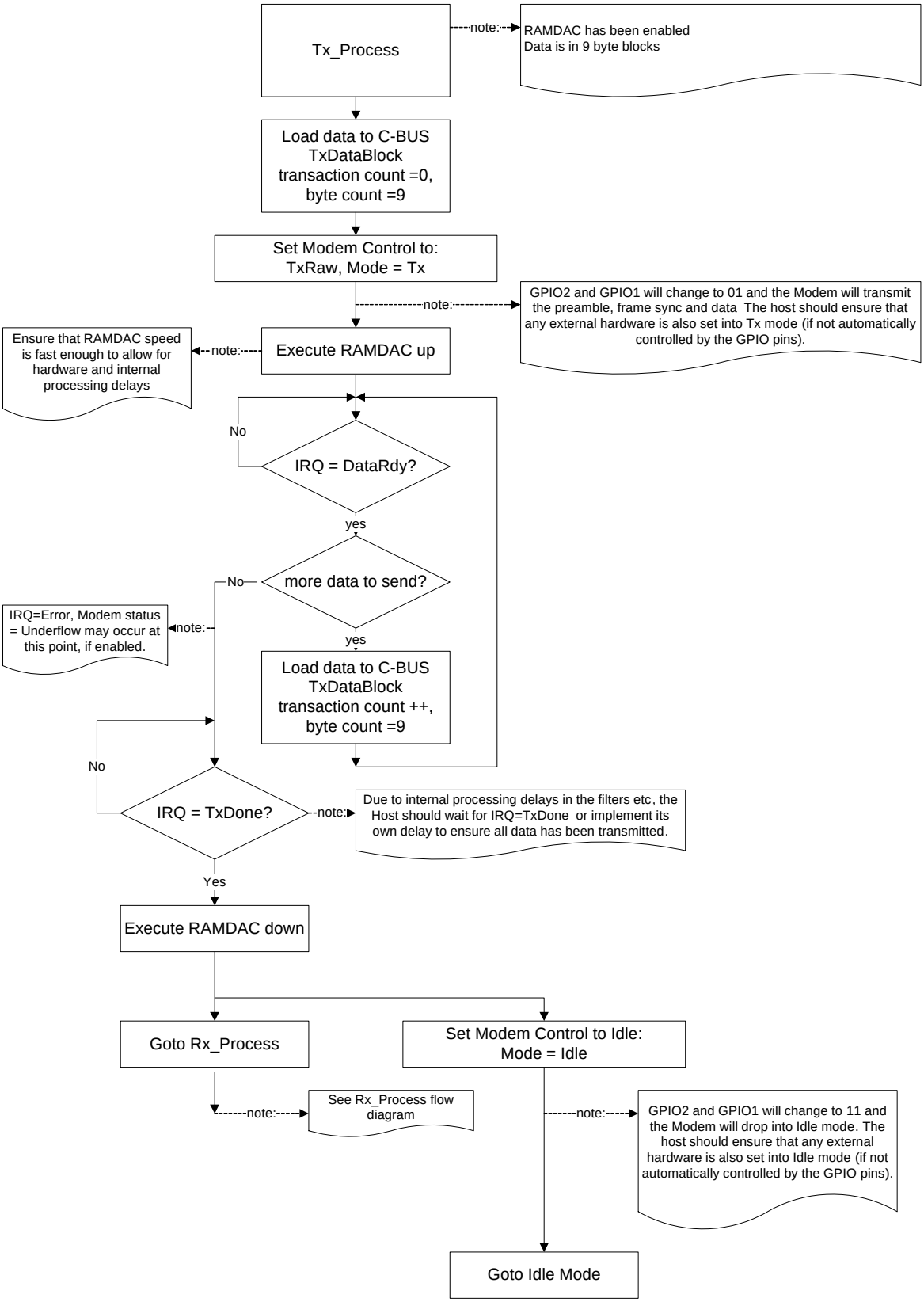


Figure 15 Tx Data Flow (Raw Data Mode)

7.5.7 Rx Mode (Raw)

In Rx Raw mode operation ($C1, Modem Control = $0021), the CMX7131/CMX7141 automatically starts searching for frame synchronisation. When a valid frame sync sequence is detected, an “FS1 Detect” or “FS2 Detect” IRQ is asserted and the data demodulator is enabled. All following payload data is loaded directly into the C-BUS RxData registers with a “DataReady” IRQ to indicate when each new block is available. This continues until the Mode is changed to Idle or Tx, even if the call has ended and there is no longer a valid signal at the input. The host MUST respond to each “DataReady” IRQ before the RxData registers are overwritten by subsequent payload data blocks.

If “soft” data mode has been selected, the payload data is encoded in 4-bit log-likelihood-ratio format. In this mode the host must be able to service the “DataReady” IRQs and RxData registers at four times the normal rate to avoid overflow.

Note that Raw Mode operation always requires the incoming data to be preceded with a valid frame sync sequence in order to derive timing information for the demodulator.

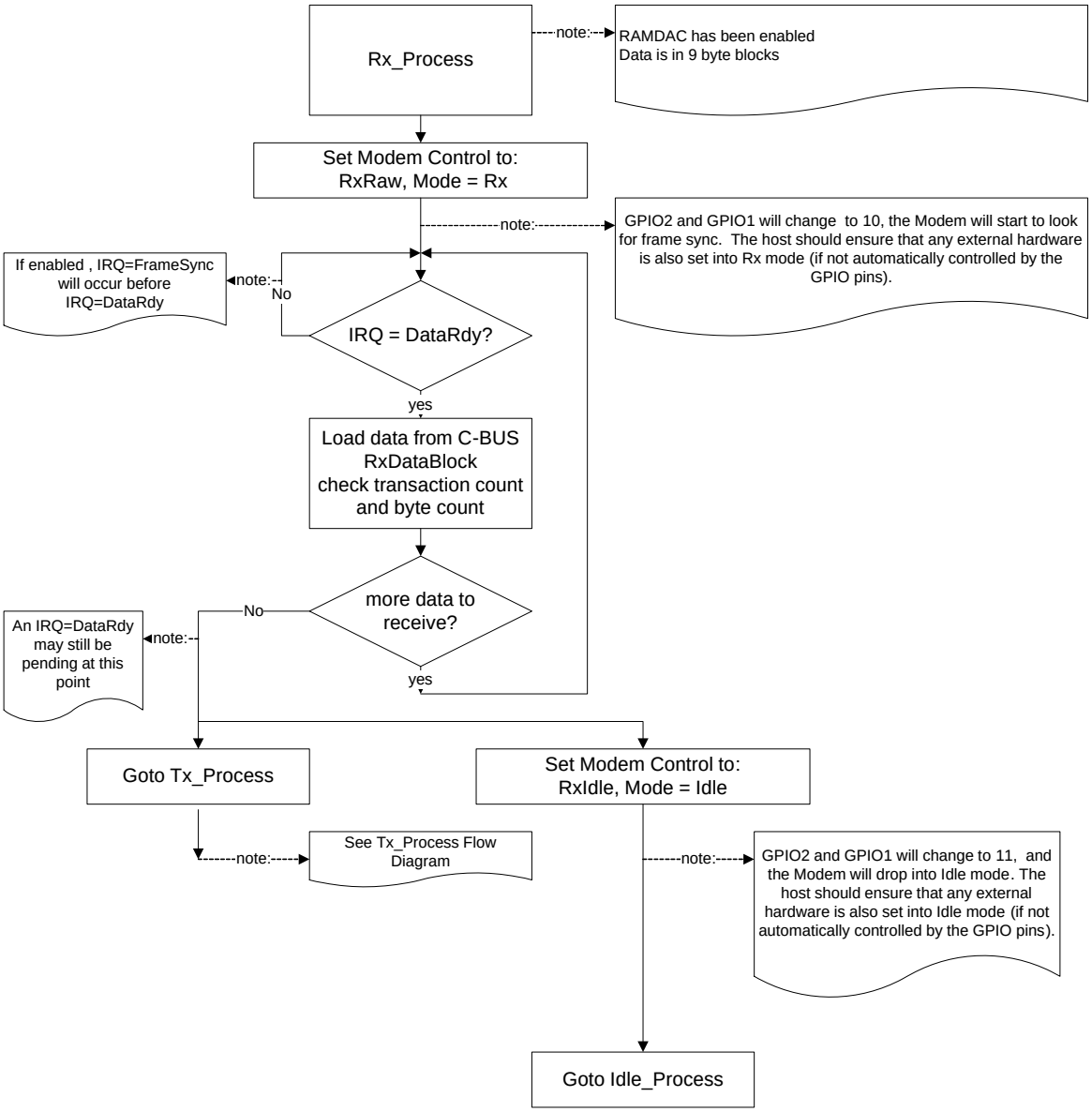


Figure 16 Rx Data Flow (Raw Data Mode)

7.5.8 Other Modem Modes

In Rx 4FSK EYE mode the filtered received signal is output at the MOD1 pin as an “eye” diagram for test and alignment purposes. A trigger pulse is output at the MOD2 pin to allow viewing on a suitable oscilloscope. The trigger pulse is generated directly from the receiver xtal source, not from the input signal.

In Tx mode a number of test and set-up modes are provided to facilitate test and alignment.

- PRBS (Preamble and Synchronisation Word are automatically transmitted first)
- Continuous preamble: a repeating sequence of [+3 +3 -3 -3] symbols
- Modulation set-up: in 2-point mode, a repeating sequence of eight +3 symbols followed by eight -3 symbols, and in I/Q mode a continuous sequence of +3 symbols.

7.5.9 Data Transfer

Payload data is transferred from/to the host using blocks of five Rx and five Tx 16-bit C-BUS registers, allowing up to 72 bits (9 bytes) of data to be transferred in sequence. The lowest 8 bits of the register block are reserved for a Byte Counter, Block ID and a Transaction Counter. The byte count indicates how

many bytes in the data block are valid and avoids the need to perform a full five word C-BUS read/write if only a smaller block of data need to be transferred.

Table 8 C-BUS Data Registers

C-BUS Address	Function	C-BUS Address	Function
$B5	Tx data 0-7 & info	$B8	Rx data 0-7 & info
$B6	Tx data 8-23	$B9	Rx data 8-23
$B7	Tx data 24-39	$BA	Rx data 24-39
$CA	Tx data 40-55	$BB	Rx data 40-55
$CB	Tx data 56-71	$C5	Rx data 56-71

The Block ID is ignored in Raw mode, but should be set to 01 (payload) for consistency with dPMR Formatted mode (see User Manual section 10.1.17).

Bits 7 and 6 hold the Transaction Counter, which is provided to allow detection of missed transfers and underflow/overflow. During a call, in Rx mode the CMX7131/CMX7141 increments the counter (modulo 4) on each transfer via the RxData block, and in Tx mode the host must increment the counter on every write to the TxData block. In Tx mode the CMX7131/CMX7141 detects that new data from the host is available by the change in the value of the Transaction Counter, so it is vital that the TxData0 register, which contains the counter, is the last TxData register to be written to in each transaction. If the CMX7131/CMX7141 identifies that a block has been written out of sequence, an Event IRQ will be issued.

7.5.10 CMX6x8 Pass-through Mode

To allow the host to communicate directly with the CMX6x8 for test and configuration purposes, a Pass-through mode is available which allows any CMX6x8 C-BUS register to be read or written (as appropriate). This mode uses the TxData0, RxData0 and Programming registers on the CMX7141.

To write to the CMX6x8:

- Set the CMX7131/CMX7141 to CMX6x8 Pass-through Mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX6x8 data value to the Txdata0 register ($B5)
- Write the CMX6x8 C-BUS address to the Programming register ($C8) with b15=0
- Wait for the Program Flag to be set ($C6 b0)

To read from the CMX6x8:

- Set the CMX7131/CMX7141 to CMX6x8 pass-through mode ($C1=$0004)
- Wait for the Program Flag to be set ($C6 b0)
- Write the CMX6x8 C-BUS address to the Programming register ($C8) with b15=1
- Wait for the Program Flag to be set ($C6 b0)
- Read the CMX6x8 data value from the RxData0 register ($B8)

CMX6x8 C-BUS addresses are all 8 bits long and should be written to bits 0-7 of the Programming Register. Bit 15 is the read/write flag (0 = read, 1 = write) and bit 14 is the register-size flag (0 = 16-bit, 1 = 8-bit). Unused bits should be cleared to zero. When an 8-bit register is read or written, the data occupies the lower 8 bits of the appropriate data register (TxData0 or RxData0).

7.6 dPMR Formatted Operation

In dPMR Formatted mode the CMX7131/CMX7141 performs all frame building/splitting and FEC coding/decoding, which relieves the host controller of a significant processing load. During voice calls the CMX7131/CMX7141 can automatically enable and control the CMX6x8, and transfer voice payload data from/to it without host intervention. In Rx mode the CMX7131/CMX7141 monitors address fields in incoming transmissions and only accepts calls if the programmed address requirements are satisfied. This allows the host to remain in a power-down or “sleep” state until it is really necessary to wake up, extending the battery life of the final product design.

7.6.1 Operating Modes and Addressing

TS 102 490 describes two operating modes for a dPMR radio:

- ISF – Initial Services and Facilities – “out of the box” mode
- CSF – Configured Services and Facilities – “managed” mode

The CMX7131/CMX7141 can support either of these modes, as selected by b9 of the Modem Configuration register, $C7 (see User Manual section 10.1.27).

The standard also defines two addressing schemes: 24-bit binary or 7-digit BCD (binary-coded-decimal). Radios operating in ISF mode are required to use binary addressing, but in CSF mode either binary or BCD addressing can be used. Both addressing schemes are supported by the CMX7131/CMX7141, selected by b11 in the Modem Configuration register, $C7 (see User Manual section 10.1.27).

The host can load two Own IDs (binary or BCD) into Program Block 1 for use in both Tx and Rx modes. In Tx mode the host can select which of these to send in the “Caller ID” field of the outgoing call. In Rx mode the CMX7131/CMX7141 compares the “Called ID” field from incoming calls against each of its Own IDs, and will accept the call if a valid ID match is found. Address matching can be disabled using b12 of the Modem Configuration register, $C7 in which case the CMX7131/CMX7141 will accept all incoming calls.

The CMX7131/CMX7141 implements BCD address translation in both Tx and Rx, to relieve the host of the processing required to map BCD digits to over-air binary values. BCD addresses can include wildcard digits in any of the lower four digits, and there are ten BCD “All-Call” addresses with wildcards in all six lower digits. The CMX7131/CMX7141 handles wildcard digits appropriately during address matching in Rx.

Binary addresses do not support group calling with wildcards, but the CMX7131/CMX7141 provides six binary-only Group Call IDs in addition to the two Own IDs. These can be programmed by the host to be used for address matching in Rx only.

TS 102 490 also specifies a system-wide All Call facility using the “Communication Format” field in the Header Frame (TS 102 490 section 5.8). The normal setting for this field is “Peer-to-peer”, but when set to “Call ALL” the CMX7131/CMX7141 will always accept the call regardless of ISF/CSF mode and all other address settings. The host should take care not to transmit in All Call mode unless actually intended.

7.6.2 ISF Addressing

The services available in ISF mode are described in TS 102 490 section 8.1. Radios using ISF mode provide a style of operation broadly similar to analogue PMR446.

ISF mode requires 24-bit binary addressing to be used, with only the top 8 bits (the Common ID field) in active use for addressing ISF mode devices. The remaining 16 bits must be set to all 1s. This is the default mode of the CMX7131/CMX7141 and the default Common IDs are:

- ID1: $01
- ID2: $02

The ISF Common All-Call ID is $FF. When in ISF mode the CMX7131/CMX7141 will always accept calls to this address regardless of other address settings.

7.6.3 CSF Addressing

The services available in CSF mode are described in TS 102 490 section 8.2 and Annex A.

CSF mode does not mandate BCD addressing unless the host implements the Standard User Interface, but the advantages of BCD addressing are direct mapping of user keypad entries to destination addresses and the option of wildcard digits to implement group calls. The host can select the addressing mode using b11 of the Modem Configuration register, $C7.

7.6.4 Tx Mode (dPMR formatted)

Device operation in Tx dPMR Formatted mode ($C1, Modem Control = $0012) is similar to Raw mode operation but the CMX7131/CMX7141 builds Header, Control Channel and End Information blocks, performs all FEC coding, interleaving and scrambling functions and inserts Frame Sync and Colour Code sequences to generate the required frame formats for transmission. During voice calls the CMX7131/CMX7141 can automatically enable and control the CMX6x8, and transfer voice payload data from/to it without host intervention.

The TxData registers are used to transfer Header and End Information fields in addition to payload data. The Block ID field in the TxData0 register informs the CMX7131/CMX7141 how to process each transfer.

b5-4	Block ID
00	HDR - Header Data
01	PLD - Payload Data
10	PLS - Payload Data with Slow Data
11	END - End Data

The host should preload the TxData registers with Header Data before placing the device in Tx dPMR Formatted mode. The CMX7131/CMX7141 reads the "Header Type" field to determine the burst type and then sends the Preamble and Header Frame. If the "Call Information" field indicates that repeated "extended wake-up" Headers are to be sent, the CMX7131/CMX7141 will do so automatically. The Header fields are saved for re-use when building the Control Channel Information blocks in following payload frames: the host does not need to re-load them.

Header Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	*reserved*		Own ID		Header Type				Counter		0	0	1	0	0	1
1	LE	0	Call Information											Comms Mode		
2	Comms Format				0	0	0	0	0	0	Colour Code					
3	0	0	0	0	Binary mode: Called Address lower 12 bits											
	BCD mode: Called Address lower 4 digits K4, K5, K6, K7															
4	0	0	0	0	Binary mode: Called Address upper 12 bits											
	0	0	0	0	BCD mode: Called Address upper 3 digits K1, K2, K3											

Header Type: See TS 102 490 section 5.11 (Communication Start, ACK, etc.)
Own ID: 00 = *reserved*
01 = send Own ID 1 (from Program Block 1)
10 = send Own ID 2 (from Program Block 1)
11 = *reserved*
reserved: See TS 102 490 section 5.4 (00)
Comms Mode: See TS 102 490 section 5.7 (sets data type and source, host or vocoder)
LE: Late-Entry (Rx only) – some data fields may be missing due to Late Entry into the call
Call Information: See TS 102 490 section 5.10 (includes extended headers, data frame size etc.)
Comms Format: See TS 102 490 section 5.8 (All-Call or peer-to-peer)
Colour Code: 6-bit index into the Colour Code table as shown in TS 102 490 section 6.1.5

Payload Data:
See Table 8 and User Manual section 10.1.14

Payload Data with Slow Data:
See Table 8 and User Manual section 10.1.14

End Data:

TxData RxData	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Tx Wait				Ack Req		End Type		Counter		1	1	0	0	1	1
1	0	0	0	0	0	0	*reserved*				0	Status Message				
2	Not used															
3	Not used															
4	Not used															

End Type: See TS 102 490 section 5.12
Ack Request: See TS 102 490 section 5.13
Tx Wait: See TS 102 490 section 5.14
Status Msg: See TS 102 490 section 5.15
reserved: 0000

Depending on the burst type, the CMX7131/CMX7141 will expect the host to load a series of payload data blocks and/or an End Data block (except for ACK bursts which consist of a bare Header Frame). Disconnect bursts contain a repeated Header/End Frame pair but the host should only load single blocks of Header and End Data fields, as the CMX7131/CMX7141 will send the duplicate frames automatically.

If the CMX6x8 vocoder is enabled and the "Communication Mode" field in the Header Frame indicates a voice call, the CMX7131/CMX7141 will automatically enable the CMX6x8 microphone input and route payload data from the CMX6x8 for transmission. Note that the CMX6x8 takes a finite time to encode the incoming voice data, during which the CMX7131/CMX7141 will automatically insert "silence" data into the payload frames. The host can load an End Frame at any point during the call. To terminate the voice call, the host should place the CMX7131/CMX7141 modem into Tx Idle mode ($C1, Modem Control = $0002). The CMX7131/CMX7141 will disable the CMX6x8 and send the End Frame that was loaded previously.

At the end of all dPMR transmissions the CMX7131/CMX7141 will issue a TxDone IRQ when it is safe for the host to place the device back into Idle mode ($C1, Modem Control = $0000).

7.6.5 Rx Mode (dPMR formatted)

Device operation in Rx dPMR Formatted mode ($C1, Modem Control = $0011) is similar to Raw mode operation but the CMX7131/CMX7141 automatically splits incoming calls to extract Header Information, Control Channel Information and End Information blocks and performs all the necessary de-scrambling, de-interleaving and FEC decoding functions. In speech calls the CMX7131/CMX7141 can automatically enable the CMX6x8 vocoder when required and transfer received speech data without host intervention.

The RxData registers are used to transfer Header and End Data fields in addition to payload data. The Block ID field in the RxData0 register informs the host what type of data block each transfer contains. The field layout in the RxData registers for the different transfer types is the same as for Tx dPMR Formatted mode (section 7.6.4).

When placed in Rx dPMR Formatted mode the CMX7131/CMX7141 automatically starts searching for the dPMR frame sync sequences. In addition to detecting the 48-bit FS1 frame sync at the start of a transmission, the CMX7131/CMX7141 can also perform "late entry" into a call by detecting two successive copies of the 24-bit FS2 sequence at the correct two-frame spacing. When a valid frame sync sequence has been detected, an "FS1 Detect" or "FS2 Detect" IRQ is issued and the data demodulator is enabled.

The CMX7131/CMX7141 then decodes the contents of the Header Frame (after an FS1 detect) or the following four Control Channel Information blocks (after an FS2 detect). The Header Information or Control Channel Information CRCs are checked and processing continues only if a full set of valid fields has been received. Header Frames contain two duplicate Header Information blocks: the CMX7131/CMX7141 checks both block CRCs, uses the first valid block and discards the other.

When repeated "extended wake-up" Header Frames are received (see TS 102 490 section 11.1) the CMX7131/CMX7141 will decode the first valid Header but delay address checking until all following repeat Headers have been received. This maximises the time the host can be kept in powersave.

Address checking now takes place depending on ISF/CSF mode and the addressing mode selected. The "Communications Format" field is checked first: if this is set to "Call ALL" the call is accepted. If not, the "Called station ID" is checked against the device's Own IDs (programmed by the host into Program Block 1) and if a match is found the call is accepted. In ISF mode the Common All-Call ID $FF is also always accepted. In any of these cases a "Called" IRQ is issued to the host, otherwise the call is dropped with no further host notification and the CMX7131/CMX7141 returns to frame sync search. Address matching can be disabled by setting b12 of the Modem Configuration register, in which case the CMX7131/CMX7141 will accept all incoming calls.

The Header fields are presented to the host in the RxData block. Late entry is indicated by bit 15 of RxData1: in this case the "Header Type" and "Call Information" fields in the Header Data block returned to

the host will not contain valid data, as these fields are only sent in Header Frames and are not re-sent in the Control Channel Information blocks during a call.

Depending on the burst type the CMX7131/CMX7141 will decode the following payload and/or End Frames and present their contents to the host or vocoder. If the CMX6x8 Vocoder is enabled and the "Communication Mode" field in the Header Frame indicates a voice call, the CMX7131/CMX7141 will automatically enable the CMX6x8 speaker output and route payload data to the CMX6x8 for decoding. In this mode, the data is transferred in 4-bit Log-Likelihood-Ratio format. Otherwise payload data is presented to the host in the RxData registers in soft or hard format as specified. When an End Frame is received the CMX7131/CMX7141 will report its contents to the host, disable the vocoder (if necessary) and return to frame sync search.

All frame sync sequences, Colour Codes and CRCs contained in payload superframes are checked and an "Event" IRQ is issued when any are received incorrectly. If all the frame sync sequences, Colour Codes and CRCs in a superframe are received incorrectly, the superframe is considered corrupt. The host can set a threshold for consecutive corrrupt superframes (in Program Block 0) after which the CMX7131/CMX7141 will issue an "Event" IRQ, drop the call and return to frame sync search.

See:
- RxData 0 - $B8 read
- AuxData Read - $CC read

7.6.6 Slow Data

Slow Data may be transferred in voice calls alongside Voice Payload Data, by setting the Block ID to "Payload with Slow Data" and using the AuxData registers. If the CMX6x8 is enabled, there will be no voice payload transfers and so dummy payload transfers are used with the Byte Counter field cleared to zero. In Type1 and Type 2 Data calls the Slow Data field is used to control the data flow over-air and so is generated or decoded by the CMX7131/CMX7141 itself and the only data field that is visible to the host is the "Format" field as defined in TS 102 490 section 5.9.2. which is made available, or supplied by the host, in the lowest 4 bits of the AuxData register.

In Tx mode:

- Load AuxData register with two bytes of Slow Data: AuxData Write - $C2 write
- Set Communications Mode to "Voice with Slow Data"
- Set BlockID to "Payload with Slow Data": TxData 0 - $B5 write
- Set Byte Counter field (to zero if CMX6x8 is in use): TxData 0 - $B5 write

The CMX7131/CMX7141 has an internal 64-byte buffer for Slow Data. While the host keeps this internal data buffer "topped-up" the CMX7131/CMX7141 will continue to transmit Slow Data and add the "continuation bits" to the over-air data. Note that only two bytes of Slow Data are sent over-air for every 36 bytes of voice payload, so the buffer may overflow if a large quantity of Slow Data is loaded continuously. An IRQ bit will be raised when there are only two bytes left in the FIFO.

When the host allows the internal buffer to empty, the CMX7131/CMX7141 will terminate the transmission of Slow Data in the current burst. It is not possible to re-start Slow Data transmission within a burst.

In Rx mode:

- BlockID will report "Payload with Slow Data": RxData 0 - $B8 read
- Communications Mode will report "Voice with Slow Data"
- If payload is being sent to the CMX6x8, then the Byte Counter field will be cleared to zero
- Slow Data is available in the AuxData register: AuxData Read - $CC read

When the Slow Data transfer has completed, the CMX7131/CMX7141 will stop presenting data to the host.

7.7 Squelch Operation

Many Limiter/Discriminator chips provide a noise-quieting squelch circuit around an op-amp configured as a filter. This signal is conventionally passed to a comparator to provide a digital squelch signal, which can be routed directly to one of the CMX7131/CMX7141's GPIO pins or to the host. However with the

CMX7131/CMX7141, the comparator and threshold operations can be replaced by one of the AuxADCs with programmable thresholds and hysteresis functions.

See:
- IRQ Status - $C6 read
- Modem Configuration - $C7 write

7.8 GPIO Pin Operation

The CMX7131/CMX7141 provides 4 pins. RXENA (GPIO1) and TXENA (GPIO2) are configured to reflect the Tx/Rx state of the Mode register (TXENA and RXENA, active low).

See:
- Modem Configuration - $C7 write

Note that RXENA and TXENA will not change state until the relevant mode change has been executed by the CMX7131/CMX7141. This is to allow the host sufficient time to load the relevant data buffers and the CMX7131/CMX7141 time to encode the data required prior to its transmission. There is thus a fixed time delay between the GPIO pins changing state and the data signal appearing at the MOD output pins. During the power-on sequence (until the FI has completed its load sequence) these pins have only a weak pull-up applied to them, so care should be taken to ensure that any loading during this period does not adversely affect the operation of the unit.

GPIO A and B are host programmable for input or output using the AuxADC Configuration register, $A7. The default state is output, high level. When set for input, the values can be read back using the Modem Status register, $C9.

7.9 Auxiliary ADC Operation

The inputs to the two auxiliary ADCs can be independently routed from any of the signal input pins under control of the AuxADC Configuration register, $A7. Conversions will be performed as long as a valid input source is selected. To stop the ADCs, the input source should be set to “off”. Register $C0, b6, BIAS, must be enabled for auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the AuxADC Configuration register, $A7, the length of the averaging is determined by the value in the Programming register (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last average value. The proportion is determined by the value of the average counter in P3.0 and P3.1.

For an average value of:

0 = 50% of the current value will be added to 50% of the last average value,

1 = 25% of the current value will be added to 75% of the last average value,

2 = 12.5% etc.

The maximum useful value of this field is 9.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated when a rising edge passes the High threshold or a falling edge passes the Low threshold, see Figure 17. The thresholds are programmed via the AuxADC Threshold register, $CD. See Figure 17.

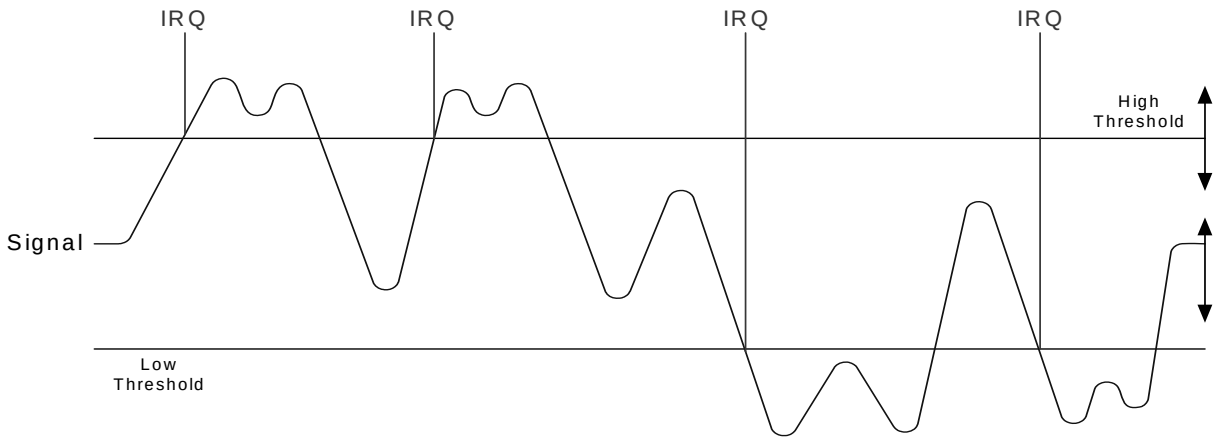


Figure 17 AuxADC IRQ Operation

Auxiliary ADC data is read back in the AuxADC Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

See:
- AuxADC Configuration - $A7 write
- AuxADC1 Data and Status - $A9 read
- AuxADC2 Data and Status - $AA read
- AuxADC Threshold Data - $CD write

7.10 Auxiliary DAC/RAMDAC Operation

The four auxiliary DAC channels are programmed via the AuxDAC Data/Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will automatically output a pre-programmed profile at a programmed rate. The AuxDAC Data/Control register, $A8, with b12 set, controls this mode of operation. The default profile is a raised cosine (see Table 13), but this may be over-written with a user-defined profile by writing to Programming register P3.11. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to Idle or Rx mode whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Data/Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

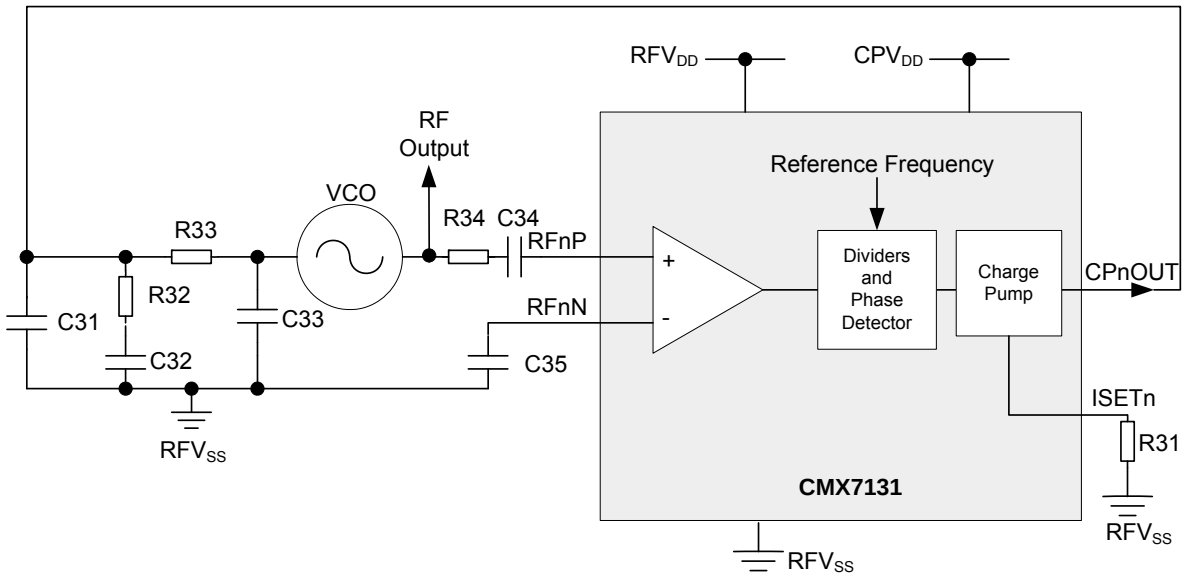
See:
- AuxDAC Data/Control - $A8 write

7.11 RF Synthesiser (CMX7131 only)

The CMX7131 includes two Integer-N RF synthesisers, each comprising a divider, phase comparator and charge pump. The divider has two sets of N and R registers: one set can be used for transmit and the other for receive. The division ratios can be set up in advance by means of C-BUS registers. A single C-BUS command will change over from the transmit to the receive division ratios, or vice versa, enabling a fast turnaround.

See:
- RF Synthesiser Data - $B2 write
- RF Synthesiser Control - $B3 write
- RF Synthesiser Status - $B4 8-bit read

External RF components are needed to complete the synthesiser circuit. A typical schematic for a 446MHz synthesiser (3.125kHz comparison frequency) is shown in Figure 18.



Note: n = 1 or 2 for Synthesiser 1 or 2

Figure 18 Example RF Synthesiser Components

R31	0Ω	C31	22nF
R32	5.6kΩ	C32	470nF
R33	10kΩ	C33	10nF
R34	100Ω	C34	1nF
		C35	1nF

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Note: R31 is chosen within the range 0Ω to 30kΩ and selects the nominal charge pump current.

It is recommended that C34 and C35 are kept close to the VCO and that the stub from the VCO to the CMX7131 is kept as short as possible. The loop filter components should be placed close to the VCO.

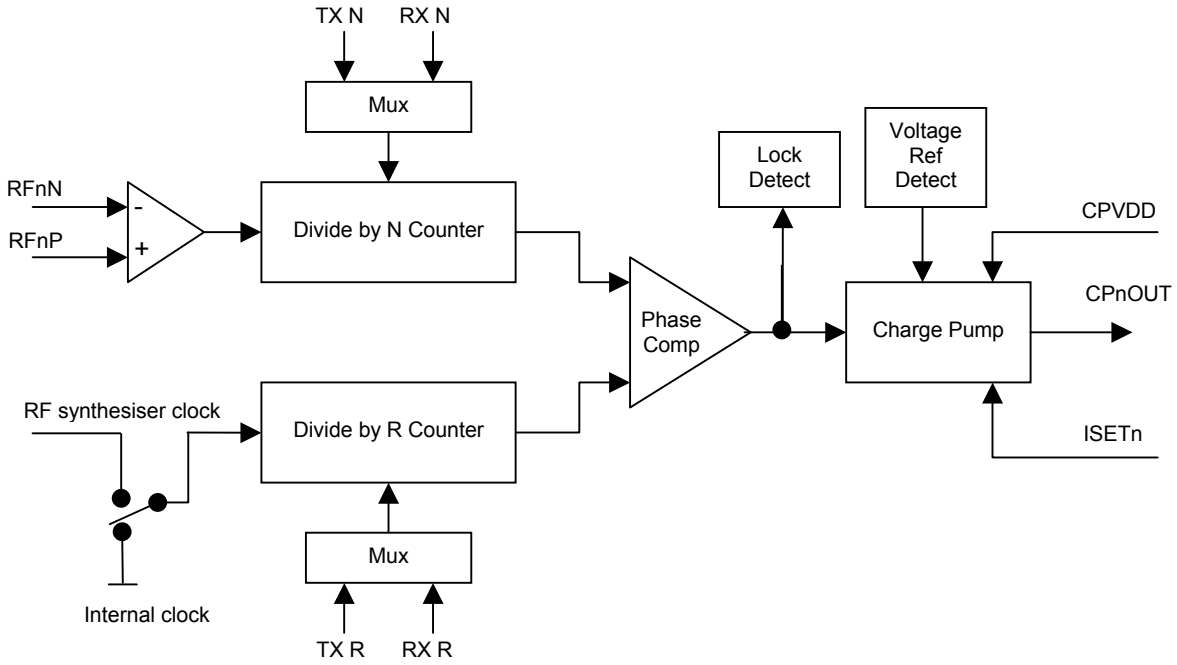


Figure 19 Single RF Synthesiser Block Diagram

The two RF synthesisers are programmable to any frequency in the range 100MHz to 600MHz. Figure 19 is a block diagram of one synthesiser channel. The RF synthesiser clock is selectable between the XTAL or the clock supplied to the RFCLK input pin. The RF synthesiser clock is common to both synthesisers. The charge pump supply (CP supply, CPVDD) is also common to both synthesisers. The RFnP and RFnN input pins, CPnOUT, ISETn and RFVSS pins are channel specific and designated as either RF1P, RF1N, CP1OUT, ISET1, RFVSS or RF2P, RF2N, CP2OUT, ISET2, RFVSS on the Signal List in section 3. The N and R values for Tx and Rx modes are synthesiser specific and can be set from the host µC via the C-BUS. Various synthesiser specific status signals are also accessible via C-BUS. The divide by N counter is 20 bits; the R counter is 13 bits. Typical external components are shown in Figure 18.

Both synthesisers are phase locked loops (PLLs) of the same design, utilising external VCOs and loop filters. The VCOs need to have good phase noise performance although it is likely that the high division ratios used will result in the dominant noise source being the reference oscillator. The phase detectors are of the phase-frequency type with a high impedance charge pump output requiring just passive components in the loop filter. Lock detect functions are built in to each synthesiser and the status reported via C-BUS. A transition to out-of-lock can be detected and communicated via a C-BUS interrupt to the host µC. This can be important in ensuring that the transmitter cannot transmit in the event of a fault condition arising.

Two levels of charge pump gain are available to the user, to facilitate the possibility of locking at different rates under program control. A current setting resistor (R31) is connected between the ISET pin (one for each PLL system) and the respective RFVSS pin. This resistor will have an internally generated band gap voltage expressed across it and may have a value of 0Ω to 30kΩ, which (in conjunction with the on-chip series resistor of 9.6kΩ) will give charge pump current settings over a range of 2.5mA down to 230µA (including the control bit variation of 4 to 1). The value of the current setting resistor (R31) is determined in accordance with the following formulae:

gain bit set to 1: $R31\ (\text{in } \Omega) = (24/I_{CP}) - 9600$
gain bit cleared to 0: $R31\ (\text{in } \Omega) = (6/I_{CP}) - 9600$
where I_{CP} is the charge pump current (in mA).

Note that the charge pump current should always be set to at least 230µA. The 'gain bit' refers to either bit 3 or bit 11 in the RF Synthesiser Control register, $B3.

The step size (comparison frequency) is programmable; to minimise the effects of phase noise this should be kept as high as possible. This can be set as low as 2.5kHz (for a reference input of 20MHz or less), or up to 200kHz – limited only by the performance of the phase comparator.

The frequency for each synthesiser is set by using two registers: an 'R' register that sets the division value of the input reference frequency to the comparison frequency (step size), and an 'N' register that sets the division of the required synthesised frequency from the external VCO to the comparison frequency. This yields the required synthesised frequency (Fs), such that:

$$Fs = (N / R) \times F_{REF}$$ where F_{REF} is the selected reference frequency

Other parameters for the synthesisers are the charge pump setting (high or low)

- Since the set-up for the PLLs takes 4 x "RF Synthesiser Data register" writes it follows that, while updating the PLL settings, the registers may contain unwanted or intermediate values of bits. These will persist until the last register is written. It is intended that users should change the content of the "RF Synthesiser Data register" on a PLL that is disabled, powersaved or selected to work from the alternate register set ("Tx" and "Rx" are alternate register sets). There are no interlocks to enforce this intention. The names "Tx" and "Rx" are arbitrary and may be assigned to other functions as required. They are independent sets of registers, one of which is selected to command each PLL by changing the settings in the RF Synthesiser Control - $B3 write register.

For optimum performance, a common master clock should be used for the RF synthesisers (the RF synthesiser clock) and the baseband sections (Main and Auxiliary System Clocks). Using unsynchronised clocks can result in spurious products being generated in the synthesiser output and in some cases difficulty may be experienced with obtaining lock in the RF synthesisers.

Lock Status

The lock status can be observed by reading the RF Synthesiser Status register, $B4, and the individual lock status bits can (subject to masking) provide a C-BUS interrupt.

The lock detector can use a tolerance of one cycle or four cycles of the reference clock (not the divided version that is used as a comparison frequency) in order to judge phase lock. An internal shift register holds the last three lock status measurements and the lock status bits are flagged according to a majority vote of these previous three states. Hence, one occasional lock error will not flag a lock fail. At least two successive phase lock events are required for the lock status to be true. Note that the lock status bits confirm phase lock to the measured tolerance and not frequency lock. The synthesiser may take more time to confirm phase lock with the lock status bits than the time to switch from channel to channel. The purpose of a 4-cycle tolerance is for the case where a high frequency reference oscillator would not forgive a small phase error.

RF Inputs

The RF inputs are differential and self biased (when not powersaved). They are intended to be capacitatively coupled to the RF signal. The signal should be in the range 0dBm to –20dBm (not necessarily balanced). To ensure an accurate input signal the RF should be terminated with 50Ω as close to the chip as possible and with the "P" and "N" inputs capacitatively coupled to the input and ground, keeping these connections as short as possible. The RF input impedance is almost purely capacitative and is dominated by package and printed circuit board parasitics.

Guidelines for using the RF Synthesisers

- RF input slew rate (dv/dt) should be 14 V/µs minimum.
- The RF Synthesiser 2.5V digital supply can be powered from the VDEC output pin.
- RF clock sources and other, different clock sources must not share common IC components, as this may introduce coupling into the RF. Unused ac-coupled clock buffer circuits should be tied off to a dc supply, to prevent them oscillating.
- It is recommended that the RF Synthesisers are operated with maximum charge pump gain (ie. ISET tied to RFVSS).
- The loop filter components should be optimised for each VCO.

7.12 Digital System Clock Generators

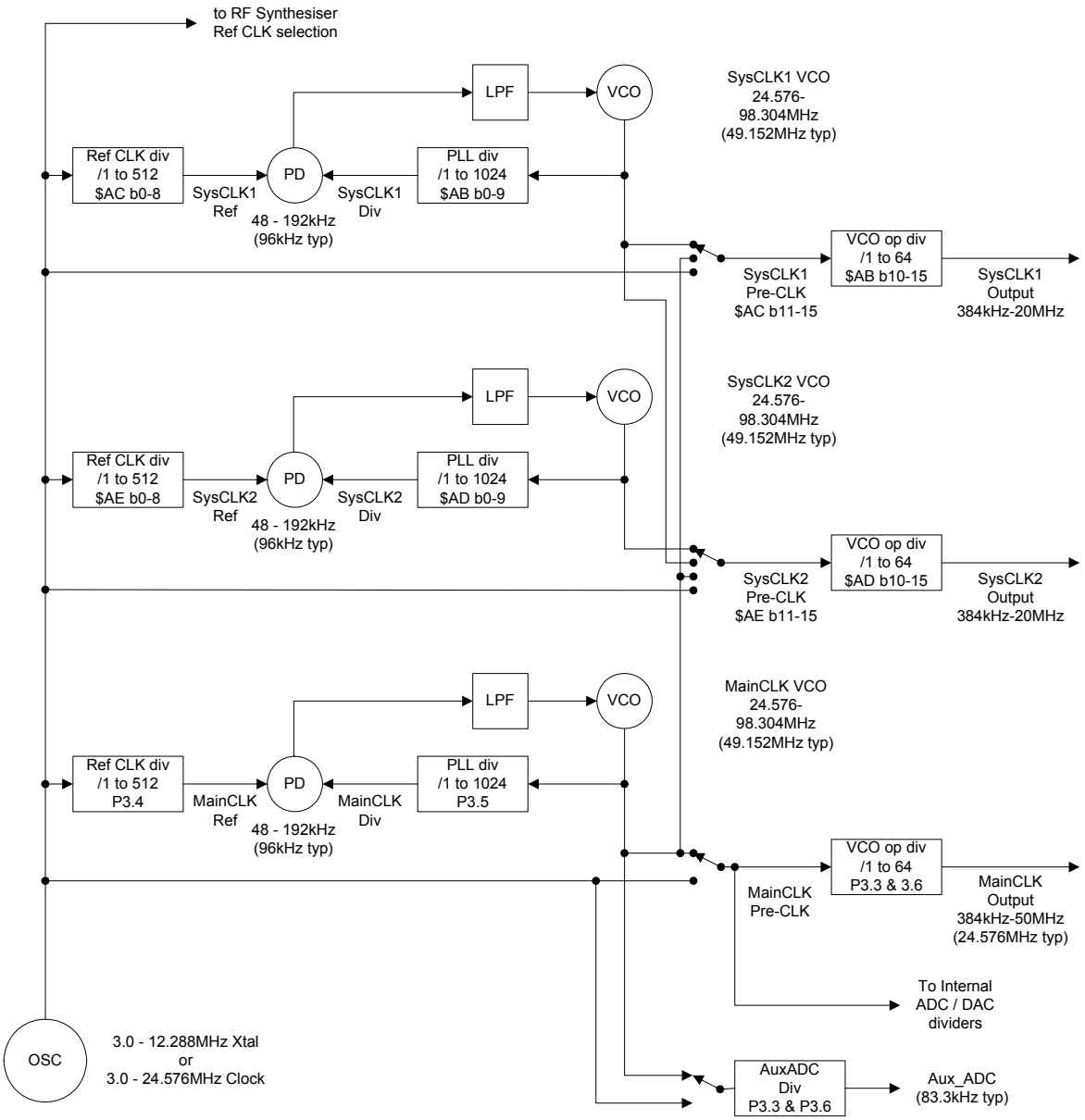


Figure 20 Digital Clock Generation Schemes

The CMX7131/CMX7141 includes a 2-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section 5, or the XTAL input can be driven by an externally generated clock. The crystal (Xtal) source frequency can go up to 12.288MHz (clock source frequency up to 24.576MHz), but a 19.2MHz oscillator is assumed by default for the functionality provided in the CMX7131/CMX7141.

7.12.1 Main Clock Operation

A digital PLL is used to create the Main Clock (nominally 24.576MHz) for the internal sections of the CMX7131/CMX7141. At the same time, other internal clocks are generated by division of either the XTAL Reference Clock or the Main Clock. These internal clocks are used for determining the sample rates and conversion times of A-to-D and D-to-A converters, running a General Purpose (GP) Timer and the signal

processing block. In particular, it should be noted that in Idle mode the setting of the GP Timer divider directly affects the C-BUS latency (with the default values this is nominally 250µs).

The CMX7131/CMX7141 defaults to the settings appropriate for a 19.2MHz oscillator, however if other frequencies are to be used then the Program Block registers P3.2 to P3.7 will need to be programmed appropriately at power-on. This flexibility allows the device to re-use an external clock source, so reducing total cost and potential noise sources. A table of common values is provided in Table 4.

See:
- Program Block 3 – AuxDAC, RAMDAC and Clock Control

7.12.2 System Clock Operation

Two System Clock outputs, SYSCLK1 and SYSCLK2, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 20. Note that at power-on, these pins are disabled.

See:
-
- SYSCLK 1 and SYSCLK 2 PLL Data - $AB, $AD write
- SYSCLK 1 and SYSCLK 2 REF - $AC and $AE write

7.13 Signal Level Optimisation

The internal signal processing of the CMX7131/CMX7141 will operate with wide dynamic range and low distortion only if the signal level at all stages in the signal processing chain is kept within the recommended limits. For a device working from a 3.3V ±10% supply, the maximum signal level which can be accommodated without distortion is [(3.3 x 90%) - (2 x 0.3V)] Volts pk-pk = 838mV rms, assuming a sine wave signal. This should not be exceeded at any stage.

7.13.1 Transmit Path Levels

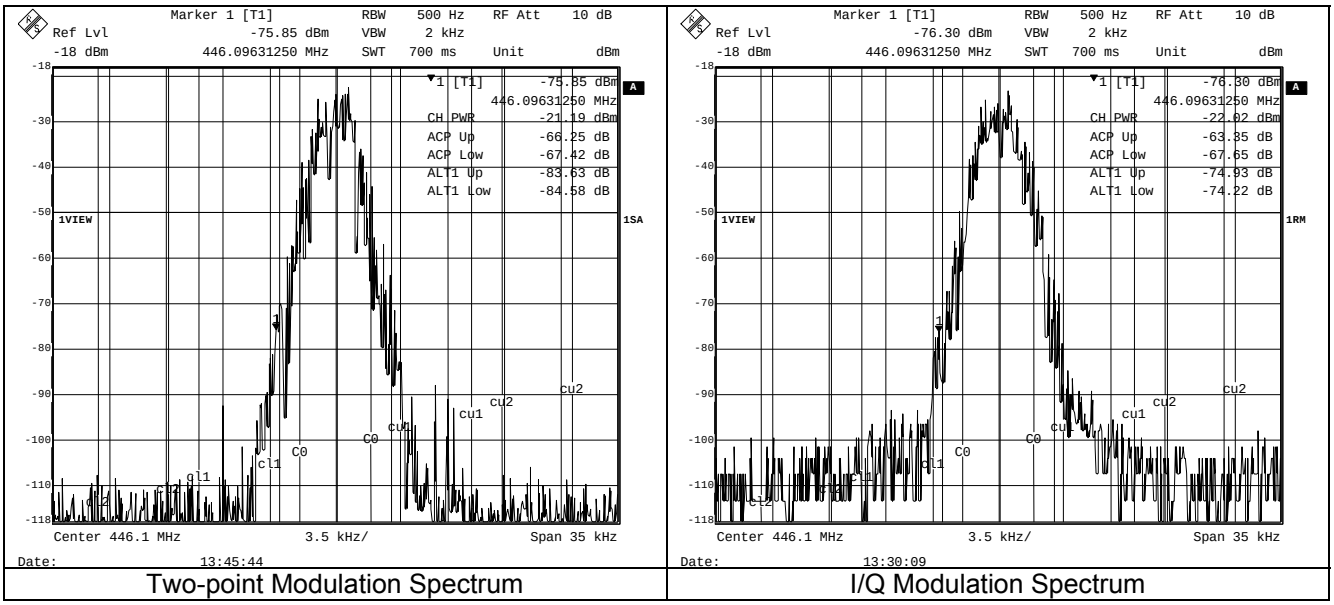
For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB, The Fine Output adjustment ($C8 P4.2-4.3) has a maximum attenuation of 3.5dB and no gain, whereas the Coarse Output adjustment ($B0) has a variable attenuation of up to +40.0dB and no gain.

7.13.2 Receive Path Levels

The Coarse Input adjustment ($B1) has a variable gain of up to +22.4dB and no attenuation. With the lowest gain setting (0dB), the maximum allowable input signal level at the DISCFB pin would be 838mV rms. This signal level is an absolute maximum, which should not be exceeded.

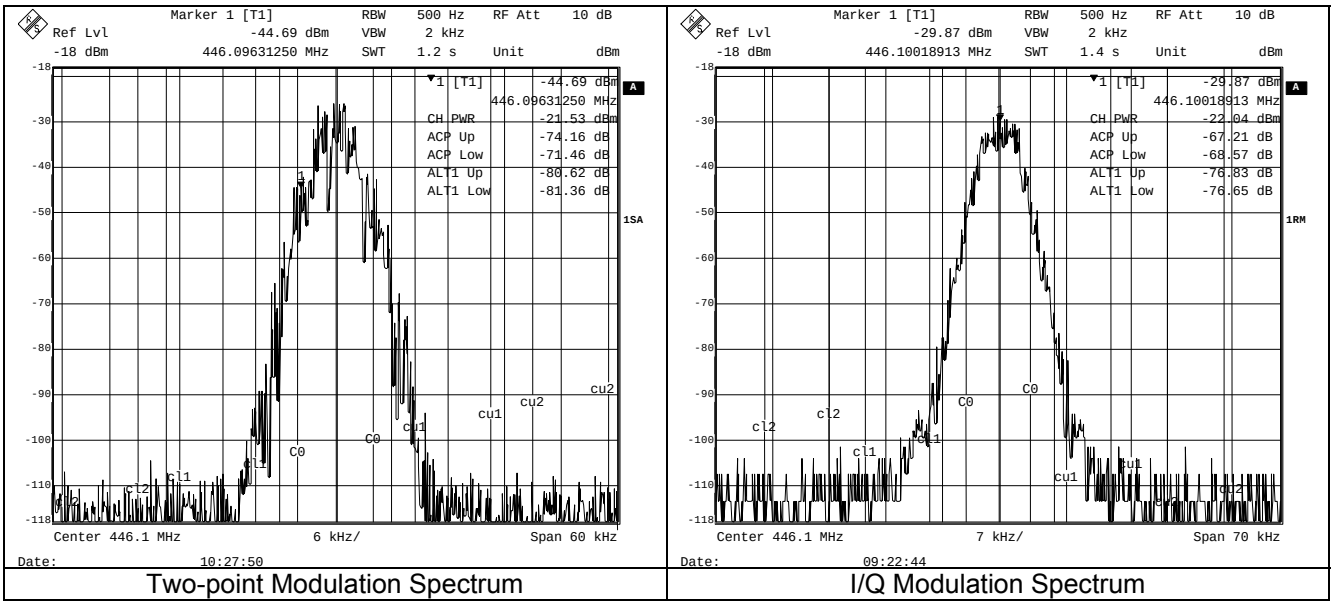
7.14 Tx Spectrum Plots

The following figure shows the Tx spectrum when using a suitable signal generator as measured on a spectrum analyser using the CMX7131/CMX7141 internal PRBS generator. Note that the I/Q mode is sensitive to variations in dc offset in the modulation path and these must be minimised.



Two-point Modulation Spectrum	I/Q Modulation Spectrum

Figure 21 Tx Modulation Spectra - 4800bps



Two-point Modulation Spectrum	I/Q Modulation Spectrum

Figure 22 Tx Modulation Spectra - 9600bps

7.15 C-BUS Register Summary

Table 9 C-BUS Registers

ADDR. (hex)		REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	AuxADC Configuration	16
$A8	W	AuxDAC Data and Control	16
$A9	R	AuxADC1 Data and Status/Checksum 2 hi	16
$AA	R	AuxADC2 Data and Status/Checksum 2 lo	16
$AB	W	SYSCLK 1 PLL Data	16
$AC	W	SYSCLK 1 Ref	16
$AD	W	SYSCLK 2 PLL Data	16
$AE	W	SYSCLK 2 Ref	16
$AF		*reserved*	
$B0	W	Analogue Output Gain	16
$B1	W	Input Gain and Signal Routing	16
$B2	W	RF Synthesiser Data (CMX7131 only)	16
$B3	W	RF Synthesiser Control (CMX7131 only)	16
$B4	R	RF Synthesiser Status (CMX7131 only)	8
$B5	W	TxData 0	16
$B6	W	TxData 1	16
$B7	W	TxData 2	16
$B8	R	RxData 0/Checksum 1 hi	16
$B9	R	RxData 1/Checksum 1 lo	16
$BA	R	RxData 2	16
$BB	R	RxData 3	16
$BC		*reserved*	
$BD		*reserved*	
$BE		*reserved*	
$BF		*reserved*	
$C0	W	Power Down Control	16
$C1	W	Modem Control	16
$C2	W	AuxData Write	16
$C3	W	CMX6x8 Analogue Gain	16
$C4		*reserved*	
$C5	R	Rx Data 4	16
$C6	R	IRQ Status	16
$C7	W	Modem Configuration	16
$C8	W	Programming Register	16
$C9	R	Modem Status	16
$CA	W	Tx Data 3	16
$CB	W	Tx Data 4	16
$CC	R	AuxData Read	16
$CD	W	AuxADC Threshold Data	16
$CE	W	Interrupt Mask	16
$CF		*reserved*	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	–0.3	4.5	V
AV_{DD}- AV_{SS}	–0.3	4.5	V
RFV_{DD}- RFV_{SS} (CMX7131 only)	–0.3	4.5	V
CPV_{DD}- RFV_{SS} (CMX7131 only)	–0.3	4.5	V
Voltage on any pin to DV_{SS}	–0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	–0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding BIAS) (i.e.VDEC, AVDD, AVSS, DVDD, DVSS, CPVDD, RFVDDorRFVSS)	–30	+30	mA
Current into or out of any other pin	–20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD} or CPV_{DD}	0	0.3	V
AV_{DD} and CPV_{DD} (CMX7131 only)	0	0.3	V
DV_{SS} and AV_{SS} or RFV_{SS}(CMX7131)	0	50	mV
AV_{SS} and RFV_{SS} (CMX7131 only)	0	50	mV

L4 Package (48-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1600	mW
... Derating	–	16	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

L9 Package (64-pin LQFP)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1690	mW
… Derating	–	16.9	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

Q1 Package (64-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	3500	mW
… Derating	–	35.0	mW/°C
Storage Temperature	–55	+125	°C
Operating Temperature	–40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
$DV_{DD} – DV_{SS}$		3.0	3.6	V
$AV_{DD} – AV_{SS}$		3.0	3.6	V
$CPV_{DD} – RFV_{SS}$ (CMX7131 only)		3.0	3.6	V
$RFV_{DD} – DV_{SS}$ (CMX7131 only)	3	2.25	2.75	V
$V_{DEC} – DV_{SS}$	2	2.25	2.75	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using a Xtal)	1	3.0	12.288	MHz
XTAL/CLK Frequency (using an external clock)	1	3.0	24.576	MHz

Notes:
1 Nominal XTAL/CLK frequency is 19.2MHz.
2 The V_{DEC} supply is automatically derived from DV_{DD} by the on-chip voltage regulator.
3 The RFV_{DD} supply can be supplied from the V_{DEC} supply, if preferred.

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = CPV_{DD} (CMX7131) = 3.0V to 3.6V; RFV_{DD} (CMX7131) = 2.25V to 2.75V.
V_{DEC} = 2.5V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB. Output stage attenuation = 0dB.

Current consumption figures quoted in this section apply to the device when loaded with FI-1.x only. The use of other Function Images, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
Idle Mode	22				
DI_{DD}		–	1.4	–	mA
AI_{DD}	23	–	1.6	–	mA
Rx Mode	22				
DI_{DD} (4800bps – search for FS)		–	4.7	–	mA
DI_{DD} (9600bps – search for FS)		–	7.5	–	mA
DI_{DD} (4800bps – FS found)		–	2.8	–	mA
DI_{DD} (9600bps – FS found)		–	3.7	–	mA
AI_{DD}		–	1.6	–	mA
Tx Mode	22				
DI_{DD} (4800bps – 2-point)		–	4.3	–	mA
DI_{DD} (9600bps – 2-point)		–	5.2	–	mA
DI_{DD} (4800bps – I/Q)		–	5.4	–	mA
DI_{DD} (9600bps – I/Q)		–	7.3	–	mA
AI_{DD} (AV_{DD} = 3.3V)		–	1.5	–	mA
Additional current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
Additional current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA
Additional Current for each RF Synthesiser	24				
CPI_{DD} + RFI_{DD} (CPV_{DD} = 3.3V, RFV_{DD} = 2.5V)		–	2.5	4.5	mA

Notes:

21 Tamb=25°C: not including any current drawn from the device pins by external circuitry.

22 System Clocks: auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled.

23 May be further reduced by power-saving unused sections

24 When using the external components shown in Figure 18 and when supplying the current for RFV_{DD} from the regulated 2.5V digital (V_{DEC}) supply. The latter is derived from DV_{DD} by an on-chip voltage regulator.

DC Parameters (continued)	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input	25				
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Current (Vin = DV_{DD})		–	–	40	µA
Input Current (Vin = DV_{SS})		–40	–	–	µA
C-BUS Interface and Logic Inputs					
Input Logic 1		70%	–	–	DV_{DD}
Input Logic 0		–	–	30%	DV_{DD}
Input Leakage Current (Logic 1 or 0)		–1.0	–	1.0	µA
Input Capacitance		–	–	7.5	pF
C-BUS Interface and Logic Outputs					
Output Logic 1 (I_{OH} = 2mA)		90%	–	–	DV_{DD}
Output Logic 0 (I_{OL} = -5mA)		–	–	10%	DV_{DD}
"Off" State Leakage Current		–	–	10	µA
IRQN (Vout = DV_{DD})		–1.0	–	+1.0	µA
REPLY_DATA (output HiZ)		–1.0	–	+1.0	µA
V_{BIAS}	26				
Output Voltage Offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)		–	±2%	–	AV_{DD}
Output Impedance		–	22	–	kΩ

Notes:
25 Characteristics when driving the XTAL/CLK pin with an external clock source.
26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input					
'High' Pulse Width	31	15	–	–	ns
'Low' Pulse Width	31	15	–	–	ns
Input Impedance (at 6.144MHz)					
Powered-up Resistance		–	150	–	kΩ
Capacitance		–	20	–	pF
Powered-down Resistance		–	300	–	kΩ
Capacitance		–	20	–	pF
Xtal Start-up Time (from powersave)		–	20	–	ms
System Clk 1/2 Outputs					
XTAL/CLK input to CLOCK_OUT timing:					
(in high to out high)	32	–	15	–	ns
(in low to out low)	32	–	15	–	ns
'High' Pulse Width	33	76	81.38	87	ns
'Low' Pulse Width	33	76	81.38	87	ns
V_{BIAS}					
Start-up Time (from powersave)		–	30	–	ms
Microphone, Alternative and Discriminator Inputs (MIC, ALT, DISC)					
Input Impedance	34	–	>10	–	MΩ
Maximum Input Level (pk-pk)	35	–	–	80%	AV_{DD}
Load Resistance (feedback pins)		80	–	–	kΩ
Amplifier Open Loop Voltage Gain (I/P = 1mV rms at 100Hz)		–	80	–	dB
Unity Gain Bandwidth		–	1.0	–	MHz
Programmable Input Gain Stage	36				
Gain (at 0dB)	37	−0.5	0	+0.5	dB
Cumulative Gain Error (wrt attenuation at 0dB)	37	−1.0	0	+1.0	dB

Notes:

31 Timing for an external input to the XTAL/CLK pin.

32 XTAL/CLK input driven by an external source.

33 6.144MHz XTAL fitted and 6.144MHz output selected (scale for 19.2MHz).

34 With no external components connected, measured at DC.

35 Centered about $AV_{DD}/2$; after multiplying by the gain of input circuit (with external components connected).

36 Gain applied to signal at output of buffer amplifier: DISCFB, ALTFB or MICFB

37 Design Value. Overall attenuation input to output has a tolerance of 0dB ±1.0dB

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 and Audio Output (MOD 1, MOD 2, AUDIO)					
Power-up to Output Stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ
Audio Attenuator					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)		−1.0	0	+1.0	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output Current Range (AV_{DD} = 3.3V)		–	–	±125	µA
Output Voltage Range	44	0.5	–	AV_{DD} –0.5	V
Load Resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centered about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Conversion Time	52	–	250	–	µs
Input Impedance					
Resistance	57	–	>10	–	MΩ
Capacitance		–	5	–	pF
Zero Error	55	0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero Error	56	0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

52 With an auxiliary clock frequency of 6.144MHz.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

55 Input offset from a nominal V_{BIAS} input, which produces a $0200 ADC output.

56 Output offset from a $0200 DAC input, measured wrt a nominal V_{BIAS} output.

57 Measured at DC.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
RF Synthesisers – Phase Locked Loops	61				
Reference Clock Input					
Input Logic 1	62	70%	–	–	RFV_{DD}
Input Logic 0	62	–	–	30%	RFV_{DD}
Frequency	64, 66	5.0	19.2	40.0	MHz
Divide Ratios (R)	63	2	–	8191	
Each RF Synthesiser	69				
Comparison Frequency		–	–	500	kHz
Input Frequency Range	67	100	–	600	MHz
Input Level (at 600MHz)		−15	–	0	dBm
Input Slew Rate		14	–	–	V/µs
Divide Ratios (N)		1024	–	1048575	
1Hz Normalised Phase Noise Floor	68	–	−197	–	dBc/Hz
Charge Pump Current (I_{CP}) (high)	65	±1.88	±2.5	±3.3	mA
Charge Pump Current (I_{CP}) (low)	65	±470	±625	±820	µA
Charge Pump Current – voltage variation		–	10%	–	per V
Charge Pump Current – sink to source match		–	5%	–	of I_{CP}

Notes:

61 Parameters only guaranteed for the L9 package.

62 Square wave input.

63 Separate dividers are provided for each PLL.

64 For optimum performance of the synthesiser subsystems, a common master clock should be used for the RF Synthesisers and the baseband sections. Using unsynchronised clocks is likely to result in spurious products being generated in the synthesiser outputs and in some cases difficulty may be experienced in obtaining lock in the RF Synthesisers.

65 External ISET resistor (R31) = 0Ω (Internal ISET resistor = 9k6Ω nominally).

66 Lower input frequencies may be used subject to division ratio requirements being maintained.

67 Operation outside these frequency limits is possible, but not guaranteed. At lower frequencies slew rate needs to be considered.

68 1Hz Normalised Phase Noise Floor (PN1Hz) can be used to calculate the phase noise within the PLL loop by:
Phase Noise (in-band) = $PN1Hz + 20\log_{10}(N) + 10\log_{10}(f_{comparison})$

69 It is recommended that RF Synthesiser 1 be used for the higher frequency use (eg: RF 1st LO) and RF Synthesiser 2 be used for lower frequency use (eg: IF LO).

8.1.4 Parametric Performance

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Oscillator Frequency = 19.2MHz ±0.01% (100ppm); Tamb = –40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mVrms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.
Input stage gain = 0dB, Output stage attenuation = 0dB.
All figures quoted in this section apply to the device when loaded with FI-1.x only. The use of other Function Images, can modify the parametric performance of the device.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Modem symbol rate		2400	–	4800	symbols /sec
Modulation			4FSK		
Filter (RC) Alpha		–	0.2	–	
Tx Output Level (MOD1, MOD2, 2-point)	70	–	2.88	–	Vpk-pk
Tx Output Level (MOD1, MOD2, I/Q)	70	–	2.20	–	Vpk-pk
Tx Adjacent Channel Power (MOD1, MOD2, prbs)	71, 73	-60	–	–	dB
Rx Sensitivity (BER 4800 symbols/sec)	72	–	TBD	–	dBm
Rx Co-channel Rejection	71, 73	15	12	–	dB
Rx Input Level		–	–	838	mVrms
Rx Input DC Offset		0.5	–	AV_{DD} - 0.5	V

Notes:

70	Transmitting continuous default preamble.
71	See user manual section 7.14.
72	Measured at baseband – radio design will affect ultimate product performance.
73	For a 6.25kHz/4800bps channel.

8.2 C-BUS Timing

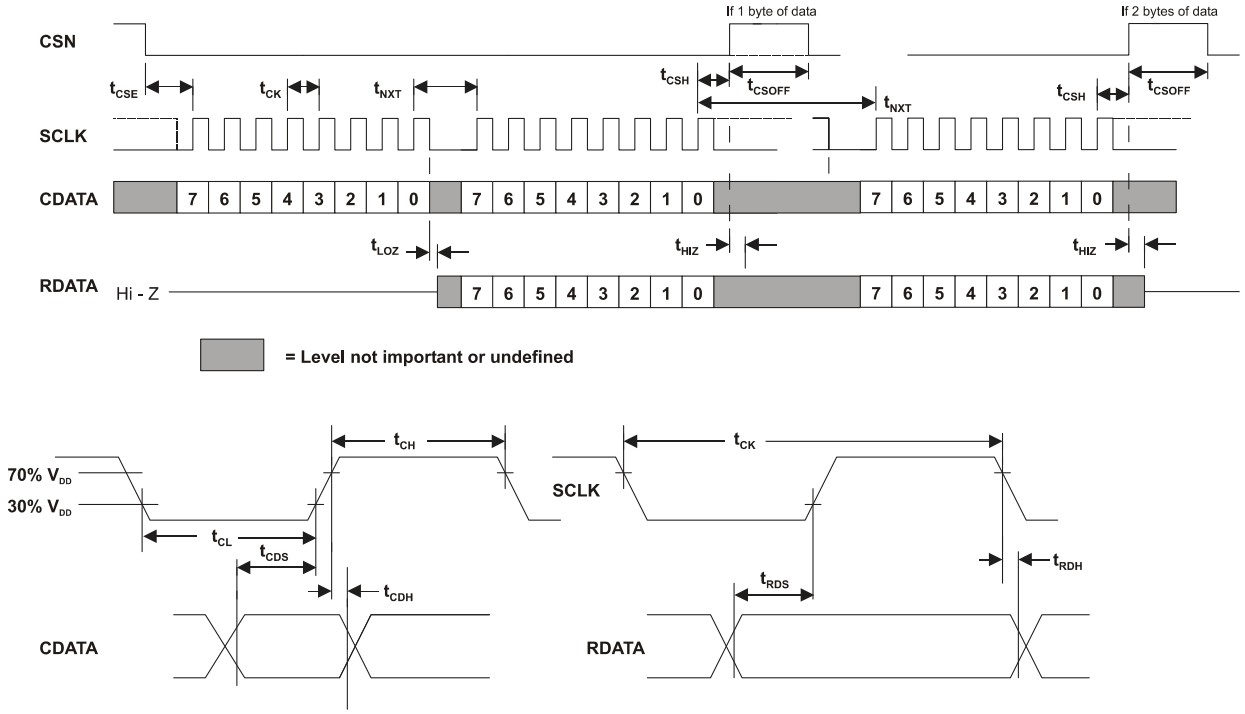


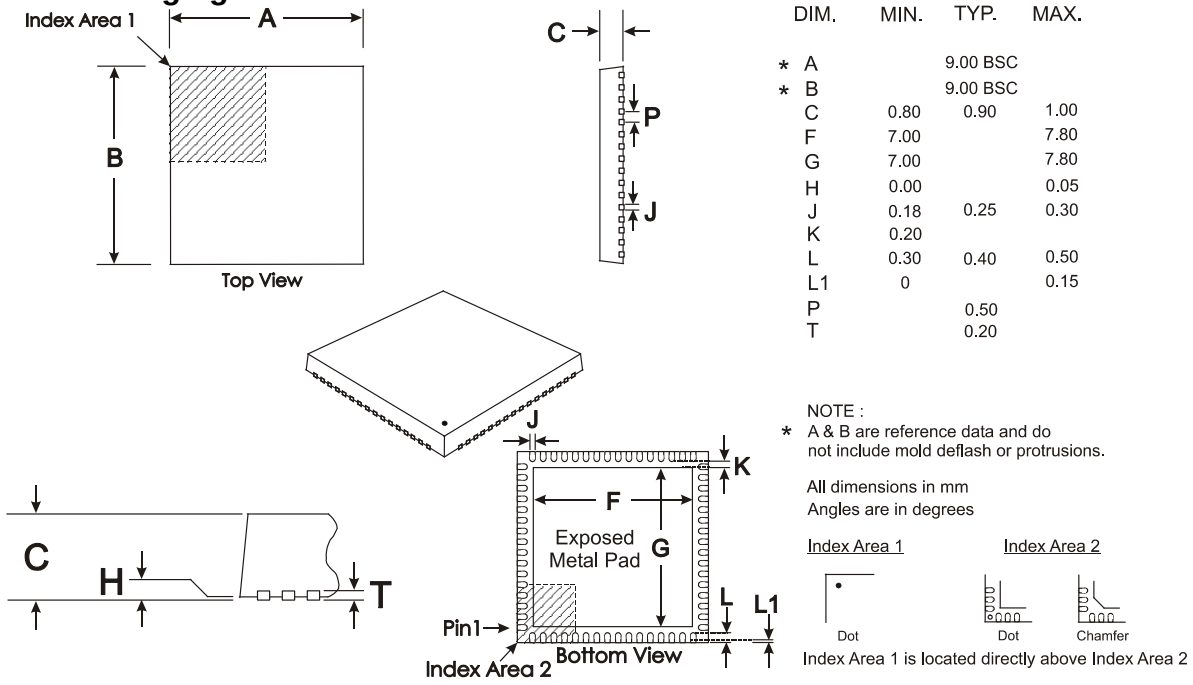
Figure 23 C-BUS Timing

C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SCLK high time		100	–	–	ns
t_{CSH}	Last SCLK high to CSN high time		100	–	–	ns
t_{LOZ}	SCLK low to RDATA Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to RDATA high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SCLK cycle time		200	–	–	ns
t_{CH}	SCLK high time		100	–	–	ns
t_{CL}	SCLK low time		100	–	–	ns
t_{CDS}	CDATA setup time		75	–	–	ns
t_{CDH}	CDATA hold time		25	–	–	ns
t_{RDS}	RDATA setup time		50	–	–	ns
t_{RDH}	RDATA hold time		0	–	–	ns

Notes:
1. Depending on the command, 1 or 2 bytes of CDATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. RDATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SCLK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SCLK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7131/CMX7141 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

8.3 Packaging.



	DIM.	MIN.	TYP.	MAX.
*	A		9.00 BSC	
*	B		9.00 BSC	
	C	0.80	0.90	1.00
	F	7.00		7.80
	G	7.00		7.80
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

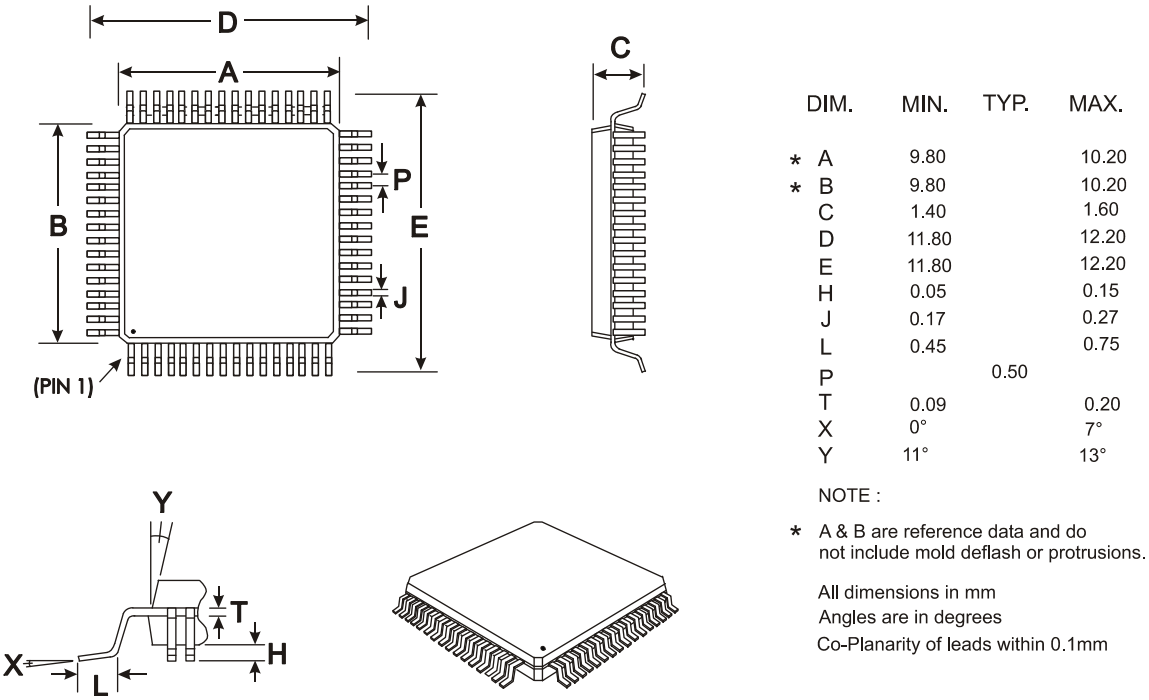
NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 24 Mechanical Outline of 64-pin VQFN (Q1)

Order as part no. CMX7131Q1



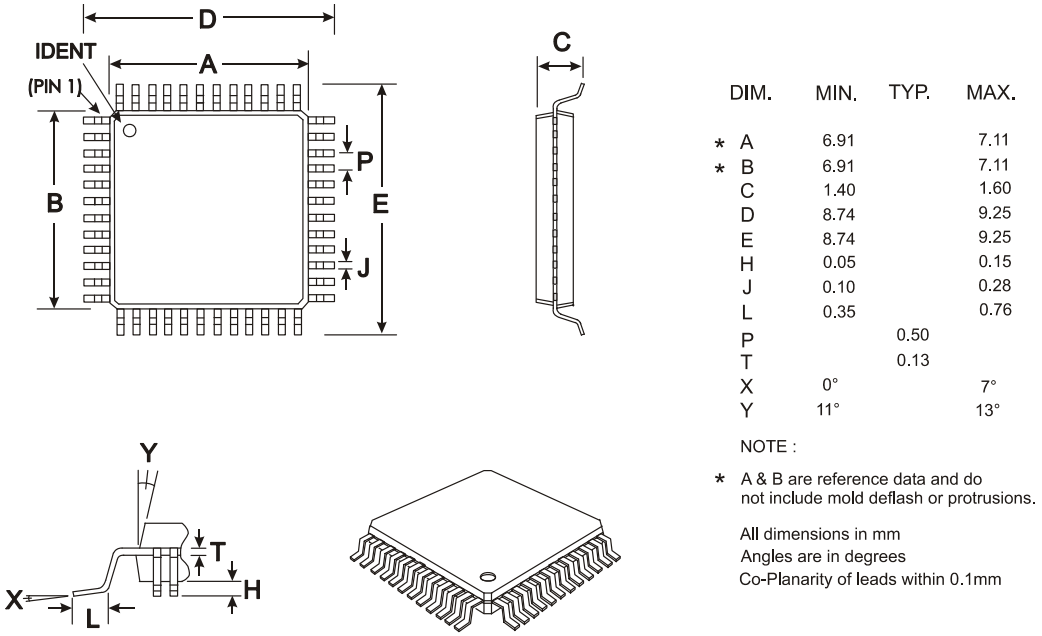
	DIM.	MIN.	TYP.	MAX.
*	A	9.80		10.20
*	B	9.80		10.20
	C	1.40		1.60
	D	11.80		12.20
	E	11.80		12.20
	H	0.05		0.15
	J	0.17		0.27
	L	0.45		0.75
	P		0.50	
	T	0.09		0.20
	X	0°		7°
	Y	11°		13°

NOTE :
* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 25 Mechanical Outline of 64-pin LQFP (L9)

Order as part no. CMX7131L9



	DIM.	MIN.	TYP.	MAX.
*	A	6.91		7.11
*	B	6.91		7.11
	C	1.40		1.60
	D	8.74		9.25
	E	8.74		9.25
	H	0.05		0.15
	J	0.10		0.28
	L	0.35		0.76
	P		0.50	
	T		0.13	
	X	0°		7°
	Y	11°		13°

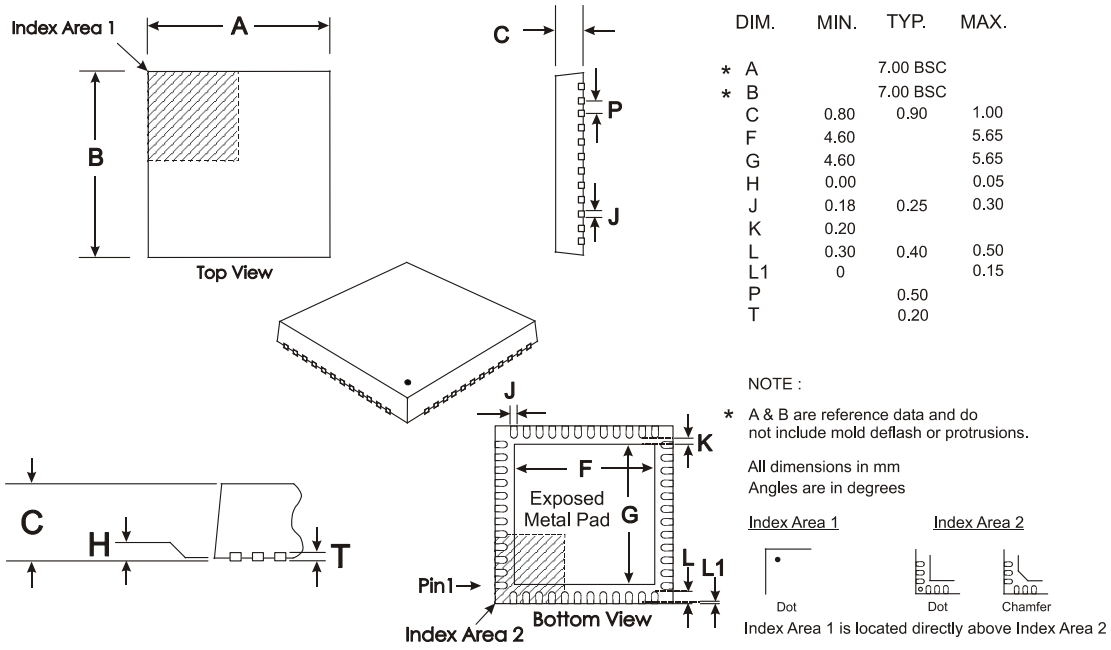
NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees
Co-Planarity of leads within 0.1mm

Figure 26 Mechanical Outline of 48-pin LQFP (L4)

Order as part no. CMX7141L4



	DIM.	MIN.	TYP.	MAX.
*	A		7.00 BSC	
*	B		7.00 BSC	
	C	0.80	0.90	1.00
	F	4.60		5.65
	G	4.60		5.65
	H	0.00		0.05
	J	0.18	0.25	0.30
	K	0.20		
	L	0.30	0.40	0.50
	L1	0		0.15
	P		0.50	
	T		0.20	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Index Area 1 Index Area 2

Index Area 1 is located directly above Index Area 2

Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 27 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7141Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Design Support/Package Information page of the CML website: [www.cmlmicro.com].

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