

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 24×24-bit digital multiplier integrated circuit.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
–1	ADSP-1024ASG/883B
–2	ADSP-1024ATG/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline: G-84A.

1.3 Absolute Maximum Ratings.

Supply Voltage	–0.3 V to 7 V
Input Voltage	–0.3 V to V_{DD}
Output Voltage	–0.3 V to V_{DD}
Operating Temperature Range (Ambient)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	+300°C

1.5 Thermal Characteristics.

Maximum Thermal Resistance θ_{JC} : see MIL-M-38510, Appendix C.

ADSP-1024A – SPECIFICATIONS

Test	Symbol	Device	Design Limit @ +25°C	Sub Group 1	Sub Group 2, 3	Sub Group 9	Sub Group 10, 11	Test Condition ¹	Units
Digital Input High Voltage	V _{IH}	–1, 2	2.2 *	2.2	2.2			V _{DD} = max	V min
Digital Input Low Voltage	V _{IL}	–1, 2	0.8	0.8	0.8			V _{DD} = min	V max
Digital Output High Voltage	V _{OH}	–1, 2	2.4	2.4	2.4			V _{DD} = min I _{OH} = –4.0 mA	V min
Digital Output Low Voltage	V _{OL}	–1, 2	0.6	0.6	0.6			V _{DD} = min I _{OL} = +4.0 mA	V max
Digital Input High Current	I _{IH}	–1, 2	10	10	10			V _{DD} = max V _{IN} = +5.0 V	μA max
Digital Input Low Current	I _{IL}	–1, 2	10	10	10			V _{DD} = max V _{IN} = 0.0 V	μA max
Three-State Leakage Current Low	I _{OZL}	–1, 2	50	50	50			V _{DD} = max V _{IL} = 0 V (High Z)	μA max
Three-State Leakage Current High	I _{OZH}	–1, 2	50	50	50			V _{DD} = max V _{IH} = max (High Z)	μA max
Supply Current*	I _{DD1}	–1, 2	75	90	90			V _{DD} = max; TTL Inputs; f = max	mA max
	I _{DD2}								

ADSP-1024A

3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (105).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).

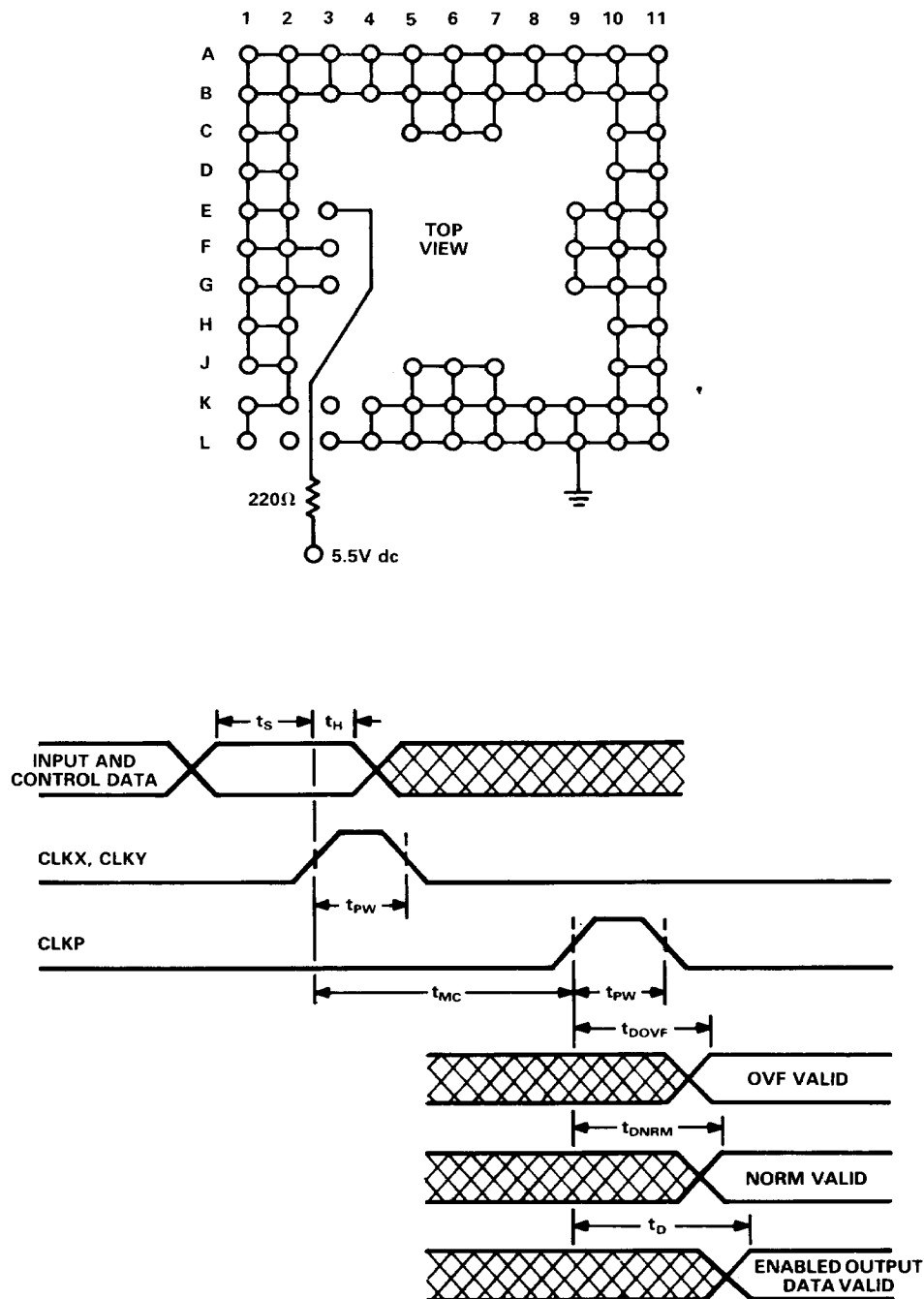


Figure 1. ADSP-1024A Timing Diagram

REV. B

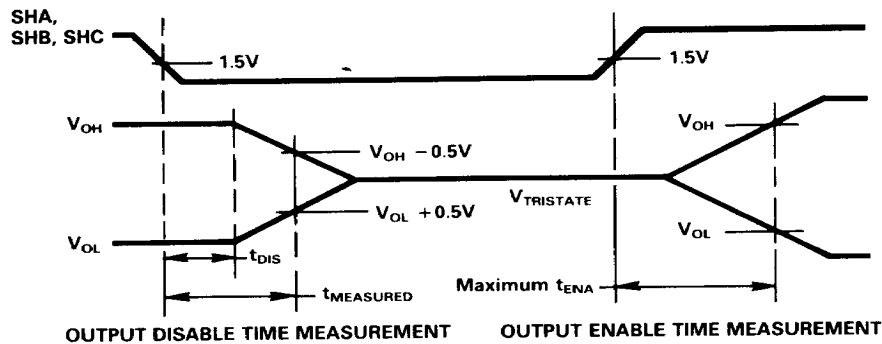


Figure 2. Three-State Disable and Enable Timing

Output disable time, t_{DIS} , is measured from the time the output enable control signal reaches 1.5 V to the time when all outputs have ceased driving. This is calculated by measuring the time, $t_{MEASURED}$, from the same starting point to when the output voltages have changed by 0.5 V toward +1.5 V. From the tester capacitive loading, C_L , and the measured current, i_L , the decay time, t_{DECAY} , can be approximated to first order by:

$$t_{DECAY} = \frac{C_L \cdot 0.5 \text{ V}}{i_L}$$

from which

$$t_{DIS} = t_{MEASURED} - t_{DECAY}$$

is calculated. Disable times are longest at the highest specified temperature.

The maximum output enable time, maximum t_{ENA} , is also measured from output enable control signal at 1.5 V to the time when all outputs have reached TTL input levels (V_{OH} or V_{OL}). This could also be considered as "data valid." Maximum enable times are longest at the highest specified temperature.

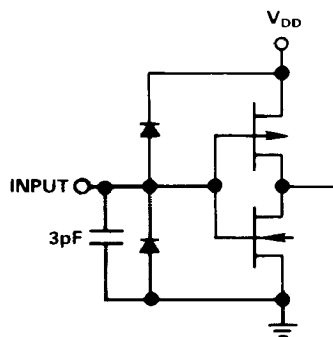


Figure 3. Equivalent Input Circuit

