REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to standardized military drawing format. Technical changes to table I. Editorial changes throughout.	89-11-16	M.A. Frye
B	Technical changes in 1.4 and table I. Editorial changes throughout.	91-12-16	M.A. Frye

CURRENT CAGE CODE 67268

REV																			
SHEET																			
REV	B	B	B																
SHEET	14	15	16																

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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CHECKED BY: Monica L. Poelking

APPROVED BY: Michael A. Frye

DRAWING APPROVAL DATE
14 JANUARY 1987

REVISION LEVEL
B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, HIGH-SPEED CMOS, MULTIVIBRATOR, DUAL, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-86847
A	14933	

SHEET 1 OF 16

DESC FORM 193-1
JUL 91

Use previous edition until exhausted.

5962-E31

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number. The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC123	Dual retriggerable monostable multivibrator
02	54HC123A	Dual retriggerable monostable multivibrator

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, .840" x .310" x .200"), dual-in-line package
2	C-2 (20-terminal, .358" x .358" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range	-0.5 V dc to V_{CC}
DC output voltage range	-0.5 V dc to V_{CC}
Clamp diode current	±20 mA
DC output current (per pin)	±25 mA
DC V_{CC} or GND current (per pin)	±50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 2/	500 mW
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+2.0 V dc to +6.0 V dc
Input voltage range (V_{IN})	0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	0.0 V dc to V_{CC}
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time:	
T_C = -55°C to +125°C:	
V_{CC} = 2.0 V	0 to 1000 ns
V_{CC} = 4.5 V	0 to 500 ns
V_{CC} = 6.0 V	0 to 400 ns

1/ Unless otherwise specified, all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C

Minimum triggering pulse width, $\overline{An}$, Bn, or $\overline{clear}$ ($\overline{CLRn}$) (t_W):
T_C = +25°C:
V_{CC} = 2.0 V dc - - - - - - - - - - - - - - - - - 123 ns
V_{CC} = 4.5 V dc - - - - - - - - - - - - - - - - - 30 ns
V_{CC} = 6.0 V dc - - - - - - - - - - - - - - - - - 21 ns
T_C = -55°C, +125°C:
V_{CC} = 2.0 V dc - - - - - - - - - - - - - - - - - 157 ns
V_{CC} = 4.5 V dc - - - - - - - - - - - - - - - - - 42 ns
V_{CC} = 6.0 V dc - - - - - - - - - - - - - - - - - 30 ns

Minimum output pulse width ($t_{WQ(MIN)}$), device type 01:
T_C = +25°C, C_{EXT} = 10 nF:
V_{CC} = 5.0 V dc, R_{EXT} = 10 kΩ - - - - - - - - - 40 µs to 50 µs

Minimum output pulse width ($t_{WQ(MIN)}$), device type 02:
T_C = +25°C, C_{EXT} = 28 pF:
V_{CC} = 2.0 V dc, R_{EXT} = 6 kΩ - - - - - - - - - 0.85 µs
V_{CC} = 4.5 V dc, R_{EXT} = 2 kΩ - - - - - - - - - 220 ns
V_{CC} = 6.0 V dc, R_{EXT} = 2 kΩ - - - - - - - - - 170 ns

Minimum removal time, $\overline{CLRn}$ to $\overline{An}$, $\overline{CLRn}$ to Bn (t_{REM}), device type 01:
T_C = -55°C to +125°C:
V_{CC} = 2.0 V dc - - - - - - - - - - - - - - - - - 75 ns
V_{CC} = 4.5 V dc - - - - - - - - - - - - - - - - - 15 ns
V_{CC} = 6.0 V dc - - - - - - - - - - - - - - - - - 13 ns

Minimum removal time, $\overline{CLRn}$ to $\overline{An}$, $\overline{CLRn}$ to Bn (t_{REM}), device type 02:
T_C = -55°C to +125°C:
V_{CC} = 2.0 V dc - - - - - - - - - - - - - - - - - 0 ns
V_{CC} = 4.5 V dc - - - - - - - - - - - - - - - - - 0 ns
V_{CC} = 6.0 V dc - - - - - - - - - - - - - - - - - 0 ns

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawing (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections and timing component. The terminal connections and timing component shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
High level output voltage 2/	V_{OH}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 20\ \mu A$	$V_{CC} = 2.0$ V	All	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V			4.4		
			$V_{CC} = 6.0$ V			5.9		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V			3.7		
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V			5.2		
Low level output voltage 2/	V_{OL}	$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert = 20\ \mu A$	$V_{CC} = 2.0$ V	All	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V				0.1	
			$V_{CC} = 6.0$ V				0.1	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert = 4.0$ mA	$V_{CC} = 4.5$ V				0.4	
		$V_{IN} = V_{IH}$ minimum or V_{IL} maximum $\lvert I_O \rvert = 5.2$ mA	$V_{CC} = 6.0$ V				0.4	
High level input voltage 3/	V_{IH}		$V_{CC} = 2.0$ V	All	1, 2, 3	1.5		V
			$V_{CC} = 4.5$ V			3.15		
			$V_{CC} = 6.0$ V			4.2		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
Low level input voltage 3/	V_{IL}		V_{CC} = 2.0 V	01	1, 2, 3		0.5	V
			V_{CC} = 4.5 V				1.35	
			V_{CC} = 6.0 V				1.8	
			V_{CC} = 2.0 V	02			0.3	
			V_{CC} = 4.5 V				0.9	
			V_{CC} = 6.0 V				1.2	
Quiescent supply current (standby)	I_{CC1}	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ µA	V_{CC} = 6.0 V	All	1, 2, 3		160	µA
Active supply current (per monostable)	I_{CC2}	$V_{IN} = V_{CC}$ or GND $R/C_{EXT} = V_{CC}/4$ 4/ 5/	V_{CC} = 2.0 V	01	1, 2, 3		130	µA
			V_{CC} = 4.5 V				1.6	mA
			V_{CC} = 6.0 V				3.2	
		$V_{IN} = V_{CC}$ or GND $R/C_{EXT} = 0.5\ V_{CC}$	V_{CC} = 2.0 V	02	1, 2, 3		130	µA
			V_{CC} = 4.5 V				1.6	mA
			V_{CC} = 6.0 V				3.2	
Input current	I_{IN}	V_{CC} = 6.0 V $V_{IN} = V_{CC}$ (R/C_{EXT}) 6/ V_{IN} = GND (R/C_{EXT}) 6/ $V_{IN} = V_{CC}$ (all other pins) V_{IN} = GND (all other pins)		All	1, 2, 3		5.0 -5.0 1.0 -1.0	µA
Functional tests		See 4.3.1d			7, 8			

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
Trigger propagation delay time (An to Qn, Bn to Qn, CLRn to Qn) 2/	t_{PLH1}	C_L = 50 pF minimum See figure 4	V_{CC} = 2.0 V	01	9		300	ns
				02			169	
			V_{CC} = 4.5 V	01			60	
				02			42	
			V_{CC} = 6.0 V	01			51	
				02			32	
			V_{CC} = 2.0 V	01	10, 11		450	ns
				02			210	
			V_{CC} = 4.5 V	01			90	
				02			57	
			V_{CC} = 6.0 V	01			76	
				02			44	
Trigger propagation delay time (An to Qn, Bn to Qn, CLRn to Qn) 2/	t_{PHL1}		V_{CC} = 2.0 V	01	9		320	ns
				02			197	
			V_{CC} = 4.5 V	01			64	
				02			48	
			V_{CC} = 6.0 V	01			54	
				02			38	
			V_{CC} = 2.0 V	01	10, 11		480	ns
				02			250	
			V_{CC} = 4.5 V	01			96	
				02			67	
			V_{CC} = 6.0 V	01			82	
				02			51	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay CLRn to Qn 2/	t_{PHL2}	C_L = 50 pF minimum See figure 4	V_{CC} = 2.0 V	01	9		215	ns
				02			114	
			V_{CC} = 4.5 V	01			43	
				02			34	
			V_{CC} = 6.0 V	01			37	
				02			28	
			V_{CC} = 2.0 V	01	10, 11		325	
				02			143	
			V_{CC} = 4.5 V	01			65	
				02			45	
			V_{CC} = 6.0 V	01			55	
				02			36	
Propagation delay CLRn to Qn 2/	t_{PLH2}		V_{CC} = 2.0 V	01	9		215	
				02			116	
			V_{CC} = 4.5 V	01			43	
				02			36	
			V_{CC} = 6.0 V	01			37	
				02			29	
			V_{CC} = 2.0 V	01	10, 11		325	
				02			147	
			V_{CC} = 4.5 V	01			65	
				02			46	
			V_{CC} = 6.0 V	01			55	
				02			37	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Output pulse width (standby) 2/ 5/	t_{WQ}	C_L = pF minimum R_{EXT} = 10 kΩ C_{EXT} = 0.1 µF See figure 4	V_{CC} = 5.0 V	01	9	0.4	0.5	ms
			V_{CC} = 4.5 V	02		0.9	1.2	
			V_{CC} = 5.0 V	01	10, 11	0.38	0.52	ms
			V_{CC} = 4.5 V	02		0.70	1.15	
Output rise and fall time 5/	t_{THL}, t_{TLH}	C_L = 50 pF minimum See figure 4	V_{CC} = 2.0 V	All	9		75	ns
			V_{CC} = 4.5 V				15	
			V_{CC} = 6.0 V				13	
			V_{CC} = 2.0 V	All	10, 11		110	ns
			V_{CC} = 4.5 V				22	
			V_{CC} = 6.0 V				19	
Maximum input capacitance	C_{IN}	R/C_{EXT}	See 4.3.1c	All	4		20	pF
		Other inputs					10	

1/ For a power supply of 5.0 V ±10 %, the worst case output voltage (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus, the 4.5 V values should be used when designing with this supply. Worst case V_{IN} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V). The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage so the 6.0 V values should be used. Power dissipation capacitance (C_{PD}), typically 80 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

2/ Testing at V_{CC} = 2.0 V and V_{CC} = 6.0 V shall be guaranteed, if not tested, to the specified limit in table I.

3/ V_{IH} and V_{IL} tests are not required if applied as forcing functions for the V_{OH} and V_{OL} tests.

4/ Limit current to I_{OL} or use a suitable series resistor ≥ 500Ω; perform test while Q is high.

5/ Guaranteed, if not tested, to the specified limits in table I.

6/ When testing I_{IL}, the Q output must be high, if Q is low (device not triggered) the pull-up P device will be on and the low resistance path from V_{DD} to the test pin will cause a current far exceeding the specification.

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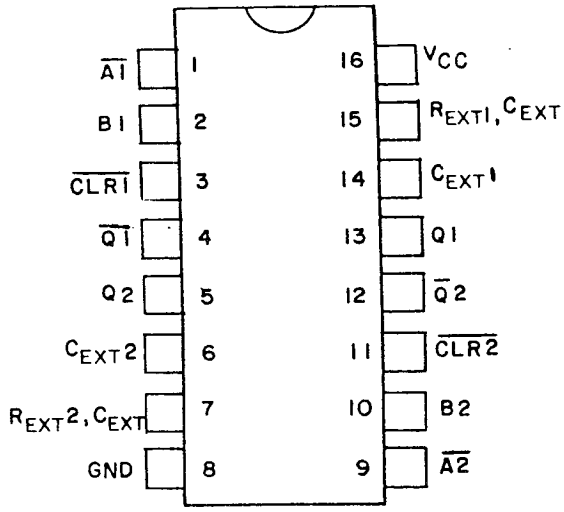
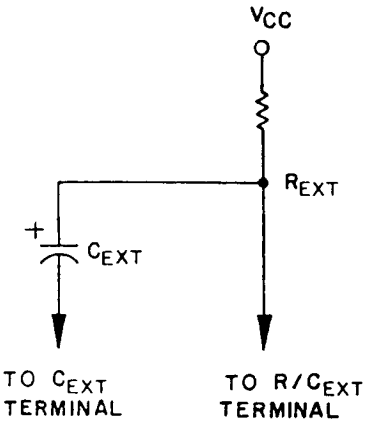
Case E



Timing component



Case 2

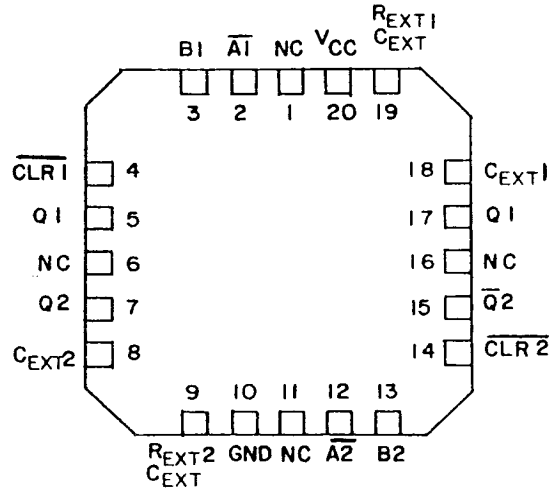


FIGURE 1. Terminal connections and timing component.

Inputs			Outputs	
$\overline{CLRn}$	$\overline{An}$	Bn	Qn	$\overline{Qn}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⎎ = One low level pulse
X = Irrelevant

FIGURE 2. Truth table.

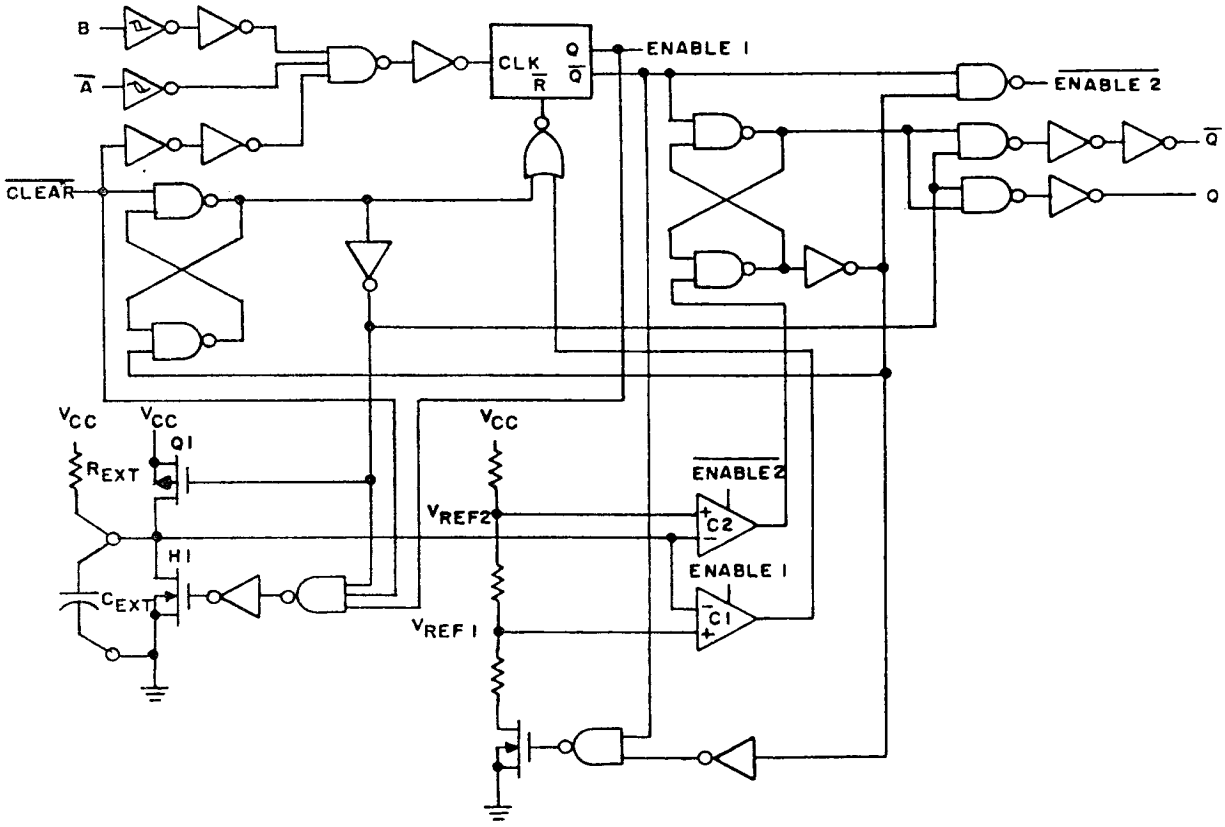
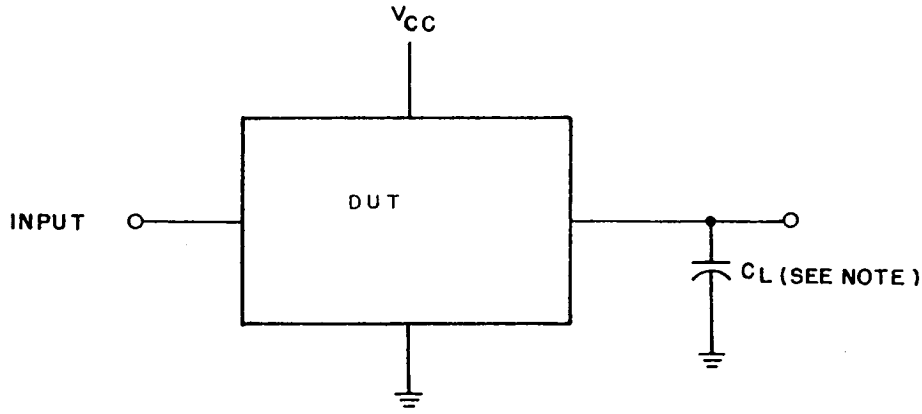
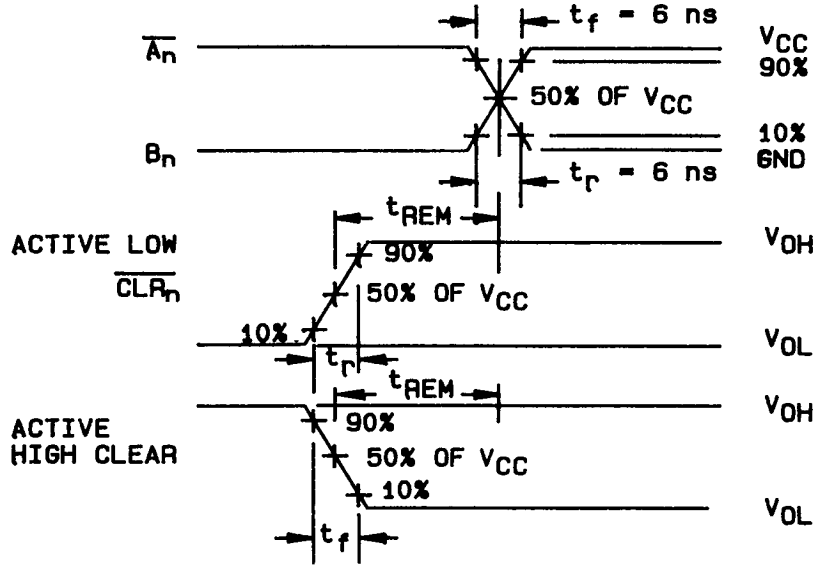


FIGURE 3. Logic diagram.

Device types 01 and 02

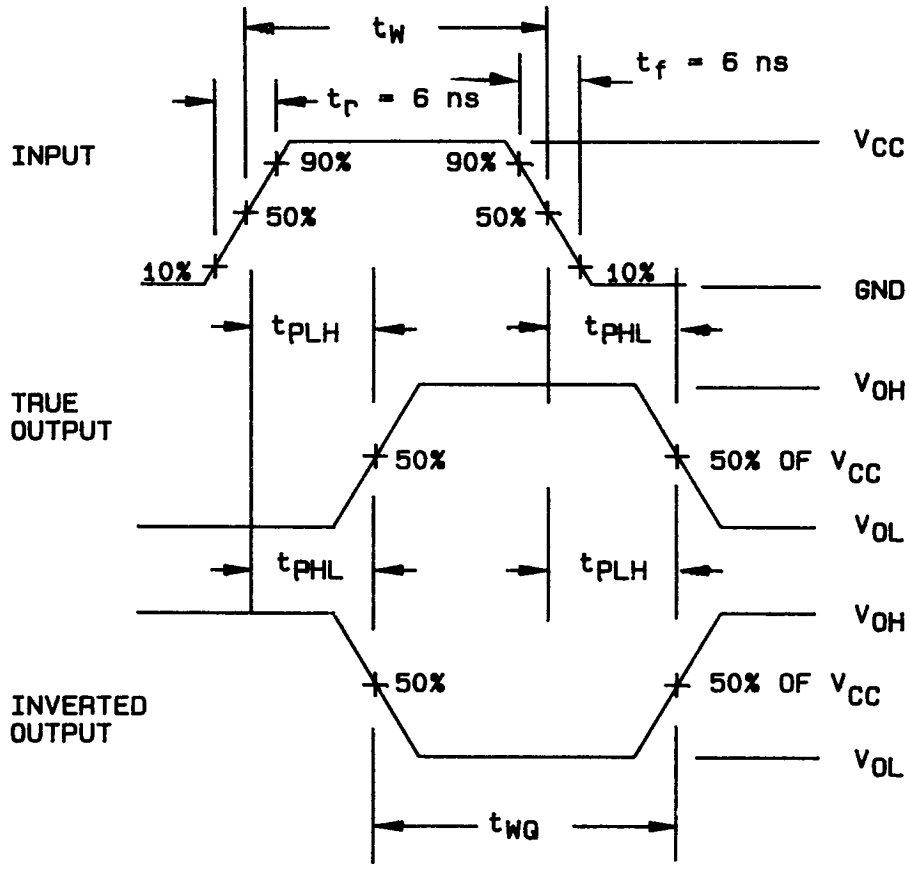


NOTE: C_L = 50 pF minimum, includes load and test jig capacitance ac test circuits.



REMOVAL TIME WAVEFORMS

FIGURE 4. Test circuit and switching waveforms.



PROPAGATION DELAY AND PULSE WIDTH WAVEFORMS

PROPAGATION DELAY AND PULSE WIDTH WAVEFORMS

FIGURE 4. Test circuit and switching waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

d. Subgroup 7 tests shall verify the truth table as specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test condition, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part specified in this drawing will be replaced by the microcircuit identified as PIN M38510/65901B--.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513) 296-6022.

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.