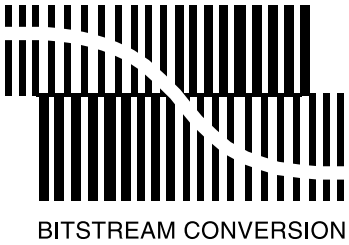
DATA SHEET



UDA1380

Stereo audio coder-decoder for MD, CD and MP3

Product specification
Supersedes data of 2003 Apr 04

2004 Apr 22

Stereo audio coder-decoder for MD, CD and MP3

UDA1380

CONTENTS

Stereo audio coder-decoder for MD, CD and MP3

UDA1380

1 FEATURES

1.1 General

- 2.4 to 3.6 V power supply
- 5 V tolerant digital inputs (at 2.7 to 3.6 V power supply)
- 24-bit data path for Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC)
- Selectable control via L3-bus microcontroller interface or I^2C-bus interface; choice of 2 device addresses in L3-bus and I^2C-bus mode

  Remark: This device does not have a static mode.
- Supports sample frequencies from 8 to 55 kHz for the ADC part, and 8 to 100 kHz for the DAC part. The ADC does not support DVD audio (96 kHz audio), only Mini-Disc (MD), Compact-Disc (CD) and Moving Picture Experts Group Layer-3 Audio (MP3). For playback 8 to 100 kHz is specified. DVD playback is supported
- Power management unit:
  - Separate power control for ADC, Automatic Volume Control (AVC), DAC, Phase Locked Loop (PLL) and headphone driver
  - Analog blocks like ADC and Programmable Gain Amplifier (PGA) have a block to power-down the bias circuits
  - When ADC and/or DAC are powered-down, the clocks to these blocks are also stopped to save power.

  Remark: By default, when the IC is powered-up, the complete chip will be in the Power-down mode.
- ADC part and DAC part can run at different frequencies, either system clock or Word Select PLL (WSPLL)
- ADC and PGA plus integrated high-pass filter to cancel DC offset
- The decimation filter is equipped with a digital Automatic Gain Control (AGC)
- Mono microphone input with Low Noise Amplifier (LNA) of 29 dB fixed gain and Variable Gain Amplifier (VGA) from 0 to 30 dB in steps of 2 dB
- Integrated digital filter plus DAC
- Separate single-ended line output and one stereo headphone output, capable of driving a 16 Ω load. The headphone driver has a built-in short-circuit protection with status bits which can be read out from the L3-bus or I^2C-bus interface
- Digital silence detection in the interpolator (playback) with read-out status via L3-bus or I^2C-bus interface
- Easy application.

BITSTREAM CONVERSION

1.2 Multiple format data input interface

- Slave BCK and WS signals
- I^2S-bus format
- MSB-justified format compatible
- LSB-justified format compatible.

1.3 Multiple format data output interface

- Select option for digital output interface: either the decimator output (ADC signal) or the output signal of the digital mixer which is in the interpolator DSP
- Selectable master or slave BCK and WS signals for digital ADC output

  Remark: SYSCLK must be applied in WSPLL mode and master mode
- I^2S-bus format
- MSB-justified format compatible
- LSB-justified format compatible.

1.4 ADC front-end features

- ADC plus decimator can run at either WSPLL, regenerating the clock from WSI signal, or on SYSCLK
- Stereo line input with PGA: gain range from 0 to 24 dB in steps of 3 dB
- LNA with 29 dB fixed gain for mono microphone input, including VGA with gain from 0 to 30 dB in steps of 2 dB
- Digital left and right independent volume control and mute from +24 to −63.5 dB in steps of 0.5 dB.

1.5 DAC features

- DAC plus interpolator can run at either WSPLL (regenerating the clock from WSI) or at SYSCLK
- Separate digital logarithmic volume control for left and right channels via L3-bus or I²C-bus from 0 to −78 dB in steps of 0.25 dB
- Digital tone control, bass boost and treble via L3-bus or I²C-bus interface
- Digital de-emphasis for sample frequencies of: 32, 44.1, 48 and 96 kHz via L3-bus or I²C-bus interface
- Cosine roll-off soft mute function
- Output signal polarity control via L3-bus or I²C-bus interface
- Digital mixer for mixing ADC output signal and digital serial input signal, if they run at the same sampling frequency.

2 APPLICATIONS

This audio coder-decoder is suitable for home and portable applications like MD, CD and MP3 players.

3 GENERAL DESCRIPTION

The UDA1380 is a stereo audio coder-decoder, available in TSSOP32 (UDA1380TT) and HVQFN32 (UDA1380HN) packages. All functions and features are identical for both package versions. The term ‘UDA1380’ in this document refers to both UDA1380TT and UDA1380HN, unless particularly specified.

The front-end of the UDA1380 is equipped with a stereo line input, which has a PGA control, and a mono microphone input with an LNA and a VGA. The digital decimation filter is equipped with an AGC which can be used in case of voice-recording.

The DAC part is equipped with a stereo line output and a headphone driver output. The headphone driver is capable of driving a 16 Ω load. The headphone driver is also capable of driving a headphone without the need for external DC decoupling capacitors, since the headphone can be connected to a pin $V_{REF(HP)}$ on the chip.

In addition, there is a built-in short-circuit protection for the headphone driver output which, in case of short-circuit, limits the current through the operational amplifiers and signals the event via its L3-bus or I²C-bus register.

The UDA1380 also supports an application mode in which the coder-decoder itself is not running, but an analog signal, for instance coming from an FM tuner, can be controlled in gain and applied to the output via the headphone driver and line outputs.

The UDA1380 supports the I²S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 18, 20 or 24 bits (LSB-justified 24 bits is only supported for the output interface).

The UDA1380 has sound processing features in playback mode, de-emphasis, volume, mute, bass boost and treble which can be controlled by the L3-bus or I²C-bus interface.

4 QUICK REFERENCE DATA

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = V_{DDA(HP)} = 3.0$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
$V_{DDA(AD)}$	ADC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(DA)}$	DAC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(HP)}$	headphone analog supply voltage	note 1	2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
$I_{DDA(AD)}$	ADC analog supply current	one ADC and microphone amplifier enabled; $f_s = 48$ kHz	–	4.5	–	mA
		two ADCs and PGA enabled; $f_s = 48$ kHz	–	7.0	–	mA
		all ADCs and PGAs power-down, but AVC activated; $f_s = 48$ kHz	–	3.3	–	mA
		all ADCs, PGAs and LNA power-down; $f_s = 48$ kHz	–	1.0	–	μA
$I_{DDA(DA)}$	DAC analog supply current	operating mode; $f_s = 48$ kHz	–	3.4	–	mA
		Power-down mode; $f_s = 48$ kHz	–	0.1	–	μA
$I_{DDA(HP)}$	headphone analog supply current	no signal applied (quiescent current)	–	0.9	–	mA
		Power-down mode	–	0.1	–	μA
I_{DDD}	digital supply current	operating mode; $f_s = 48$ kHz	–	10.0	–	mA
		playback mode; $f_s = 48$ kHz	–	5.0	–	mA
		record mode; $f_s = 48$ kHz	–	6.0	–	mA
		Power-down mode; $f_s = 48$ kHz	–	1.0	–	μA
$I_{DD(tot)}$	total supply current	playback mode (without headphone); $f_s = 48$ kHz	–	8	–	mA
		playback mode (with headphone); no signal; $f_s = 48$ kHz	–	9	–	mA
		record mode (audio); $f_s = 48$ kHz	–	13	–	mA
		record mode (speech); $f_s = 48$ kHz	–	10	–	mA
		record mode (audio and speech); $f_s = 48$ kHz	–	13	–	mA
		fully operating; $f_s = 48$ kHz	–	23	–	mA
		signal mix-in operating, using FSDAC, AVC (with headphone); no signal; $f_s = 48$ kHz	–	12	–	mA
		Power-down mode; $f_s = 48$ kHz	–	2	–	μA
T_{amb}	ambient temperature		−40	–	+85	°C

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter (supply voltage 3.0 V)						
D_o	digital output level	at 0 dB setting; $V_{i(rms)}$ = 1.0 V	−1.5	−1	−0.5	dBFS
(THD+N)/S_{48}	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at −1 dBFS	−	−85	−80	dB
		at −60 dBFS; A-weighted	−	−37	−32	dB
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	V_i = 0 V; A-weighted	92	97	−	dB
α_{cs}	channel separation		−	100	−	dB
LNA input plus analog-to-digital converter (supply voltage 3.0 V)						
$V_{i(rms)}$	input voltage (RMS value)	at 0 dBFS digital output; 2.2 kΩ source impedance	−	−	35	mV
(THD+N)/S_{48}	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at 0 dB	−	−74	−	dB
		at −60 dB; A-weighted	−	−25	−	dB
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	V_i = 0 V; A-weighted	−	85	−	dB
α_{cs}	channel separation		−	70	−	dB
Digital-to-analog converter (supply voltage 3.0 V)						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input; note 2	−	0.9	−	V
(THD+N)/S_{48}	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at 0 dB	−	−85	−80	dB
		at −60 dB; A-weighted	−	−40	−35	dB
(THD+N)/S_{96}	total harmonic distortion-plus-noise to signal ratio at f_s = 96 kHz	at 0 dB	−	−80	−75	dB
		at −60 dB; A-weighted	−	−37	−32	dB
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	code = 0; A-weighted	95	100	−	dB
S/N_{96}	signal-to-noise ratio at f_s = 96 kHz	code = 0; A-weighted	92	97	−	dB
α_{cs}	channel separation		−	90	−	dB
AVC (line input via ADC input; output on line output and headphone driver; supply voltage 3.0 V)						
$V_{i(rms)}$	input voltage (RMS value)		−	150	−	mV
(THD+N)/S_{48}	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at 0 dB	−	−80	−	dB
		at −60 dB; A-weighted	−	−28	−	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	V_i = 0 V; A-weighted	–	87	–	dB
Headphone driver (supply voltage 3.0 V)						
$P_{o(rms)}$	output power (RMS value)	at 0 dBFS digital input; R_L = 16 Ω	30	35	40	mW
(THD+N)/S_{48}	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at 0 dB; R_L = 16 Ω; note 1	–	–60	–52	dB
		at 0 dB; R_L = 5 kΩ	–	–82	–77	dB
		at –60 dB; A-weighted	–	–33	–27	dB
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	code = 0; A-weighted	87	93	–	dB
α_{cs}	channel separation	R_L = 16 Ω using pin $V_{REF(HP)}$; no DC decoupling capacitors; note 3	55	60	–	dB
		R_L = 16 Ω single-ended application with DC decoupling capacitors (100 μF typical)	63	68	–	dB
		R_L = 32 Ω single-ended application with DC decoupling capacitors (100 μF typical)	69	74	–	dB
Power consumption (supply voltage 3.0 V; f_s = 48 kHz)						
P_{tot}	total power dissipation	playback mode (without headphone)	–	24	–	mW
		playback mode (with headphone)	–	27	–	mW
		record mode (audio)	–	39	–	mW
		record mode (speech)	–	30	–	mW
		record mode (audio and speech)	–	40	–	mW
		full operation	–	69	–	mW
		Power-down mode	–	6	–	μW

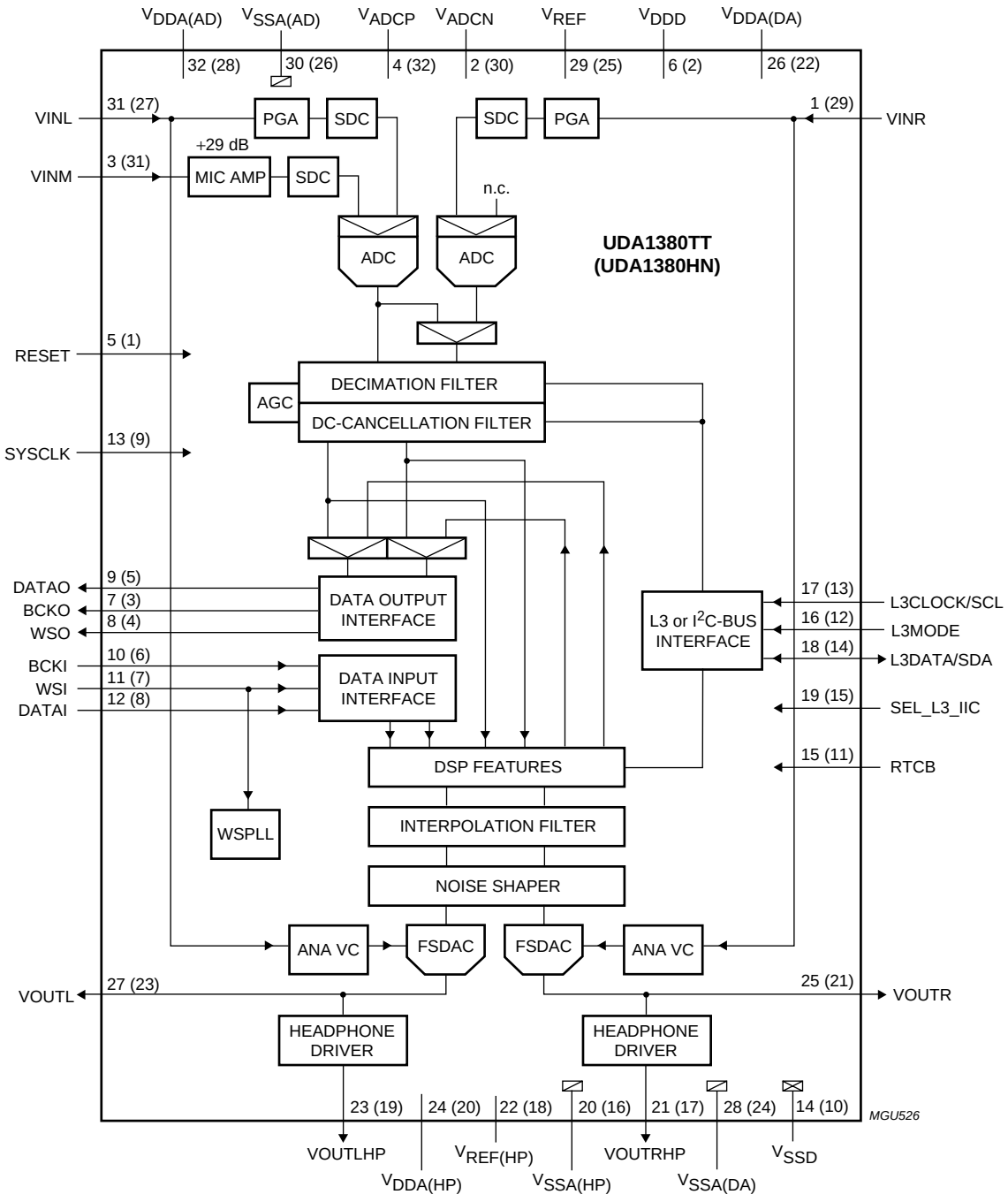
Notes

1. When the supply voltages are below 2.7 V and the headphone load impedance is 16 Ω, it is recommended to limit the DAC and the headphone output to less than -2dB; otherwise clipping may occur.
2. The output voltage of the DAC is proportional to the DAC power supply voltage.
3. Channel separation performance is measured at the IC pin.

5 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1380TT	TSSOP32	plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm	SOT487-1
UDA1380HN	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1

6 BLOCK DIAGRAM



Pin numbers for UDA1380HN in parentheses.

Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN		TYPE	DESCRIPTION
	UDA1380TT	UDA1380HN		
VINR	1	29	analog pad	ADC input right, also connected to the mixer input of the FSDAC
V_{ADCN}	2	30	analog pad	ADC reference voltage
VINM	3	31	analog pad	microphone input
V_{ADCP}	4	32	analog pad	ADC reference voltage
RESET	5	1	5 V tolerant digital input pad; push-pull; TTL with hysteresis; pull-down	pin RESET with pull-down, for making Power-On Reset (POR)
V_{DDD}	6	2	digital supply pad	digital supply voltage
BCKO	7	3	5 V tolerant digital bidirectional pad; push-pull input; 3-state output; 5 ns slew-rate control; TTL with hysteresis	bit clock output
WSO	8	4		word select output
DATAO	9	5	output pad; push-pull; 5 ns slew-rate control; CMOS	data output
BCKI	10	6	5 V tolerant digital input pad; push-pull; TTL with hysteresis	bit clock input
WSI	11	7		word select input
DATAI	12	8		data input
SYSCLK	13	9		system clock $256f_s$, $384f_s$, $512f_s$ or $768f_s$ input
V_{SSD}	14	10	digital ground pad	digital ground
RTCB	15	11	5 V tolerant digital input pad; push-pull; TTL with hysteresis; pull-down	test control input, to be connected to digital ground in the application
L3MODE	16	12	5 V tolerant digital bidirectional pad; push-pull input; 3-state output; 5 ns slew-rate control; TTL with hysteresis	L3-bus mode input or pin A1 for I^2C-bus slave address setting
L3CLOCK/SCL	17	13	5 V tolerant digital input pad; push-pull; TTL with hysteresis	L3-bus or I^2C-bus clock input
L3DATA/SDA	18	14	I^2C-bus pad; 400 kHz I^2C-bus specification	L3-bus or I^2C-bus data input and output
SEL_L3_IIC	19	15	5 V tolerant digital input pad; push-pull; TTL with hysteresis	input channel select
$V_{SSA(HP)}$	20	16	analog ground pad	headphone ground
VOUTRHP	21	17	analog pad	headphone output right
$V_{REF(HP)}$	22	18	analog pad	headphone reference voltage
VOUTLHP	23	19	analog pad	headphone output left
$V_{DDA(HP)}$	24	20	analog supply pad	headphone supply voltage
VOUTR	25	21	analog pad	DAC output right
$V_{DDA(DA)}$	26	22	analog supply pad	DAC analog supply voltage
VOUTL	27	23	analog pad	DAC output left

SYMBOL	PIN		TYPE	DESCRIPTION
	UDA1380TT	UDA1380HN		
$V_{SSA(DA)}$	28	24	analog ground pad	DAC analog ground
V_{REF}	29	25	analog pad	ADC and DAC reference voltage
$V_{SSA(AD)}$	30	26	analog ground pad	ADC analog ground
VINL	31	27	analog pad	ADC input left, also connected to the mixer input of the FSDAC
$V_{DDA(AD)}$	32	28	analog supply pad	ADC analog supply voltage

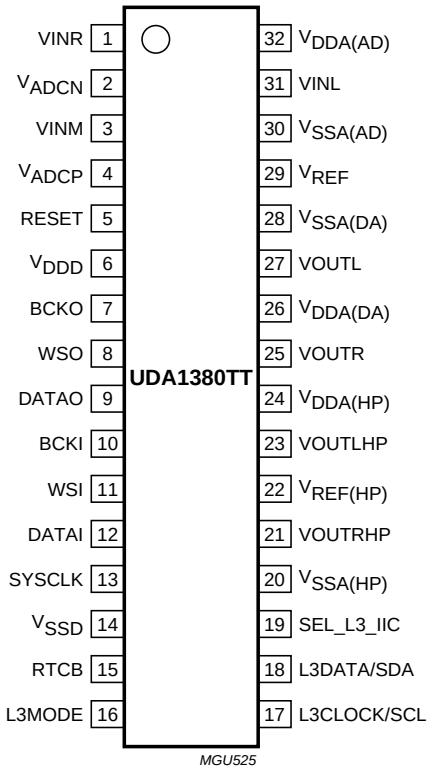


Fig.2 Pin configuration UDA1380TT.

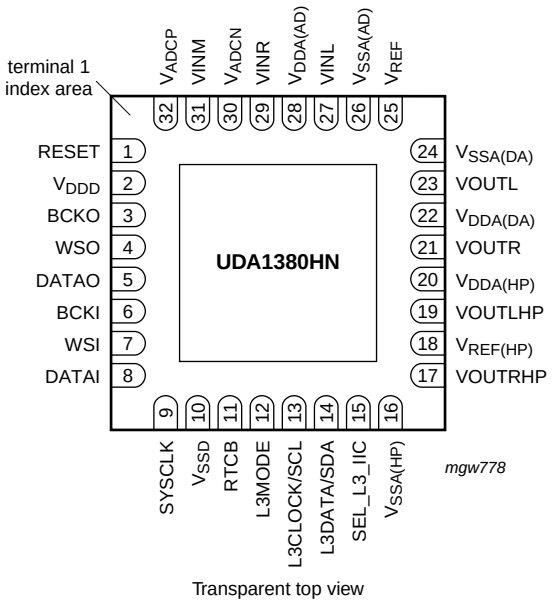


Fig.3 Pin configuration UDA1380HN.

8 FUNCTIONAL DESCRIPTION

8.1 Clock modes

There are two clock systems:

- A SYSCLK signal, coming from the system
- A WSPLL which generates the internal clocks from the incoming WSI signal.

The system frequency applied to pin SYSCLK is selectable. The options are $256f_s$, $384f_s$, $512f_s$ and $768f_s$. The system clock must be locked in frequency to the digital interface signals.

Remark: Since there is neither a fixed reference clock available in the IC itself, nor a fixed clock available in the system the IC is in, there is no auto sample rate conversion detection circuitry.

The system can run in several modes, using the two clock systems:

- Both the DAC and the ADC part can run at the applied SYSCLK input. In this case the WSPLL is powered-down
- The ADC can run at the SYSCLK input, and at the same time the DAC part can run (at a different frequency) at the clock re-generated from the WSI signal
- The ADC and the DAC can both run at the clock regenerated from the WSI signal.

8.1.1 WSPLL REQUIREMENTS

The WSPLL is meant to lock onto the WSI input signal, and regenerates $256f_s$ and $128f_s$ signals for the FSDAC and the interpolator core (and for the decimator if needed). Since the operating range of the WSPLL is from 75 to 150 MHz, the complete range of 8 to 100 kHz sampling frequency must be divided into smaller parts, as given in Table 1, using Fig.4 as a reference. This means that the user must set the input range of the WSI input signal.

In case the SYSCLK is used for clocking the complete system (decimator including interpolator) the WSPLL must be powered-down with bit ADC_CLK via the L3-bus or I^2C-bus.

The SEL_LOOP_DIV[1:0] can be controlled by the PLL1 and PLL0 bits in the L3-bus or I^2C-bus register.

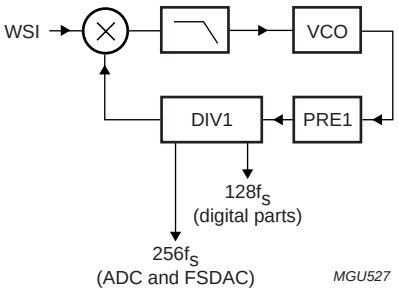


Fig.4 WSPLL set-up.

Table 1 WSPLL divider settings

WORD SELECT FREQUENCY (kHz)	SEL_LOOP_DIV[1:0]	PRE1	DIV1	VCO FREQUENCY (MHz)
6.25 to 12.5	00	8	1536	76 to 153
12.5 to 25	01	4	1536	
25 to 50	10	2	1536	
50 to 100	11	2	768	

8.1.2 CLOCK DISTRIBUTION

Figure 5 shows the main clock distribution for the SYSCLK domain and the WSPLL clock domain.

For power saving reasons each clock signal inside the system must be controlled and enabled via a separate bit in the L3-bus and I²C-bus registers (ADC_CLK).

The DAC part of the UDA1380 can operate from 8 to 100 kHz sampling frequency (f_s). This applies to the DAC part only; the ADC part can run from 8 to 55 kHz.

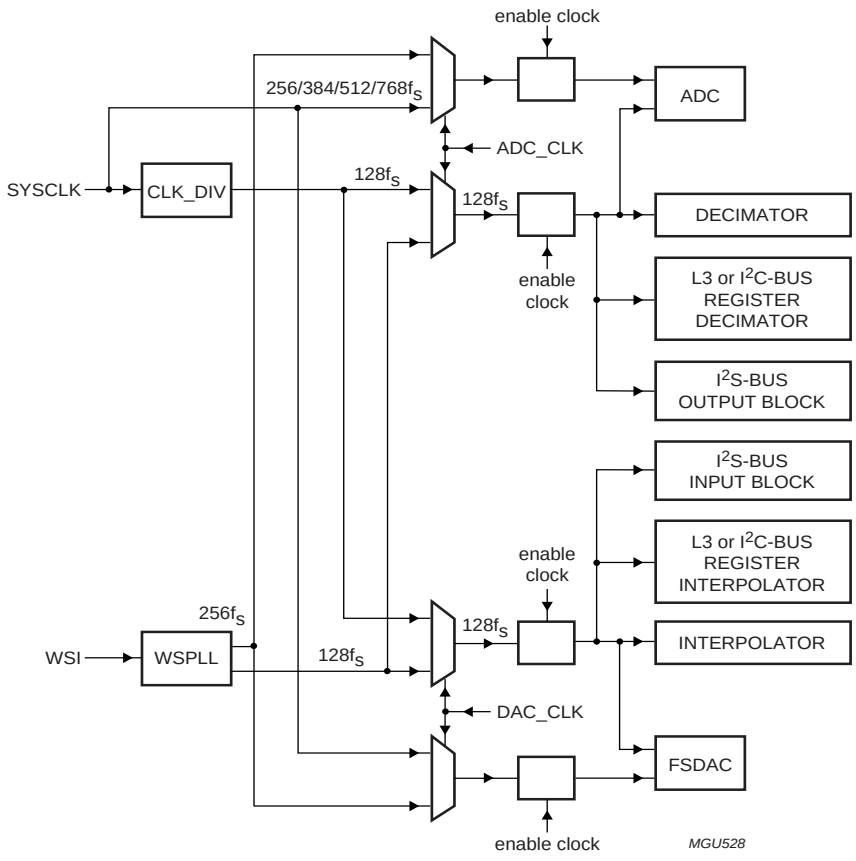


Fig.5 Clock routing for the main blocks inside the coder-decoder.

8.2 ADC analog front-end

The analog front-end of the UDA1380 consists of one stereo ADC with a selector in front of it (see Fig.6). Using this selector one can either select the microphone input with the microphone amplifier (LNA) with a fixed 29 dB gain and VGA (no PGA, since a real microphone amplifier is much better with respect to noise), or the line input which has a PGA for having 0 or 6 dB gain (for supporting 1 and 2 V (RMS) input). The PGA also provides gain control from 0 to 24 dB in steps of 3 dB.

Remark:

- The input impedance of the PGA (line input) is 12 kΩ, for the LNA this is 5 kΩ

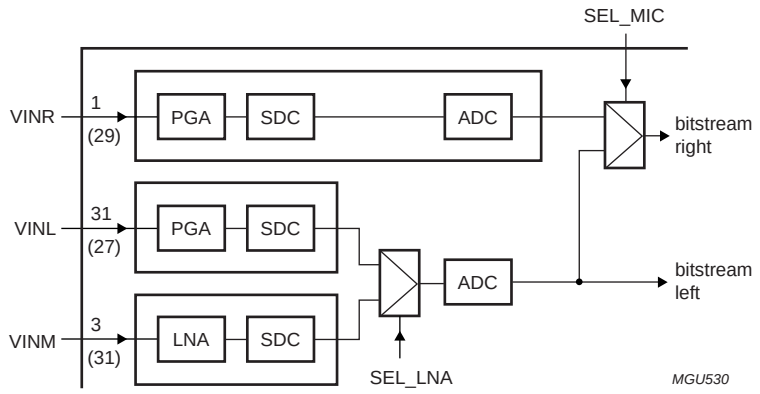
8.2.1 Applications and Power-down modes

The following Power-down modes and functional modes are supported:

- Power-down mode in which the power consumption is very low (only leakage currents)

  In this mode there is no reference voltage at the line input
- Line input mode, in which the PGA can be used
- Microphone mode, in which the rest of the non-used PGAs and ADCs are powered-down
- Mixed PGA and LNA mode: one line input and one microphone input.

More information on the analog frond-end is given in Section 8.11.1.



Pin numbers for UDA1380HN in parentheses.

Fig.6 Analog front-end.

8.2.2 LNA with VGA

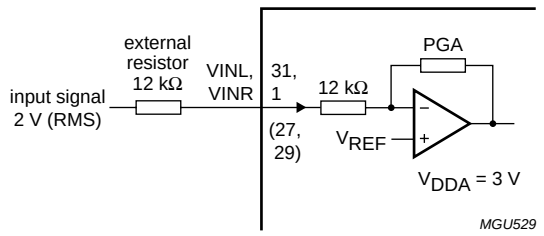
The LNA is equipped with a VGA. The function of the VGA is to have additional variable analog gain from 0 to 30 dB in steps of 2 dB. This provides more flexibility in the choice of the microphone.

8.2.3 Applications with 2 V (RMS) input

For the line input it is preferable to have 0 dB and 6 dB gain settings in order to be able to apply both 1 and 2 V (RMS) input signals, using a series resistance. For this purpose a PGA is used which has 0 to 24 dB gain, in steps of 3 dB.

In applications in which a 2 V (RMS) input signal is used, a 12 kΩ resistor must be used in series with the input of the ADC (see Fig.7). This forms a voltage divider together with the internal ADC resistor and ensures that the voltage, applied to the input of the IC, never exceeds 1 V (RMS). Using this application for a 2 V (RMS) input signal, the switch must be set to 0 dB. When a 1 V (RMS) input signal is applied to the ADC in the same application, the gain switch must be set to 6 dB.

An overview of the maximum input voltages allowed against the presence of an external resistor and the setting of the gain switch is given in Table 2; the power supply voltage is assumed to be 3 V.



Pin numbers for UDA1380HN in parentheses.

Fig.7 ADC front-end with PGA (line input).

Table 2 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
	6 dB	0.5 V (RMS)

8.3 Decimation filter (ADC)

The decimation from $128f_s$ is performed in two stages. The first stage realizes a $\frac{\sin x}{x}$ characteristic with a decimation factor of 16. The second stage consists of 3 half-band filters, each decimating by a factor 2. The filter characteristics are shown in Table 3.

Table 3 Decimation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to $0.45f_s$	0.01
Stop band	$>0.55f_s$	−70
Dynamic range	0 to $0.45f_s$	>135
Digital output level	at 0 dB input analog	−1.5

8.3.1 Overload detection

The UDA1380 is equipped with an overload detector which can be read out from the L3-bus or I²C-bus interface.

In practice the output is used to indicate whenever the output data, in either the output of the left or right channel, exceeds −1 dB (the actual figure is −1.16 dB) of the maximum possible digital swing. When this condition is detected output bit OVERFLOW in the L3-bus register is forced to logic 1 for at least $512f_s$ cycles (11.6 ms at f_s = 44.1 kHz). This time-out is reset for each infringement.

8.3.2 Volume control

The decimator is equipped with a digital volume control. This volume control is separate for left and right, and can be set with bits ML_DEC [7:0] and bits MR_DEC [7:0] via the L3-bus or I²C-bus interface. The range is from +24 dB to −63.5 dB and mutes in steps of 0.5 dB.

8.3.3 Mute

The decimator is equipped with a dB-linear mute which mutes the signal in 256 steps of 0.5 dB.

8.3.4 AGC function

The decimation filter is equipped with an AGC block. This function is intended, when enabled, to keep the output signal at a constant level. The AGC can be used for microphone applications in which the distance to the microphone is not always the same.

The AGC can be enabled via an L3-bus or I²C-bus bit by setting the bit to logic 1. In that case it bypasses the digital volume control.

Via the L3-bus or I²C-bus interface also some other settings of the AGC, like the attack and decay settings and the target level settings, can be made.

Remark: The DC filter before the decimation filter must be enabled by setting the L3-bus or I²C-bus bit SKIP_DCFIL to logic 0 when AGC is in operation; otherwise the output will be disturbed by the DC offset added in the ADC.

8.4 Interpolation filter (DAC)

The interpolation digital filter interpolates from 1 to 64f_s or to 128f_s, by cascading FIR filters, see Table 4. The interpolator is equipped with several sound features like volume control, mute, de-emphasis and tone control.

Table 4 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to 0.45f_s	±0.025
Stop band	>0.55f_s	−60
Dynamic range	0 to 0.45f_s	>135

8.4.1 DIGITAL MUTE

Muting the DAC will result in a cosine roll-off soft mute, using 4 × 32 = 128 samples in normal mode (or 3 ms at 44.1 kHz sampling frequency). The cosine roll-off curve is illustrated in Fig.8. These cosine roll-off functions are implemented for both the digital mixer and the master mute inside the DAC data path, see Section 8.8.

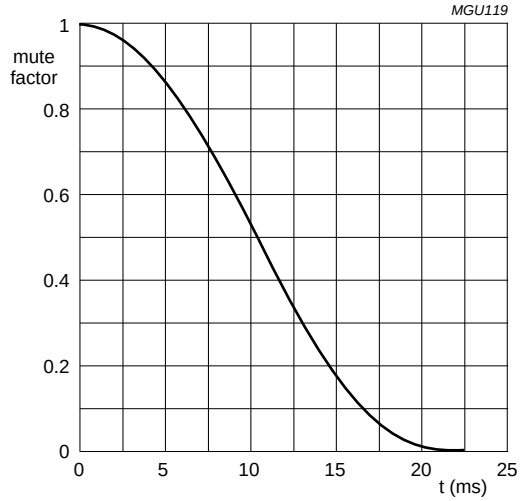


Fig.8 Mute as a function of raised cosine roll-off, displayed assuming 44.1 kHz.

8.4.2 SOUND FEATURES

In addition, there are basic sound features:

- dB-linear volume control using 14-bit coefficients in steps of 0.25 dB: range 0 to −78 dB maximum suppression and −∞ dB: applies to both master volume and mixing volume control
- De-emphasis for 32, 44.1, 48 and 96 kHz for both channel 1 and 2 (selectable independently)
- Treble, which is selectable gain for high frequencies (positive gain only), the edge frequency of the treble is fixed (depends on the sampling frequency). Can be set for left and right independently:
  - Two settings: f_c = 1.5 kHz and f_c = 3 kHz, assuming sampling frequency is 44.1 kHz
  - Both settings have 0 to 6 dB gain range in steps of 2 dB
- Bass boost, which is selectable gain for low frequencies (positive gain only). The edge frequency of the bass boost is fixed and depends on the sampling frequency. Can be set for left and right independently:
  - Two settings: f_c = 250 Hz and f_c = 300 Hz, assuming sampling frequency is 44.1 kHz
  - First setting: 0 to 18 dB gain range in steps of 2 dB
  - Second setting: 0 to 24 dB gain range in steps of 2 dB.

8.5 Noise shaper

The noise shaper consists of two mono 3rd-order noise shapers and one time-multiplexed stereo 5th-order noise shaper.

The order of the noise shaper can be chosen between 3rd-order (which runs at 128f_s) and 5th-order (which runs at 64f_s) via bit SEL_NS in the L3-bus or I^2C-bus register. The preferable choice for the noise shaper order is:

- 3rd-order noise shaper is preferred at low sampling frequencies, for instance between 8 and 32 kHz. This is for preventing out-of-band noise from the noise shaper to move into the audio band
- 5th-order noise shaper is normally used at higher sampling frequencies, normally from 32 to 100 kHz.

The noise shaper shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using an FSDAC.

8.6 FSDAC

8.6.1 General information

The Filter-Stream Digital-to-Analog Converter (FSDAC) is a semi-digital reconstruction filter that converts the 1-bit data stream (running at either $64f_s$ for the 5th-order noise shaper or $128f_s$ for the 3rd-order noise shaper) of the noise shaper into an analog output voltage. The filter coefficients are implemented as current sources, and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity are achieved. A post-filter is not needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal, capable of driving a line output. The output voltage of the FSDAC scales proportionally with the power supply voltage.

Remark: When the FSDAC is powered-down, the output of the FSDAC becomes high impedance.

8.6.2 Analog mixer input

The FSDAC has a mixer input, which makes it possible to mix an analog signal to the output signal of the FSDAC itself. In schematic form this is given in Fig.9.

This mixer input can be used for instance for mixing-in a GSM signal or an FM signal directly to the line output. In the UDA1380, the mixer input is connected from the ADC line input via an AVC unit.

Remark: Before the AVC unit can be used stand-alone, meaning without the digital part running, first the DAC part must be initialised in order to have the DAC output generating zero current. Otherwise the signal will be clipped.

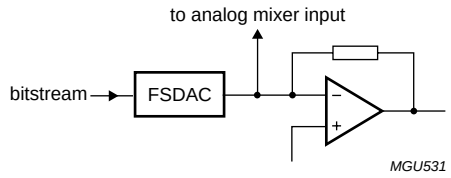


Fig.9 Mixing signals to the FSDAC output (analog domain).

8.7 Headphone driver

The UDA1380 is equipped with a headphone driver which can deliver 35 mW (at 3.0 V power supply) into a 16 Ω load.

The headphone driver does not need external DC decoupling capacitors because it can be DC coupled with respect to a special headphone output reference voltage. This saves two external capacitors (which is quite useful in a portable device).

The headphone driver is equipped with short-circuit protection on all three operational amplifiers (left, right and the virtual ground). Each of the operational amplifiers has a signalling bit which becomes logic 1 in case the limiter is activated, for instance in case of a short-circuit. This means the microcontroller in the system can poll the L3-bus or I^2C-bus register of the headphone driver and as soon as (and for as long as) the short-circuit detection bits are activated, the microcontroller can signal the user that something is wrong or power-down the headphone driver (for instance, for energy-saving purposes).

Remark: To improve headphone channel separation performance, the distance between $V_{REF(HP)}$ and the micro speaker port must be minimized.

8.8 Digital and analog mixers (DAC)

8.8.1 Digital mixer

The ADC output signal and digital input signal can be mixed without external DSP as shown in Fig.10. This mixer can be controlled via the microcontroller interface, and must only be enabled when the ADC and the DAC are running at the same frequency. In addition, the mixer output signal can also be applied to the I^2S-bus output interface.

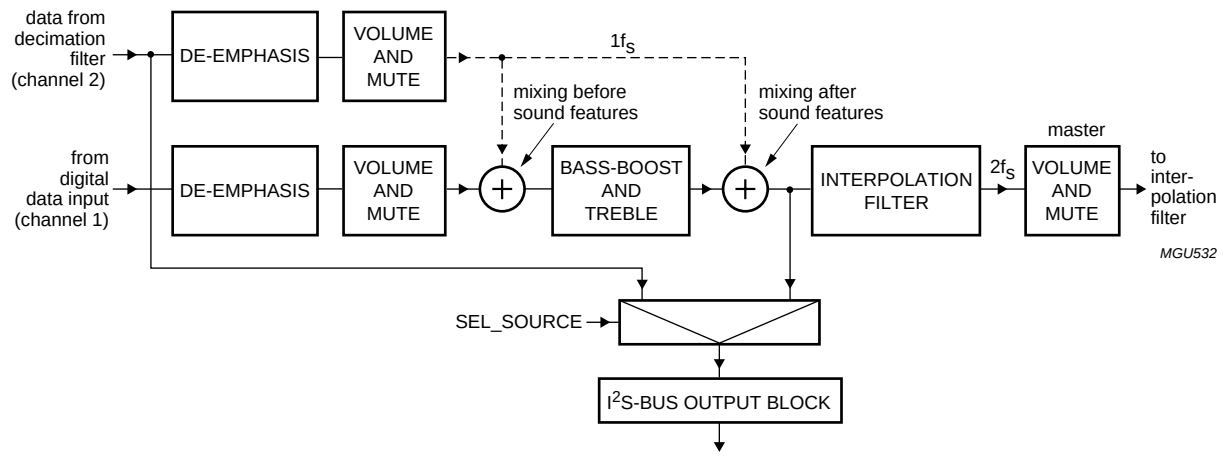


Fig.10 Digital mixer (DAC).

8.8.2 Analog mixer

The analog mixer, which uses the mixer input of the FSDAC, can mix a signal into the FSDAC output signal via an AVC unit (see Fig.11). The mixer can be used to mix a signal into the FSDAC output signal and play it via the headphone driver without the complete coder-decoder running. The analog control range is 0 to −64.5 dB with a gain of 16.5 dB, and mutes in steps of 1.5 dB (so actually the range is from +16.5 dB to −48 dB plus mute).

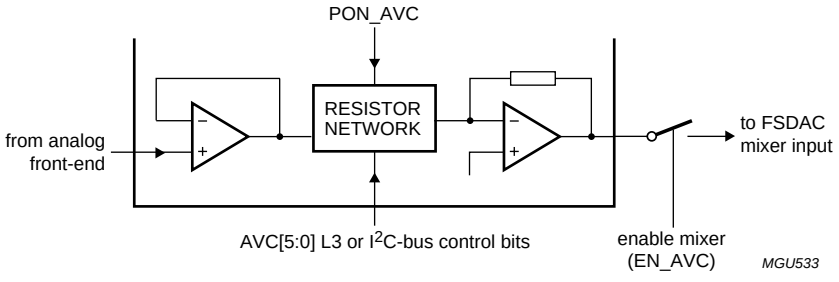


Fig.11 Analog mixer configuration.

8.9 Application modes

The operation mode can be set with pin SEL_L3_IIC, either to L3-bus mode (LOW) or to the I²C-bus mode (HIGH) as given in Table 5.

For all features in microcontroller mode see Chapter 9.

Table 5 Pin function in the selected mode

PIN	L3-BUS MODE SEL_L3_IIC = L	I²C-BUS MODE SEL_L3_IIC = H
L3CLOCK/SCL	L3CLOCK	SCL
L3MODE	L3MODE	A1
L3DATA/SDA	L3DATA	SDA

Remark: In the I²C-bus mode there is a bit A1 which sets the LSB bit of the address of the UDA1380. In L3-bus mode this bit is not available, meaning the device has only one L3-bus device address.

8.10 Power-on reset

The UDA1380 has a dedicated reset pin, which has a pull-down resistor. This way a Power-on reset circuit can be made with a capacitor and a resistor at the pin. The internal pull-down resistor cannot be used because of the 5 V tolerant nature of the pad. The pull-down resistor is shielded from the outside world by a transmission gate in order to support 5 V tolerance.

The reset timing is determined by the external capacitor and resistor which are connected to pin RESET, and the internal pull-down resistor. On Power-on reset, all the digital sound processing features and the system controlling features are set to the default setting of the L3-bus and I²C-bus control modes.

Remark: The reset time should be at least 1 μs, and during the reset time the system clock should be running. In case the WSPLL is selected as the clock source, a clock must be connected to the SYSCLK input in order to have a proper reset of the L3-bus or I²C-bus registers. This is because the clock source is set to SYSCLK by default.

8.11 Power-down requirements

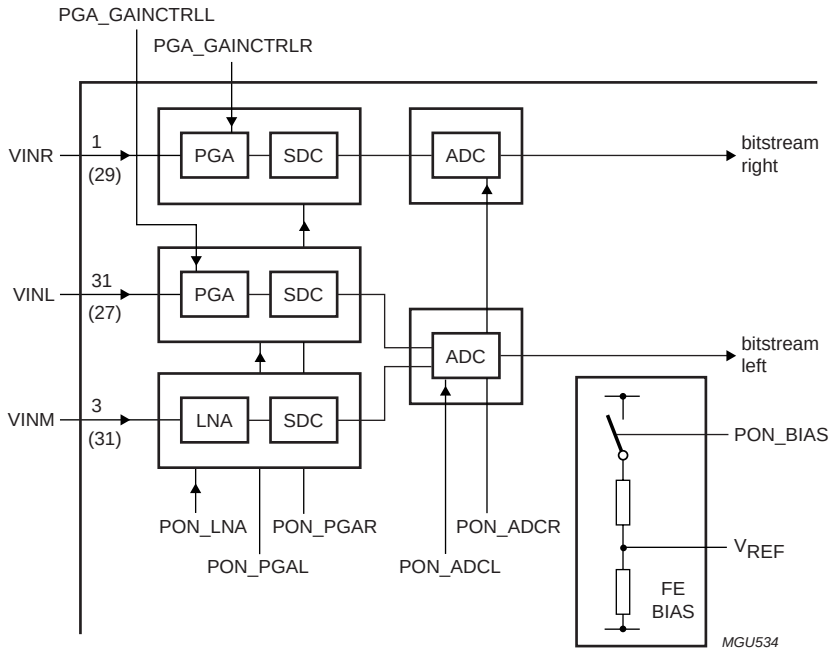
The following blocks have power-down control via the L3-bus or I²C-bus interface:

- Microphone amplifier (LNA) including its Single-Ended to Differential Converter (SDC) and VGA
- ADC plus SDC and the PGA, for left and right separate
- Bias generation circuit for the front-end and the FSDAC
- Headphone driver
- WSPLL
- FSDAC.

Clocks of the decimator, interpolator and the analog blocks have separate enable and disable controls.

8.11.1 Analog front-end

Figure 12 shows the power control inside the analog front-end. The control of all power-on pins of the ADC front-end is done via separate L3-bus or I²C-bus bits.



Pin numbers for UDA1380HN in parentheses.

Fig.12 Analog front-end power-down.

8.11.2 FSDAC power control

The FSDAC block has power-on pins: one of which shuts down the DAC itself, but leaves the output still at V_{REF} voltage (which is half the power supply). This function is set by the bit PON_DAC in the L3-bus or I²C-bus register.

A second L3-bus or I²C-bus bit shuts down the complete bias circuit of the FSDAC, via bit PON_BIAS in the L3-bus or I²C-bus register. This bit PON_BIAS acts the same as given in Fig.12 for the analog front-end.

8.12 Plop prevention

Plops are ticks and other strange sounds that can occur when a part of a device is powered-up or powered-down, or when switching between modes is done.

Some ways to prevent plops from occurring are:

- When the FSDAC or headphone driver must be powered-down, first a digital mute is applied. After that the FSDAC or headphone driver can be powered-down. In case the FSDAC or headphone driver must be powered-up, first the analog part is switched on, then the digital part is demuted
- When the ADC must be powered-down, a digital mute sequence must be applied. When the digital output signal is completely muted, the ADC can be powered-down. In case the ADC must be powered-up, first the analog part must be powered-up, then the digital part must be demuted
- When there is a change of, for example, clock divider settings or clock source (selecting between SYSCLK and WSPLL clock), then also digital mute for that block (either decimator or interpolator) should be used.

Remark: All items mentioned in Section 8.12 are not ‘hard-wired’ implemented, but are to be followed by the user as a guideline for plop prevention.

8.13 Digital audio data input and output

The supported audio formats for the control modes are:

- I^2S-bus
- MSB-justified
- LSB-justified, 16 bits
- LSB-justified, 18 bits
- LSB-justified, 20 bits
- LSB-justified, 24 bits (only for the output interface).

The bit clock BCK can be up to $128f_s$, or in other words the BCK frequency is 128 times the WS frequency or less: $f_{BCK} \leq 128f_{WS}$.

Remark: The WS edge must coincide with the negative edge of the BCK at all times, for proper operation of the digital I/O data interface. Figure 13 shows the interface signals.

8.13.1 Digital audio input interface

The digital audio input interface is slave only, meaning the system must provide the WSI and BCKI signals (next to the DATAI signal).

Either the WSPLL locks onto the WSI signal and provides the internal clocks for the interpolator and the FSDAC, or a system clock must be applied which must be in frequency lock to the digital data input interface signals.

8.13.2 Digital audio output interface

The digital audio output interface can be either master or slave. The data source for the data output can be selected from either the decimator (ADC front-end) or the digital mixer output.

Remark: The digital mixer output is only valid if both the decimator and the interpolator run at the same clock:

- In slave mode the signals on pins BCKO, WSO and SYSCLK must be applied from the application (signals must be in frequency lock) and the UDA1380 returns the DATAO signal from the decimator. The applied signal from pin BCKO can be for instance: $32f_s$, $48f_s$, $64f_s$, $96f_s$ or $128f_s$
- In master mode the SYSCLK signal must be applied from the system, then the UDA1380 returns with the BCKO, WSO and the DATAO signals. For the BCKO clock, there are 2 general rules:
  - When the SYSCLK is either $256f_s$ or $512f_s$, the BCKO frequency is $64f_s$
  - When the SYSCLK is either $384f_s$ or $768f_s$, the BCKO signal is $48f_s$.

The slave and master modes can be selected by the bit Serial Interface Mode (SIM) in the L3-bus or I^2C-bus interface.

9 L3-BUS INTERFACE DESCRIPTION

The UDA1380 has an L3-bus microcontroller interface mode. Controllable system and digital sound processing features are:

- Software reset
- System clock frequency (selection between $256f_s$, $384f_s$, $512f_s$ and $768f_s$ clock divider settings)
- Clock mode setting, for instance, which block runs at which clock, and clock enabling
- Power control for the WSPLL
- Data input and data output format control, for input and output independently including data source selection for the digital output interface
- ADC features:
  - Digital mute
  - AGC enable and settings
  - Polarity control
  - Input line amplifier control (0 to 24 dB in steps of 3 dB)
  - DC filtering control
  - Digital gain control (+24 to −63 dB gain in steps of 0.5 dB) for left and right
  - Power control
  - VGA of the microphone input
  - Selection of line or microphone input.
- DAC and headphone driver features:
  - Power control FSDAC and headphone driver
  - Polarity control
  - Mixing control (only available when both decimator and interpolator run at the same speed). This includes the mixer volumes, mute and mixer position switch
  - De-emphasis control
  - Master volume and balance control
  - Flat/minimum/maximum settings for bass boost and treble
  - Tone control: bass boost and treble
  - Master mute control
  - Headphone driver short-circuit protection status bits.

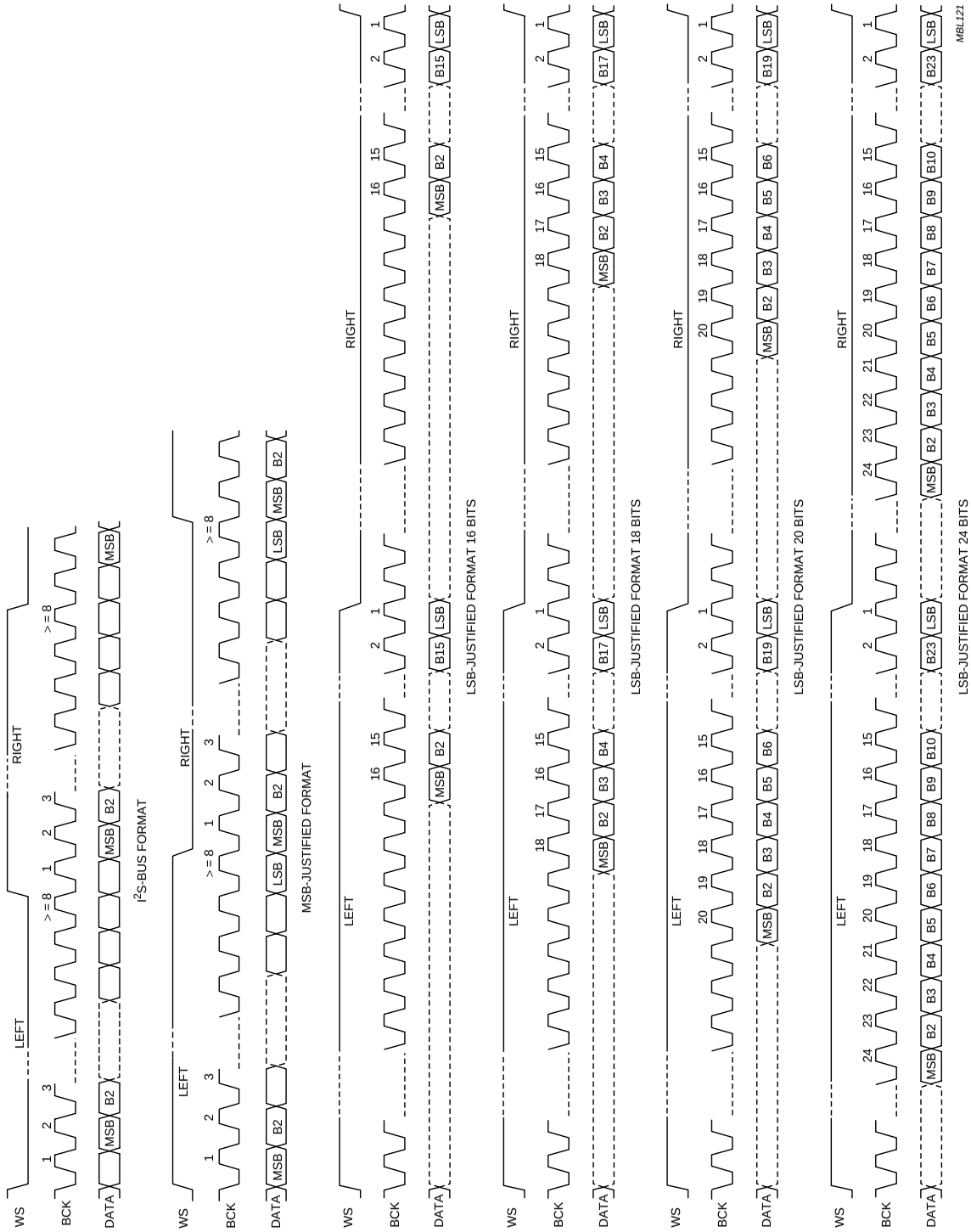


Fig.13 Serial interface input and output formats.

9.1 Introduction

The exchange of data and control information between the microcontroller and the UDA1380, is accomplished through a serial hardware interface comprising the following pins:

L3DATA/SDA: microcontroller interface data line

L3MODE: microcontroller interface mode line

L3CLOCK/SCL: microcontroller interface clock line.

Information transfer via the microcontroller bus is organized LSB first, and in accordance with the so called 'L3' format, in which two different modes of operation can be distinguished: address mode and data transfer mode.

Inside the microcontroller interface there is a hand-shake mechanism which takes care of proper data transfer from the microcontroller interface clock to the destination clock domains. This means that when data is sent to the microcontroller interface, the system clock must be running.

9.2 Device addressing

The device addressing mode is used to select a device for subsequent data transfer. The address mode is characterized by the signal on pin L3MODE being LOW and a burst of 8 pulses on pin L3CLOCK/SCL, accompanied by an 8 bit device address on pin L3DATA/SDA. The fundamental timing is shown in Figs 14 and 15.

Table 6 Selection of data transfer

DOM BIT 1	DOM BIT 0	TRANSFER
0	0	not used
0	1	not used
1	0	DATA and STATUS write or pre-read
1	1	DATA and STATUS read

Table 6 shows that there are two types of data transfers: DATA and STATUS which can be read and written. Table 6 also shows that the DATA and STATUS read and write actions are combined.

The device address consists of one byte, which is split-up in two parts:

- Bits 7 to 2 represent a 6-bit device address. In the UDA1380 this is 000001
- Bits 1 to 0 called Data Operation Mode, or DOM bits, represent the type of data transfer according to Table 6.

9.3 Slave address

The UDA1380 acts as a slave receiver or a slave transmitter. Therefore the signals L3CLOCK and L3MODE are only input signals. The data signal L3DATA is a bidirectional line. The UDA1380 slave address is shown in Table 7.

Table 7 L3 slave address

(MSB)		BIT			(LSB)
0	0	0	0	0	1

9.4 Register addressing

After sending the device address, including the flags (the DOM bits) whether information is read or written, one byte is sent with the destination register address using 7 bits, and one bit which signals whether information will be read or written. The fundamental timing for L3 is given in Fig.19.

Basically there are three forms for register addressing:

- Register addressing for L3 write: the first bit is a logic 0 indicating a write action to the destination register, followed by seven register address bits
- Prepare read addressing: the first bit of the byte is logic 1; signalling data will be read from the register indicated
- The read action itself: in this case the device returns a register address prior to sending data from that register. When the first bit of the byte is logic 0, the register address was valid, in case the first bit is a logic 1 the register address was invalid.

Remarks:

- Each time a new destination address needs to be written, the device address must be sent again
- When addressing the device for the first time after power-up of the device, at least one L3 clock-cycle must be given to enable the L3 interface.

9.5 Data write mode

For writing data to a device, four bytes must be sent. Figure 14 explains the data write mode in a signal diagram:

- One byte with the device address, being ‘00000110’, which is including the LSB code 01 for signalling write to the device
- One byte starting with a logic 0 for signalling write, followed by 7 bits indicating the destination address
- Two data bytes.

The SYSCLK signal must be applied in data write mode.

Table 8 L3 write data

L3 MODE	DATA TYPE	BIT							
		0(1)	**1**	**2**	**3**	**4**	**5**	**6**	**7**(2)
Addressing mode	device address	0	1	1	0	0	0	0	0
Data transfer 1	register address	0	A6	A5	A4	A3	A2	A1	A0
Data transfer 2	MS data byte	D15	D14	D13	D12	D11	D10	D9	D8
Data transfer 3	LS data byte	D7	D6	D5	D4	D3	D2	D1	D0

Notes

1. First bit in time.
2. Last bit in time.

9.6 Data read mode

For reading from the device, first a prepare-read must be done. After this, the device address is sent again. The device then returns with the register address, indicating whether the address was valid or not, and the data of the register. The following five steps explain this procedure, and an example of transmission is given in Fig.15.

- One byte with the device address, being ‘00000110’, which is including the LSB code 01 for signalling write to the device
- One byte is sent with the register address from which it needs to be read. This byte starts with a logic 1, which indicates that there will be a read action from the register
- One byte with the device address including ‘11’ is sent to the device, being 00000111. The ‘11’ indicates that the device must write data to the microcontroller, then the microcontroller frees the L3DATA-bus so the UDA1380 can send the register address byte and its two-byte contents
- The device now writes the requested register address on the bus, indicating whether the requested register was valid or not (logic 0 means valid, logic 1 means invalid)
- The device writes the data from the requested register on the bus, being two bytes.

The SYSCLK signal must be applied in data read mode.

Table 9 L3 prepare read data

L3 MODE	DATA TYPE	BIT							
		0[1]	**1**	**2**	**3**	**4**	**5**	**6**	**7**[2]
Addressing mode	device address	0	1	1	0	0	0	0	0
Data transfer 1	register address	1	A6	A5	A4	A3	A2	A1	A0

Notes

1. First bit in time.
2. Last bit in time.

Table 10 L3 read data

L3 MODE	DATA TYPE	BIT							
		0[1]	**1**	**2**	**3**	**4**	**5**	**6**	**7**[2]
Addressing mode	device address	1	1	1	0	0	0	0	0
Data transfer 1; note 3	register address	0: valid 1: invalid	A6	A5	A4	A3	A2	A1	A0
Data transfer 2; note 3	MS data byte	D15	D14	D13	D12	D11	D10	D9	D8
Data transfer 3; note 3	LS data byte	D7	D6	D5	D4	D3	D2	D1	D0

Notes

1. First bit in time.
2. Last bit in time.
3. Data transfer from the UDA1380 to the microcontroller.

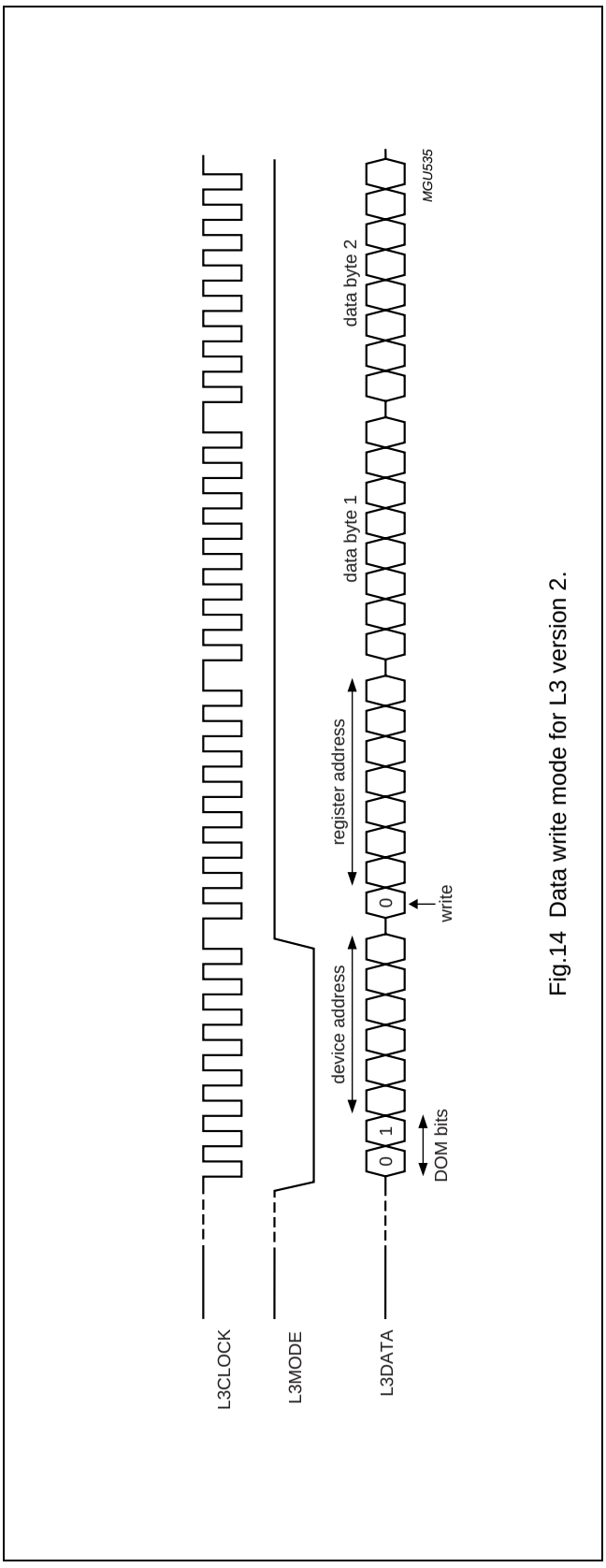


Fig.14 Data write mode for L3 version 2.

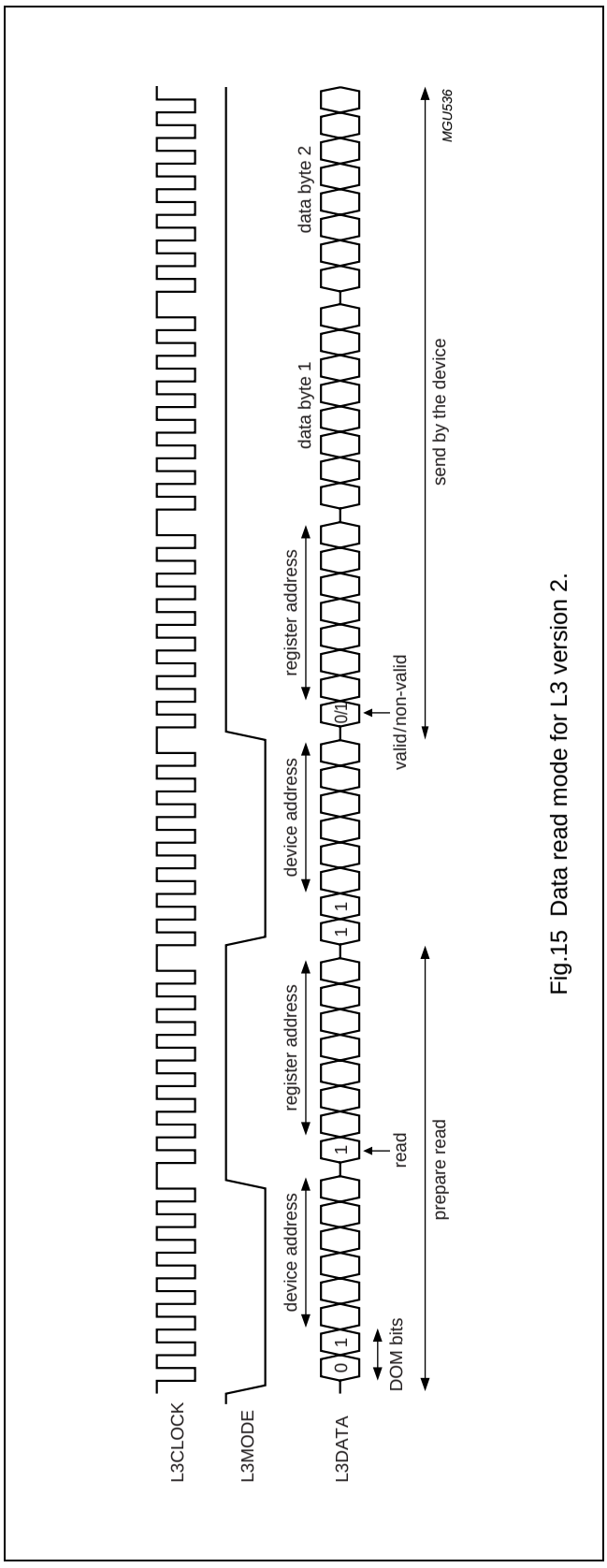


Fig.15 Data read mode for L3 version 2.

10 I²C-BUS INTERFACE DESCRIPTION

The UDA1380 supports I²C-bus microcontroller interface mode as well as the L3-bus mode; all features can be controlled by the microcontroller with the same register addresses as in the L3-bus mode.

The exchange of data and control information between the microcontroller and the UDA1380 in I²C-bus mode is accomplished through a serial hardware interface comprising the following pins:

L3CLOCK/SCL: microcontroller interface clock line, SCL

L3MODE: sets the bit A1of the I²C-bus device address

L3DATA/SDA: microcontroller interface data line, SDA.

Figure 20 shows the clock and data timing of the I²C-bus transfer.

10.1 Addressing

Before any data is transmitted on the I²C-bus, the device which should respond is addressed first. The addressing is always done with the first byte transmitted after the start procedure. The UDA1380 device address is [A6 to A0] 00110(A1)0, with bit A1 as the address selection bit (two addresses possible).

10.1.1 Device address (pin A1)

The UDA1380 acts as either a slave receiver or a slave transmitter. Therefore the clock signal SCL is only an input signal. The data signal SDA is a bidirectional line. Table 11 shows the device address of the UDA1380.

The device can be set to one of the two addresses by using bit A1 (which is pin L3MODE) to select.

Table 11 I²C-bus device address

(MSB)			BIT				(LSB)
0	0	1	1	0	A1	0	R/$\overline{W}$

10.1.2 Register address

Table 12 shows the register address format of the UDA1380. The register mapping in I²C-bus mode is the same as for the L3-bus interface.

Table 12 I²C-bus register address

(MSB)			BIT				(LSB)
0	A6	A5	A4	A3	A2	A1	A0

10.2 WRITE cycle

Table 13 shows the I^2C-bus configuration for a WRITE cycle. The WRITE cycle is used to write the data to the internal registers. The device and register addresses are one byte each, the setting data is always a pair of two bytes.

The format of the WRITE cycle is as follows:

1. The microcontroller begins by asserting a start condition (S).
2. The first byte (8 bits) contains the device address '00110$A_1$0' and the R/$\overline{W}$ bit is set to logic 0 (WRITE).
3. The UDA1380 asserts an acknowledge (A).
4. The microcontroller writes the 8-bit address (ADDR) of the UDA1380 register to which the data will be written.
5. The UDA1380 acknowledges this register address (A).
6. The microcontroller sends two bytes of data with the Most Significant (MS) byte first, followed by the Least Significant (LS) byte; after each byte the UDA1380 asserts an acknowledge (A).
7. After each pair of bytes transmitted, the register address is auto-incremented; after each byte the UDA1380 asserts an acknowledge (A).
8. The UDA1380 frees the I^2C-bus allowing the microcontroller to generate a stop condition (P).

Table 13 Master transmitter writes to UDA1380 registers in the I^2C-bus mode

INITIAL BYTE			**ACKNOWLEDGE FROM UDA1380**															
START	**DEVICE ADDRESS**	**R/$\overline{W}$**		**REGISTER ADDRESS**		**MS data byte**		**LS data byte**										**STOP**
S	00110$A_1$0	0	A	ADDR	A	MS1	A	LS1	A	...	A	...	A	MSn	A	LSn	A	P
						auto increment if repeated n groups of 2 bytes are transmitted												

10.3 READ cycle

Table 14 shows the I²C-bus configuration for a READ cycle. The READ cycle is used to read the data values from the internal registers.

The format of the READ cycle is as follows:

1. The microcontroller begins by asserting a start condition (S).
2. The first byte (8 bits) contains the device address '00110$A_1$0' and the R/$\overline{W}$ bit is set to logic 0 (WRITE).
3. The UDA1380 asserts an acknowledge (A).
4. The microcontroller writes the 8-bit address (ADDR) of the UDA1380 register from which the data will be read.
5. The UDA1380 acknowledges this register address (A).
6. The microcontroller generates a repeated start (Sr).
7. The microcontroller generates the device address '00110$A_1$0' again, but this time the R/$\overline{W}$ bit is set to logic 1 (READ).
8. The UDA1380 asserts an acknowledge (A).
9. The UDA1380 sends two bytes of data with the Most Significant (MS) byte first, followed by the Least Significant (LS) byte; after each byte the microcontroller asserts an acknowledge (A).
10. After each pair of bytes transmitted, the register address is auto-incremented; after each byte the microcontroller asserts an acknowledge (A).
11. The microcontroller stops this cycle by generating a negative acknowledge (NA).
12. The UDA1380 frees the I2C-bus allowing the microcontroller to generate a stop condition (P).

Table 14 Master transmitter reads from the UDA1380 registers in the I²C-bus mode

INITIAL BYTE			**ACKNOWLEDGE FROM UDA1380**							**ACKNOWLEDGE FROM MICROCONTROLLER**											
	DEVICE ADDRESS	**R/$\overline{W}$**					**REGISTER ADDRESS**	**R/$\overline{W}$**		**MS data byte**		**LS data byte**									
S	00110$A_1$0	0	A	ADDR	A	Sr	00110$A_1$0	1	A	MS1	A	LS1	A	...	A	...	A	MSn	A	LSn	NA	P
										auto increment if repeated n groups of 2 bytes are transmitted												

11 REGISTER MAPPING

Table 15 Register map of control settings (write)

REGISTER ADDRESS	FUNCTION
System settings (running at the L3-bus or I^2C-bus clock itself)	
00H	evaluation modes, WSPLL settings, clock divider and clock selectors
01H	I^2S-bus I/O settings
02H	power control settings
03H	analog mixer settings
04H	headphone amplifier settings
Interpolation filter (running at $128f_s$ interpolator clock)	
10H	master volume control
11H	mixer volume control
12H	mode selection, left and right bass boost, and treble settings
13H	master mute, channel 1 and channel 2 de-emphasis and channel mute
14H	mixer, silence detector and interpolation filter oversampling settings
Decimator (running at $128f_s$ decimator clock)	
20H	decimator volume control
21H	PGA settings and mute
22H	ADC settings
23H	AGC settings
Software reset	
7FH	restore L3-default values

Table 16 Register map of status bits (read-out)

REGISTER ADDRESS	FUNCTION
Headphone driver and interpolation filter	
18H	interpolation filter status
Decimator	
28H	decimator status

11.1 Evaluation modes and clock settings

Table 17 Register address 00H

BIT	15	14	13	12	11	10	9	8
Symbol	EV2	EV1	EV0	–	EN_ADC	EN_DEC	EN_DAC	EN_INT
Default	0	0	0	0	0	1	0	1

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	ADC_CLK	DAC_CLK	sys_div1	sys_div0	PLL1	PLL0
Default	0	0	0	0	0	0	1	0

Table 18 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 13	EV[2:0]	**Evaluation bits.** Bits EV2, EV1 and EV0 are special control bits for manufacturer's evaluation and must always be kept at their default values for normal operation of UDA1380; default value 000.
12	–	default value 0
11	EN_ADC	**ADC clock enable.** A 1-bit value to enable the system clock (from SYSCLK input) to the analog part of the ADC. See Fig.5 for more detailed information. When this bit is logic 0: clock to ADC disabled and when this bit is logic 1: clock to ADC running. Default value 0.
10	EN_DEC	**Decimator clock enable.** A 1-bit value to enable the $128f_s$ clock to the decimator, the $128f_s$ part of the I^2S-bus output block and the clock to the ADC L3-bus or I^2C-bus registers. See Fig.5 for more detailed information. When this bit is logic 0: clock to the decimator disabled. When this bit is logic 1: clock to the decimator running. Default value 1.
9	EN_DAC	**FSDAC clock enable.** A 1-bit value to enable the $256f_s$ clock to the analog part of the FSDAC. See Fig.5 for more detailed information. When this bit is logic 0: clock to FSDAC disabled. When this bit is logic 1: clock to the FSDAC running. Default value 0.
8	EN_INT	**Interpolator clock enable.** A 1-bit value to enable the $128f_s$ clock to the interpolator, the $128f_s$ part of the I^2S-bus input block and the interpolator registers of the L3-bus or I^2C-bus interface. See Fig.5 for more detailed information. When this bit is logic 0: clock to the interpolator disabled. When this bit is logic 1: clock to the interpolator running. Default value 1.
7 and 6	–	default value 00
5	ADC_CLK	**ADC clock select.** A 1-bit value to select the $128f_s$ clock and the clock of the analog part for the decimator and the ADC. This can either be the clock derived from the SYSCLK input or from the WSPLL. When this bit is logic 0: SYSCLK is used. When this bit is logic 1: WSPLL is used. Default value 0.

BIT	SYMBOL	DESCRIPTION
4	DAC_CLK	**DAC clock select.** A 1-bit value to select the clocks for the DAC (interpolator and FSDAC analog block). In both cases the clocks must be $128f_s$ and $256f_s$ (for the analog part), but in one case the clock is derived from the WSI clock, and in the other case the clock is derived from the SYSCLK. When this bit is logic 0: SYSCLK is used. When this bit is logic 1: WSPLL is used. Default value 0.
3 and 2	sys_div[1:0]	**Dividers for system clock input.** A 2-bit value to select the proper division factor for the SYSCLK input in such a way that a$128f_s$ clock will be generated from the SYSCLK clock signal. The $128f_s$ clock is needed for clocking the decimator and interpolator. Default value 00, see Table 19.
1 and 0	PLL[1:0]	**WSPLL setting.** A 2-bit value to select the WSPLL input frequency range. These set the proper divider setting for the WSPLL. The input is the WSI signal, the output inside the IC is a $128f_s$ and a $256f_s$ clock. Default value 10, see Table 20.

Table 19 Dividers for system clock input

sys_div1	sys_div0	INPUT CLOCK ON PIN SYSCLK
0	0	$256f_s$ (default)
0	1	$384f_s$
1	0	$512f_s$
1	1	$768f_s$

Table 20 WSPLL settings

PLL1	PLL0	INPUT FREQUENCY RANGE (kHz) ON PIN WSI
0	0	6.25 to 12.5
0	1	12.5 to 25
1	0	25 to 50 (default)
1	1	50 to 100

11.2 I²S-bus input and output settings

Table 21 Register address 01H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	SFORI2	SFORI1	SFORI0
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	SEL_ SOURCE	–	SIM	–	SFORO2	SFORO1	SFORO0
Default	0	0	0	0	0	0	0	0

Table 22 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 11	–	default value 00000
10 to 8	SFORI[2:0]	**Digital data input formats. A 3-bit value to select the digital input data format (DATAI input).** Default value 000, see Table 23.
7	–	default value 0
6	SEL_SOURCE	**Digital output interface mode settings.** A 1-bit value SEL_SOURCE to set the mode of the digital output interface source to either the decimator output or the digital mixer output. When this bit is logic 0: source digital output interface mode set to decimator. When this bit is logic 1: source digital output interface mode set to digital mixer output. Default value 0.
5	–	default value 0
4	SIM	**Digital output interface mode settings.** A 1-bit value SIM sets the mode of the digital output interface. The speed of the BCKO pad, being $64f_s$ or $48f_s$, is selected by the bits sys_div[1:0]. In case the $384f_s$ or $768f_s$ mode is selected the output clock is $48f_s$, in case $256f_s$ or $512f_s$ is selected, the BCKO is $64f_s$. When this bit is logic 0: mode of digital output interface is set to slave. When this bit is logic 1: mode of digital output interface is set to master. Default value 0.
3	–	default value 0
2 to 0	SFORO[2:0]	**Digital data output formats.** A 3-bit value to set the digital data output format (on pin DATAO). Default value 000, see Table 24.

Table 23 Digital data input formats

SFORI2	SFORI1	SFORI0	SERIAL_FORMAT_DAI
0	0	0	I²S-bus (default)
0	0	1	LSB-justified, 16 bits
0	1	0	LSB-justified, 18 bits
0	1	1	LSB-justified, 20 bits
1	0	1	MSB-justified
1	0	0	not used: mapped to I²S-bus
1	1	0	
1	1	1	

Table 24 Digital data output formats

SFORO2	SFORO1	SFORO0	SERIAL_FORMAT_DAO
0	0	0	I^2S-bus (default)
0	0	1	LSB-justified, 16 bits
0	1	0	LSB-justified, 18 bits
0	1	1	LSB-justified, 20 bits
1	0	0	LSB-justified, 24 bits
1	0	1	MSB-justified
1	1	0	not used: mapped to I^2S-bus
1	1	1	

11.3 Power control settings

11.3.1 Power control setting bias circuits

Using a 1-bit value, the power control settings of the bias circuits of the ADC, AVC and FSDAC can be set. When this bit is set to logic 0, the complete bias circuits of the analog front-end and the FSDAC are shut down. In this case, the reference voltage disappears from the input of the ADCs and LNA and the output of the FSDAC, this can cause plops but saves power.

Table 25 Register address 02H

BIT	15	14	13	12	11	10	9	8
Symbol	PON_PLL	–	PON_HP	–	–	PON_DAC	–	PON_BIAS
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	EN_AVC	PON_AVC	–	PON_LNA	PON_PGAL	PON_ADCL	PON_PGAR	PON_ADCR
Default	0	0	0	0	0	0	0	0

Table 26 Description of register bits

BIT	SYMBOL	DESCRIPTION
15	PON_PLL	**Power-on WSPLL.** When this bit is logic 0: power-off; when this bit is logic 1: power-on. Default value 0.
14	–	default value 0
13	PON_HP	**Power-on headphone driver.** A 1-bit value to switch the headphone driver into power-on or Power-down mode. When this bit is logic 0: headphone driver is powered-off; when this bit is logic 1: headphone driver is powered-on. Default value 0.
12 and 11	–	default value 00
10	PON_DAC	**Power-on DAC.** A 1-bit value to switch the DAC into power-on or Power-down mode. In this Power-down mode the V_{REF} (half the power supply voltage) will remain on the FSDAC output. When this bit is logic 0: DAC is powered-off; when this bit is logic 1: DAC is powered-on. Default value 0.
9	–	default value 0

BIT	SYMBOL	DESCRIPTION
8	PON_BIAS	**Power-on BIAS.** A 1-bit value to set the power control setting of the ADC, AVC and FSDAC. When this bit is logic 0: ADC, AVC and FSDAC bias circuits are powered-off; when this bit is logic 1: Power-on bias for ADC, AVC and FSDAC. Default value 0.
7	EN_AVC	**Enable control AVC.** A 1-bit value to enable or disable the analog mixer. When this bit is logic 0: analog mixer is disabled; when this bit is logic 1: analog mixer is enabled. Default value 0.
6	PON_AVC	**Power-on AVC.** A 1-bit value to have power-on control for the analog mixer. When this bit is logic 0: analog mixer powered-off; when this bit is logic 1: analog mixer powered-on. Default value 0.
5	–	default value 0
4	PON_LNA	**Power-on LNA.** A 1-bit value to power-on the LNA and SDC. When this bit is logic 0: LNA and SDC are powered-off; when this bit is logic 1: LNA and SDC are powered-on. Default value 0.
3	PON_PGAL	**Power-on PGAL.** A 1-bit value to have power-on control for the PGA left. When this bit is logic 0: left PGA is powered-off; when this bit is logic 1: left PGA is powered-on. Default value 0.
2	PON_ADCL	**Power-on ADCL.** A 1-bit value to have power-on control for the ADC left. When this bit is logic 0: left ADC is powered-off; when this bit is logic 1: left ADC is powered-on. Default value 0.
1	PON_PGAR	**Power-on PGAR.** A 1-bit value to have power-on control for the PGA right. When this bit is logic 0: right PGA is powered-off; when this bit is logic 1: right PGA is powered-on. Default value 0.
0	PON_ADCR	**Power-on ADCR.** A 1-bit value to have power-on control for the ADC right. When this bit is logic 0: right ADC is powered-off; when this bit is logic 1: right ADC is powered-on. Default value 0.

11.4 Analog mixer settings

Table 27 Register address 03H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	AVCL5	AVCL4	AVCL3	AVCL2	AVCL1	AVCL0
Default	0	0	1	1	1	1	1	1

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	AVCR5	AVCR4	AVCR3	AVCR2	AVCR1	AVCR0
Default	0	0	1	1	1	1	1	1

Table 28 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 and 14	–	default value 00
13 to 8	AVCL[5:0]	**Analog volume control.** A 6-bit value to program the left master volume attenuation. The range is from +16.5 to −48 and −∞ dB in steps of 1.5 dB. The 16.5 dB gain is there to boost the 150 mV (RMS) which comes from for instance an FM tuner IC to 1 V (RMS) needed to drive the headphone driver full-swing. Default value 111111, see Table 29.
7 and 6	–	default value 00
5 to 0	AVCR[5:0]	**Analog volume control.** A 6-bit value to program the right master volume attenuation. The range is from +16.5 to −48 and −∞ dB in steps of 1.5 dB. The 16.5 dB gain is there to boost the 150 mV (RMS) which comes from for instance an FM tuner IC to 1 V (RMS) needed to drive the headphone driver full-swing. Default value 111111, see Table 29.

Table 29 Analog volume control

AVCL5 AVCR5	AVCL4 AVCR4	AVCL3 AVCR3	AVCL2 AVCR2	AVCL1 AVCR1	AVCL0 AVCR0	VOLUME (dB)
0	0	0	0	0	0	16.5
0	0	0	0	0	1	15
0	0	0	0	1	0	13.5
0	0	0	0	1	1	12
0	0	0	1	0	0	10.5
:	:	:	:	:	:	:
1	0	1	0	1	1	−48
1	0	1	1	0	0	−∞
:	:	:	:	:	:	:
1	1	1	1	1	1	−∞ (default)

11.5 Headphone amplifier settings

Using a 1-bit value, it is possible to disable the short-circuit protection of the headphone amplifier. This function is provided to offer maximum freedom to users, however due to the nature of this function there is the drawback of possible damage. Bits RSV12, RSV11, RSV10, RSV02, RSV01, and RSV00 are special control bits for manufacturer's evaluation and must always be kept at their default values for normal operation of UDA1380.

Table 30 Register address 04H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	RSV12	RSV11	RSV10
Default	–	–	–	–	–	0	1	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	–	RSV02	EN_SCP	RSV00
Default	–	–	–	–	–	0	1	0

Table 31 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 11	–	not used
10	RSV12	**Reserved bit.** Default value 0
9	RSV11	**Reserved bit.** Default value 1
8	RSV10	**Reserved bit.** Default value 0
7 to 3	–	not used
2	RSV02	**Reserved bit.** Default value 0
1	EN_SCP	Short circuit protection enable. A 1-bit value to enable the short circuit protection of the headphone amplifier. When this bit is set to logic 0: short-circuit protection is disabled. When this bit is set to logic 1: short-circuit protection is enabled. Default value 1. Short-circuit detection is always enabled regardless of this bit.
0	RSV00	**Reserved bit.** Default value 0

11.6 Master volume control

Table 32 Register address 10H

BIT	15	14	13	12	11	10	9	8
Symbol	MVCR_7	MVCR_6	MVCR_5	MVCR_4	MVCR_3	MVCR_2	MVCR_1	MVCR_0
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	MVCL_7	MVCL_6	MVCL_5	MVCL_4	MVCL_3	MVCL_2	MVCL_1	MVCL_0
Default	0	0	0	0	0	0	0	0

Table 33 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 8	MVCR_[7:0]	**Master volume control right.** An 8-bit value to program the right channel volume attenuation. The range is from 0 to −78 dB and −∞ dB in steps of 0.25 dB. Default value 00000000, see Table 34.
7 to 0	MVCL_[7:0]	**Master volume control left.** An 8-bit value to program the left channel volume attenuation. The range is from 0 to −78 dB and −∞ dB in steps of 0.25 dB. Default value 00000000, see Table 34.

Table 34 Master volume control bits

MVCR_7 MVCL_7	MVCR_6 MVCL_6	MVCR_5 MVCL_5	MVCR_4 MVCL_4	MVCR_3 MVCL_3	MVCR_2 MVCL_2	MVCR_1 MVCL_1	MVCR_0 MVCL_0	VOLUME (dB)
0	0	0	0	0	0	0	0	0 (default)
0	0	0	0	0	0	0	1	−0.25
0	0	0	0	0	0	1	0	−0.50
0	0	0	0	0	0	1	1	−0.75
0	0	0	0	0	1	0	0	−1
:	:	:	:	:	:	:	:	:
1	1	0	0	1	0	0	0	−50
1	1	0	0	1	1	0	0	−51
1	1	0	0	1	1	0	1	−51.25
1	1	0	0	1	1	1	0	−51.50
1	1	0	0	1	1	1	1	−51.75
1	1	0	1	0	0	0	0	−52
1	1	0	1	0	1	0	0	−54
1	1	0	1	1	0	0	0	−56
:	:	:	:	:	:	:	:	:
1	1	1	0	1	1	0	0	−66
1	1	1	1	0	0	0	0	−69
1	1	1	1	0	1	0	0	−72
1	1	1	1	1	0	0	0	−78
1	1	1	1	1	1	0	0	−∞

11.7 Mixer volume control

Table 35 Register address 11H

BIT	15	14	13	12	11	10	9	8
Symbol	VC2_7	VC2_6	VC2_5	VC2_4	VC2_3	VC2_2	VC2_1	VC2_0
Default	1	1	1	1	1	1	1	1

BIT	7	6	5	4	3	2	1	0
Symbol	VC1_7	VC1_6	VC1_5	VC1_4	VC1_3	VC1_2	VC1_1	VC1_0
Default	0	0	0	0	0	0	0	0

Table 36 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 8	VC2_[7:0]	**Digital mixer volume control.** An 8-bit value to program the channel 2 volume attenuation. The range is 0 to −72 dB and −∞ dB in steps of 0.25 dB. Default value for channel 2 is 11111111, see Table 37.
7 to 0	VC1_[7:0]	**Digital mixer volume control.** An 8-bit value to program the channel 1 volume attenuation. The range is 0 to −72 dB and −∞ dB in steps of 0.25 dB. Default value for channel 1 is 00000000, see Table 37.

Table 37 Digital mixer volume control

VC2_7 VC1_7	VC2_6 VC1_6	VC2_5 VC1_5	VC2_4 VC1_4	VC2_3 VC1_3	VC2_2 VC1_2	VC2_1 VC1_1	VC2_0 VC1_0	VOLUME (dB)
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	−0.25
0	0	0	0	0	0	1	0	−0.50
0	0	0	0	0	0	1	1	−0.75
0	0	0	0	0	1	0	0	−1
:	:	:	:	:	:	:	:	:
1	0	1	1	0	1	0	0	−45
1	0	1	1	0	1	0	1	−45.25
1	0	1	1	0	1	1	0	−45.50
1	0	1	1	0	1	1	1	−45.75
1	0	1	1	1	0	0	0	−46
1	0	1	1	1	1	0	0	−48
1	1	0	0	0	0	0	0	−50
:	:	:	:	:	:	:	:	:
1	1	0	1	0	1	0	0	−60
1	1	0	1	1	0	0	0	−63
1	1	0	1	1	1	0	0	−66
1	1	1	0	0	0	0	0	−72

VC2_7 VC1_7	VC2_6 VC1_6	VC2_5 VC1_5	VC2_4 VC1_4	VC2_3 VC1_3	VC2_2 VC1_2	VC2_1 VC1_1	VC2_0 VC1_0	VOLUME (dB)
1	1	1	0	0	1	0	0	−∞
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	0	0	−∞

11.8 Mode, bass boost and treble

Table 38 Register address 12H

BIT	15	14	13	12	11	10	9	8
Symbol	M1	M0	TRL1	TRL0	BBL3	BBL2	BBL1	BBL0
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	TRR1	TRR0	BBR3	BBR2	BBR1	BBR0
Default	0	0	0	0	0	0	0	0

Table 39 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 and 14	M[1:0]	**Flat/minimum/maximum setting.** A 2-bit value to program the mode of the sound processing filters of bass boost and treble. Default value 00, see Table 40.
13 and 12	TRL[1:0]	**Treble setting left.** A 2-bit value to program the mode of the sound processing filter of treble. The used setting depends on the bits M1 and M0. Default value 00, see Table 41.
11 to 8	BBL[3:0]	**Bass boost setting left.** A 4-bit value to program the bass boost setting, which can be set for left and right independently. The used set depends on the bits M1 and M0. Default value 0000, see Table 42.
7 and 6	–	default value 00
5 and 4	TRR[1:0]	**Treble setting right.** A 2-bit value to program the mode of the sound processing filter of treble. Default value 00, see Table 41.
3 to 0	BBR[3:0]	**Bass boost setting right.** A 4-bit value to program the bass boost setting, which can be set for left and right independently. The used set depends on the mode bits. Default value 0000, see Table 42.

Table 40 Flat/minimum/maximum setting bits

M1	M0	Mode
0	0	flat (default)
0	1	minimum
1	0	minimum
1	1	maximum

Table 41 Treble setting bits

TRL1 TRR1	TRL0 TRR0	FLAT SET (dB)	MINIMUM SET (dB)	MAXIMUM SET (dB)
0	0	0 (default)	0 (default)	0 (default)
0	1	0	2	2
1	0	0	4	4
1	1	0	6	6

Table 42 Bass boost setting bits

BBL3 BBR3	BBL2 BBR2	BBL1 BBR1	BBL0 BBR0	FLAT SET (dB)	MINIMUM SET (dB)	MAXIMUM SET (dB)
0	0	0	0	0 (default)	0 (default)	0 (default)
0	0	0	1	0	2	2
0	0	1	0	0	4	4
0	0	1	1	0	6	6
0	1	0	0	0	8	8
0	1	0	1	0	10	10
0	1	1	0	0	12	12
0	1	1	1	0	14	14
1	0	0	0	0	16	16
1	0	0	1	0	18	18
1	0	1	0	0	18	20
1	0	1	1	0	18	22
1	1	0	0	0	18	24
1	1	0	1	0	18	24
1	1	1	0	0	18	24
1	1	1	1	0	18	24

11.9 Master mute, channel de-emphasis and mute

Table 43 Register address 13H

BIT	15	14	13	12	11	10	9	8
Symbol	–	MTM	–	–	MT2	DE2_2	DE2_1	DE2_0
Default	0	1	0	0	1	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	MT1	DE1_2	DE1_1	DE1_0
Default	0	0	0	0	0	0	0	0

Table 44 Description of register bits

BIT	SYMBOL	DESCRIPTION
15	–	default value 0
14	MTM	**Master mute.** A 1-bit value to enable the digital mute for the master. When this bit is logic 0: no soft mute of master. When this bit is logic 1: soft mute of master. Default value 1.
13 and 12	–	default value 00
11	MT2	**Channel 2 mute.** A 1-bit value to enable the digital mute for channel 2. After enabling the mixer, bit MT2 must be set to logic 0. When this bit is logic 0: no soft mute of channel 2. When this bit is logic 1: soft mute of channel 2. Default value 1 (meaning that channel 2 is always muted, even when the mixer is enabled).
10 to 8	DE2_[2:0]	**De-emphasis.** A 3-bit value to enable the digital de-emphasis filter for channel 2. Default value 000, see Table 45.
7 to 4	–	default value 0000
3	MT1	**Channel 1 mute.** A 1-bit value to enable the digital mute for channel 1. When this bit is logic 0: no soft mute of channel 1. When this bit is logic 1: soft mute of channel 1. Default value 0.
2 to 0	DE1_[2:0]	**De-emphasis.** A 3-bit value to enable the digital de-emphasis filter for channel 1. Default value 000, see Table 45.

Table 45 De-emphasis selection bits

DE2_2 DE1_2	DE2_1 DE1_1	DE2_0 DE1_0	FUNCTION
0	0	0	off (default)
0	0	1	32 kHz
0	1	0	44.1 kHz
0	1	1	48 kHz
1	0	0	96 kHz

11.10 Mixer, silence detector and oversampling settings

Table 46 Register address 14H

BIT	15	14	13	12	11	10	9	8
Symbol	DA_POL_INV	SEL_NS	MIX_POS	MIX	–	–	–	–
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	SILENCE	SDET_ON	SD_VALUE1	SD_VALUE0	–	–	OS1	OS0
Default	0	0	0	0	0	0	0	0

Table 47 Description of register bits

BIT	SYMBOL	DESCRIPTION
15	DA_POL_INV	**DAC polarity control.** A 1-bit value to control the signal polarity of the DAC output signal. When this bit is logic 0: DAC output not inverted. When this bit is logic 1: DAC output inverted. Default value 0.
14	SEL_NS	**Noise shaper order select.** A 1-bit value to select between the 3rd-order and the 5th-order noise shaper. When this bit is logic 0: select 3rd-order noise shaper. When this bit is logic 1: select 5th-order noise shaper. Default value 0.
13	MIX_POS	**Mixer signal control.** A 2-bit value to select the digital mixer settings inside the interpolation filter. Default value 0. By default the mixer is off, see Table 48.
12	MIX	
11 to 8	–	default value 0000
7	SILENCE	**Silence mode.** A 1-bit value to force the DAC output to silence. When this bit is logic 0: no overruling. The setting of the FSDAC silence switch depends on the status of the digital silence detector circuit and the master_mute status. When this bit is logic 1: overruling. The FSDAC silence switch is activated, independent of the status of the digital silence detector circuit or the master_mute status. Default value 0.
6	SDET_ON	**Silence detector enable.** A 1-bit value to enable the digital silence detector. When this bit is logic 0: silence detection circuit disabled. When this bit is logic 1: silence detection circuit enabled. Default value 0.
5 and 4	SD_VALUE[1:0]	**Silence detector settings.** A 2-bit value to program the silence detector, the number of ‘ZERO’ samples counted before the silence detector signals whether there has been digital silence. Default value 00, see Table 49.
3 and 2	–	default value 00
1 and 0	OS[1:0]	**Oversampling input settings.** A 2-bit value to select the oversampling input mode. Default value 00, see Table 50.

Table 48 Mixer signal control setting bits

MIX_POS	MIX	FUNCTION
0	0	no mixing; default
1	0	volume of channel 1 is forced to 0 dB and volume of channel 2 is forced to $-\infty$ dB
0	1	mixing is done before the sound processing: input signals are automatically scaled by 6 dB in order to prevent clipping during adding; after the addition, the 6 dB scaling is compensated
1	1	mixing is done after the sound processing: input signals are automatically scaled in order to prevent clipping during adding

Table 49 Silence detector setting bits

SD_VALUE1	SD_VALUE0	FUNCTION
0	0	3200 samples; default
0	1	4800 samples
1	0	9600 samples
1	1	19200 samples

Table 50 Oversampling input setting bits

OS1	OS0	FUNCTION
0	0	single-speed input is normal input; mixing possible; default
0	1	double-speed input is after first half-band; no mixing possible
1	0	quad-speed input is in front of noise shaper; no mixing possible
1	1	reserved

11.11 Decimator volume control

Table 51 Register address 20H

BIT	15	14	13	12	11	10	9	8
Symbol	ML_DEC7	ML_DEC6	ML_DEC5	ML_DEC4	ML_DEC3	ML_DEC2	ML_DEC1	ML_DEC0
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	MR_DEC7	MR_DEC6	MR_DEC5	MR_DEC4	MR_DEC3	MR_DEC2	MR_DEC1	MR_DEC0
Default	0	0	0	0	0	0	0	0

Table 52 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 8	ML_DEC[7:0]	**ADC volume control left.** An 8-bit value to program the gain of the decimator for left and right independently. The ranges are +24 to −63.5 dB and $-\infty$ dB in steps of 0.5 dB. The default setting is 0 dB (value 00000000), see Table 53.
7 to 0	MR_DEC[7:0]	**ADC volume control right.** An 8-bit value to program the gain of the decimator for left and right independently. The ranges are +24 to −63.5 dB and $-\infty$ dB in steps of 0.5 dB. The default setting is 0 dB (value 00000000), see Table 53.

Table 53 ADC volume control setting bits

ML_DEC7 MR_DEC7	ML_DEC6 MR_DEC6	ML_DEC5 MR_DEC5	ML_DEC4 MR_DEC4	ML_DEC3 MR_DEC3	ML_DEC2 MR_DEC2	ML_DEC1 MR_DEC1	ML_DEC0 MR_DEC0	GAIN (dB)
0	0	1	1	0	0	0	0	24
0	0	1	0	1	1	1	1	23.5
0	0	1	0	1	1	1	0	23
:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	1	0.5
0	0	0	0	0	0	0	0	0 (default)
1	1	1	1	1	1	1	1	−0.5
:	:	:	:	:	:	:	:	:
1	0	0	0	0	1	0	0	−62
1	0	0	0	0	0	1	1	−62.5
1	0	0	0	0	0	1	0	−63
1	0	0	0	0	0	0	1	−63.5
1	0	0	0	0	0	0	0	−∞

11.12 PGA settings and mute

Table 54 Register address 21H

BIT	15	14	13	12	11	10	9	8
Symbol	MT_ADC	–	–	–	PGA_GAIN CTRLR3	PGA_GAIN CTRLR2	PGA_GAIN CTRLR1	PGA_GAIN CTRLR0
Default	1	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	PGA_GAIN CTRLL3	PGA_GAIN CTRLL2	PGA_GAIN CTRLL1	PGA_GAIN CTRLL0
Default	0	0	0	0	0	0	0	0

Table 55 Description of register bits

BIT	SYMBOL	DESCRIPTION
15	MT_ADC	**Decimator mute.** A 1-bit value to enable the digital linear mute. When this bit is logic 0: no muting. When this bit is logic 1: muting. Default value 1.
14 to 12	–	default value 000

BIT	SYMBOL	DESCRIPTION
11 to 8	PGA_GAIN CTRLR[3:0]	**ADC input amplifier right gain settings.** A 4-bit value to program the gain of the input amplifier. There are nine settings, for a gain range from 0 to 24 dB in steps of 3 dB. The gain control of the PGA is independent for left and right. Default value 0000, see Table 56.
7 to 4	–	default value 0
3 to 0	PGA_GAIN CTRLL[3:0]	**ADC input amplifier left gain settings.** A 4-bit value to program the gain of the input amplifier. There are nine settings, for a gain range from 0 to 24 dB in steps of 3 dB. The gain control of the PGA is independent for left and right. Default value 0000, see Table 56.

Table 56 ADC input amplifier PGA gain setting bits

PGA_GAINCTRLR3 PGA_GAINCTRLL3	PGA_GAINCTRLR2 PGA_GAINCTRLL2	PGA_GAINCTRLR1 PGA_GAINCTRLL1	PGA_GAINCTRLR0 PGA_GAINCTRLL0	PGA_GAIN (dB)
0	0	0	0	0 (default)
0	0	0	1	3
0	0	1	0	6
0	0	1	1	9
0	1	0	0	12
0	1	0	1	15
0	1	1	0	18
0	1	1	1	21
1	X	X	X	24

11.13 ADC settings

Table 57 Register address 22H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	ADCPOL_ INV	VGA_CTRL3	VGA_CTRL2	VGA_CTRL1	VGA_CTRL0
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	SEL_LNA	SEL_MIC	SKIP_DCFIL	EN_DCFIL
Default	0	0	0	0	0	0	1	0

Table 58 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 13	–	default value 000
12	ADCPOL_INV	**ADC polarity control.** A 1-bit value to select ADC polarity. When this bit is logic 0: polarity of ADC non-inverting. When this bit is logic 1: polarity of ADC inverting. Default value 0.
11 to 8	VGA_CTRL[3:0]	**Microphone input VGA gain settings.** A 4-bit value to program the gain of the LNA in the microphone input channel. The range is 0 to 30 dB in steps of 2 dB. Default value 0000, see Table 59.

BIT	SYMBOL	DESCRIPTION
7 to 4	–	default value 0000
3	SEL_LNA	**Line input select.** A 1-bit value to set the multiplexer in the analog front-end to select between the LNA or the enable-in input for the left ADC. When this bit is logic 0: select line input. When this bit is logic 1: select LNA for the left ADC. Default value 0.
2	SEL_MIC	**Microphone input select.** A 1-bit value to set the multiplexer at the ADC right channel output (on bit-stream level) which selects either the right channel data or the left channel data. In case only the microphone input is used, the microphone signal can be applied to the decimator for both left and right. When this bit is logic 0: select right channel ADC. When this bit is logic 1: select left channel ADC (for instance for microphone input). Default value 0.
1	SKIP_DCFIL	**DC filter bypass.** A 1-bit value set to skip the DC filter which is just before the decimator. This DC filter is there to compensate for the DC offset added in the ADC (to remove idle tones from the audio band). This DC signal added (the DC dither) must not be amplified in order to prevent clipping. Therefore this DC offset is removed first. When this bit is logic 0: DC filter enabled. When this bit is logic 1: DC filter bypassed. Default value 1.
0	EN_DCFIL	**DC filter enable.** A 1-bit value set to enable the DC filter which is at the output of the decimator (running at $1f_s$). When this bit is logic 0: DC filter disabled. When this bit is logic 1: DC filter enabled. Default value 0.

Table 59 Microphone input VGA gain setting bits

VGA_CTRL3	VGA_CTRL2	VGA_CTRL1	VGA_CTRL0	LNA GAIN (dB)
0	0	0	0	0 (default)
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	8
0	1	0	1	10
0	1	1	0	12
0	1	1	1	14
1	0	0	0	16
1	0	0	1	18
1	0	1	0	20
1	0	1	1	22
1	1	0	0	24
1	1	0	1	26
1	1	1	0	28
1	1	1	1	30

11.14 AGC settings

Table 60 Register address 23H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	AGC_TIME2	AGC_TIME1	AGC_TIME0
Default	0	0	0	0	0	0	0	0

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	–	AGC_LEVEL1	AGC_LEVEL0	–	AGC_EN
Default	0	0	0	0	0	0	0	0

Table 61 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 11	–	Default value 00000.
10 to 8	AGC_TIME[2:0]	**AGC time constant settings.** A 3-bit value to set the AGC time constants, being the attack and decay time constants. The given constants are for 44.1 and 8 kHz sampling frequencies, and must be scaled either down or up according to the sampling frequency used. Default value 000, see Table 62.
7 to 4	–	default value 0000
3 and 2	AGC_LEVEL[1:0]	**AGC target level settings.** A 2-bit value to set the AGC target level. Default value 00, see Table 63.
1	–	default value 0
0	AGC_EN	**AGC enable control.** A 1-bit value to enable or disable the AGC. When the AGC is enabled, the bit SKIP_DCFIL must be set to logic 0 to avoid disturbance on the output signal due to the DC offset added in the ADC. When this bit is logic 0: AGC off, manual gain control via the left and right decimator volume control. When this bit is logic 1: AGC enabled, with manual microphone gain setting via VGA. Default value 0.

Table 62 AGC time constant setting bits

AGC_TIME2	AGC_TIME1	AGC_TIME0	AGC SETTING			
			44.1 kHz SAMPLING		8 kHz SAMPLING	
			ATTACK TIME (ms)	DECAY TIME (ms)	ATTACK TIME (ms)	DECAY TIME (ms)
0	0	0	11	100	61	551 (default)
0	0	1	16	100	88.2	551
0	1	0	11	200	61	1102
0	1	1	16	200	88.2	1102
1	0	0	21	200	116	1102
1	0	1	11	400	61	2205
1	1	0	16	400	88.2	2205
1	1	1	21	400	116	2205

Table 63 AGC target level setting bits

AGC_LEVEL1	AGC_LEVEL0	AGC TARGET LEVEL VALUE (dBFS)
0	0	−5.5 (default)
0	1	−8
1	0	−11.5
1	1	−14

11.15 Restore L3 default values (software reset)

Table 64 Register address 7FH

BIT	15	14	13	12	11	10	9	8
Default value	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Default value	–	–	–	–	–	–	–	–

11.16 Headphone driver and interpolation filter (read-out)

Table 65 Register address 18H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	HP_STCTV	HP_STCTL	HP_STCTR

BIT	7	6	5	4	3	2	1	0
Symbol	–	SDETR2	SDETL2	SDETR1	SDETL1	MUTE_ STATE_M	MUTE_ STATE_CH2	MUTE_ STATE_CH1

Table 66 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 11	–	not used
10	HP_STCTV	**Headphone driver short-circuit detection.** When this bit is logic 0: headphone driver is not short-circuit protected. When this bit is logic 1: headphone driver short-circuit protection is activated.
9	HP_STCTL	**Left headphone driver short-circuit detection.** When this bit is logic 0: left channel headphone driver is not short-circuit protected. When this bit is logic 1: left channel headphone driver short-circuit protection is activated.
8	HP_STCTR	**Right headphone driver short-circuit detection.** When this bit is logic 0: right channel headphone driver not short-circuit protected. When this bit is logic 1: right channel headphone driver short-circuit protection activated.
7	–	not used
6	SDETR2	**Interpolator silence detect channel 2 right.** When this bit is logic 0: interpolator on channel 2 right input has detected no silence. When this bit is logic 1: interpolator on channel 2 right input has detected silence.
5	SDETL2	**Interpolator silence detect channel 2 left.** When this bit is logic 0: interpolator on channel 2 left input has detected no silence. When this bit is logic 1: interpolator on channel 2 left input has detected silence.

BIT	SYMBOL	DESCRIPTION
4	SDETR1	**Interpolator silence detect channel 1 right.** When this bit is logic 0: interpolator on channel 1 right input has detected no silence. When this bit is logic 1: interpolator on channel 1 right input has detected silence.
3	SDETL1	**Interpolator silence detect channel 1 left.** When this bit is logic 0: interpolator on channel 1 left input has detected no silence. When this bit is logic 1: interpolator on channel 1 left input has detected silence.
2	MUTE_STATE_M	**Interpolator muting.** A 1-bit value which signals whether the interpolator has reached mute or not. When this bit is logic 0: interpolator is not muted. When this bit is logic 1: interpolator is muted.
1	MUTE_STATE_CH2	**Interpolator muting channel 2.** When this bit is logic 0: interpolator channel 2 is not muted. When this bit is logic 1: interpolator channel 2 is muted.
0	MUTE_STATE_CH1	**Interpolator muting channel 1.** When this bit is logic 0: interpolator channel 1 is not muted. When this bit is logic 1: interpolator channel 1 is muted.

11.17 Decimator read-out

Table 67 Register address 28H

BIT	15	14	13	12	11	10	9	8
Symbol	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Symbol	–	–	–	AGC_STAT	–	MT_ADC_STAT	–	OVERFLOW

Table 68 Description of register bits

BIT	SYMBOL	DESCRIPTION
15 to 5	–	not used
4	AGC_STAT	**AGC gain status.** A 1-bit value which signals whether the AGC gain exceeds 8 dB or not. Only valid when the AGC is switched on. When this bit is logic 0: AGC gain <8 dB. When this bit is logic 1: AGC gain ≥8 dB.
3	–	not used
2	MT_ADC_STAT	**Decimator mute.** A 1-bit value which signals whether the decimator has reached mute or not. When this bit is logic 0: decimator has not muted. When this bit is logic 1: decimator has muted.
1	–	not used
0	OVERFLOW	**Digital output overflow detection.** A 1-bit value which signals whether the digital output amplitude exceeds −1.16 dB or not. When this bit is logic 0: no overflow detected (read-out). When this bit is logic 1: overflow detected (read-out).

12 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	4	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		−65	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{es}	electrostatic handling voltage	note 2	−2000	+2000	V
		note 3	−200	+200	V
$I_{lu(prot)}$	latch-up protection current	T_{amb} = 125 °C; V_{DD} = 3.6 V	–	100	mA
$I_{sc(DAC)}$	short-circuit current of DAC	T_{amb} = 0 °C; V_{DD} = 3 V; note 4			
		output short-circuited to $V_{SSA(DA)}$	–	450	mA
		output short-circuited to $V_{DDA(DA)}$	–	325	mA

Notes

1. All supply connections must be made to the same power supply.
2. Equivalent to discharging a 100 pF capacitor via a 1.5 kΩ series resistor.
3. Equivalent to discharging a 200 pF capacitor via a 0.75 μH series inductor.
4. DAC operation after short-circuiting cannot be warranted.

13 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is advised to take normal precautions appropriate to handling MOS devices.

14 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
	TSSOP32 package		115	K/W
	HVQFN32 package		35	K/W

15 QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611D"*.

16 DC CHARACTERISTICS

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = V_{DDA(HP)} = 3.0$ V; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; note 1						
$V_{DDA(AD)}$	ADC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(DA)}$	DAC analog supply voltage		2.4	3.0	3.6	V
$V_{DDA(HP)}$	headphone analog supply voltage	note 2	2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
$I_{DDA(AD)}$	ADC analog supply current	one ADC and microphone amplifier enabled; $f_s = 48$ kHz	–	4.5	–	mA
		two ADCs and PGA enabled; $f_s = 48$ kHz	–	7.0	–	mA
		all ADCs and PGAs power-down, but AVC activated; $f_s = 48$ kHz	–	3.3	–	mA
		all ADCs, PGAs and LNA power-down; $f_s = 48$ kHz	–	1.0	–	μA
$I_{DDA(DA)}$	DAC analog supply current	operating mode; $f_s = 48$ kHz	–	3.4	–	mA
		Power-down mode; $f_s = 48$ kHz	–	0.1	–	μA
$I_{DDA(HP)}$	headphone analog supply current	no signal applied (quiescent current)	–	0.9	–	mA
		Power-down mode	–	0.1	–	μA
I_{DDD}	digital supply current	operating mode; $f_s = 48$ kHz	–	10.0	–	mA
		playback mode; $f_s = 48$ kHz	–	5.0	–	mA
		record mode; $f_s = 48$ kHz	–	6.0	–	mA
		Power-down mode; $f_s = 48$ kHz	–	1.0	–	μA
$I_{DD(tot)}$	total supply current	playback mode (without headphone); $f_s = 48$ kHz	–	8	–	mA
		playback mode (with headphone); no signal; $f_s = 48$ kHz	–	9	–	mA
		record mode (audio); $f_s = 48$ kHz	–	13	–	mA
		record mode (speech); $f_s = 48$ kHz	–	10	–	mA
		record mode (audio and speech); $f_s = 48$ kHz	–	13	–	mA
		fully operating; $f_s = 48$ kHz	–	23	–	mA
		signal mix-in operating, using FSDAC, AVC (with headphone); no signal; $f_s = 48$ kHz	–	12	–	mA
		Power-down mode; $f_s = 48$ kHz	–	2	–	μA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input pins (5 V tolerant TTL compatible)						
V_{IH}	HIGH-level input voltage		2.0	–	5.5	V
V_{IL}	LOW-level input voltage		−0.5	–	+0.8	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	10	pF
Digital output pins						
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
Reference voltage						
V_{REF}	reference voltage	with respect to $V_{SSA(AD)}$; note 3	$0.45V_{DDA}$	$0.5V_{DDA}$	$0.55V_{DDA}$	V
$R_{o(VREF)}$	output resistance on pin V_{REF}		–	12.5	–	kΩ
Analog-to-digital converter						
V_{ADCP}	positive reference voltage of the ADC		–	$V_{DDA(AD)}$	–	V
V_{ADCN}	negative reference voltage of the ADC		–	0	–	V
R_i	input resistance		–	12	–	kΩ
C_i	input capacitance		–	24	–	pF
Digital-to-analog converter						
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 4	–	–	50	pF
Power consumption (supply voltage 3.0 V; f_s = 48 kHz)						
P_{tot}	total power dissipation	playback mode (without headphone)	–	24	–	mW
		playback mode (with headphone)	–	27	–	mW
		record mode (audio)	–	39	–	mW
		record mode (speech)	–	30	–	mW
		record mode (audio and speech)	–	40	–	mW
		full operation	–	69	–	mW
		Power-down mode	–	6	–	μW

Notes

1. All supply connections must be made to the same power supply unit.
2. When the supply voltages are below 2.7 V and the headphone load impedance is 16 Ω, it is recommended to limit the DAC and the headphone output to less than -2 dB, otherwise clipping may occur.
3. $V_{DDA} = V_{DDA(DA)} = V_{DDA(AD)}$.
4. When higher capacitive loads must be driven, a 100 Ω resistor must be connected in series with the DAC output in order to prevent oscillations in the output operational amplifier.

17 AC CHARACTERISTICS

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = V_{DDA(HP)} = 3.0$ V; $f_i = 1$ kHz at −1 dB; $T_{amb} = 25$ °C; $R_L = 5$ kΩ; all voltages measured with respect to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Analog-to-digital converter						
D_o	digital output level	0 dB setting; $V_{i(rms)} = 1.0$ V	−1.5	−1	−0.5	dBFS
		3 dB setting; $V_{i(rms)} = 708$ mV	−1.5	−1	−0.5	dBFS
		6 dB setting; $V_{i(rms)} = 501$ mV	−1.5	−1	−0.5	dBFS
		9 dB setting; $V_{i(rms)} = 354$ mV	−1.5	−1	−0.5	dBFS
		12 dB setting; $V_{i(rms)} = 252$ mV	−1.5	−1	−0.5	dBFS
		15 dB setting; $V_{i(rms)} = 178$ mV	−1.5	−1	−0.5	dBFS
		18 dB setting; $V_{i(rms)} = 125$ mV	−1.5	−1	−0.5	dBFS
		21 dB setting; $V_{i(rms)} = 89$ mV	−1.5	−1	−0.5	dBFS
		24 dB setting; $V_{i(rms)} = 63$ mV	−1.5	−1	−0.5	dBFS
ΔV_i	unbalance between channels		–	<0.1	–	dB
(THD + N)/S_{48}	total harmonic distortion-plus-noise to signal at $f_s = 48$ kHz	at −1 dBFS				
		0 dB setting	–	−85	−80	dB
		3 dB setting	–	−85	–	dB
		6 dB setting	–	−85	–	dB
		9 dB setting	–	−85	–	dB
		12 dB setting	–	−84	–	dB
		15 dB setting	–	−83	–	dB
		18 dB setting	–	−82	–	dB
		21 dB setting	–	−80	–	dB
		24 dB setting	–	−78	–	dB
		at −60 dBFS; A-weighted				
		0 dB setting	–	−37	−32	dB
		3 dB setting	–	−36	–	dB
		6 dB setting	–	−36	–	dB
		9 dB setting	–	−36	–	dB
		12 dB setting	–	−35	–	dB
		15 dB setting	–	−34	–	dB
		18 dB setting	–	−33	–	dB
		21 dB setting	–	−32	–	dB
		24 dB setting	–	−30	–	dB
S/N_{48}	signal-to-noise ratio at $f_s = 48$ kHz	$V_i = 0$ V; A-weighted	92	97	–	dB
α_{cs}	channel separation		–	100	–	dB
PSRR	power supply rejection ratio	$f_{ripple} = 1$ kHz; $V_{ripple} = 30$ mV (p-p)	–	80	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
LNA input plus analog-to-digital converter						
$V_{i(rms)}$	input voltage (RMS value)	at 0 dBFS digital output; 2.2 kΩ source impedance	–	–	35	mV
$(THD+N)/S_{48}$	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at 0 dB	–	−74	–	dB
		at −60 dB; A-weighted	–	−25	–	dB
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	V_i = 0 V; A-weighted	–	85	–	dB
α_{cs}	channel separation		–	70	–	dB
Digital-to-analog converter						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dBFS digital input; note 1	–	0.9	–	V
ΔV_o	unbalance between channels		–	<0.1	–	dB
$(THD+N)/S_{48}$	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at 0 dB	–	−85	−80	dB
		at −60 dB; A-weighted	–	−40	−35	dB
$(THD+N)/S_{96}$	total harmonic distortion-plus-noise to signal ratio at f_s = 96 kHz	at 0 dB	–	−80	−75	dB
		at −60 dB; A-weighted	–	−37	−32	dB
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	code = 0; A-weighted	95	100	–	dB
S/N_{96}	signal-to-noise ratio at f_s = 96 kHz	code = 0; A-weighted	92	97	–	dB
α_{cs}	channel separation		–	90	–	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 30 mV (p-p)	–	60	–	dB
Headphone driver						
$P_{o(rms)}$	output power (RMS value)	at 0 dBFS digital input, assuming R_L = 16 Ω	30	35	40	mW
$(THD+N)/S_{48}$	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at 0 dB; R_L = 16 Ω; note 2	–	−60	−52	dB
		at 0 dB; R_L = 5 kΩ	–	−82	−77	dB
		at −60 dB; A-weighted	–	−33	−27	dB
α_{cs}	channel separation	R_L = 16 Ω using pin $V_{REF(HP)}$; no DC decoupling capacitors; note 3	55	60	–	dB
		R_L = 16 Ω single-ended application with DC decoupling capacitors (100 μF typical)	63	68	–	dB
		R_L = 32 Ω single-ended application with DC decoupling capacitors (100 μF typical)	69	74	–	dB
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	code = 0; A-weighted	87	93	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
AVC (line input via ADC input, output on line output and headphone driver)						
$V_{i(rms)}$	input voltage (RMS value)		–	150	–	mV
(THD+N)/S_{48}	total harmonic distortion-plus-noise to signal ratio at f_s = 48 kHz	at 0 dB	–	–80	–	dB
		at –60 dB; A-weighted	–	–28	–	dB
S/N_{48}	signal-to-noise ratio at f_s = 48 kHz	V_i = 0 V; A-weighted	–	87	–	dB
α_{cs}	channel separation		–	82	–	dB

Notes

1. The output voltage of the DAC is proportional to the DAC power supply voltage.
2. When the supply voltages are below 2.7 V and the headphone load impedance is 16 Ω, it is recommended to limit the DAC and the headphone output to less than -2 dB, otherwise clipping may occur.
3. Channel separation performance is measured at the IC pin.

18 TIMING

$V_{DDD} = V_{DDA(AD)} = V_{DDA(DA)} = V_{DDA(HP)}$ = 2.7 to 3.6 V; T_{amb} = −20 to +85 °C; all voltages referenced to ground; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock timing; note 1						
T_{sys}	system clock cycle time	$f_{sys} = 256f_s$	35	81	250	ns
		$f_{sys} = 384f_s$	23	54	170	ns
		$f_{sys} = 512f_s$	17	41	130	ns
		$f_{sys} = 768f_s$	17	27	90	ns
t_{CWL}	system clock LOW time	$f_{sys} < 19.2$ MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
t_{CWH}	system clock HIGH time	$f_{sys} < 19.2$ MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		$f_{sys} \geq 19.2$ MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
Serial interface input/output data timing (see Fig.17)						
f_{BCK}	bit clock frequency		–	–	$128f_s$	Hz
$T_{cy(BCK)}$	bit clock cycle time		–	–	$^1/_{128}T_{cy(s)}$ (2)	s
t_{BCKH}	bit clock HIGH time		30	–	–	ns
t_{BCKL}	bit clock LOW time		30	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{su(WS)}$	word select set-up time		10	–	–	ns
$t_{h(WS)}$	word select hold time		10	–	–	ns
$t_{su(DATAI)}$	data input set-up time		10	–	–	ns
$t_{h(DATAI)}$	data input hold time		10	–	–	ns
$t_{h(DATAO)}$	data output hold time		0	–	–	ns
$t_{d(DATAO-BCK)}$	data output to bit clock delay		–	–	30	ns
$t_{d(DATAO-WS)}$	data output to word select delay		–	–	30	ns
L3-bus interface timing (see Figs 18 **and** 19**)**						
t_r	rise time	note 3	–	–	10	ns/V
t_f	fall time	note 3	–	–	10	ns/V
$T_{cy(CLK)L3}$	L3CLOCK cycle time	note 4	500	–	–	ns
$t_{CLK(L3)H}$	L3CLOCK HIGH time	note 4	250	–	–	ns
$t_{CLK(L3)L}$	L3CLOCK LOW time	note 4	250	–	–	ns
$t_{su(L3)A}$	L3MODE set-up time in address mode		190	–	–	ns
$t_{h(L3)A}$	L3MODE hold time in address mode		190	–	–	ns
$t_{su(L3)D}$	L3MODE set-up time in data transfer mode		190	–	–	ns
$t_{h(L3)D}$	L3MODE hold time in data transfer mode		190	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{stp(L3)}$	L3MODE stop time in data transfer mode		190	–	–	ns
$t_{su(L3)DA}$	L3DATA set-up time in address and data transfer mode		190	–	–	ns
$t_{h(L3)DA}$	L3DATA hold time in address and data transfer mode		30	–	–	ns
$t_{d(L3)R}$	L3DATA delay time in data transfer mode		0	–	50	ns
$t_{dis(L3)R}$	L3DATA disable time for read data		0	–	50	ns
I^2C-bus interface timing; see Fig.20						
f_{SCL}	SCL clock frequency		0	–	400	kHz
t_{LOW}	SCL LOW time		1.3	–	–	μs
t_{HIGH}	SCL HIGH time		0.6	–	–	μs
t_r	rise time SDA and SCL	note 5	$20 + 0.1C_b$	–	300	ns
t_f	fall time SDA and SCL	note 5	$20 + 0.1C_b$	–	300	ns
$t_{HD;STA}$	hold time START condition	note 6	0.6	–	–	μs
$t_{SU;STA}$	set-up time repeated START		0.6	–	–	μs
$t_{SU;STO}$	set-up time STOP condition		0.6	–	–	μs
t_{BUF}	bus free time between a STOP and START condition		1.3	–	–	μs
$t_{SU;DAT}$	data set-up time		100	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	μs
t_{SP}	pulse width of spikes	note 7	0	–	50	ns
C_b	capacitive load for each bus line		–	–	400	pF

Notes

1. The typical value of the timing is specified at 48 kHz sampling frequency (see Fig.16).
2. $T_{cy(s)}$ is the cycle time of the sample frequency.
3. In order to prevent digital noise interfering with the L3-bus communication, it is best to have the rise and fall times as short as possible.
4. When the sampling frequency is below 32 kHz, the L3CLOCK cycle must be limited to $\frac{1}{64fs}$ cycle.
5. C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.
6. After this period, the first clock pulse is generated.
7. To be suppressed by the input filter.

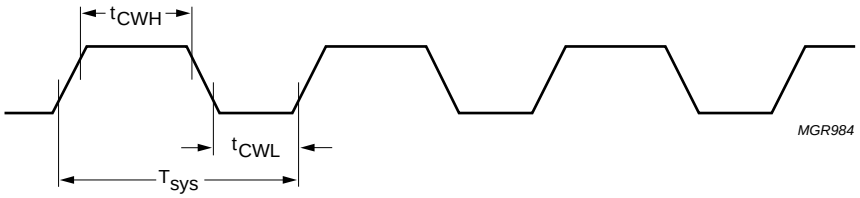


Fig.16 Timing of system clock.

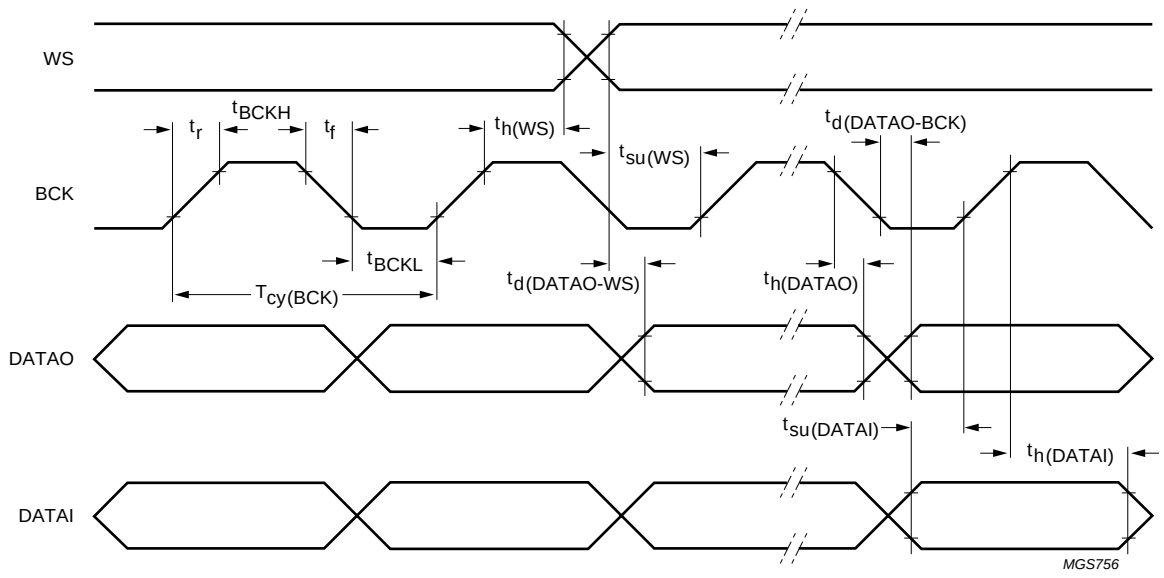


Fig.17 Serial interface input data timing.

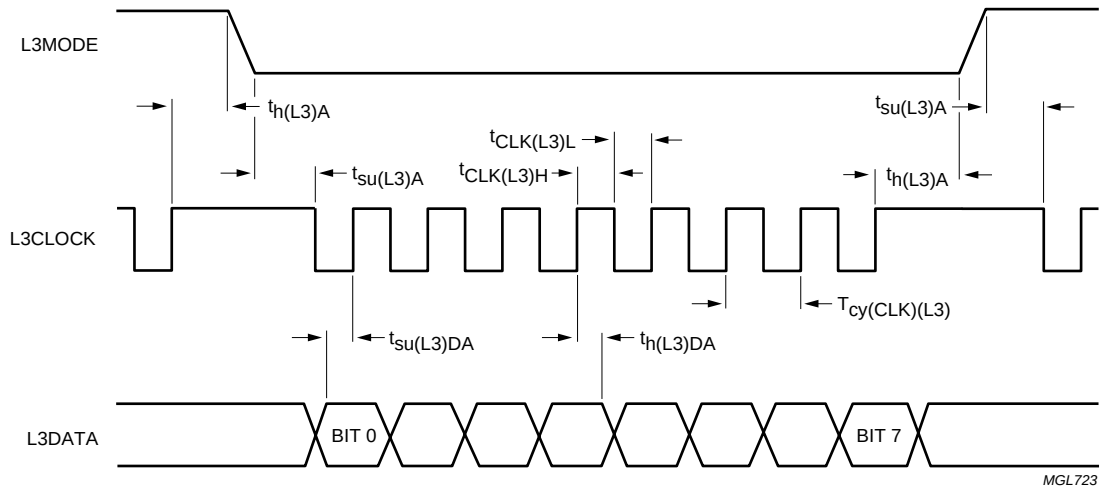


Fig.18 Timing of address mode.

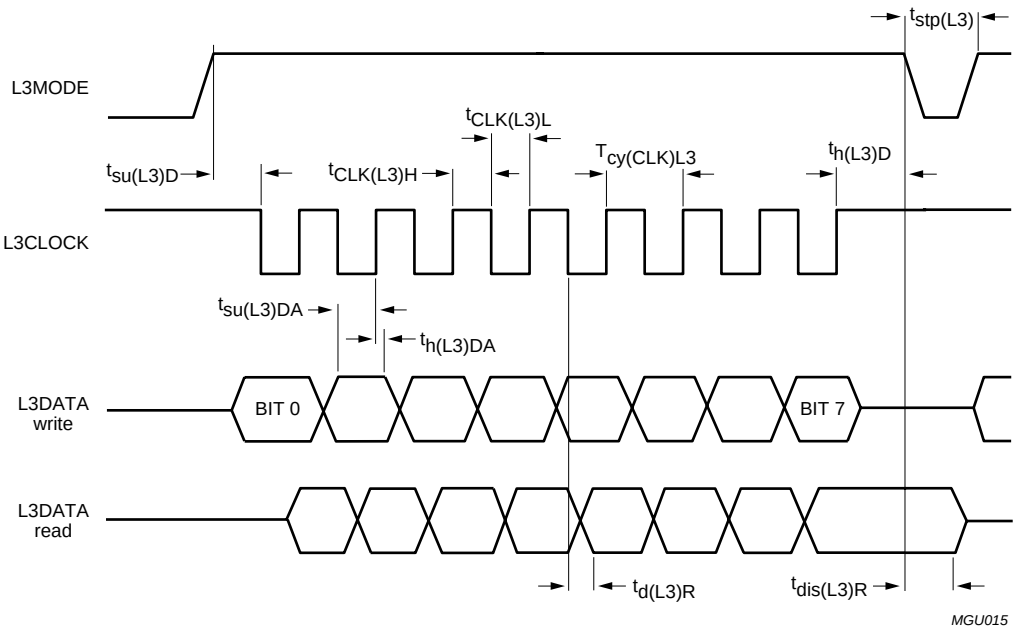


Fig.19 Timing of data transfer mode for write and read.

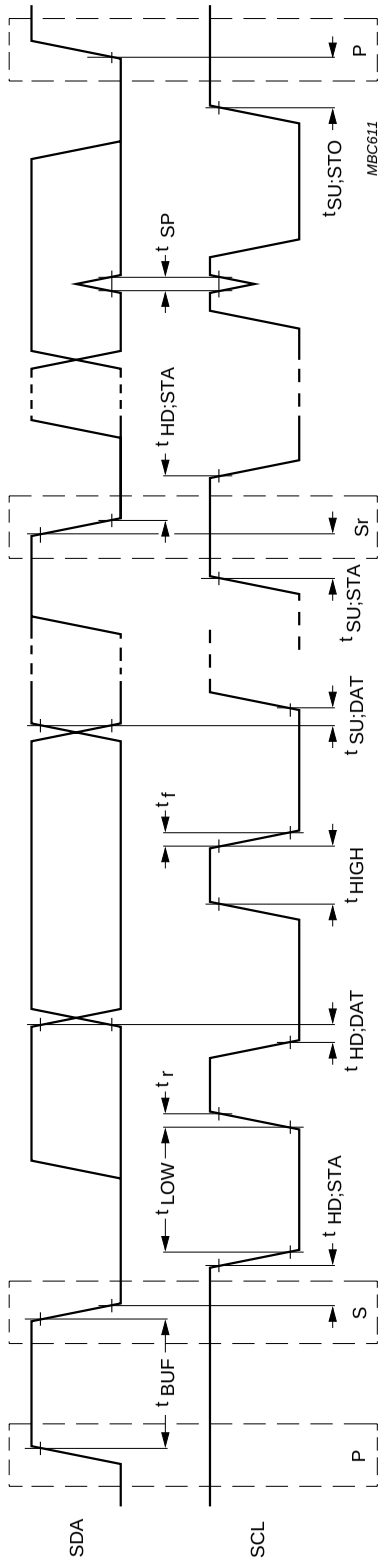
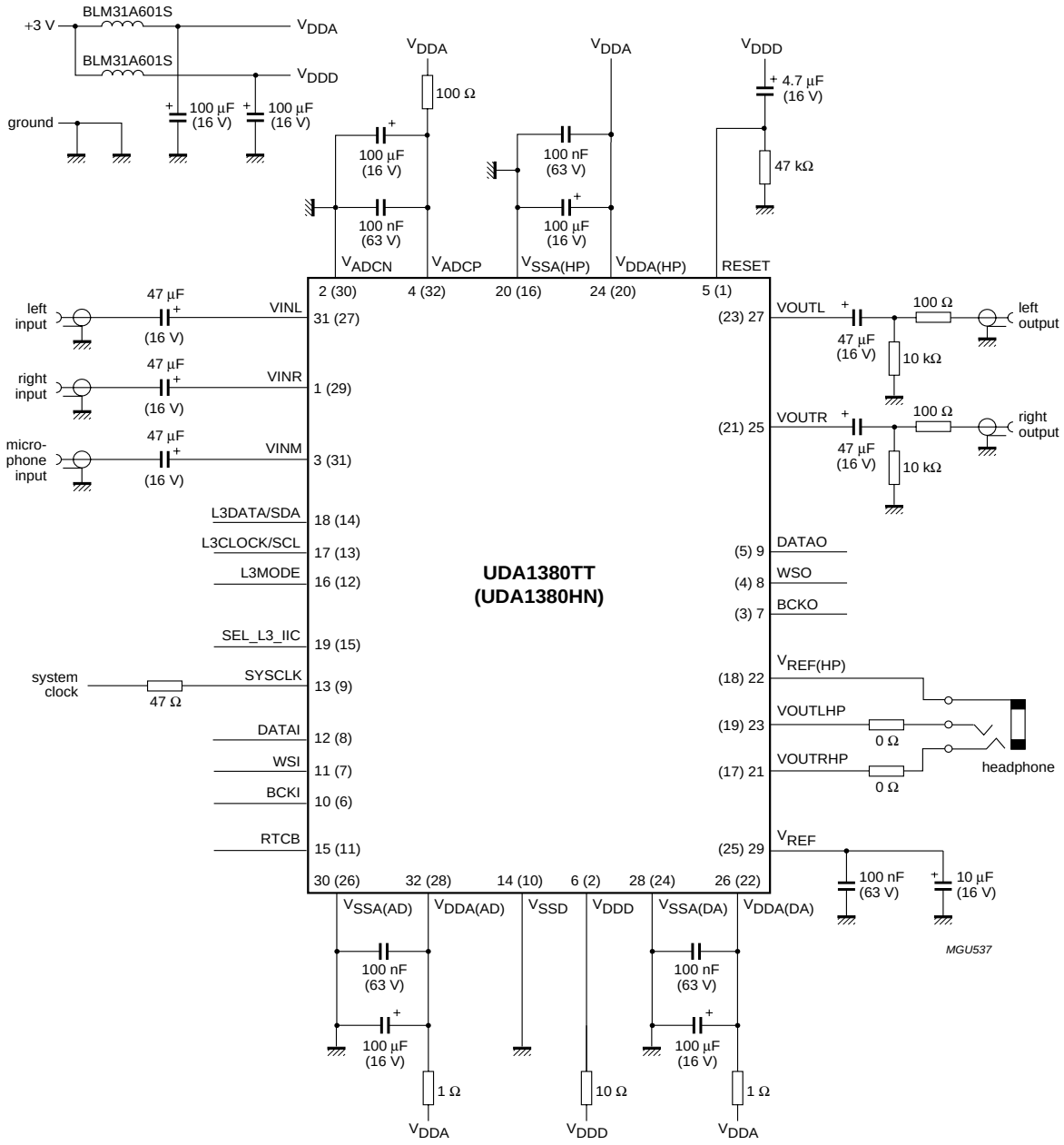


Fig.20 Timing of the I²C-bus transfer.

19 APPLICATION INFORMATION

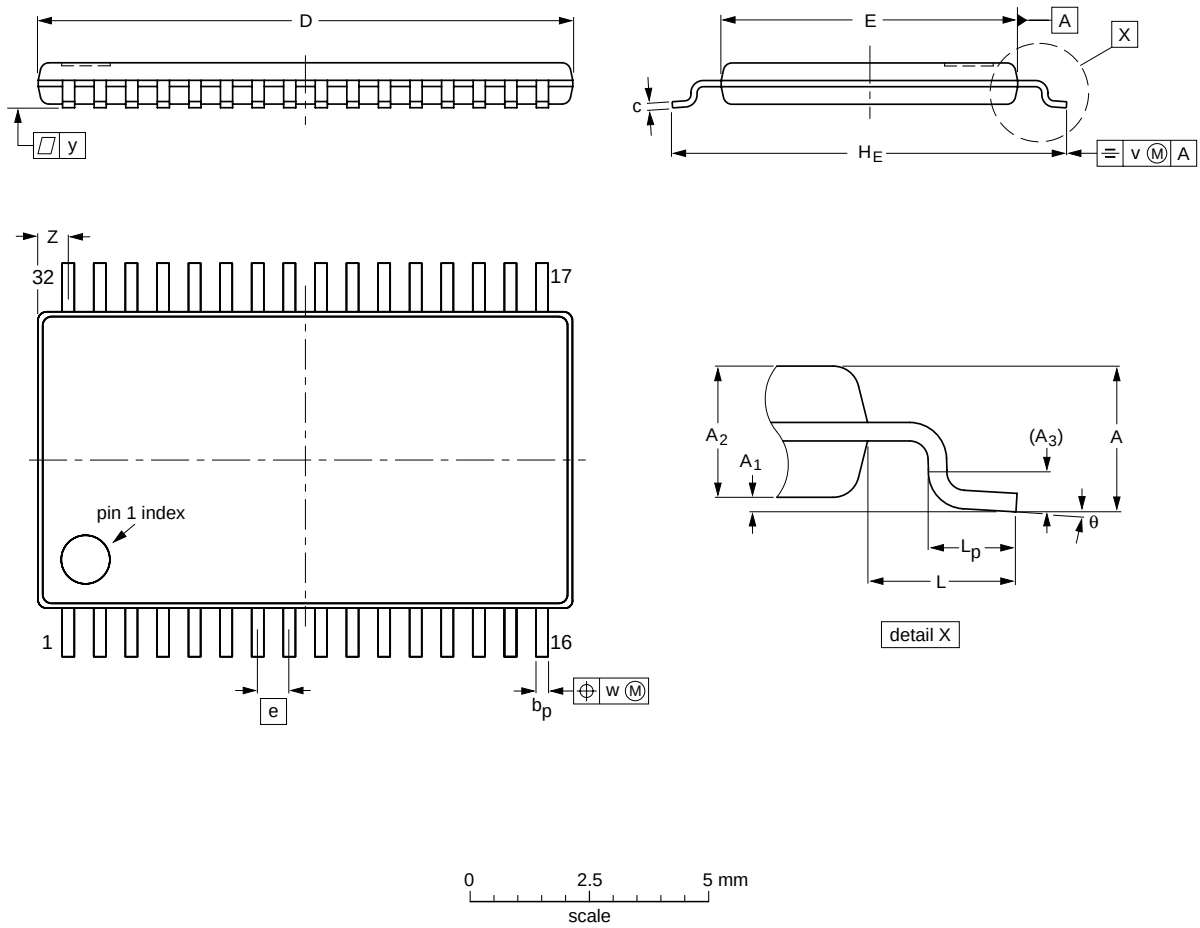


Pin numbers for UDA1380HN in parentheses.

Fig.21 Application diagram.

20 PACKAGE OUTLINES

TSSOP32: plastic thin shrink small outline package; 32 leads; body width 6.1 mm; lead pitch 0.65 mm **SOT487-1**



DIMENSIONS (mm are the original dimensions)

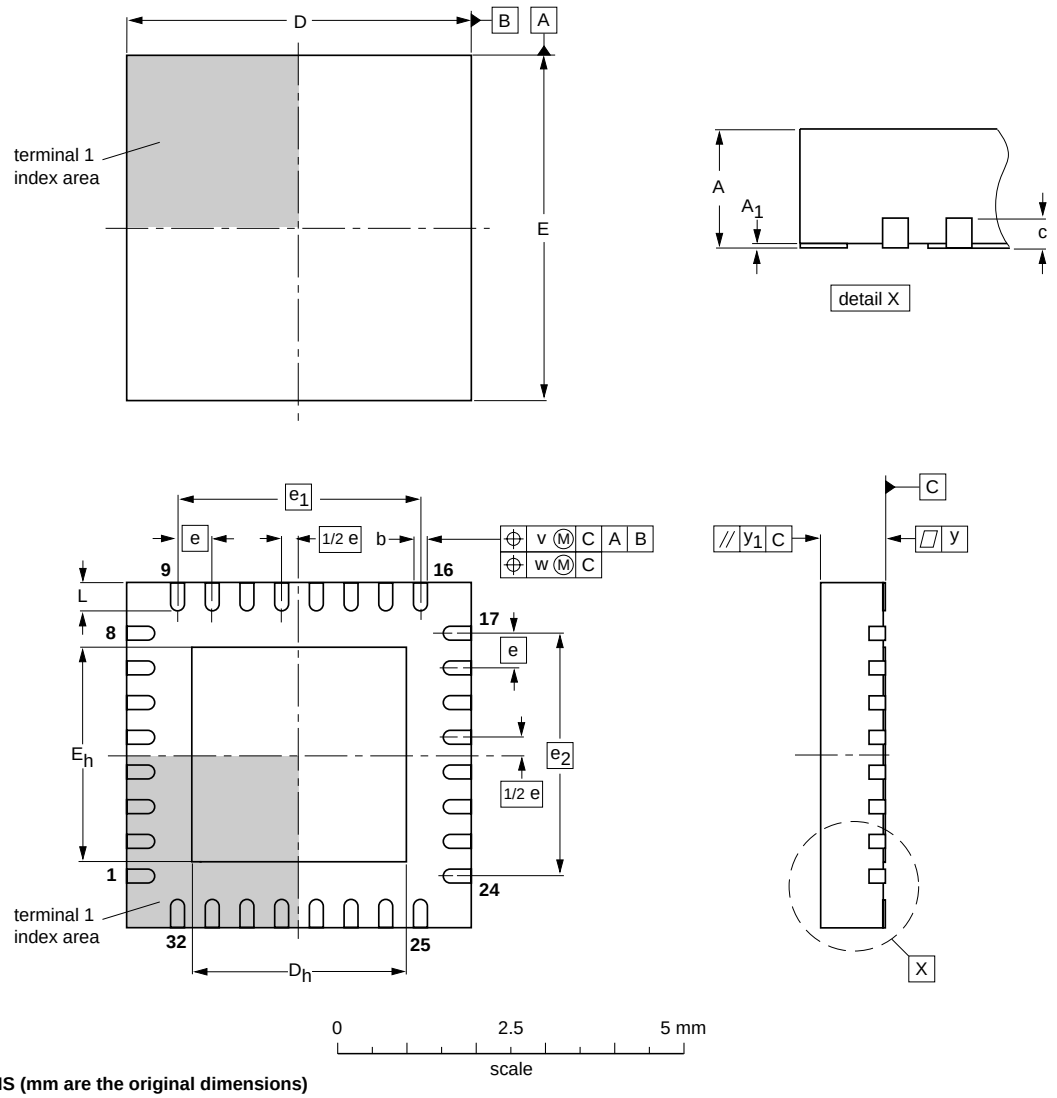
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	Z	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.09	11.1 10.9	6.2 6.0	0.65	8.3 7.9	1	0.75 0.50	0.2	0.1	0.1	0.78 0.48	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT487-1		MO-153				~~99-12-27~~ 03-02-18

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

21 SOLDERING

21.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

21.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON-T and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

21.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

21.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

21.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, HTSSON..T[3], LBGA, LFBGA, SQFP, SSOP..T[3], TFBGA, USON, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
CWQCCN..L[8], PMFP[9], WQCCN..L[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note*" (AN01026); order a copy from your NXP Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.
9. Hot bar or manual soldering is suitable for PMFP packages.

22 DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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