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SSI 32R1555R
+5, -3V, 10/8 Channel MR Head Read/Write Device
Advance Information

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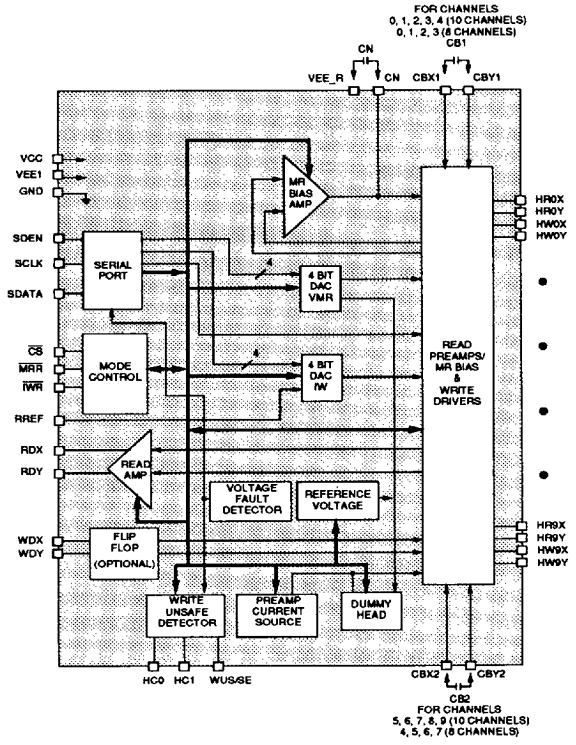
DESCRIPTION

The SSI 32R1555R is a BiCMOS monolithic integrated circuit designed for use with four-terminal Magneto-Resistive recording heads. The reader architecture is MR voltage bias/voltage sense. A serial port is provided to enable the implementation of on-chip MR bias and write current DACs. It provides a write driver, low noise read amplifier, serial port controlled head selection, servo bank write, write current, MR read bias voltage and fault detection circuitry for up to ten channels. In servo write mode, 5 channels can be separately selected. The device requires +5V and -3V and comes in a 64-lead TQFP package.

FEATURES

- **+5V, -3V ±10% supply**
- **Designed for four-terminal MR heads with minimum external components**
- **Truly differential voltage bias/voltage sense MR read Amp**
- **MR head bias voltage range = 200-500 mV**
- **MR read gain = 200 V/V (nom)**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R1555R
+5, -3V, 10/8 Channel
MR Head Read/Write Device

FEATURES (continued)

- MR read input noise = 0.70 nV√Hz (Nom)
- MR read input resistance = 900Ω (Nom)
- Differential PECL write data input with optional flip-flop
- Head voltage swing = 10.0 Vp-p (Typ)
- Write current range = 10 - 40 mA
- Write unsafe detection
- Enhanced system write to read recovery time
- Power supply fault protection
- Head select, write current magnitude and MR bias voltage are controlled by serial interface

FUNCTIONAL DESCRIPTION

The SSI 32R1555R addresses up to 10 MR heads providing write drive or read bias and amplification. Mode control is accomplished with TTL pins $\overline{MRR}$, $\overline{IWR}$ and $\overline{CS}$. The TTL inputs have internal pull-up resistors so that when left opened, they will default to the TTL High state.

SERIAL PORT OPERATION

The write only serial data port is used to control head selection, write current magnitude, MR bias voltage, vendor query and MR head resistance measurement. It does this by writing data into two on board registers addressed E2 and F2.

A complete data transfer is sixteen (16) bits long and loaded LSB first. Addresses and data are loaded least significant bit (LSB) first, and addresses are loaded first. The first bit is the $R/\overline{W}$ bit and is always set to zero. The next three bits (S0-S2) are the device select bits and are always written S0=1, S1=0 and S2=0 for R/W amplifiers. The following four bits (A0-A3) are the address bits and the last eight (D0-D7) are the data bits.

Asserting the serial port enable line SDEN initiates a transfer. SDATA is clocked into the internal shift register by the rising edge of SCLK. A counter on the chip ensures that exactly 16 clock pulses occurred prior to SDEN being de-asserted otherwise the transfer will be aborted. Loading of the registers takes place on the falling edge of SDEN.

WRITE MODE

Taking both $\overline{CS}$ and $\overline{IWR}$ low with $\overline{MRR}$ high selects the write mode which configures the 32R1555R as a current switch and activates the Write Unsafe (WUS) detect circuitry. The head current is toggled between the X (HWnX) and Y (HWnY) side of the selected head on each transition of the differential PECL signal WDX-WDY. With WDX>WDY Iw will flow from the X to the Y pin, i.e., the X side of the head will be higher potential than the Y side. Write current magnitude is controlled by a four bit on-board digital to analog converter. This DAC is programmed via the serial port. The magnitude of the write current (0-pk) is given by:

$$Iw = 10\ mA + 30\ mA\ (N/15)$$

where N = decimal value of WIMV0-WIMV3 (Digital input to write current DAC)

Note that the actual head current Ix,y is given by:

$$Ix,y = \frac{Iw}{1+Rh/Rd}$$

where Rh is the head DC resistance and Rd is the damping resistance.

While in the write mode the voltages on CN and CB1/CB2 will be held to the values they were during the last read. This facilitates fast switching from write to read.

SERVO WRITE MODE

This mode allows for writing to multiple channels at once, which is useful during servo formatting. In this mode the write driver will drive the channels according to Table 3

To enable servo write mode follow these steps:

(1) Place the device in the read mode. $\overline{IWR} = \overline{MRR} = 0$

(2) Pull WUS/SE Vcc +2.0V

(3) Place the device in write mode, $\overline{MRR} = 1$, $\overline{IWR} = 0$.

READ MODE

Taking $\overline{CS}$ and $\overline{MRR}$ low and $\overline{IWR}$ high selects the read mode which activates the MR bias voltage generator and low noise differential amplifier. The outputs of the read amplifier RDX and RDY are emitter followers and are in phase with the resistivity change at the selected input ports HRnX and HRnY where the respective MR head is attached. The voltage across the MR head is regulated by the chip and is adjustable from 200 mV to 500 mV. The magnitude of this voltage is controlled by an on board digital to analog converter. This DAC is programmed via the serial port. The actual magnitude is given by:

$$VMR = 200\ mV + (M/15)(300\ mV)$$

where M = decimal value of MRB0-MRB3 (Digital input to MR bias DAC)

An external capacitor connected from pin CN to CNR is used for reducing the noise from the MR bias current source. A low inductance capacitor with a value of 0.1 µF is recommended. Two external floating capacitors CB1 and CB2 connected between pins CBX1/CBY1 and CBX2/CBY2, respectively, are required for DC blocking. Care should be taken to use low inductance high frequency capacitors and to locate them as close to the pins as possible. The stray inductance will degrade amplifier's noise and frequency response performance. The value of the DC blocking capacitors CB1/CB2 will have direct effect on the write to read recovery time. For fast recovery time, the capacitor value should be kept as small as possible. The value of the capacitor CB1/CB2 also sets the low frequency cutoff of the read amplifier. The -3 dB low-frequency corner is given by:

$$f_L = 1/[2 \cdot \pi \cdot 15\Omega \cdot CB(1,2)]$$

For example, a 0.03 µF capacitor for CB1/CB2 will result in the -3 dB low-frequency of about 350 kHz.

In read mode, the voltage at the midpoint of the selected MR head is forced to a virtual ground.

If either the X or Y side of the head is shorted to ground the head bias voltage will not exceed it's programmed value. For the unselected MR heads, the head ports become high impedance and thus will prevent the heads from conducting current in the event of head to disk contact.

RBAW MODE

Taking $\overline{CS}$, $\overline{IWR}$ and $\overline{MRR}$ low selects the RBAW (read bias active in write) mode. In this mode the write driver is active just as in the write mode but the MR voltage bias circuitry is also active. The outputs of the read amplifier RDX/RDY remain inactive, i.e., high impedance. The purpose of this mode is to speed up the write to read transition times by selecting this mode just prior to switching to the read mode. To be effective it is suggested that RBAW be selected at least 5 µs prior to selecting read mode. Switching times from RBAW to read mode are guaranteed to be less than 1 µs.

STANDBY MODE

Taking $\overline{CS}$ low and $\overline{MRR}$ and $\overline{IWR}$ high selects the standby mode. In this mode the write driver and read amplifier are both inactive. The voltages across CN and CB1/CB2 are held to the values they were during the last read. This facilitates fast switching from standby to read. The serial port is active in this mode and it is suggested for fastest performance that head switching be done in standby rather than IDLE.

IDLE MODE

Taking $\overline{CS}$ high selects Idle mode which deactivates both the write driver and read amp/MR bias circuitry. The pins RDX/RDY are switched into high impedance state to facilitate multiple device applications where these pins could be wire OR'ed. The serial port is active while in idle mode.

VENDOR QUERY MODE

This mode is entered by selecting idle mode and setting bits D4=0 and D5=1 in register E2. The purpose of this mode is for the host system to interrogate the read/write IC for information regarding the specific vendor associated with the head and the read/write IC itself. Pins HC0 and HC1 are used to create a two-bit code unique to the particular head being used in this drive. They default to logic high if left open. The SSI 32R1555R is programmed at the factory to have the two-bit code CC0=0 and CC1=0. Bits WIMV0-WIMV3 of register E2 are used to guess the value of HC0,HC1, CC0,CC1. When the value of WIMV0-WIMV3 matches HC0,HC1,CC0,CC1, WUS/SE will go high.

MR RESISTANCE MEASURE MODE

This mode is entered by selecting READ ($\overline{CS}$, $\overline{MRR}$=0 $\overline{IWR}$=1) and setting bits D4=1 and D5=0 in register E2. There are two purposes for using this mode. They are to measure MR head resistance and to test for an open MR head. The open head test can only be done in this mode, not in the normal read mode. It is not intended as a read unsafe monitor during read mode operation but as a means to verify the heads were installed properly and for two and four channel drives to verify head count and location.

Referring to the equation below, the MR resistance measurement is done by setting VMR to a known value by programming MRB0-MRB3. A scaled version of the actual MR bias current is then compared to a scaled version of the write DAC output current. This current is set by WIMV0-WIMV3. When used this way the write DAC is switched out of the write circuit and into the measure circuit. The write driver is not active. WIMV0-WIMV3 are adjusted until WUS/SE toggles low to high or high to low (depending on whether the initial guess was less than or greater than the actual RMR). RMR is determined by:

$$RMR = \frac{VMR}{(N+5)mA}$$

where: N = decimal value of WIMV0-WIMV3 at WUS/SE toggle. Note: The level of WUS/SE can take up to 1µs to settle after WIMV0-WIMV3 are changed.

There are limitations to the range of resistance that can be measured. They are determined by the operating range of VMR and IMR.

$$200\ mV < VMR < 500\ mV$$
$$5\ mA < IMR < 20\ mA$$

For example with VMR set to 200 mV, the range of resistance it is possible to measure is 10 to 40Ω. With VMR set to 500 mV the range is 25 to 100Ω.

For open head testing it should be noted that there is 7 kΩ internal resistance in parallel with the head. This is for biasing purposes. With open head conditions IMR can't exceed 5 mA and WUS/SE will be low for all values of VMR.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator and the MR bias current/read amplifier during a voltage fault or power startup regardless of mode.

WUS/SE OPERATION

WUS/SE pin behavior can be divided into four categories:

- write and RBAW
- idle, read and standby
- MR resistance measure
- vendor query

When in the Write or RBAW modes the following faults will cause WUS/SE to go high:

- WDX/WDY frequency low
- no head current
- open head
- low supply voltage

The WUS/SE flag can be unlatched by setting bit D7 in Register E2. In this case, WUS/SE will remain high even if the fault has been cleared before leaving the write mode. To clear WUS/SE it is necessary to exit the write mode and enter either idle, read or standby then re-enter the write mode with the fault removed. WUS/SE will then go low after two transitions of WDX-WDY (following the required 500 ns mode transition time).

When in idle, read or standby modes WUS/SE is high.

WUS/SE behavior for the MR resistance measure and vendor query modes has been described in previous sections.

TABLE 1: Mode Select

$\overline{CS}$	$\overline{MRR}$	$\overline{IWR}$	REG E2 D4	REG E2 D5	MODE	RDX/RDY	MR BIAS	WRITE DRIVER
0	1	0	0	0	Write/Servo*	Hi-Z	OFF	ON
0	0	1	0	0	Read	ON	ON	OFF
0	0	0	0	0	RBAW	Hi-Z	ON	ON
0	1	1	X	X	Standby	Hi-Z	OFF	OFF
1	X	X	0	0	Idle	Hi-Z	OFF	OFF
1	X	X	0	1	VENDOR QUERY	Hi-Z	OFF	OFF
0	0	1	1	0	MR RESISTANCE MEASURE	Hi-Z	ON	OFF

* To put in servo mode, pull WUS/SE Vcc +2.0V.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS port for writing programming data to the internal registers. For data transfers, the SDEN pin is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. The data is clocked in on the rising edge of the clock LSB first. After SDEN goes high, an internal counter requires exactly 16 clock pulses before SDEN goes low or no data is transferred. The data in the shift register is latched when SDEN goes low.

The first bit transferred on SDATA is the R/W bit which is always set to zero. The next three bits (SO - S2) are the device select bits and are always written as S0 = 1, S1 = 0, and S2 = 0 for R/W amplifiers. The following four bits (A0 - A3) are the register address bits and the last eight are the data bits. The serial port diagram and bit map are shown below.

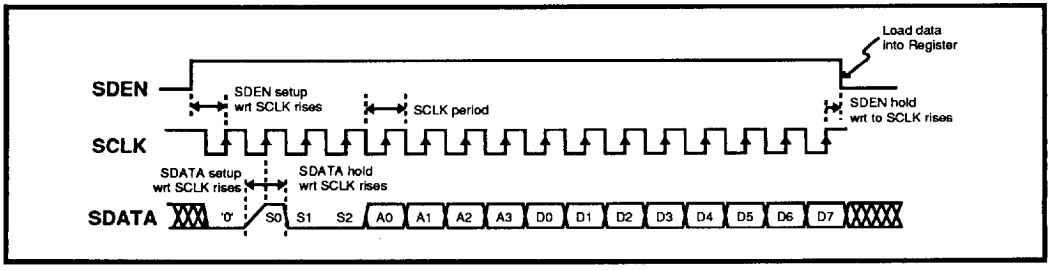


FIGURE 1: Serial Interface Timing Diagram - Writing Control Register

TABLE 2: Serial Port Bit Map

FUNCTION	REG	R/W	S0	S1	S3	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
Head Select/ MR Bias Set	F2	0	1	0	0	1	1	1	1	HS0	HS1	HS2	HS3	MRB0	MRB1	MRB2	MRB3
Write Current	E2	0	1	0	0	0	1	1	1	WIMV0	WIMV1	WIMV2	WIMV3	0	0	WDFF	WUSL
MR Measure	E2	0	1	0	0	0	1	1	1	WIMV0	WIMV1	WIMV2	WIMV3	1	0	WDFF	WUSL
Vendor Query	E2	0	1	0	0	0	1	1	1	WIMV0	WIMV1	WIMV2	WIMV3	0	1	WDFF	WUSL

Note: D6: WDFF = 1, enable write data Flip Flop, default = 0.
D7: WUFF = 1, enable WUS latch, default = 0.

TABLE 3: Register Definitions

REGISTER	BIT	DESCRIPTION
F2	3-0	Head select address (HS)
F2	7-4	MR bias voltage set (MRB)
E2	3-0	Write current, MR measure, vendor query (WIMV)
E2	5-4	Set WIMV mode
E2	6	Not used
E2	7	Write unsafe latch set (WUSL)

TABLE 4: Register Address E2, WIMV Definitions

The definition of WIMV0- WIMV3 is determined by bits D4 and D5 of Register E2.

D4	D5	DEFINITION OF WIMV0- WIMV3
0	0	Write current magnitude (LSB = 2.0 mA)
0	1	Chip and head vendor query/ identification
1	0	MR resistance measurment/ open head detection

Conditions following power up or power supply fault:

1. No head selected
2. MRB0 - MRB3 = "0", VMR = 200 mV
3. Register E2, bits D4-D5 = "0"
4. WIMV0 - WIMV3 = "0", IW = 10 mA
5. WUS/SE latch is disabled

TABLE 5: Serial Port Bit Map, Power Up or Power Supply Fault

FUNCTION	REG	R/W	S0	S1	S3	A0	A1	A2	A3	D0	D1	D2	D3	D4	D5	D6	D7
Head Select/ MR Bias Set	F2	0	1	0	0	1	1	1	1	1	1	1	1	0	0	0	0
Write Current	E2	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0
MR Measure	E2	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0
Vendor Query	E2	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0

TABLE 6: 10-Channel Head Select, Normal Mode

HS3	HS2	HS1	HS0	CHANNEL SELECTED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

TABLE 7: 10-Channel Head Select, Servo Mode

HS0	CHANNELS SELECTED
0	0-4
1	5-9

TABLE 8: 8-Channel Head Select, Normal Mode

HS3	HS2	HS1	HS0	CHANNEL SELECTED
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7

TABLE 9: 8-Channel Head Select, Servo Mode

HS0	CHANNELS SELECTED
0	0-3
1	4-7

PIN DESCRIPTION

CONTROL INPUT PINS

NAME	TYPE	DESCRIPTION
HR0X–HR9X HR0Y–HR9Y	I	MR read head input X and Y connections
HW0X–HW9X HW0Y–HW9Y	O	Inductive write head X and Y connections
CN	I	Noise filter Cap
VEE_R	I	-3V Supply (noise filter cap return)
CBX1/CBY1	I	Floating DC blocking cap CB1; for head 0, 1, 2, 3, 4 (0-3 for 8 Channels)
CBX2/CBY2	I	Floating DC blocking cap CB2: for head 5, 6, 7, 8, 9 (4-7 for 8 Channels)
WDX, WDY	I	Differential PECL Write Data Input
RDX, RDY	O	Differential MR head Read Data Output
RREF	I	2 kΩ resistor to ground sets reference current for write DAC
WUS/SE	I/O	Write Unsafe; open collector; a high level indicates an unsafe writing condition or outcome of vendor query or MR head resistance measurement. When in Servo Bank Write Mode, pulling this pin above Vcc enables servo bank write. See servo write mode section.
$\overline{CS}$	I	Chip Select; a high inhibits the chip; TTL
$\overline{MRR}$	I	Mode control, TTL
$\overline{IWR}$	I	Mode control, TTL
SDATA	I	Serial data used for head selection, setting write current magnitude and MR bias voltage, vendor query and MR head resistance measurement, CMOS
SCLK	I	Serial clock, CMOS
SDEN	I	Serial data enable, CMOS
HC0, HC1	I	Head code bit 0 and bit 1
VCC	I	+5V Supply
VEE	I	-3V Supply
GND	I	Ground

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these maximum ratings may cause permanent damage to this device.

PARAMETER		RATING
DC Supply Voltage	VCC VEE	+6 VDC -6 VDC
Logic Input Voltage	CMOS/TTL PECL	-0.3 to VCC +0.3 VDC 0 to VCC VDC
Write Current	Iw	75 mA
MR Bias Current	Ir	30 mA
Output Current	WUS/SE RDX/RDY	+8 mA -5 mA
Operating Junction Temperature	Tj	+135°C
Storage Temperature	Tstg	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC VEE	4.5V to 5.5V -3.3V to -2.7V
Operating Ambient Temperature	Ta	0 to 70°C

DC CHARACTERISTICS

Iw = 40 mA, RMR = 30, VMR = 500 mV, IMR = 17 mA

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply Current	VCC	read mode		58	71	mA
		write mode		74	91	mA
		RBAW mode		104	128	mA
		standby mode		10		mA
		idle mode		2.3	2.8	mA
		servo write		TBD		
Supply Current	VEE	read mode		36	44	mA
		write mode (no RBAW)		63	78	mA
		RBAW mode		92	113	mA
		standby mode		2		mA
		idle mode		0.7	0.9	mA
		servo write		TBD		mA

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Power Dissipation	read mode, Imr = 10 mA		TBD		mW
	write mode, Iw = 40 mA		TBD		mW
	RBAW mode, Iw = 40 mA, Imr = 10 mA		TBD		mW
	standby mode, Imr = 10 mA		TBD		mW
	idle mode		TBD		mW
VCC Fault Voltage	Iw < 0.2 mA, Imr < 0.2 mA	3.5	3.85	4.2	VDC
VEE Fault Voltage	Iw < 0.2 mA, Imr < 0.2 mA	-2.52	-2.31	-2.10	VDC

LOGIC INPUTS AND OUTPUTS

Input Low Voltage	Vil	TTL	-0.3		0.8	VDC
Input High Voltage	Vih	TTL	2		Vcc+0.3	VDC
Input Low Current	Iil	Vil = 0.8V	-0.4	-0.2		mA
Input High Current	Iih	Vih = 2V			100	µA
Input Low Voltage (WDX, WDY)	Vil2		Vcc-2		Vih2-0.25	VDC
Input High Voltage (WDX, WDY)	Vih2		Vcc-1.1		Vcc-0.4	VDC
Input Differential Voltage V(WDX, WDY)			0.3			VDC
Input Low Current	Iil2	Vil = Vcc-1.4V			50	µA
Input High Current	Iih2	Vih = Vcc-0.4V			50	µA
Output High Current (WUS/SE)	Ioh				50	µA
Output Low Current (WUS/SE)	Iol				4	mA
Output Low Voltage (WUS/SE)	Vol	Iol = 4 mA			0.5	VDC
Input High Voltage (WUS/SE)	VIH		Vcc +1.5	Vcc +2.0	7.0	V
Input Low Voltage (WUS/SE)	VIL				Vcc +0.3	V
Input High Current (WUS/SE)	IIH	VIH = Vcc +2.0		130	400	µA
Input Low Current (WUS/SE)	IIL	VIL = Vcc +0.3		0	10	µA

ELECTRICAL SPECIFICATIONS (continued)

SERIAL PORT TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
SCLK Data Clock Period	TC		100			ns
SCLK Low Time	TCKL		40			ns
SCLK High Time	TCKH		40			ns
Enable to SCLK	TSENS		30			ns
SCLK to Disable	TSENH		30			ns
Data Set-up Time	TDS		15			ns
Data Hold Time	TDH		15			ns
SDEN Min. Low Time	Tsl		200			ns

READ CHARACTERISTICS, MR HEAD AMPLIFIER
Recommended operating conditions apply unless otherwise specified
Rmr = 24Ω, CN = 0.1 µF, CB1 = CB2 = 0.03 µF
CL (RDX, RDY) < 20 pF, RL (RDX, RDY) > 1K

MR Current Range			5		20	mA
MR Head Voltage	selected Head (differential)		200		500	mV
	unselected Heads (single ended)		-0.6		-0.4	V
MR Head Voltage Resolution (LSB)				20		mV
MR Head Voltage Accuracy			-10		+10	%
Unselected MR Current				0.1		mA
Differential Voltage Gain	Vin = 1 mVp-p @ 5 MHz Rmr = 24Ω;		150	200	250	V/V
Voltage BW	Lmr = 20 nH	-1 dB				MHz
	Vin = 1 mVp-p	-3 dB Upper	90			MHz
	CB1/CB2 = 0.03 µF	-3 dB Lower		350		kHz
Input Noise Voltage	exclude head noise			0.7		nV/√Hz
Differential Input Resistance	Vin = 1 mVp-p @ 5 MHz CB1/CB2 = 0.03 µF			1.5		kΩ
MR Measurement Mode Accuracy			-6		+6	%

READ CHARACTERISTICS, MR HEAD AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Differential input Capacitance	Vin = 1 mVp-p @ 5 MHz CB1/CB2 = 0.03 µF		10	15	pF
CMRR	Vin = 100 mVp-p @ 5 MHz	55			dB
PSRR	100 mVp-p @ 5 MHz on VCC or VEE	50			dB
Channel Separation	unselected channels driven with 100 mVp-p @ 5 MHz	45			dB
Output offset Voltage		-300		300	mV
Output Resistance	single ended			100	Ω
Output Current		1.5			mA
RDX/RDY Common Mode Output Voltage			VCC-1.65		V
Input Dynamic Range	AC input voltage where gain falls to 90% of its small signal value, @ 5 MHz	3			mV
Total Harmonic Distortion	Vin ≤ 2 mV @ 5 MHz			1	%
Amplifier Saturation Recovery Time	Vin = 20 mV step		2	3	µs

WRITE CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified
Iw = 20 mA, Lh = 150 nH, Rh = 17Ω

Write Current Range		10		40	mA(0-pk)
Write Current Resolution			2.0		mA
Write Current Accuracy		-15		+15	%
Differential Head Voltage Swing	open head	8	10		Vp-p
Unselected Head Current DC				0.1	mA
AC				1	mApk
Head Differential Damping Resistance		385	475	565	Ω
Head Differential Load Capacitance				15	pF
Write DAC Reference Resistor			2		kΩ

Note: Write Current accuracy can be increased to ±10 % for 30 mA < Iw < 50 mA & RREF = 7.5 kΩ

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified
12Ω < Rmr < 35Ω; CL (RDX, RDY) < 20 pF; Iw = 20 mA, CN = 0.1 µF, CB1 = CB2= 0.03 µF
RL (RDX, RDY) > 1K; Lh = 180 nH, Rh = 17Ω; F (WDX/WDY) = 5 MHz

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Read to Write		To 90% of write current		100	500	ns
Write/Standby to Read		To 90% of 100 mV, 5 MHz read signal envelope		2	5	µs
RBAW to Read		Same as above RBAW selected at least 5 µs prior to read		0.5	1	µs
Idle to Read		Same as above			50	µs
Head switch to Read		Same as above. Switch done in standby mode.			30	µs
WUS/SE	Safe to Unsafe (TD1)	Write mode, from loss of WDX-WDY transitions	0.25		1	µs
	Unsafe to Safe (TD2)	Fault cleared from second WDX-WDY transition.			500	ns
Head Current: (WDX - WDY) to Ix-y (TD3)		From 50% point			30	ns
Rise/Fall Time		With head, 10% to 90%		2.5	4	ns
Write Current Asymmetry					0.5	ns

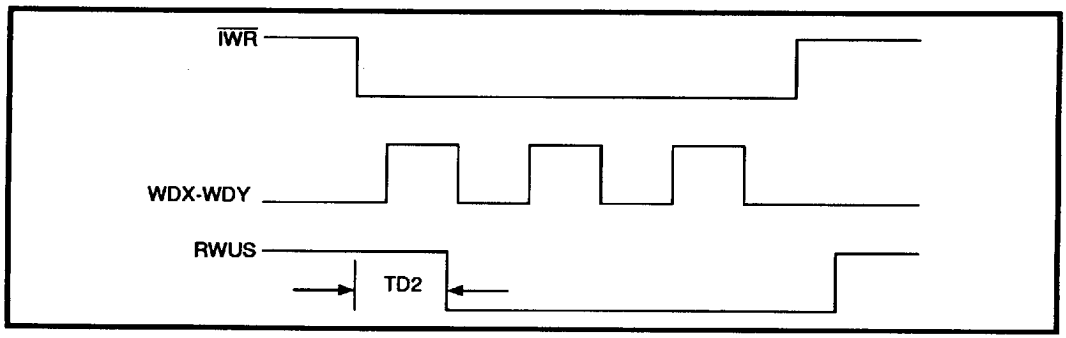


FIGURE 2: Normal Write Conditions

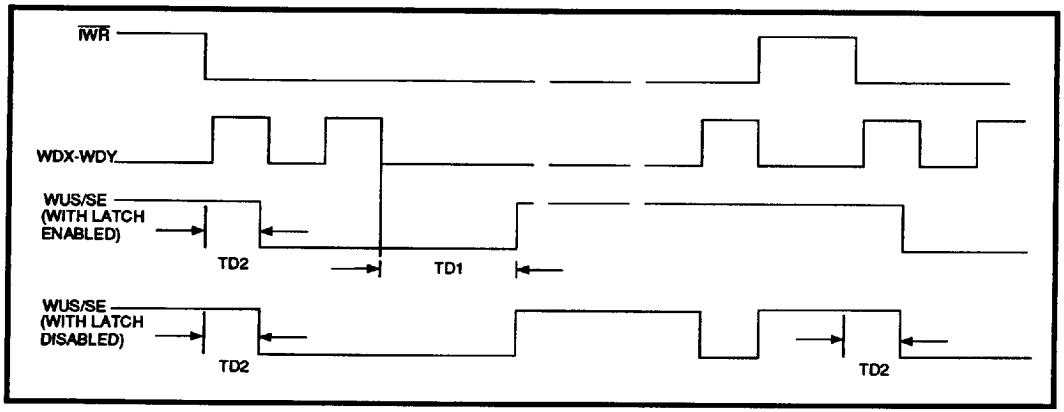
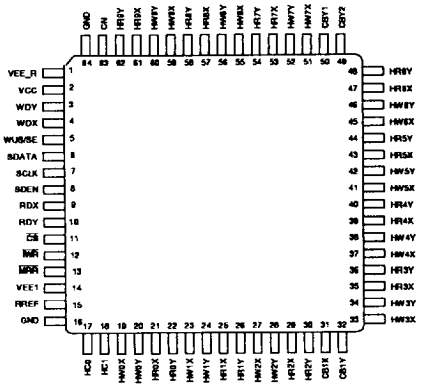


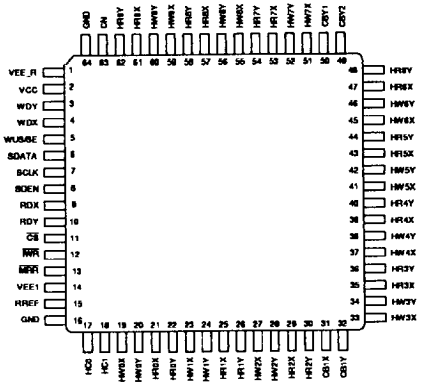
FIGURE 3: WUS Timing

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32R1555R-10CGT
10 Channel
64-Lead TQFP



32R1555R-8CGT
8 Channel
64-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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