

RCM2044M

16 characters × 2 line, LED backlit, transfective-type, character module

RCM2044M is a transfective TN-type, liquid crystal module incorporating a controller and driver LSI, with a display capacity of 16 characters on each of two lines. LCD has a yellow green side-type LED backlight.

Features

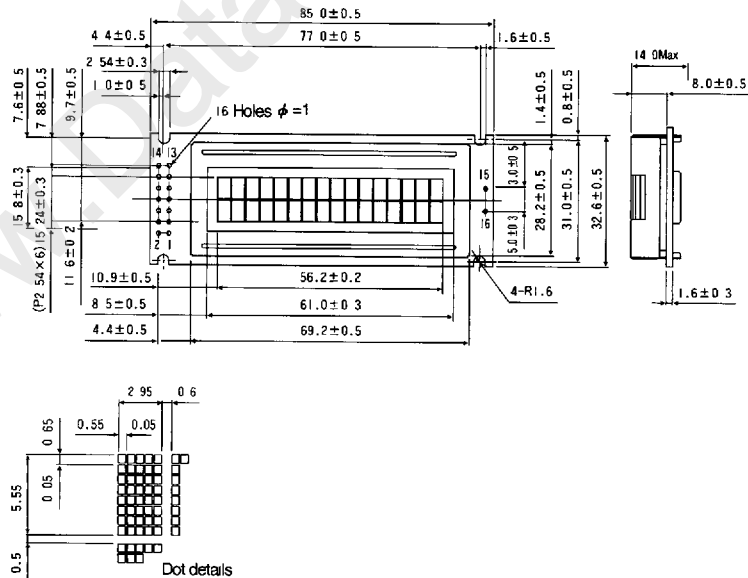
- very small light structure
- operates from 5 V dc supply
- low power consumption
- wide angle of view and high contrast
- 5 × 7 dots with cursor
- may use 4-bit or 8-bit interface
- 226 characters and symbols are supported

- character pattern selected can be displayed using the character RAM
- extra functions include:
 - clear display
 - cursor on and off
 - character blinking
- EL built-in transparent and opaque types are available

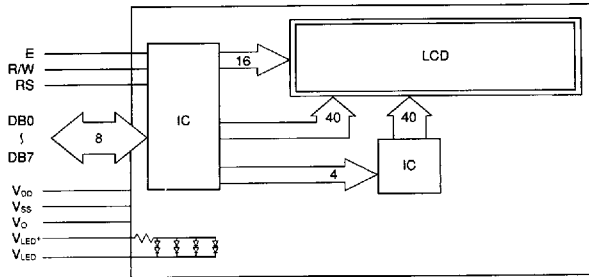
Applications

- personal computers
- word processors
- facsimile machines
- telephone sets

Dimensions (Units : mm)



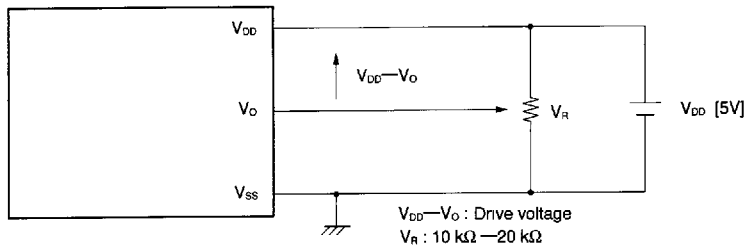
Block diagram



Pinout diagram

Pin no.	Signal	Pin no.	Signal	Pin no.	Signal	Pin no.	Signal
1	V _{SS}	5	R/W	9	DB2	13	DB6
2	V _{DD}	6	E	10	DB3	14	DB7
3	V _O	7	DB0	11	DB4	15	V _{LED-}
4	RS	8	DB1	12	DB5	16	V _{LED+}

Figure 1 Power supply example



Absolute maximum ratings ($T_a = 25^\circ\text{C}$)

Parameter	Symbol	Min	Typical	Max	Unit
Logic power supply	$V_{DD} - V_{SS}$	0		6.5	V
LCD drive supply	$V_{DD} - V_O$	0		6.5	V
Input voltage	V_{IN}	V_{SS}		V_{DD}	V
Operating temperature	T_{opr}	0		+50	$^\circ\text{C}$
Storage temperature	T_{stg}	-20		+70	$^\circ\text{C}$

Electrical characteristics ($V_{DD} = 5 V \pm 0.25 V$, $T_a = 25^\circ C$)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
High level input voltage	V_{IH}	2.0		V_{DD}	V	
Low level input voltage	V_{IL}			0.8	V	
High level output voltage	V_{OH}	2.4			V	$-I_{OH} = 1.2 \text{ mA}$
Low level output voltage	V_{OL}			0.4	V	$I_{OL} = 2 \text{ mA}$
Power supply current	I_{DD}		1.5	3	mA	$V_{DD} = 5 \text{ V}$
LED forward current	I_{LED}			80	mA	$V_{LED} = 5 \text{ V}$
LED forward voltage	V_{LED}	3.8	4.2	5.0	V	$I_{LED} = 20 \text{ mA}$

Optical characteristics ($T_a = 25^\circ C$, $\phi = 0^\circ$)

Parameter	Symbol	Min	Typical	Max	Unit	Conditions
Rise time	t_r		100	250	ms	$\theta = 10^\circ, \phi = 0^\circ$
Fall time	t_d		150	250	ms	$\theta = 10^\circ, \phi = 0^\circ$
Contrast ratio	K		3			$\theta = 10^\circ, \phi = 0^\circ$
Viewing angle	θ_1			20	deg	$\phi = 0^\circ, K \geq 1.4$
	θ_2	40			deg	$\phi = 0^\circ, K \geq 1.4$
	ϕ	± 30			deg	$\theta_1 = 20^\circ, K \geq 1.4$

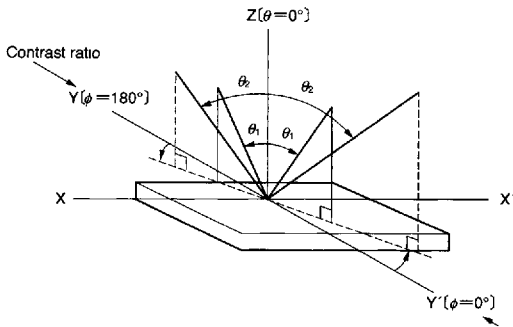


Figure 2 Definition of θ and ϕ

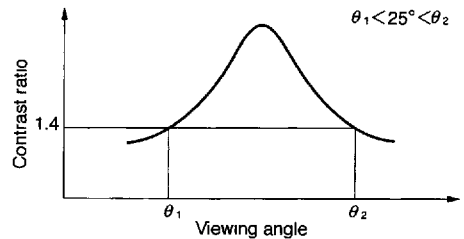


Figure 3 Definition of θ_1 and θ_2

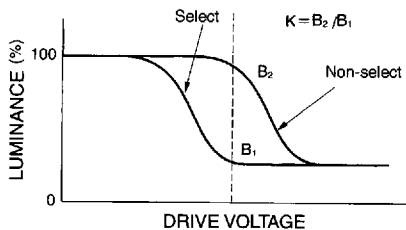


Figure 4 Definition of contrast ratio (K)

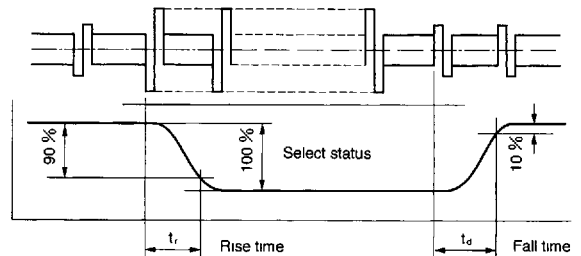
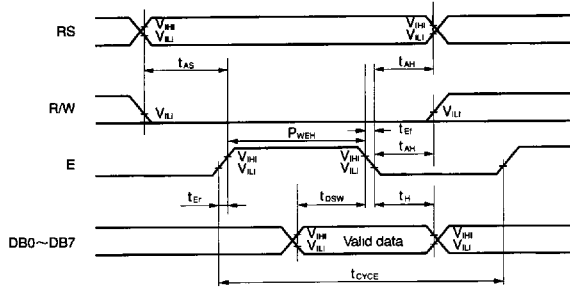


Figure 5 Definition of optical response

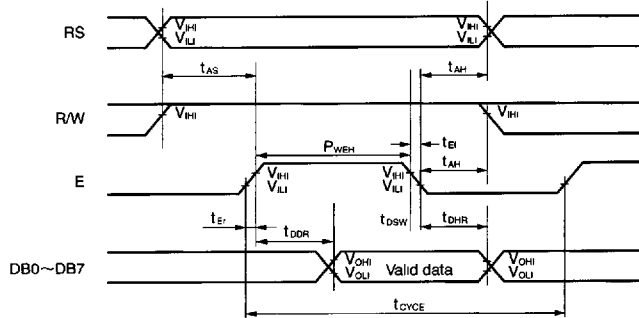
Timing chart

Writing



Parameter	Symbol	Min	Typical	Max	Unit
Enable cycle time	t _{CYCE}	500			ns
Enable pulse time	P _{WEH}	220			ns
Enable rise and fall time	t _{Er} , t _{Ef}			20	ns
Address setup time	t _{AS}	40			ns
Address hold time	t _{AH}	10			ns
Data setup time	t _{DSW}	60			ns
Data hold time	t _H	10			ns

Reading



Parameter	Symbol	Min	Typical	Max	Unit
Enable cycle time	t _{CYCE}	500			ns
Enable pulse time	P _{WEH}	220			ns
Enable rise and fall time	t _{Er} , t _{Ef}			20	ns
Address setup time	t _{AS}	40			ns
Address hold time	t _{AH}	10			ns
Data delay time	t _{DDR}			120	ns
Data hold time	t _{DHR}	20			ns

Pin description

Pin name	Level	Input or output	Function
V _{SS}			Power supply voltage
V _{DD}			
V _O			
RS	HIGH or LOW	Input	Register select signal 0: Instruction register (writing) Busy flag or address counter (reading) 1: Data register (writing/reading)
R/W	HIGH or LOW	Input	Reading (R) and writing (W) select signal 0: Writing processor→LCD module 1: Reading processor←LCD module
E	HIGH or HIGH→LOW	Input	Signal activates start of data read or write
DB0 ~ DB3	HIGH or LOW	Input and output	The lower 4 data lines are bi-directional and are used for data transfer between the MPU and the module. They are not used in 4-bit operation.
DB4 ~ DB7	HIGH or LOW	Input and output	The higher 4 data lines are bi-directional and are used for data transfer between the MPU and the module. DB7 can also be used as a busy flag.

Note 1: With this LCD module, you can use a 4 or 8-bit interface.

Note 2: When a 4-bit data interface is used, only four buses, DB4 ~ DB7, are used for data transfer. Buses DB0 ~ DB3 are not used. Data transfer between the module and the MPU is completed when 4-bit data is transferred two times.

Note 3: When an 8-bit data interface is used, eight data buses (DB0 ~ DB7) are used for data transfer. The higher 4-bit data (DB4 ~ DB7) is transferred first followed by the lower 4-bit data (DB0 ~ DB3).

DD RAM address

	1	2		7	8	9	10		15	16
1 line	00H	01H		06H	07H	08H	09H		0EH	0FH
2 line	40H	41H		46H	47H	48H	49H		4EH	4FH

Instructions

Instruction	Pin										Description	Execution time @ $f_{CP} = 250 \text{ kHz}$
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	0	0	0	0	0	0	0	0	0	1	After all displays have been cleared, address 0 of DD RAM is set in the address counter.	1.64 ms
Cursor home	0	0	0	0	0	0	0	0	1	*	Set address 0 of DD RAM in the address counter. The shifted display returns to its original status. Contents of DD RAM do not change.	1.64 ms
Entry mode set	0	0	0	0	0	0	0	0	I/D	S	Sets the direction of cursor progression and whether the display is shifted. This operation occurs when data is read or written.	40 μ s
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF(D) of all displays, ON/OFF(C) of cursor, and blink(B) of the character where the cursor is located.	40 μ s
Cursor/display shift	0	0	0	0	0	1	S/C	R/L	*	*	Cursor is moved and display is shifted without changing contents of DD RAM.	40 μ s
Function set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of lines of display (N) and character font (F).	40 μ s
CG RAM address set	0	0	0	1	ACG					Sets address of CG RAM. After this, all data transmitted and received is CG RAM data.		40 μ s
DD RAM address set	0	0	1	ADD					Sets address of DD RAM. After this, all data transmitted and received is DD RAM data.		40 μ s	
Busy flag address reading	0	1	BF	AC					Reads contents of busy flag (BF), (internal operation is in progress), and of address counter.		0 μ s	
CG RAM, DD RAM data writing	1	0	Write data					Writes data from DD RAM and from CG RAM.		46 μ s		
CG RAM, DD RAM data reading	1	1	Read data					Reads data to CG RAM or DD RAM.		46 μ s		
Key												
* = invalid			DL = 0: 4 bit			DD RAM: Display data RAM			Execution time varies with frequency			
I/D = 1: Increment			N = 1: 2 lines			CG RAM: Character generator RAM						
I/D = 0: Decrement			N = 0: 1 line			ACG: CG RAM address						
S = 1: Accompanies shift of display			F = 1: 5 \times 10 dots			ADD: DD RAM address.						
S/C = 1: Display shift			F = 0: 5 \times 7 dots			Corresponds to cursor address.						
S/C = 0: Cursor movement			BF = 1: Internal operation in progress			AC: Address counter. Used with both DD RAM and CG RAM.						
R/L = 1: Right shift			BF = 0: Instructions can be accepted.									
R/L = 0: Left shift												
DL = 1: 8 bit												

Letter code and letter pattern applications

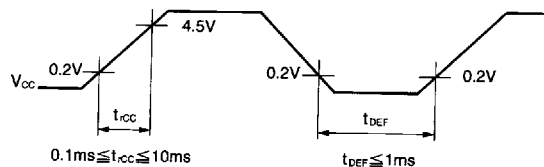
Higher 4 bit Lower 4 bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
XXXX0000	CGRAM (0)	≡		0	a	P	`	P	T	市		一	ウ	E	o	p
XXXX0001	(1)	±	!	1	A	0	a	a	-	E		フ	7	4	a	g
XXXX0010	(2)	?	"	2	B	R	b	r	=	T		イ	ウ	×	P	θ
XXXX0011	(3)	?	#	3	C	S	c	s	=	E		ウ	T	e	e	∞
XXXX0100	(4)	?	*	4	D	T	d	t	E	大		工	ト	+	μ	o
XXXX0101	(5)	?	%	5	E	U	e	u	E	中		才	*	1	o	o
XXXX0110	(6)	?	&	6	F	V	f	v	*	中		ウ	中	二	3	p
XXXX0111	(7)	?	'	7	B	W	b	w	±	上		フ	7	又	7	g
XXXX1000	(0)	#	(C	H	X	h	x	A	T		イ	ウ	*	U	7
XXXX1001	(1)	#)	9	I	V	i	v	A	9		ウ	7	U	W	4
XXXX1010	(2)		*	:	J	Z	j	z	+	9		工	中	レ	U	7
XXXX1011	(3)		+	:	K	L	k	l	(白		火	*	ウ	E	o
XXXX1100	(4)	?	:	<	L	*	l	*	生	*		ウ	7	ウ	7	o
XXXX1101	(5)	?	-	=	M	N	m	n)	*		ウ	*	ウ	7	±
XXXX1110	(6)	?	.	>	N	^	n	→	月	金		3	E	7	7	7
XXXX1111	(7)	?	/	7	O	_	o	+	E	i		ウ	ウ	7	7	o

Reset function

When the power supply is set to ON by using the internal reset circuit, the initial state (reset) is established in the module. In this state, the following instructions are carried out:

- 1 Clear display: The busy flag remains in the busy state ($BF = 1$) until the initial settings are completed. This takes 15 ms.
- 2 Set function $DL = 1$: Interface data length is 8 bits.
 - $N = 0$: One line of display
 - $F = 0$: 5×7 dots
- 3 Display ON/OFF control
 - $D = 0$: Display OFF
 - $C = 0$: Cursor OFF
 - $B = 0$: Cursor blinking OFF
- 4 Set input mode
 - $1D = 1$: +1 (increment)
 - $S = 0$: No shift
- 5 Select DD RAM

Note: Be aware of the following timing relationship. There may be cases in which the initial state is not set after the power has been turned ON because of the power supply rise time.



t_{OFF} regulates the time when the power supply is cut off momentarily or when turned ON and OFF.

If these power supply conditions are not established, the internal reset circuit will not operate normally.